TEXAS INSTRUMENTS

LMK60E2-150M, LMK60E0-156257
LMK60A0-148351, LMK60A0-148M
ZHCSFA1C – JUNE 2016 – REVISED NOVEMBER 2017

LMK60XX 高性能低抖动振荡器

1 特性

- 低噪声、高性能
  - 抖动：Fout > 100MHz 时的典型值为 150fs (RMS)
  - 电源抑制比 (PSRR)：-60dBc，出色的电源抗扰度
- 支持的输出格式
  - 低压正发射极耦合逻辑 （LVPECL） 和低压差分信令 (LVDS) 高达 800MHz
  - HCSL 高达 400MHz
- 总频率容差为 ±50ppm (LMK60X2) 和 ±25ppm (LMK60X0)
- 3.3V 工作电压
- 工业温度范围（-40ºC 至 +85ºC）
- 7mm × 5mm 6 引脚封装，与行业标准 7050 XO 封装引脚兼容

2 应用

- 晶体振荡器、表面声波 (SAW) 振荡器或芯片振荡器的高性能替换产品
- 开关、路由器、网卡、基带装置 (BBU)、服务器、存储/SAN
- 测试和测量
- 医疗成像
- FPGA，处理器连接

3 说明

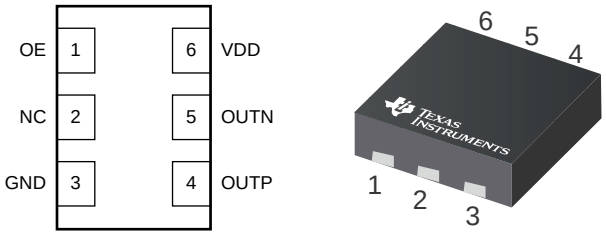
LMK60XX 器件是一款低抖动振荡器，可生成常用参考时钟。该器件在工厂预编程，可支持任何参考时钟频率；支持的输出格式包括 LVPECL、LVDS（最高 800MHz）和 HCSL（最高 400MHz）。内部电源调节功能提供出色的电源纹波抑制 (PSRR)，降低了供电网络的成本和复杂性。该器件由单个 3.3V ± 5% 电源供电。

器件信息(1)

器件型号	输出频率 (MHz) 及格式	总频率稳定性 (ppm)	封装/尺寸
LMK60E2-150M	150 LVPECL	±50	6 引脚四方扁平无引线模块 (QFM) 封装，7mm × 5mm
LMK60E0-156257	156.257 LVPECL	±25	
LMK60A0-148351	148 + 32/91 LVDS	±25	
LMK60A0-148M	148.5 LVDS	±25	

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

引脚分配



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4 修订历史记录

Changes from Revision B (December 2016) to Revision C **Page**

- LMK60A0-148351 新品发布 ... 1
- LMK60A0-148M 新品发布 ... 1

Changes from Revision A (August 2016) to Revision B **Page**

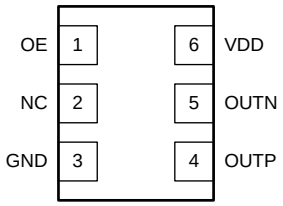
- 将 LMK60E2-150M00 更改为 LMK60E2-150M ... 1
- 删除了 LMK60E2-156M 并将其移动到其他产品说明书 ... 1

Changes from Original (June 2016) to Revision A **Page**

- LMK60E0-156257 新品发布 ... 1

5 Pin Configuration and Functions

SIA Package
6-pin QFM
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device ground
VDD	6	Analog	3.3-V power supply
OUTPUT BLOCK			
OUTP, OUTN	4, 5	Universal	Differential output pair (LVPECL, LVDS or HCSL).
DIGITAL CONTROL / INTERFACES			
NC	2	N/A	No connect
OE	1	LVCMOS	Output enable (internal pullup). When set to low, output pair is disabled and set at high impedance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device supply voltage	–0.3	3.6	V
V_{IN}	Output voltage for logic inputs	–0.3	VDD + 0.3	V
V_{OUT}	Output voltage for clock outputs	–0.3	VDD + 0.3	V
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device supply voltage	3.135	3.3	3.465	V
T_A	Ambient temperature	–40	25	85	°C
T_J	Junction temperature			120	°C
t_{RAMP}	VDD power-up ramp time	0.1		100	ms

6.4 Thermal Information

THERMAL METRIC(1)		LMK60XX (2) (3) (4) SIA (QFM) 6 PINS			UNIT
		Airflow (LFM) 0	Airflow (LFM) 200	Airflow (LFM) 400	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.2	46.4	43.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.6	n/a	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.7	n/a	n/a	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	17.6	22.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	41.5	40.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal resistance is calculated on a 4 layer JEDEC board.
(3) Connected to GND with 3 thermal vias (0.3-mm diameter).
(4) ψJB (junction to board) is used when the main heat flow is from the junction to the GND pad. See the *Layout Guidelines* section for more information on ensuring good system reliability and quality.

6.5 Electrical Characteristics - Power Supply(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device current consumption	LVPECL(2)		162	208	mA
		LVDS		152	196	
		HCSL		155	196	
IDD-PD	Device current consumption when output is disabled	OE = GND		136		mA

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150 Ω termination resistors, from total power dissipation.

6.6 LVPECL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(2)		10		800	MHz
V_{OD}	Output voltage swing (V_{OH} – V_{OL})(2)		700	800	1200	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × $\lvert V_{OD} \rvert$		V
V_{OS}	Output common-mode voltage			VDD – 1.55		V
t_R / t_F	Output rise/fall time (20% to 80%)(3)			150	250	ps
ODC	Output duty cycle(3)		45%		55%	

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(3) Ensured by characterization.

6.7 LVDS Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(1)		10		800	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})(1)		300	390	480	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × $\|V_{OD}\|$		V
V_{OS}	Output common-mode voltage			1.2		V
t_R / t_F	Output rise/fall time (20% to 80%)(2)			150	250	ps
ODC	Output duty cycle(2)		45%		55%	
R_{OUT}	Differential output impedance			125		Ω

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(2) Ensured by characterization.

6.8 HCSL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency		10		400	MHz
V_{OH}	Output high voltage		600		850	mV
V_{OL}	Output low voltage		–100		100	mV
V_{CROSS}	Absolute crossing voltage(2)(3)		250		475	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS}(2)(3)		0		140	mV
dV/dt	Slew rate(4)		0.8		2	V/ns
ODC	Output duty cycle(4)		45%		55%	

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.
(3) Ensured by design.
(4) Ensured by characterization.

6.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF

6.10 Frequency Tolerance Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_T	Total frequency tolerance	LMK60X2: All output formats, frequency bands and device junction temperature up to 125°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and aging (10 years)	–50		50	ppm
		LMK60X0: All output formats, frequency bands and device junction temperature up to 115°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and aging (5 years at 40°C)	–25		25	ppm

(1) Ensured by characterization.

6.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{THRESH}	Threshold voltage(1)		2.72		2.95	V
V_{DROOP}	Allowable voltage droop(2)				0.1	V
$t_{STARTUP}$	Start-up time (1)	Time elapsed from VDD at 3.135 V to output enabled			10	ms
t_{OE-EN}	Output enable time(2)	Time elapsed from OE at V_{IH} to output enabled			50	µs
t_{OE-DIS}	Output disable time(2)	Time elapsed from OE at V_{IL} to output disabled			50	µs

(1) Ensured by characterization.
(2) Ensured by design.

6.12 PSRR Characteristics(1)

VDD = 3.3 V, T_A = 25°C, FS[1:0] = NC, NC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs induced by 50-mV power supply ripple(2)(3) at 156.25-MHz output, all output types	Sine wave at 50 kHz		–60		dBc
		Sine wave at 100 kHz		–60		
		Sine wave at 500 kHz		–60		
		Sine wave at 1 MHz		–60		

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin
(3) DJ_{SPUR} (ps, pk-pk) = [2*10(SPUR/20) / (π*f_{OUT})]*1e6, where PSRR or SPUR in dBc and f_{OUT} in MHz.

6.13 PLL Clock Output Jitter Characteristics(1)(2)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS phase jitter(3) (12 kHz – 20 MHz)	f_{OUT} ≥ 100 MHz, All output types		150	250	fs RMS

(1) Refer to Parameter Measurement Information for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).
(3) Ensured by characterization.

6.14 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

6.15 Typical Characteristics

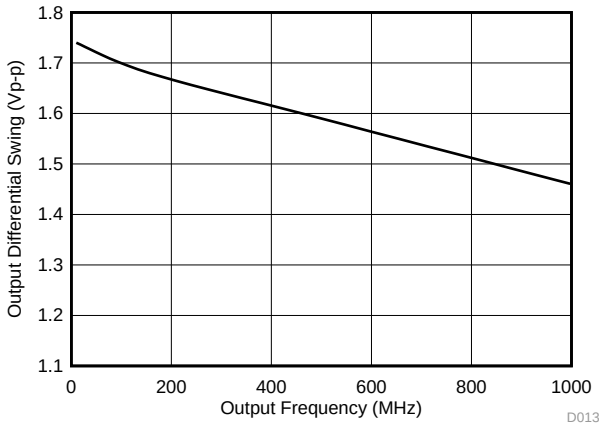


Figure 1. LVPECL Differential Output Swing vs Frequency

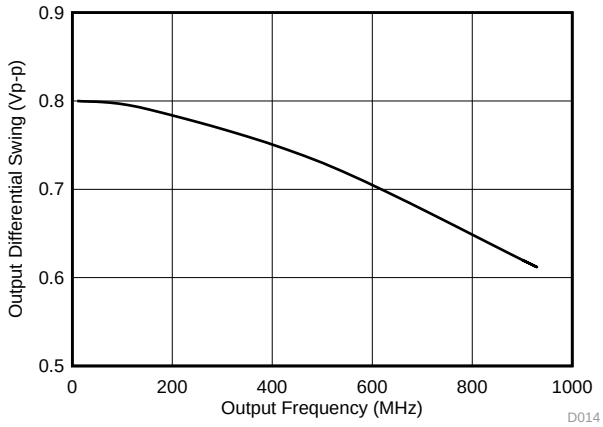


Figure 2. LVDS Differential Output Swing vs Frequency

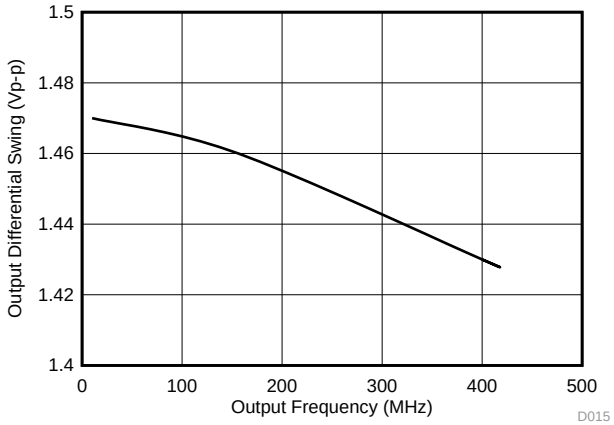


Figure 3. HCSL Differential Output Swing vs Frequency

7 Parameter Measurement Information

7.1 Device Output Configurations

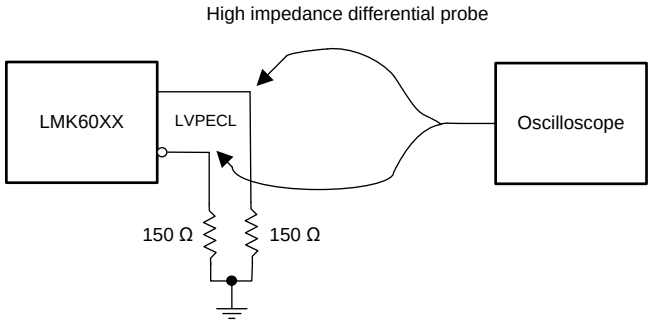


Figure 4. LVPECL Output DC Configuration During Device Test

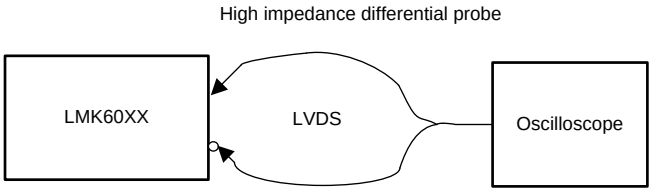


Figure 5. LVDS Output DC Configuration During Device Test

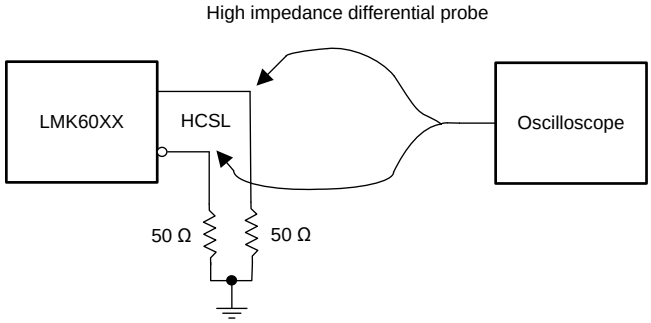


Figure 6. HCSL Output DC Configuration During Device Test

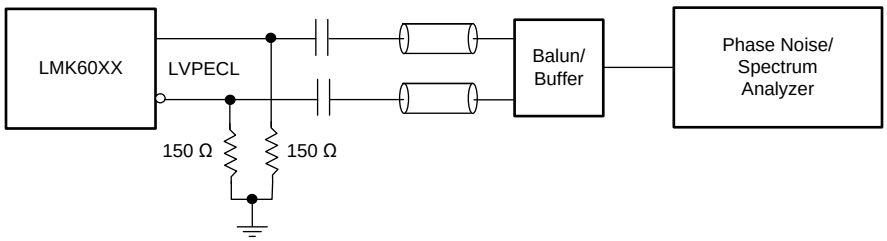


Figure 7. LVPECL Output AC Configuration During Device Test

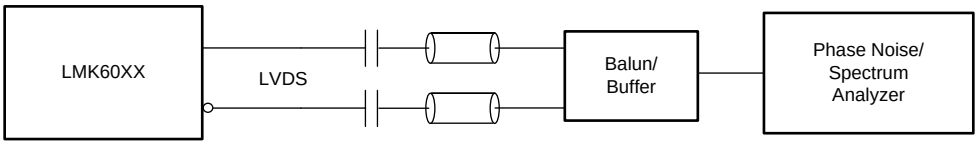


Figure 8. LVDS Output AC Configuration During Device Test

Device Output Configurations (continued)

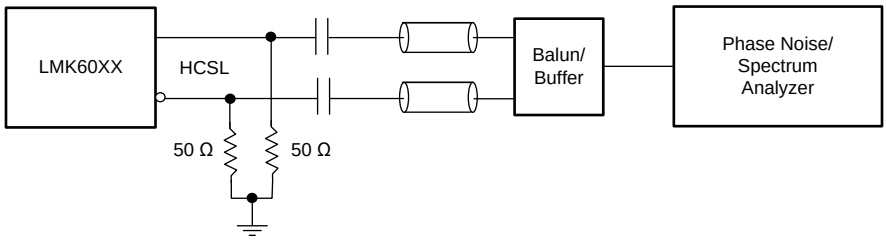


Figure 9. HCSL Output AC Configuration During Device Test

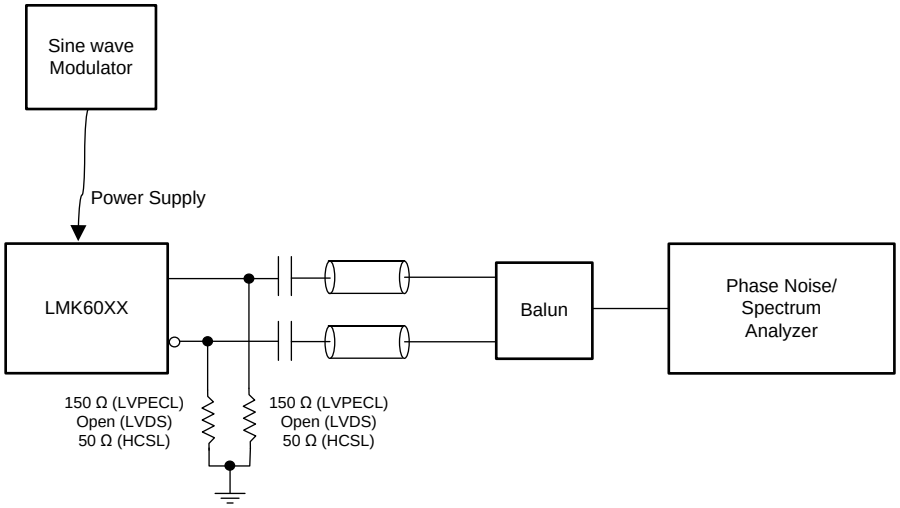


Figure 10. PSRR Test Setup

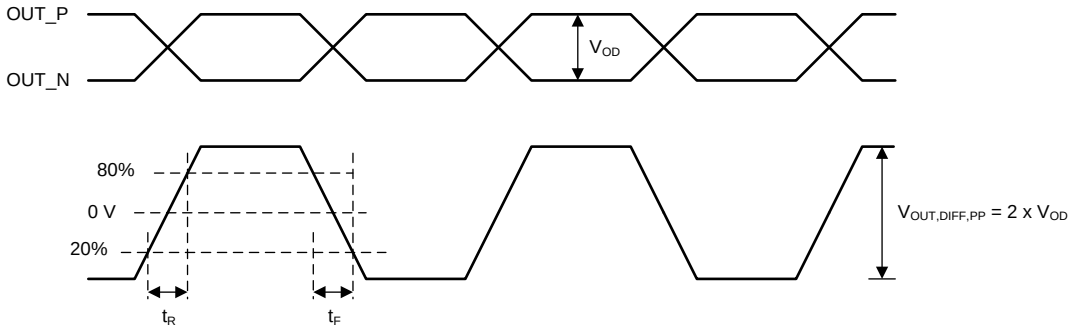


Figure 11. Differential Output Voltage and Rise/Fall Time

8 Power Supply Recommendations

For best electrical performance of LMK60XX, TI recommends using a combination of 10 µF, 1 µF and 0.1 µF on its power supply bypass network. TI also recommends using component side mounting of the power supply bypass capacitors, and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. Figure 12 shows the layout recommendation for power supply decoupling of LMK60XX.

9 Layout

9.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power supply bypassing when using LMK60XX to ensure good thermal / electrical performance and overall signal integrity of entire system.

9.1.1 Ensuring Thermal Reliability

The LMK60XX is a high performance device. Therefore pay careful attention to device configuration and printed-circuit board (PCB) layout with respect to power consumption. The ground pin needs to be connected to the ground plane of the PCB through three vias or more, as shown in Figure 12, to maximize thermal dissipation out of the package.

Equation 1 describes the relationship between the PCB temperature around the LMK60XX and its junction temperature.

$$T_B = T_J – \Psi_{JB} * P \quad (1)$$

where

- T_B: PCB temperature around the LMK60XX
- T_J: Junction temperature of LMK60XX
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK60XX (37.7°C/W without airflow)
- P: On-chip power dissipation of LMK60XX

To ensure that the maximum junction temperature of LMK60XX is below 120°C, it can be calculated that the maximum PCB temperature without airflow should be at 90°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.68 W.

9.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK60XX, TI recommends routing vias into decoupling capacitors and then into the LMK60XX. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high-frequency current flow. Figure 12 shows the layout recommendation for LMK60XX.

Layout Guidelines (接下页)

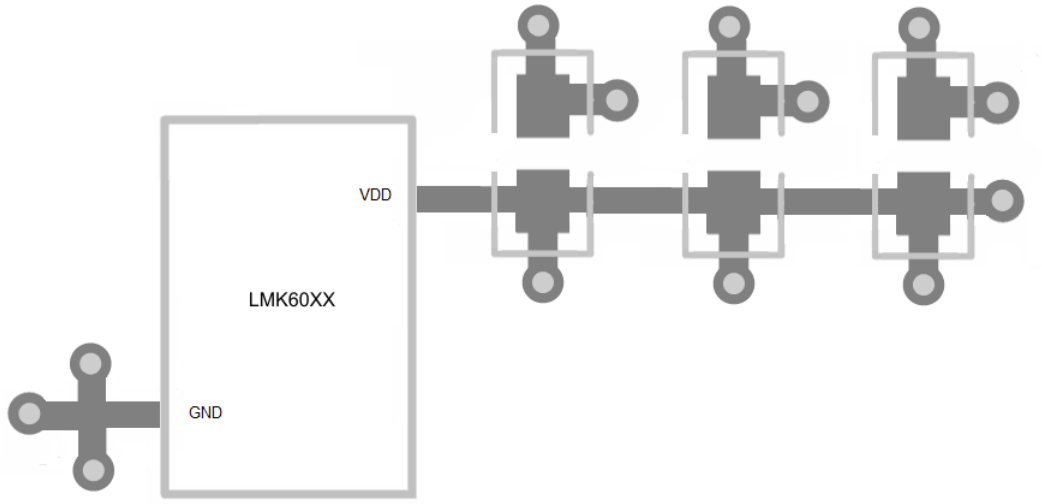


Figure 12. LMK60XX Layout Recommendation for Power Supply and Ground

9.1.3 Recommended Solder Reflow Profile

TI recommends following the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferable for the LMK60XX to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

10 器件和文档支持

10.1 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
LMK60E2-150M	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LMK60E0-156257	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

10.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

10.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

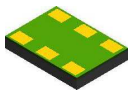
10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

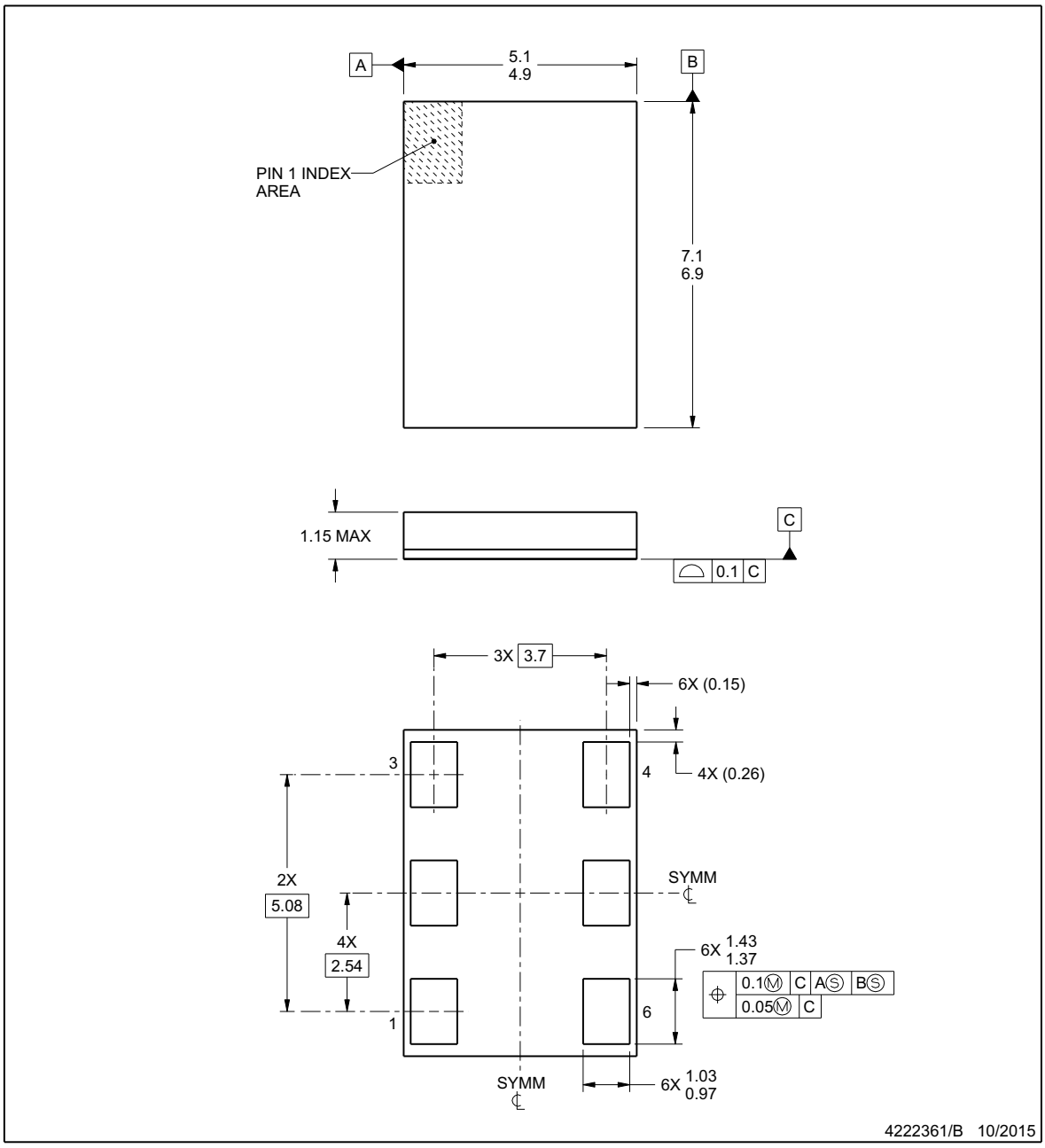


PACKAGE OUTLINE

SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



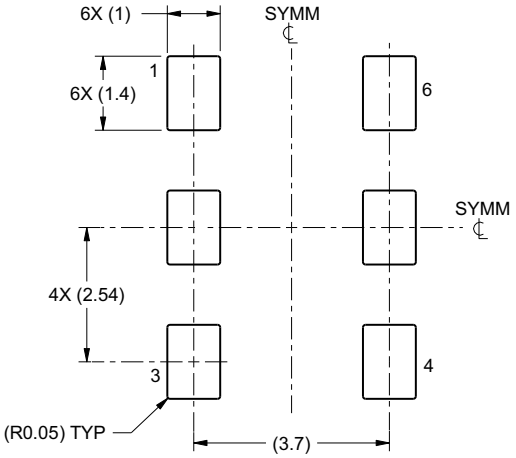
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

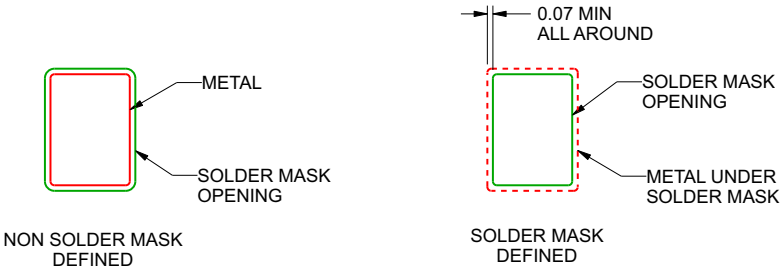
EXAMPLE BOARD LAYOUT

SIA0006A — **QFM - 1.15 mm max height**

QUAD FLAT MODULE



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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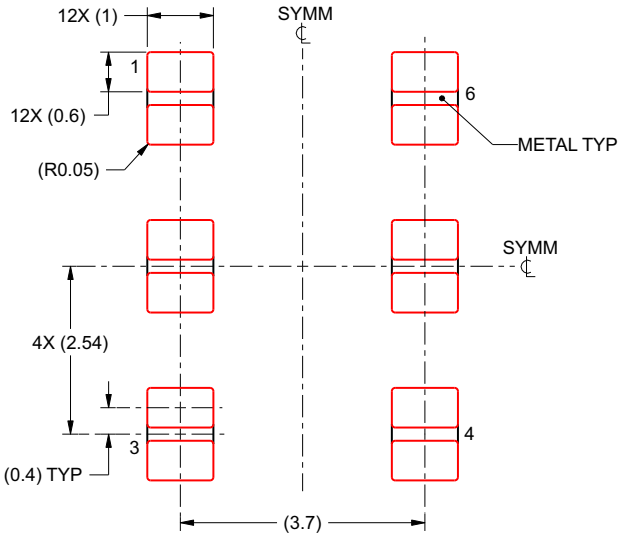
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIA0006A — **QFM - 1.15 mm max height**

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
ALL PADS: 86%
SCALE:10X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK60A0-148M35SIAR	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M35
LMK60A0-148M35SIAR.A	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M35
LMK60A0-148M35SIAR.B	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK60A0-148M35SIAT	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M35
LMK60A0-148M35SIAT.A	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M35
LMK60A0-148M35SIAT.B	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
LMK60A0-148M50SIAR	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M50
LMK60A0-148M50SIAR.A	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M50
LMK60A0-148M50SIAR.B	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK60A0-148M50SIAT	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M50
LMK60A0-148M50SIAT.A	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60A0 148M50
LMK60A0-148M50SIAT.B	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
LMK60E0-156257SIAR	Active	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156257
LMK60E0-156257SIAR.A	Active	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156257
LMK60E0-156257SIAR.B	Active	Production	QFM (SIA) | 6	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMK60E0-156257SIAT	Active	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156257
LMK60E0-156257SIAT.A	Active	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156257
LMK60E0-156257SIAT.B	Active	Production	QFM (SIA) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
LMK60E2-150M00SIAR	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK60E2-150M00SIAR.A	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00
LMK60E2-150M00SIAR.B	NRND	Production	QFM (SIA) | 6	2500 | LARGE T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00
LMK60E2-150M00SIAT	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00
LMK60E2-150M00SIAT.A	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	Yes	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00
LMK60E2-150M00SIAT.B	NRND	Production	QFM (SIA) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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