LMH6521 高性能双路 DVGA

1 特性

- 200MHz 频率下 OIP3 为 48.5dBm
- 最大电压增益为 26dB
- 增益范围：31.5dB，步长为 0.5dB
- 通道增益匹配为 ±0.04dB
- 最大增益时的噪声系数：7.3dB
- –3dB 带宽为 1200MHz
- 功耗低
- 独立通道关断
- 三种增益控制模式：
  - 并行接口
  - 串行接口 (SPI)
  - 脉冲模式接口
- 温度范围：-40°C 至 +85°C
- 热增强型 32 引脚 WQFN 封装

2 应用

- 蜂窝基站
- 宽带和窄带 IF 采样接收器
- 宽带直接转换
- 数字预失真
- ADC 驱动器

3 说明

LMH6521 包含两个高性能数控可变增益放大器 (DVGA)。

LMH6521 的两个通道均具有独立的数控衰减器，后跟高线性度差动输出放大器。每个块都经过优化，可实现低失真和最大的系统设计灵活性。每个通道都具有高速关断模式。

内部数控衰减器可在 31.5dB 范围内提供精确的 0.5dB 增益步长。该器件提供了串行和并行编程选项。串行模式编程使用 SPI 接口。它还提供脉冲模式，其中简单的上升或下降命令可以一次将增益改变一个步长。

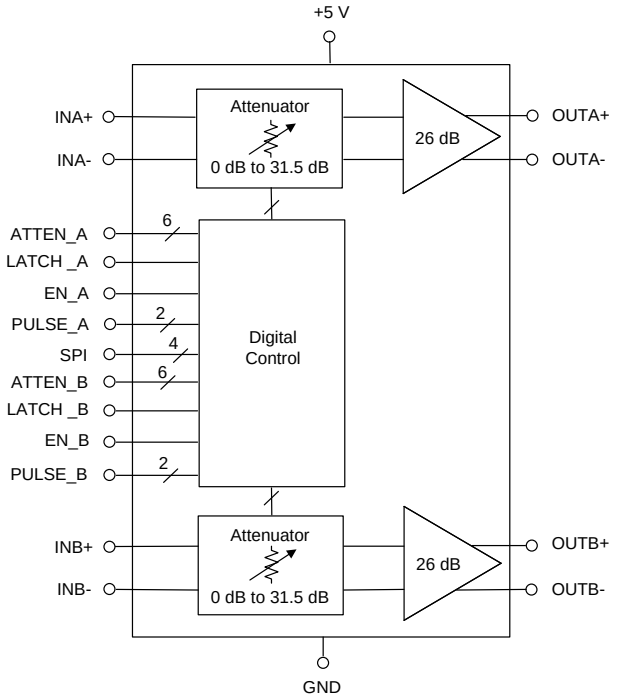
输出放大器有差动输出，允许单个 5V 电源上有 $10V_{PPD}$ 信号摆动。低阻抗输出在驱动滤波器或模数转换器时可提供最大的灵活性。

器件信息(1)

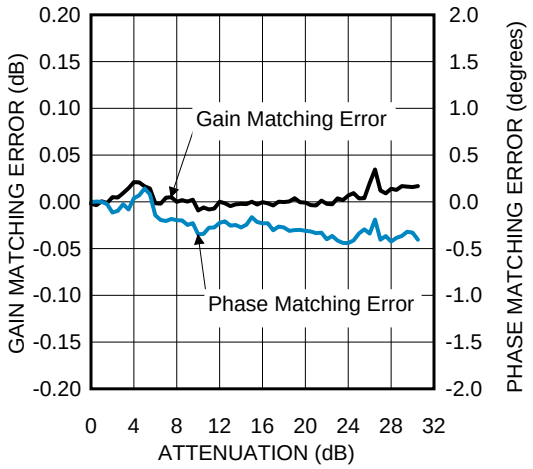
器件型号	封装	封装尺寸（标称值）
LMH6521	WQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

LMH6521 方框图



通道匹配错误（通道 **A** – 通道 **B**）



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (March 2013) to Revision E **Page**

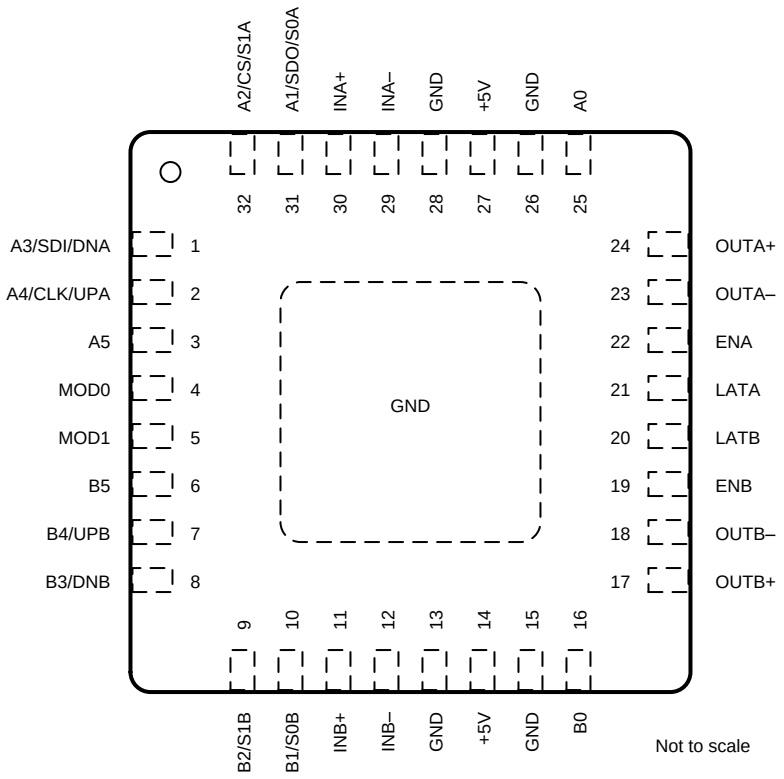
- 添加了 *ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1

Changes from Revision C (March 2013) to Revision D **Page**

- 已更改 从美国国家半导体产品说明书的布局更改为 TI 格式 ... 1

5 Pin Configuration and Functions

RTV Package
32-Pin WQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	A3/SDI/DNA	I	A3: Attenuation bit three = 4-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). SDI: Serial data in. Digital inputs serial mode (MOD1 = 1, MOD0 = 0) SPI compatible. See *Application Information* for more details. DNA: Down pulse pin. A logic 0 pulse decreases gain one step. Digital inputs pulse mode (MOD1 = 0, MOD0 = 1). Pulsing this pin together with pin 2 resets the gain to maximum gain.
2	A4/CLK/UPA	I	A4: Attenuation bit four = 8-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). CLK: Serial clock. Digital inputs serial mode (MOD1 = 1, MOD0 = 0) SPI compatible. UPA: Up pulse pin. A logic 0 pulse increases gain one step. Digital inputs pulse mode (MOD1 = 0, MOD0 = 1). Pulsing this pin together with pin 1 resets the gain to maximum gain.
3	A5	I	Attenuation bit five = 16-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). Pins unused in serial mode, connect to DC ground. Pins unused in pulse mode, connect to DC ground.
4	MOD0	I	Digital mode control pins. These pins float to the logic hi state if left unconnected. Pins unused in serial mode, connect to DC ground. See *Application Information* for mode settings.
5	MOD1	I	Digital mode control pins. These pins float to the logic hi state if left unconnected. Pins unused in pulse mode, connect to DC ground. See *Application Information* for mode settings.
6	B5	I	Attenuation bit five = 16-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). Pins unused in serial mode, connect to DC ground. Pins unused in pulse mode, connect to DC ground.

(1) I = Input, O = Output, P = Power

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
7	B4/UPB	I	B4: Attenuation bit four = 8-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). UPB: Up pulse pin. A logic 0 pulse increases gain one step. Digital inputs pulse mode (MOD1 = 0, MOD0 = 1). Pulsing this pin together with pin 8 resets the gain to maximum gain. Pins unused in serial mode, connect to DC ground.
8	B3/DNB	I	B3: Attenuation bit three = 4-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). DNB: Down pulse pin. A logic 0 pulse decreases gain one step. Digital inputs pulse mode (MOD1 = 0, MOD0 = 1). Pulsing this pin together with pin 7 resets the gain to maximum gain. Pins unused in serial mode, connect to DC ground.
9	B2/S1B	I	B2: Attenuation bit two = 2-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). S1B: Step size zero and step size 1. (0,0) = 0.5 dB; (0, 1)= 1 dB; (1,0) = 2 dB, and (1, 1)= 6 dB. Digital inputs pulse mode (MOD1 = 0, MOD0 = 1). Pins unused in serial mode, connect to DC ground.
10	B1/S0B	I	B1: Attenuation bit one = 1-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). S0B: Step size zero and step size 1. (0,0) = 0.5 dB; (0, 1)= 1 dB; (1,0) = 2 dB, and (1, 1)= 6 dB. Digital inputs pulse mode (MOD1 = 0, MOD0 = 1). Pins unused in serial mode, connect to DC ground.
11	INB+	I	Amplifier noninverting input. Internally biased to mid supply. Input voltage must not exceed V+ or go below GND by more than 0.5 V.
12	INB–	I	Amplifier inverting input. Internally biased to mid supply. Input voltage must not exceed V+ or go below GND by more than 0.5 V.
13	GND	P	Ground pin. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
14	+5V	P	Power supply pins. Valid power supply range is 4.75 V to 5.25 V.
15	GND	P	Ground pin. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
16	B0	I	Attenuation bit zero = 0.5-dB step. Gain steps down from maximum gain (000000 = Maximum Gain). Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). Pins unused in serial mode, connect to DC ground. Pins unused in pulse mode, connect to DC ground.
17	OUTB+	O	Amplifier noninverting output. Externally biased to 0 V.
18	OUTB–	O	Amplifier inverting output. Externally biased to 0 V.
19	ENB	I	Enable pins. Logic 1 = enabled state. See *Application Information* for operation in serial mode.
20	LATB	I	Latch pins. Logic zero = active, logic 1 = latched. Gain does not change once latch is high. Connect to ground if the latch function is not desired. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). Pins unused in serial mode, connect to DC ground.
21	LATA	I	Latch pins. Logic zero = active, logic 1 = latched. Gain does not change once latch is high. Connect to ground if the latch function is not desired. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). Pins unused in serial mode, connect to DC ground.
22	ENA	I	Enable pins. Logic 1 = enabled state. See *Application Information* for operation in serial mode.
23	OUTA–	O	Amplifier inverting output. Externally biased to 0 V.
24	OUTA+	O	Amplifier noninverting output. Externally biased to 0 V.
25	A0	I	Attenuation bit zero = 0.5-dB step. Gain steps down from maximum gain (000000 = Maximum Gain). Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). Pins unused in serial mode, connect to DC ground. Pins unused in pulse mode, connect to DC ground.
26	GND	P	Ground pin. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
27	+5V	P	Power supply pins. Valid power supply range is 4.75 V to 5.25 V.
28	GND	P	Ground pin. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
29	INA–	I	Amplifier inverting input. Internally biased to mid supply. Input voltage must not exceed V+ or go below GND by more than 0.5 V.
30	INA+	I	Amplifier noninverting input. Internally biased to mid supply. Input voltage must not exceed V+ or go below GND by more than 0.5 V.

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
31	A1/SDO/S0A	I	A1: Attenuation bit one = 1-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). SDO: Serial data out. Digital inputs serial mode (MOD1 = 1, MOD0 = 0) SPI compatible. S0A: Step size zero and step size 1. (0,0) = 0.5 dB; (0, 1)= 1 dB; (1,0) = 2 dB, and (1, 1)= 6 dB. Digital inputs pulse mode (MOD1 = 0, MOD0 = 1).
32	A2/CS/S1A	I	A2: Attenuation bit two = 2-dB step. Digital inputs parallel mode (MOD1 = 1, MOD0 = 1). CS: Serial chip select (active low). Digital inputs serial mode (MOD1 = 1, MOD0 = 0) SPI compatible. S1A: Step size zero and step size 1. (0,0) = 0.5 dB; (0, 1)= 1 dB; (1,0) = 2 dB, and (1, 1)= 6 dB. Digital inputs pulse mode (MOD1 = 0, MOD0 = 1).
GND	GND	P	Ground plane. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Positive supply voltage (pin 14 and 27)	–0.6	5.5	V
Differential voltage between any two grounds		< 200	mV
Analog input voltage	–0.6	V+	V
Digital input voltage	–0.6	5.5	V
Soldering temperature, infrared or convection (30 s)		260	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)(2)	±2000	V
		Charged-device model (CDM)(3)	±750	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human-body model, applicable std. MIL-STD-883, Method 3015.7. Field-induced Charge-device model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC). Machine model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC).
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply voltage (pin 14 and 27)	4.75	5.25	V
	Differential voltage between any two grounds		<10	mV
	Analog input voltage, AC coupled	0	V+	V
T_A	Ambient temperature(2)	–40	85	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see *Electrical Characteristics*.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC(1)		LMH6521 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

The following specifications apply for single supply with V+ = 5 V, differential V_{OUT} = 4 V_{PP}, R_L= 200 Ω, T_A = 25°C, f_{in} = 200 MHz, and maximum gain (0 attenuation)(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
DYNAMIC PERFORMANCE						
SSBW	3-dB small signal bandwidth			1200		MHz
	Output noise voltage	Amplifier output with R_{SOURCE} = 200 Ω		33		nV/√Hz
	Noise figure	Source = 200 Ω		7.3		dB
OIP3	Output 3rd-order intercept point	f = 100 MHz, P_O= 4 dBm per tone		56		dBm
		f = 200 MHz, P_O= 4 dBm per tone		48.5		
		f = 250 MHz, P_O= 4 dBm per tone		46.5		
OIP2	Output 2nd-order intercept point	f = 100 MHz, P_O= 4 dBm per tone		92		dBm
		f = 200 MHz, P_O= 4 dBm per tone		80		
		f = 250 MHz, P_O= 4 dBm per tone		73		
HD2	2nd harmonic distortion	f = 200 MHz, P_O= 6 dBm		–84		dBc
HD3	3rd harmonic distortion	f = 200 MHz, P_O= 6 dBm		–83		dBc
P1dB	1-dB compression point			17		dBm
ANALOG I/O						
	Input resistance	Differential		200		Ω
	Input common mode voltage	Self biased (AC coupled)		2.5		V
	Input common mode voltage range	Externally driven (DC coupled)		2 to 3		V
	Maximum input voltage swing	Differential		11		V_{PPD}
	Output resistance	Differential		20		Ω
	Maximum differential output voltage swing	Differential		10		V_{PPD}
CMRR	Common mode rejection ratio	DC, V_{ID} = 0 V, V_{CM} = 2.5 V ±0.5 V		80		dB
PSRR	Power supply rejection ratio	DC, V+ = 5 V ±0.5 V, V_{IN} = 2.5 V		77		dB
	Channel to channel isolation	f = 200 MHz, minimum attenuation setting		73		dB
GAIN PARAMETERS						
	Maximum voltage gain	Gain Code 000000 (min. attenuation), Av = V_O / V_{IN}		26		dB
	Minimum voltage gain	Gain Code 111111 (max. attenuation), Av = V_O / V_{IN}		–5.5		dB
	Gain accuracy			1%		
	Gain step size			0.5		dB
	Channel gain matching	ChA – ChB, any gain setting		±0.04		dB
	Channel phase matching	ChA – ChB, any gain setting		±0.45		°
	Cumulative gain error	0 to 12 dB attenuation setting		±0.1		dB
		0 to 24 dB attenuation setting		±0.3		
		0 to 31 dB attenuation setting		±0.5		
	Cumulative phase shift	0 to 12 dB attenuation setting		±0.6		°
		0 to 24 dB attenuation setting		±5.3		
		0 to 31 dB attenuation setting		±16.5		
	Gain step switching time			15		ns
	Gain temperature sensitivity	0 attenuation setting		2.7		mdB/°C

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No ensurance of parametric performance is indicated in the electrical tables under conditions different than those tested
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Electrical Characteristics (continued)

The following specifications apply for single supply with V+ = 5 V, differential V_{OUT} = 4 V_{PP}, R_L= 200 Ω, T_A = 25°C, f_{in} = 200 MHz, and maximum gain (0 attenuation)(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER REQUIREMENTS							
VCC	Supply voltage			4.75	5	5.25	V
ICC	Supply current	Both channels enabled	T_A = –40°C to 85°C		225		mA
			T_A = –65°C to 150°C			245	
ICC	Disabled supply current	Both channels			35		mA
ALL DIGITAL INPUTS(4)							
VIL	Logic input low voltage				0.5		V
VIH	Logic input high voltage				1.8		V
IIH	Logic input high input current	Digital input voltage = 5 V			200		µA
IIL	Logic input low input current	Digital input voltage = 0 V			–60		µA

(4) Logic compatibility is TTL, 2.5-V CMOS, and 3.3-V CMOS.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
PARALLEL AND PULSE MODE TIMING					
t_{GS}	Setup time		3		ns
t_{GH}	Hold time		3		ns
t_{LP}	Latch low pulse width		7		ns
t_{PG}	Pulse gap between pulses		20		ns
t_{PW}	Minimum pulse width (pulse mode)		15		ns
t_{RW}	Reset width		10		ns
SERIAL MODE TIMING AND AC CHARACTERISTICS (SPI COMPATIBLE)					
f_{SCLK}	Max serial clock frequency		50		MHz
t_{PH}	SCLK high state duty cycle		50%		SCLK
t_{PL}	SCLK low state duty cycle		50%		SCLK
t_{SU}	Serial data in setup time		2		ns
t_H	Serial data in hold time		2		ns
t_{OZD}	Serial data out TRI-STATE-to-driven time (referenced to negative edge of SCLK)		10		ns
t_{OD}	Serial data out output delay time (referenced to negative edge of SCLK)		10		ns
t_{CSS}	Serial chip select setup time (referenced to positive edge of SCLK)		5		ns

6.7 Typical Characteristics

V+ = 5 V, Differential V_{OUT} = 4 V_{PP}, R_L = 200 Ω, T_A = 25°C, f_{in} = 200 MHz, and Maximum Gain (0 Attenuation)

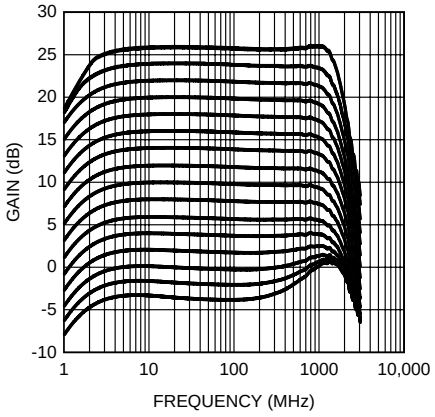


Figure 1. Frequency Response 2-dB Gain Steps

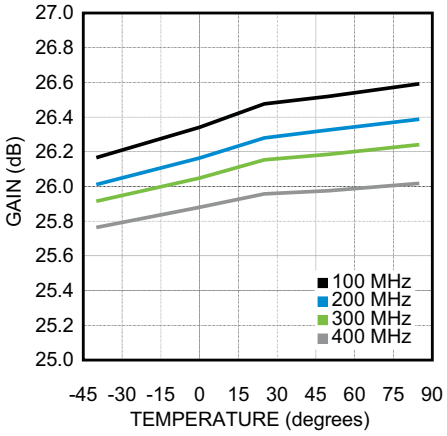


Figure 2. Gain Flatness vs Temperature

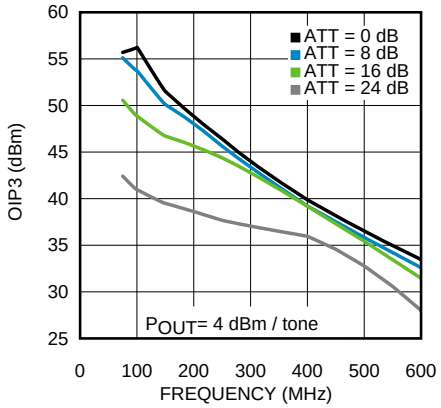


Figure 3. OIP3 vs Frequency

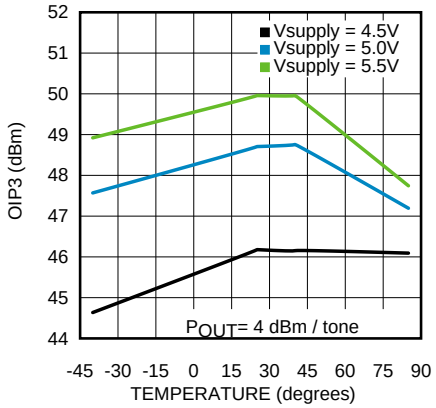


Figure 4. OIP3 vs Temperature

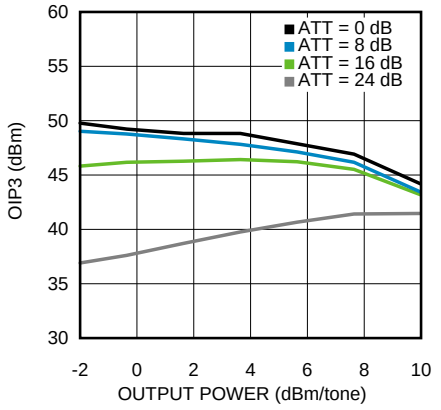


Figure 5. OIP3 vs Pout

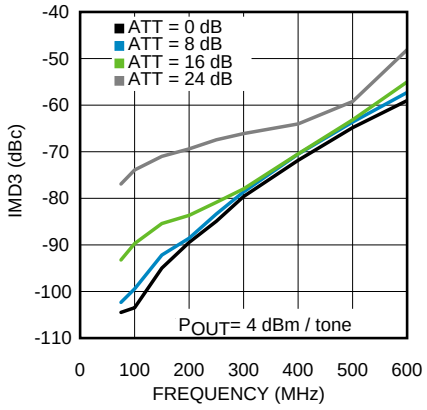


Figure 6. Third Order Intermodulation Products vs Frequency

Typical Characteristics (continued)

V+ = 5 V, Differential V_{OUT} = 4 V_{PP}, R_L = 200 Ω, T_A = 25°C, f_{in} = 200 MHz, and Maximum Gain (0 Attenuation)

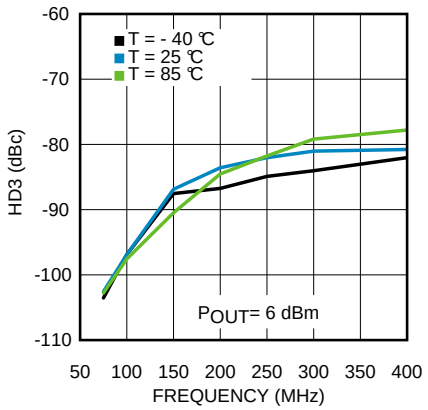


Figure 7. Third Order Harmonic Distortion vs Frequency

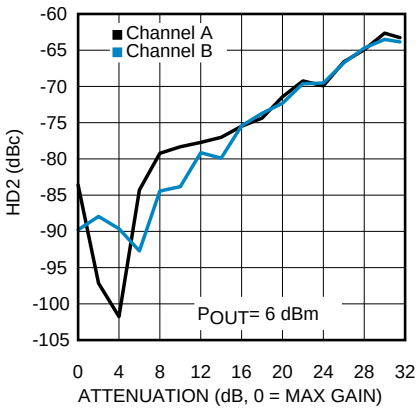


Figure 8. Second Order Harmonic Distortion vs Attenuation

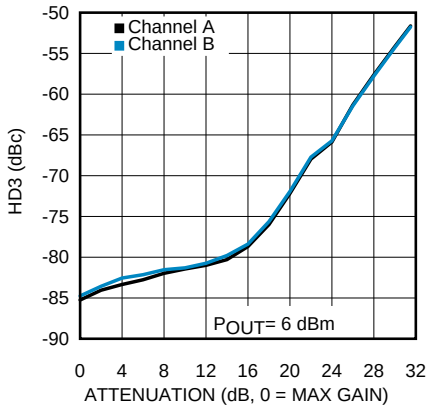


Figure 9. Third Order Harmonic Distortion vs Attenuation

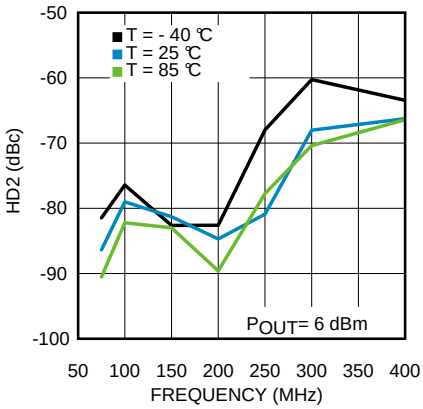


Figure 10. Second Order Harmonic Distortion vs Frequency

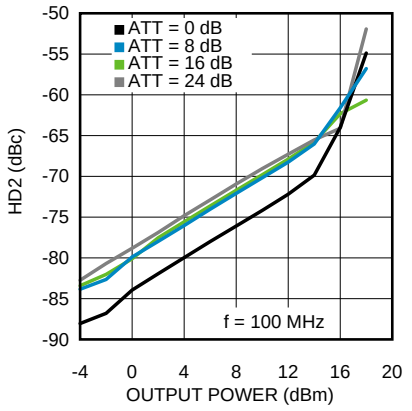


Figure 11. Second Order Harmonic Distortion at 100 MHz

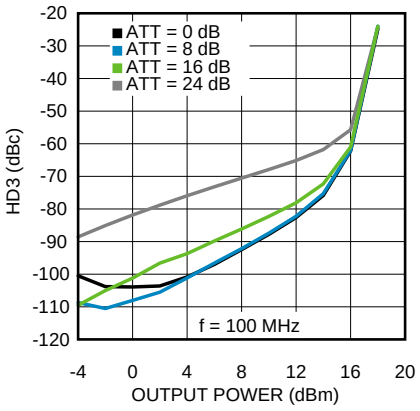


Figure 12. Third Order Harmonic Distortion at 100 MHz

Typical Characteristics (continued)

V+ = 5 V, Differential V_{OUT} = 4 V_{PP}, R_L = 200 Ω, T_A = 25°C, f_{in} = 200 MHz, and Maximum Gain (0 Attenuation)

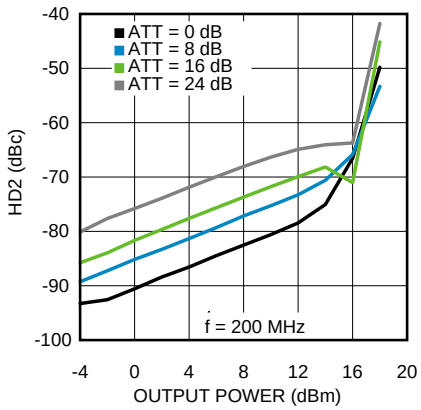


Figure 13. Second Order Harmonic Distortion at 200 MHz

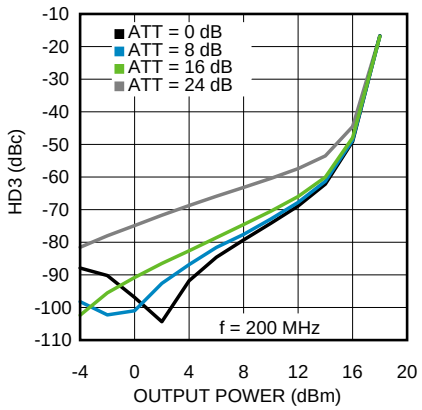


Figure 14. Third Order Harmonic Distortion at 200 MHz

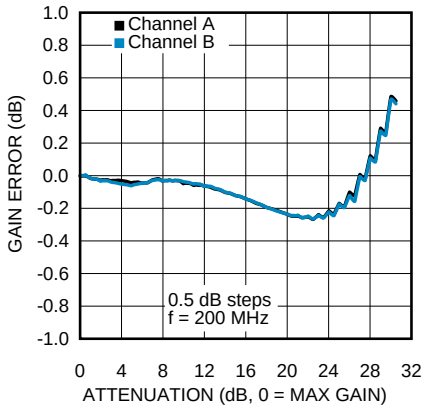


Figure 15. Cumulative Gain Error

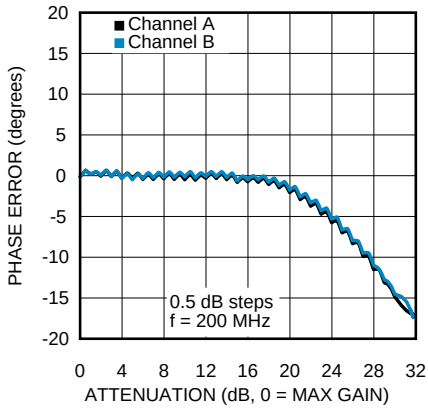


Figure 16. Cumulative Phase Shift

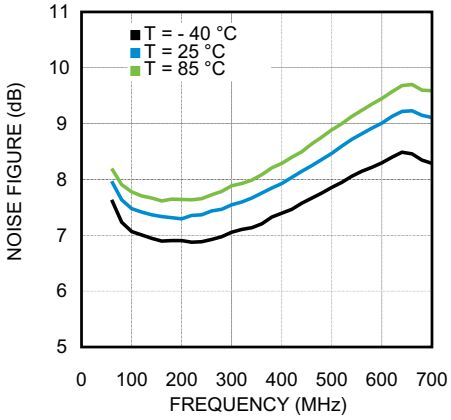


Figure 17. Noise Figure vs Frequency

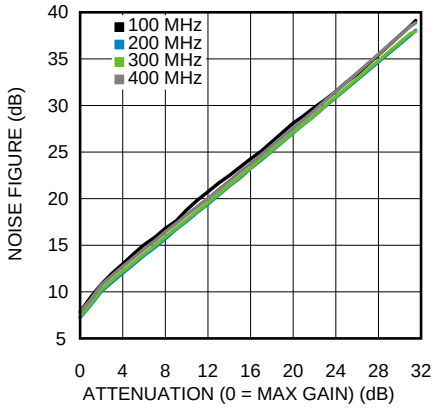


Figure 18. Noise Figure vs Attenuation

Typical Characteristics (continued)

V+ = 5 V, Differential V_{OUT} = 4 V_{PP}, R_L = 200 Ω, T_A = 25°C, f_{in} = 200 MHz, and Maximum Gain (0 Attenuation)

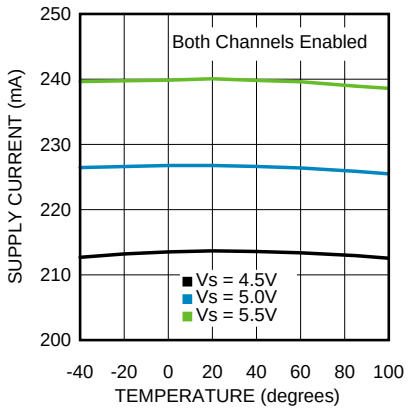


Figure 19. Supply Current vs Temperature

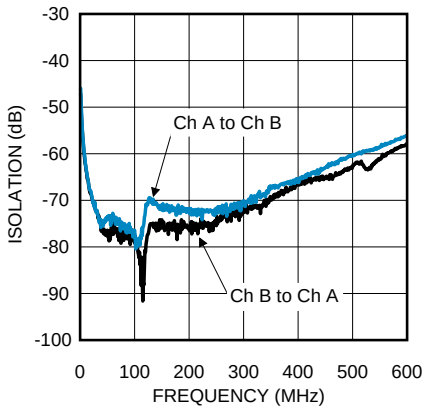


Figure 20. Channel-to-Channel Isolation

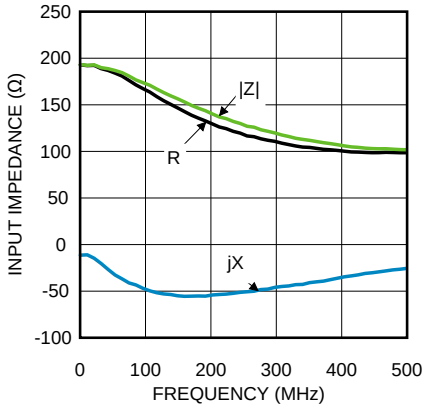


Figure 21. Input Impedance

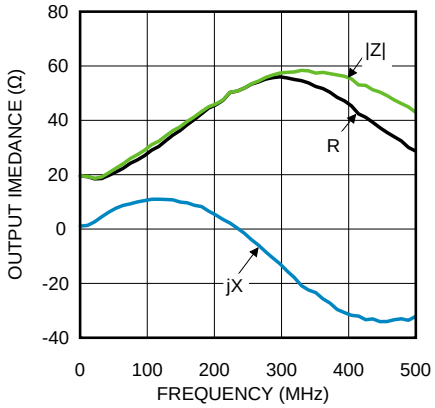


Figure 22. Output Impedance

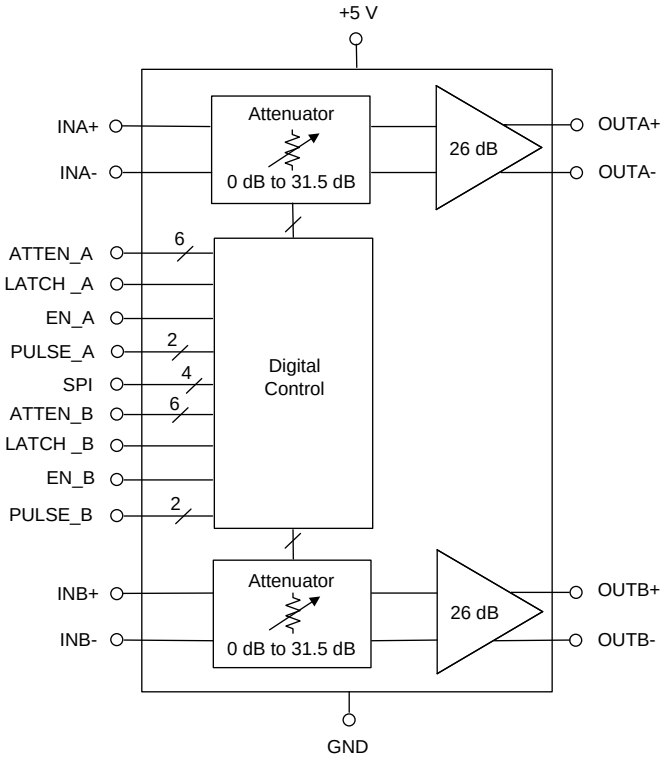
7 Detailed Description

7.1 Overview

The LMH6521 is a dual, digitally controlled variable gain amplifier designed for narrowband and wideband intermediate frequency sampling applications. The LMH6521 is optimized for accurate 0.5-dB gain steps with exceptional gain and phase matching between channels combined with low distortion products. Gain matching error is less than ±0.05 dB and phase matching error less than ±0.5° over the entire attenuation range. This makes the LMH6521 ideal for driving analog-to-digital converters where high linearity is necessary. Figure 38 shows a typical application circuit.

The LMH6521 has been designed for AC-coupled applications and has been optimized to operate at frequencies greater than 3 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Characteristics

The LMH6521 input impedance is set by internal resistors to a nominal 200 Ω. At higher frequencies, device parasitic reactances starts to impact the input impedances. See Figure 21 in *Typical Characteristics* for more details.

For many AC-coupled applications, the impedance can be easily changed using LC circuits to transform the actual impedance to the desired impedance.

Feature Description (continued)

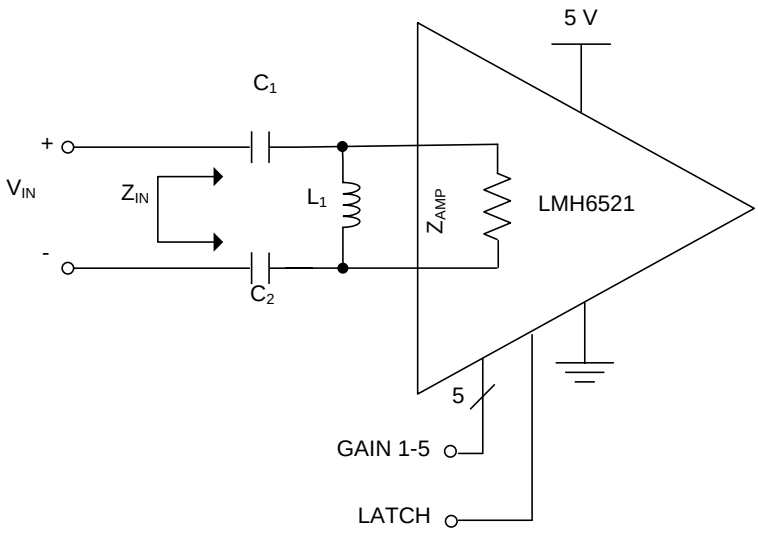


Figure 23. Differential 200-Ω LC Conversion Circuit

In Figure 23 a circuit is shown that matches the amplifier 200-Ω input with a source impedance of 100 Ω.

To avoid undesirable signal transients, the LMH6521 must not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs.

7.3.2 Output Characteristics

The LMH6521 has a low output impedance very similar to a traditional operational amplifier output. This means that a wide range of load impedance can be driven with minimal gain loss. Matching load impedance for proper termination of filters is as easy as inserting the proper value of resistor between the filter and the amplifier. This flexibility makes system design and gain calculations very easy. The LMH6521 was designed to run from a single 5-V supply. In spite of this low supply voltage the LMH6521 is still able to deliver very high power gains when driving low impedance loads.

7.3.3 Output Connections

The LMH6521, like most high frequency amplifiers, is sensitive to loading conditions on the output. Load conditions that include small amounts of capacitance connected directly to the output can cause stability problems. An example of this is shown in Figure 24. A more sophisticated filter may require better impedance matching. See Figure 36 for an example filter configuration and table Table 7 for some IF filter components values.

Feature Description (continued)

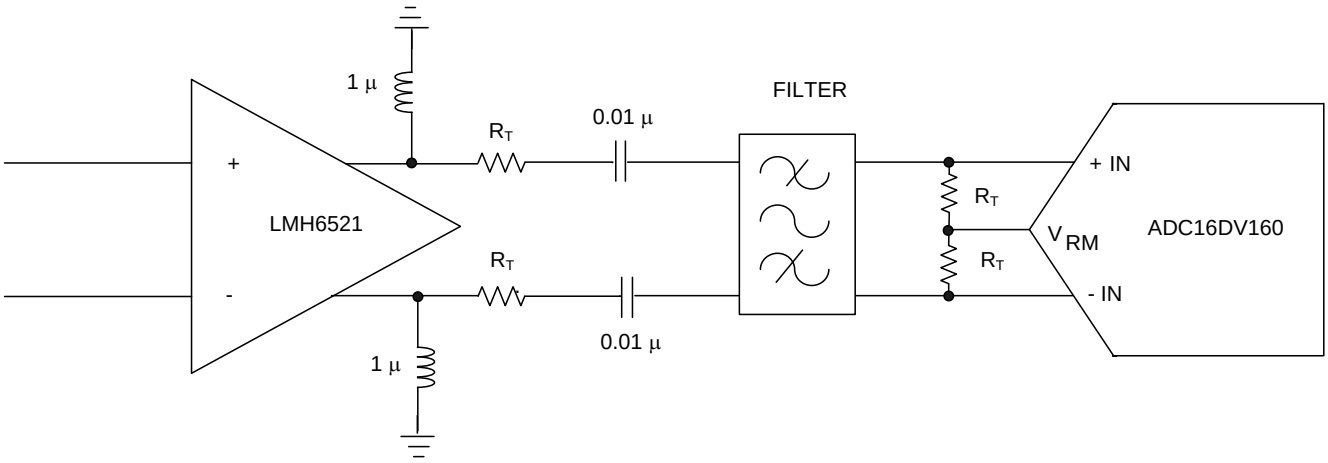


Figure 24. Example Output Configuration

The outputs of the LMH6521 must be biased near the ground potential. On the evaluation board, 1-µH inductors are installed to provide proper output biasing. The bias current is approximately 36 mA per output pin and is not a function of the load condition, which makes the LMH6521 robust to handle various output load conditions while maintaining superior linearity as shown in Figure 25. With large inductors and high operating frequencies the inductor presents a very high impedance and has minimal AC current. If the inductor is chosen to have a smaller value, or if the operating frequency is very low there could be enough AC current flowing in the inductor to become significant. Make sure to check the inductor datasheet to not exceed the maximum current limit.

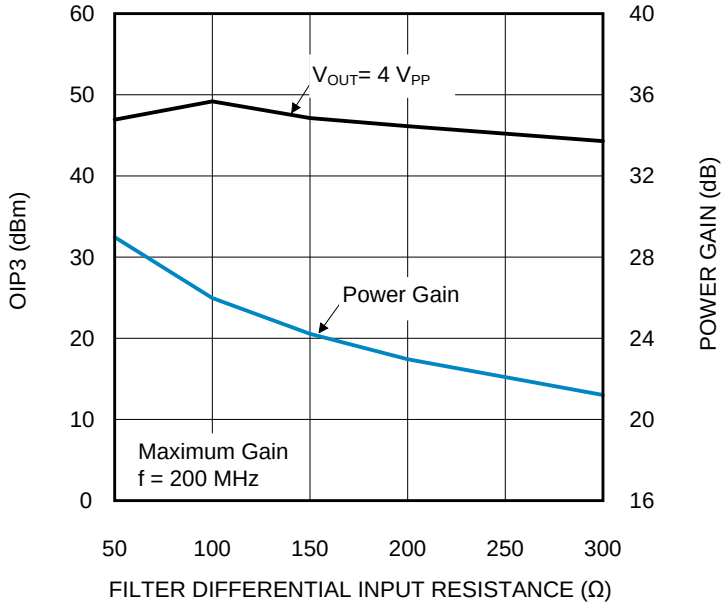


Figure 25. OIP3 vs Amplifier Load Resistance

7.4 Device Functional Modes

The LMH6521 is a differential input, differential output, digitally controlled variable gain amplifier (DVGA). This is the primary functional mode. The LMH6521 is designed to support large voltage swings with excellent linearity. For this reason the amplifier output stage is biased separately than the rest of the amplifier. Like many RF amplifiers, the LMH6521 output stage is powered through the output pins.

Device Functional Modes (continued)

Power to the LMH6521 output stage is accomplished by using RF chokes to supply the DC current required by the output transistors. The EVM and all data sheet plots were derived using 1-µH RF chokes. Other values can be used if desired. The rule of thumb is that using a larger value RF choke improves low-frequency performance while using a smaller RF choke improves high-frequency performance. RF chokes must be between 10 µH and 300 nH in value. Values outside this range can work, but performance must be thoroughly verified before committing to a design.

7.5 Programming

7.5.1 Digital Control

The LMH6521 supports three modes of gain control: parallel mode, serial mode (SPI compatible), and pulse mode. Parallel mode is fastest and requires the most board space for logic line routing. Serial mode is compatible with existing SPI compatible systems. The pulse mode is both fast and compact, but must step through intermediate gain steps when making large gain changes.

Pins MOD0 and MOD1 are used to configure the LMH6521 for the three gain control modes. MOD0 and MOD1 have weak pullup resistors to an internal 2.5-V reference but is designed for 2.5-V to 5-V CMOS logic levels. MOD0 and MOD1 can be externally driven (LOGIC HIGH) to voltages between 2.5 V to 5 V to configure the LMH6521 into one of the three digital control modes. Some pins on the LMH6521 have different functions depending on the digital control mode. Table 1 lists these functions.

Table 1. Digital Control Mode Pin Functions

PIN NUMBER	PARALLEL MODE	SERIAL MODE	PULSE MODE
1	A3	SDI	DNA
2	A4	CLK	UPA
3	A5	NC	GND
4 (MOD0)	LOGIC HIGH (MOD0=1)	LOGIC LOW (MOD0=0)	LOGIC HIGH (MOD0=1)
5 (MOD1)	LOGIC HIGH (MOD1=1)	LOGIC HIGH (MOD1=1)	LOGIC LOW (MOD1=0)
6	B5	GND	GND
7	B4	NC	UPB
8	B3	NC	DNB
9	B2	NC	S1B
10	B1	NC	S0B
11	INB+		
12	INB-		
13	GND		
14	+5 V		
15		GND	
16	B0	GND	GND
17	OUTB+		
18	OUTB-		
19	ENB		
20	LATB	GND	GND
21	LATA	GND	GND
22	ENA		
23	OUTA-		
24	OUTA+		
25	A0	NC	GND
26	GND		
27	+5 V		
28	GND		

Programming (continued)

Table 1. Digital Control Mode Pin Functions (continued)

29	INA-		
30	INA+		
31	A1	SDO	S0A
32	A2	CS	S1A

7.5.2 Parallel Mode (MOD1 = 1, MOD0 = 1)

When designing a system that requires very fast gain changes parallel mode is the best selection. See Table 1 for pin definitions of the LMH6521 in parallel mode.

The LMH6521 has a 6-bit gain control bus as well as latch pins LATA and LATB for channels A and B. When the latch pin is low, data from the gain control pins is immediately sent to the gain circuit (that is, gain is changed immediately). When the latch pin transitions high the current gain state is held and subsequent changes to the gain set pins are ignored. To minimize gain change glitches multiple gain control pins must not change while the latch pin is low. Gain glitches could result from timing skew between the gain set bits. This is especially the case when a small gain change requires a change in state of three or more gain control pins. If continuous gain control is desired the latch pin can be tied to ground. This state is called transparent mode and the gain pins are always active. In this state the timing of the gain pin logic transitions must be planned carefully to avoid undesirable transients

ENA and ENB pins are provided to reduce power consumption by disabling the highest power portions of the LMH6521. The gain register preserves the last active gain setting during the disabled state. These pins float high and can be left disconnected if they won't be used. If the pins are left disconnected, a 0.01-µF capacitor to ground helps prevent external noise from coupling into these pins.

Figure 26, Figure 27, and Figure 28 show the various connections in parallel mode with respect to the latch pin.

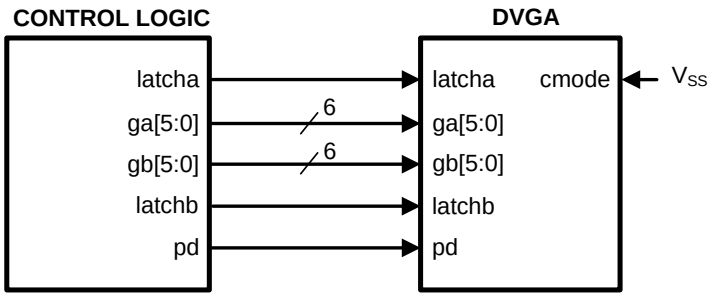
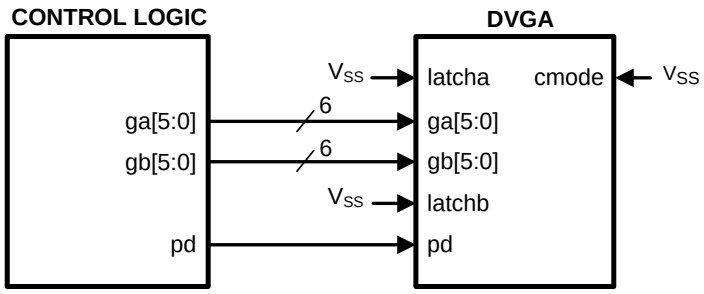


Figure 26. Parallel Mode Connection for Fastest Response



Latch pins tied to logic low state

Figure 27. Parallel Mode Connection Not Using Latch Pins

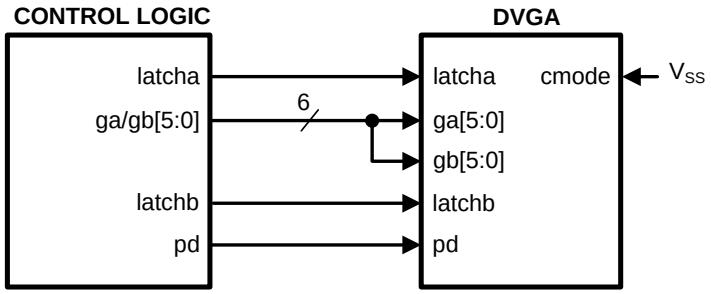


Figure 28. Parallel Mode Connection Using Latch Pins to Mulitplex Digital Data

7.5.3 Serial Mode: SPI Compatible Interface (MOD1 = 1, MOD0 = 0)

Serial interface allows a great deal of flexibility in gain programming and reduced board complexity. Using only 4 wires for both channels allows for significant board space savings. The trade-off for this reduced board complexity is slower response time in gain state changes. For systems where gain is changed only infrequently or where only slow gain changes are required serial mode is the best choice. See Table 1 table for pin definitions of the LMH6521 in serial mode.

The serial interface is a generic 4-wire synchronous interface that is compatible with SPI standard interfaces and used on many microcontrollers and DSP controllers.

The serial mode is active when the two mode pins are set as follows: MOD1=1, MOD0=0). In this configuration the pins function as shown in *Pin Configuration and Functions*. The SPI interface uses the following signals: clock input (CLK), serial data in (SDI), serial data out, and serial chip select (CS)

ENA and ENB pins are active in serial mode. For fast disable capability these pins can be used and the serial register holds the last active gain state. These pins float high and can be left disconnected for serial mode. The serial control bus can also disable the DVGA channels, but at a much slower speed. The serial enable function is an AND function. For a channel to be active both the enable pin and the serial control register must be in the enabled state. To disable a channel, either method will suffice. See *Typical Characteristics* for disable and enable timing information.

LATA and LATB pins are not active during serial mode.

The serial clock pin CLK is used to register the input data that is presented on the SDI pin on the rising edge; and to source the output data on the SDO pin on the falling edge. User may disable clock and hold it in the low state, as long as the clock pulse-width minimum specification is not violated when the clock is enabled or disabled.

The chip select pin CS starts a new register access with each assertion; that is, the SDATA field protocol is required. The user is required to deassert this signal after the 16th clock. If the SCSb is deasserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted-in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-width requirement for the deasserted pulse - which is specified in *Electrical Characteristics*.

SDI is an input pin for the serial data. It must observe setup or hold requirements with respect to the SCLK. Each cycle is 16-bits long

SDO is the data output pin and is normally at TRI-STATE and is driven only when SCSb is asserted. Upon SCSb assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. Upon power up, the default register address is 00h.

The SDO internal driver circuit is an open-collector device with a weak pullup resistor to an internal 2.5-V reference. It is 5-V tolerant so an external pullup resistor can connect to 2.5 V, 3.3 V, or 5 V as shown in Figure 30. However, the external pullup resistor must be chosen to limit the current to 11 mA or less. Otherwise the SDO logic low output level (V_{OL}) may not achieve close to ground and in extreme case could cause problem for FPGA input gate. Using minimum values for external pullup resistor is a good to maximize speed for SDO signal. So if high SPI clock frequency is required, then minimum value external pullup resistor is the best choice as shown in Figure 30.

Each serial interface access cycle is exactly 16 bits long as shown in Figure 29. Each signal's function is described below. The read timing is shown in Figure 31, while the write timing is shown in figure Figure 32.

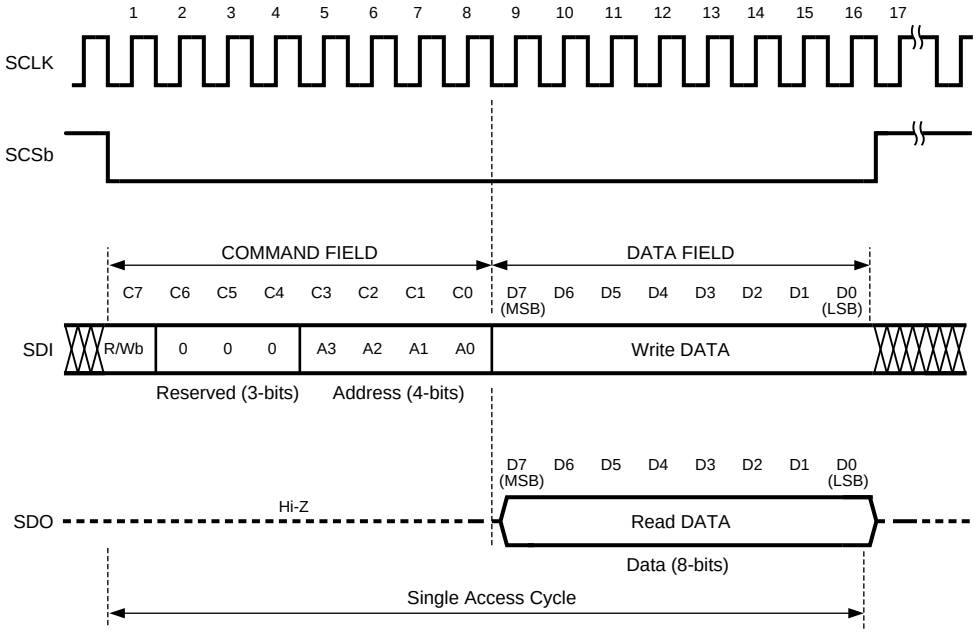


Figure 29. Serial Interface Protocol (SPI Compatible)

Table 2. Serial Interface Protocol

ADDRESS	DESCRIPTION
R/Wb	Read / Write bit. A value of 1 indicates a read operation, while a value of 0 indicates a write operation.
Reserved	Not used. Must be set to 0.
ADDR	Address of register to be read or written.
DATA	In a write operation the value of this field is written to the addressed register when the chip select pin is deasserted. In a read operation this field is ignored.

Table 3. Serial Word Format for LMH6521

C7	C6	C5	C4	C3	C2	C1	C0
0 = write 1 = read	0	0	0	0	0	0	0 = Ch A 1 = Ch B

Table 4. Serial Word Format for LMH6521 (cont)

Enable	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0	RES
0 = Off 1 = On	1 = +16 dB	1 = +8 dB	1 = +4 dB	1 = +2 dB	1 = +1 dB	1 = +0.5 dB	0

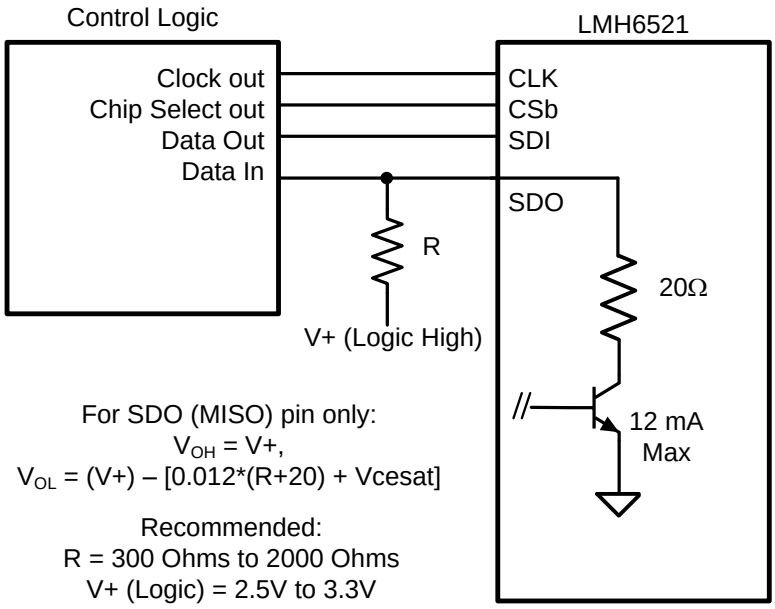


Figure 30. Serial Mode 4–Wire Connection

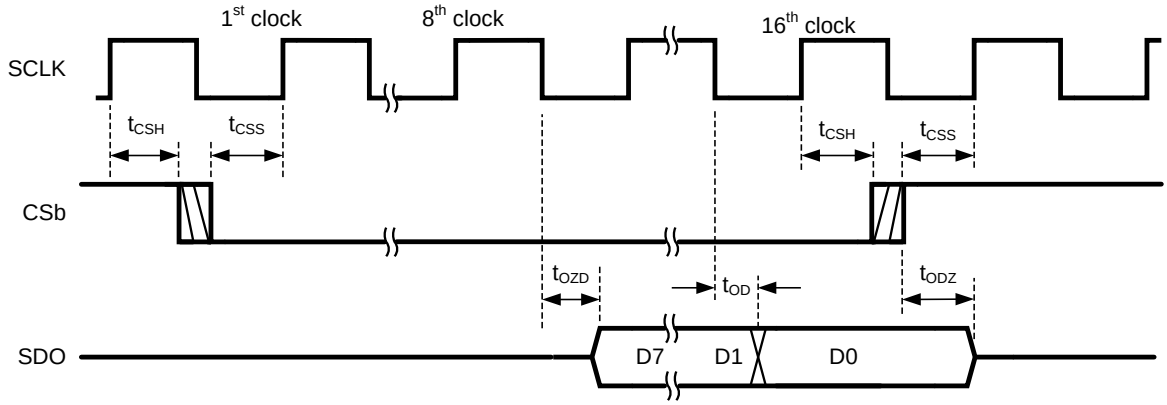


Figure 31. Read Timing

Table 5. Read Timing, Data Output on SDO Pin

PARAMETER	DESCRIPTION
t_{CSH}	Chip select hold time
t_{CSS}	Chip select setup time
t_{OZD}	Initial output data delay
t_{ODZ}	High impedance delay
t_{OD}	Output data delay

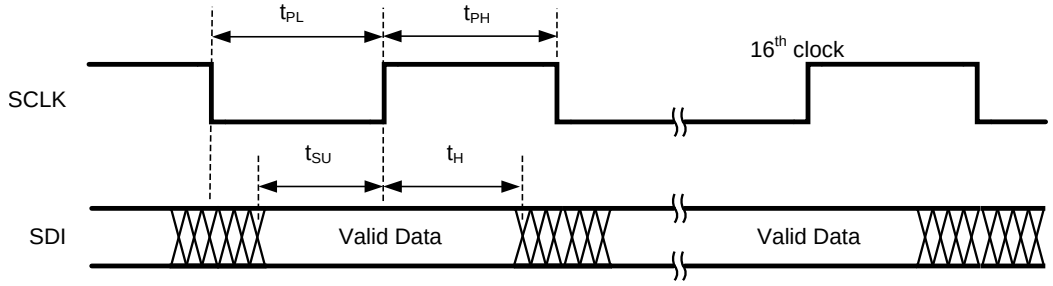


Figure 32. Write Timing, Data Written to SDI Pin

Table 6. Write Timing, Data Input on SDI Pin

PARAMETER	DESCRIPTION
t_{PL}	Minimum clock low time (clock duty dycle)
t_{PH}	Minimum clock high time (clock duty cycle)
t_{SU}	Input data setup time
t_H	Input data hold time

7.5.4 Pulse Mode (MOD1 = 0, MOD0 = 1)

Pulse mode is a simple yet fast way to adjust gain settings. Using only two control lines per channel the LMH6521 gain can be changed by simple up and down signals. Gain step sizes is selectable either by hard wiring the board or using two additional logic inputs. For a system where gain changes can be stepped sequentially from one gain to the next and where board space is limited this mode may be the best choice. The ENA and ENB pins are fully active during pulse mode, and the channel gain state is preserved during the disabled state. See Table 1 for pin definitions of the LMH6521 in pulse mode.

In this mode the gain step size can be selected from a choice of 0.5-, 1-, 2-, or 6-dB steps. During operation the gain can be quickly adjusted either up or down one step at a time by a negative pulse on the UP or DN pins. As shown in Figure 34, each gain step pulse must have a logic high state of at least t_{PW}= 20 ns and a logic low state of at least t_{PG}= 20 ns for the pulse to register as a gain change signal.

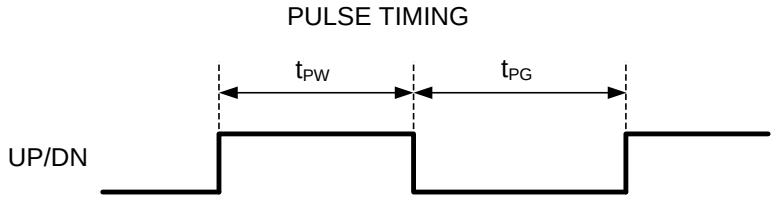


Figure 33. Pulse Timing

To provide a known gain state, there is a reset feature in pulse mode. To reset the gain to maximum gain both the UP and DN pins must be strobed low together as shown in Figure 34. There must be an overlap of at least t_{RW} = 20 ns for the reset to register.

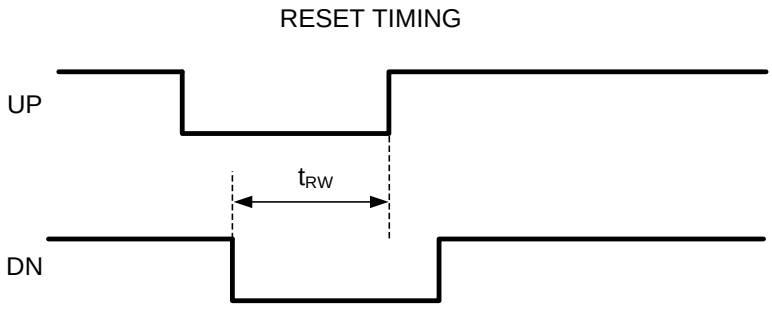


Figure 34. Pulse Mode Timing

7.5.5 Interface to ADC

The LMH6521 was designed to be used with TI's high speed ADC's. As shown in Figure 38, AC coupling provides the best flexibility especially for IF sub-sampling applications.

The inputs of the LMH6521 will self bias to the optimum voltage for normal operation. The internal bias voltage for the inputs is approximately mid-rail which is 2.5 V with the typical 5-V power supply condition. In most applications the LMH6521 input is required to be AC coupled.

The LMH6521 output common mode voltage is biased to 0 V and has a maximum differential output voltage swing of 10 V_{PPD} as shown in Figure 35. This means that for driving most ADCs AC coupling is required. Because most often a band pass filter is desired, the amplifier and ADC the bandpass filter can be configured to block the DC voltage of the amplifier output from the ADC input. Figure 36 shows a wideband bandpass filter configuration that could be designed for a 200-Ω impedance system for various IF frequencies.

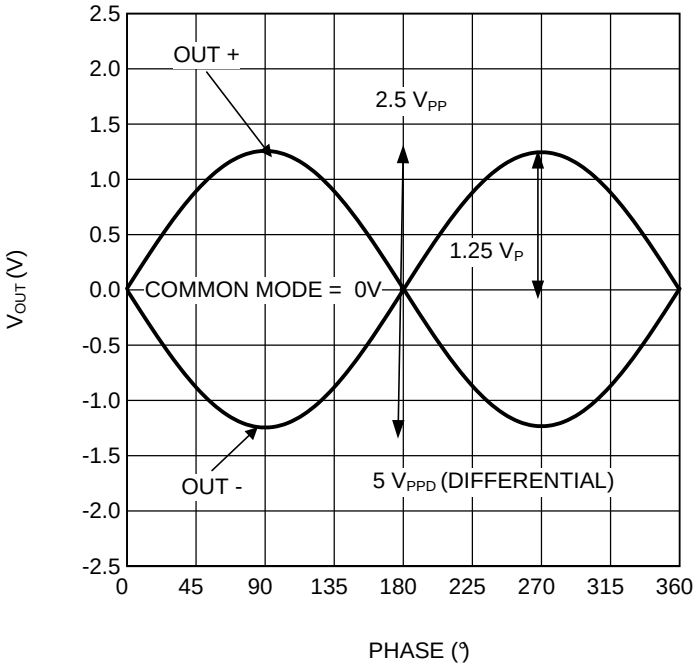


Figure 35. Output Voltage with Respect to Output Common Mode

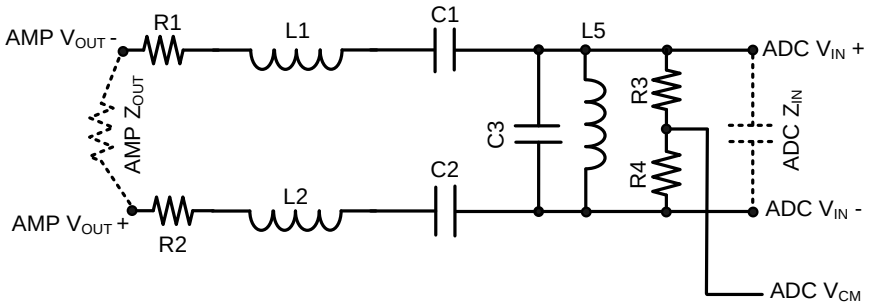


Figure 36. Wideband Bandpass Filter

Table 7 shows values for some common IF frequencies for Figure 36. The filter shown in Figure 36 offers a good compromise between bandwidth, noise rejection, and cost. This filter topology works best with the 12- to 16-bit analog to digital converters shown in Table 8.

Table 7. IF Frequency Bandpass Filter Component Values

CENTER FREQUENCY	75 MHz	150 MHz	180 MHz	250 MHz

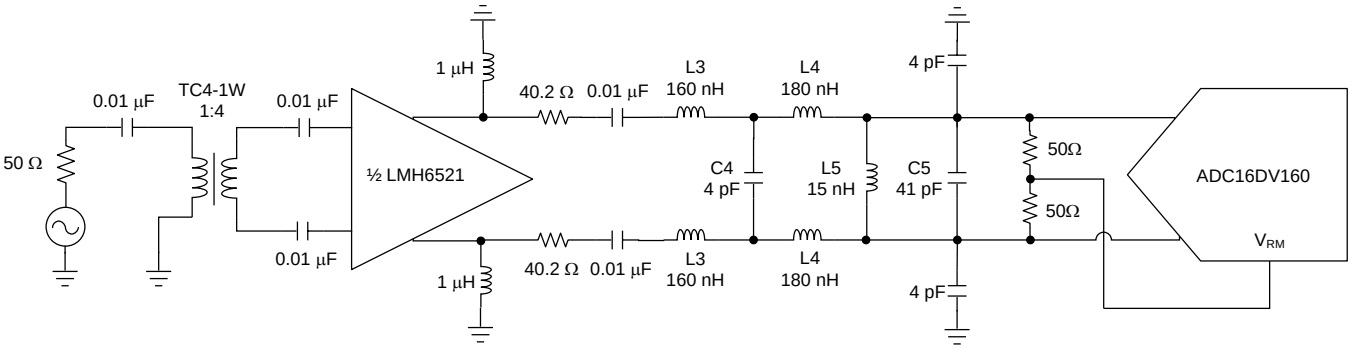
Table 7. IF Frequency Bandpass Filter Component Values (continued)

Bandwidth	40 MHz	60 MHz	75 MHz	100 MHz
R1, R2	90 Ω	90 Ω	90 Ω	90 Ω
L1, L2	390 nH	370 nH	300 nH	225 nH
C1, C2	10 pF	3 pF	2.7 pF	1.9 pF
C3	22 pF	19 pF	15 pF	11 pF
L5	220 nH	62 nH	54 nH	36 nH
R3, R4	100 Ω	100 Ω	100 Ω	100 Ω

Table 8. Compatible High-Speed Analog-to-Digital Converters

PRODUCT NUMBER	MAX SAMPLING RATE (MSPS)	RESOLUTION	CHANNELS
ADC12L063	62	12	SINGLE
ADC12DL065	65	12	DUAL
ADC12L066	66	12	SINGLE
ADC12DL066	66	12	DUAL
CLC5957	70	12	SINGLE
ADC12L080	80	12	SINGLE
ADC12DL080	80	12	DUAL
ADC12C080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12C170	170	12	SINGLE
ADC12V170	170	12	SINGLE
ADC14C080	80	14	SINGLE
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE
ADC14V155	155	14	SINGLE
ADC16V130	130	16	SINGLE
ADC16DV160	160	16	DUAL
ADC08D500	500	8	DUAL
ADC08500	500	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC081000	1000	8	SINGLE
ADC08D1500	1500	8	DUAL
ADC081500	1500	8	SINGLE
ADC08(B)3000	3000	8	SINGLE
ADC08L060	60	8	SINGLE
ADC08060	60	8	SINGLE
ADC10DL065	65	10	DUAL
ADC10065	65	10	SINGLE
ADC10080	80	10	SINGLE
ADC08100	100	8	SINGLE
ADCS9888	170	8	SINGLE
ADC08(B)200	200	8	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE

An alternate narrowband filter approach is presented in Figure 37. The narrow band-pass antialiasing filter between the LMH6521 and ADC16DV160 attenuates the output noise of the LMH6521 outside the Nyquist zone helping to preserve the available SNR of the ADC. Figure 37 shows a 1:4 input transformer used to match the 200-Ω balanced input of the LMH6521 to the 50 unbalanced source to minimize insertion lost at the input. Figure 37 shows the LMH6521 driving the ADC16DV160 (16-bit ADC). The band-pass filter is a 3rd order 100-Ω matched tapped-L configured for a center frequency of 192 MHz with a 20-MHz bandwidth across the differential inputs of the ADC16DV160. The ADC16DV160 is a dual channel 16-bit ADC with maximum sampling rate of 160 MSPS. Using a 2-tone large input signal with the LMH6521 set to maximum gain (26dB) to drive an input signal level at the ADC of –1 dBFS, the SNR and SFDR results are shown in Table 9.



Center frequency is 192 MHz with a 20-MHz bandwidth. Designed for 200-Ω impedance.

Figure 37. Narrowband Tapped-L Bandpass Filter

Table 9. LMH6521+BPF+ADC16DV160 vs Typical ADC16DV160 Specifications

CONFIGURATION	ADC INPUT	SNR (dBFS)	SFDR (dBFS)
LMH6521+BPF+ADC16DV160	–1 dBFS	75.5	82
ADC16DV160 only	–1 dBFS	76	89

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Common applications for the LMH6521 would be an IF amplifier, RF amplifier, and ADC driver.

Many applications require impedance matching and filtering. The large voltage swing of the LMH6521 makes it ideal for use with a filter.

The LMH6521 is ideal for applications requiring variable gain and very high linearity for frequencies ranging from 1 MHz to 500 MHz. The LMH6521 can support output voltage swing up to 10 V_{PP}.

8.2 Typical Application

The most typical application for the LMH5621 is shown in Figure 38. In this application the LMH6521 is driving an ADC through a band pass filter.

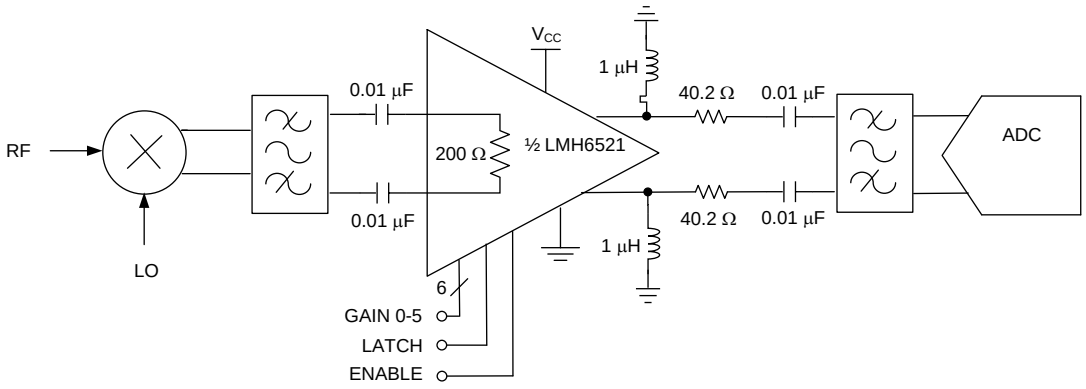


Figure 38. ADC Driver Application

8.2.1 Design Requirements

An ADC driver is required to deliver a full-scale signal to the ADC input pins with harmonic and intermodulation distortion products that meet the system requirements.

In this example we want to meet the following requirements:

- Amplifier output voltage: 4 V_{PP}
- SFDR > 80 dB at 300 MHz
- Noise voltage < 0 nV/rt Hz

8.2.2 Detailed Design Procedure

A voltage between 4.75 V and 5.25 V must be applied to the supply pin labeled 5 V. Each supply pin must be decoupled with a additional capacitance along with some low inductance, surface-mount ceramic capacitor of 0.01 µF as close to the device as possible where space allows.

The outputs of the LMH6521 are low impedance devices that requires connection to ground with 1-µH RF chokes and require AC-coupling capacitors of 0.01 µF. The input pins are self biased to 2.5 V and must be ac-coupled with 0.01-µF capacitors as well. The output RF inductors and AC-coupling capacitors are the main limitations for operating at low frequencies.

Typical Application (continued)

Each channel of the LMH6521 consists of a digital step attenuator followed by a low-distortion, 26-dB fixed gain amplifier and a low impedance output stage. The gain is digitally controlled over a 31.5-dB range from 26 dB to −5.5 dB. The LMH6521 has a 200-Ω differential input impedance and a low 20-Ω differential output impedance.

To enable each channel of the LMH6521, the ENA and ENB pins can be left to float, which internally is connected high with a weak pullup resistor. Externally connecting ENA and ENB to ground disables the channels of the LMH6521 and reduce the current consumption to 17.5 mA per channel.

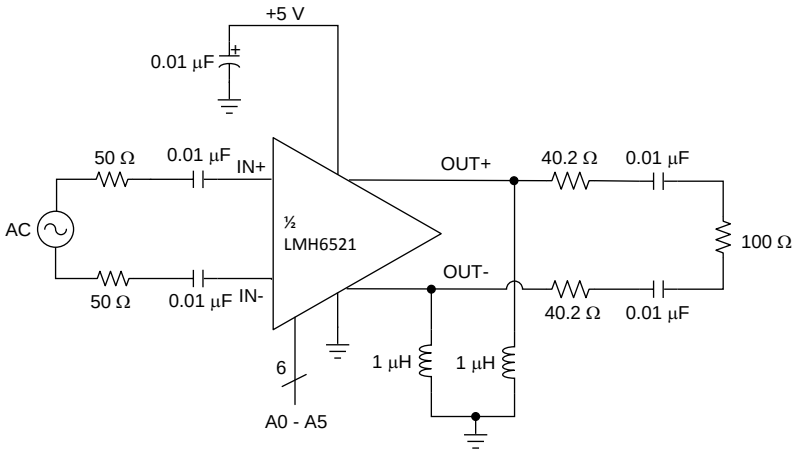


Figure 39. Basic Operating Connection

The LMH6521 meets the SFDR and output voltage swing requirements with no additional design details. However, the noise requires an additional filter as shown in Figure 38. The filter termination reduces the LMH6521 output noise voltage from 33 nV/rt Hz to 16.5 nV/rt Hz. A simple third order filter reduces out of band noise that would alias into the signal path. For filter details, see *Interface to ADC*.

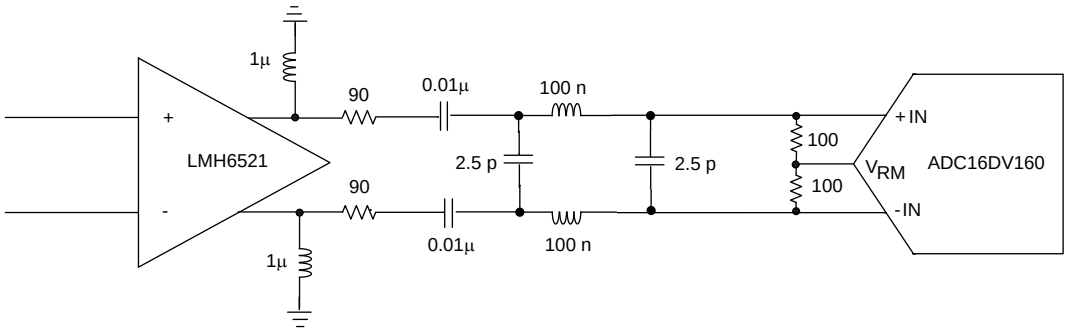


Figure 40. Filter Schematic

For further design assistance, see *SP16160CH1RB Reference Design Board User's Guide* (SNAU079).

Typical Application (continued)

8.2.3 Application Curve

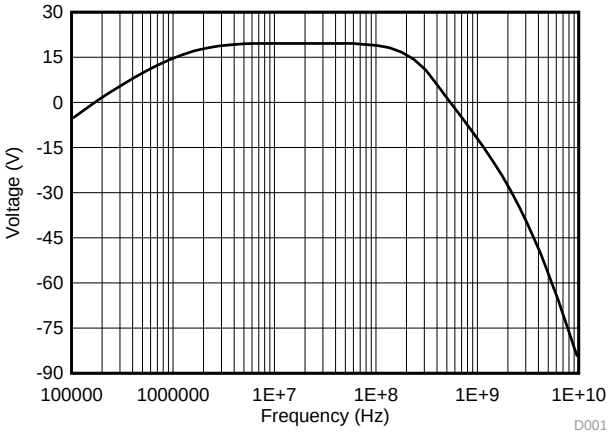


Figure 41. Filter Frequency Response

9 Power Supply Recommendations

The LMH6521 was designed primarily to be operated on 5-V power supplies. The voltage range for V_{CC} is 4.75 V to 5.25 V. When operated on a board with high-speed digital signals, it is important to provide isolation between digital signal noise and the LMH6521 inputs. *700-2700 MHZ Dual-Channel Receiver with 16-Bit ADC and 100 MHz IF Bandwidth Reference Design* (TIDA-00360) provides an example of good board layout.

10 Layout

10.1 Layout Guidelines

Layout for the LMH6521 is critical to achieve specified performance. Circuit symmetry is necessary for good HD2 performance. Input traces must be 200-Ω impedance transmission lines. To reduce output to input coupling, use ground plane fill between the amplifier input and output traces as shown in Figure 42. The output inductors contribute to crosstalk if placed too closely together. See Figure 42 for recommended placement of the output bias inductors. Output termination resistors and coupling capacitors must be placed as closely to the output inductors as possible.

10.2 Layout Example

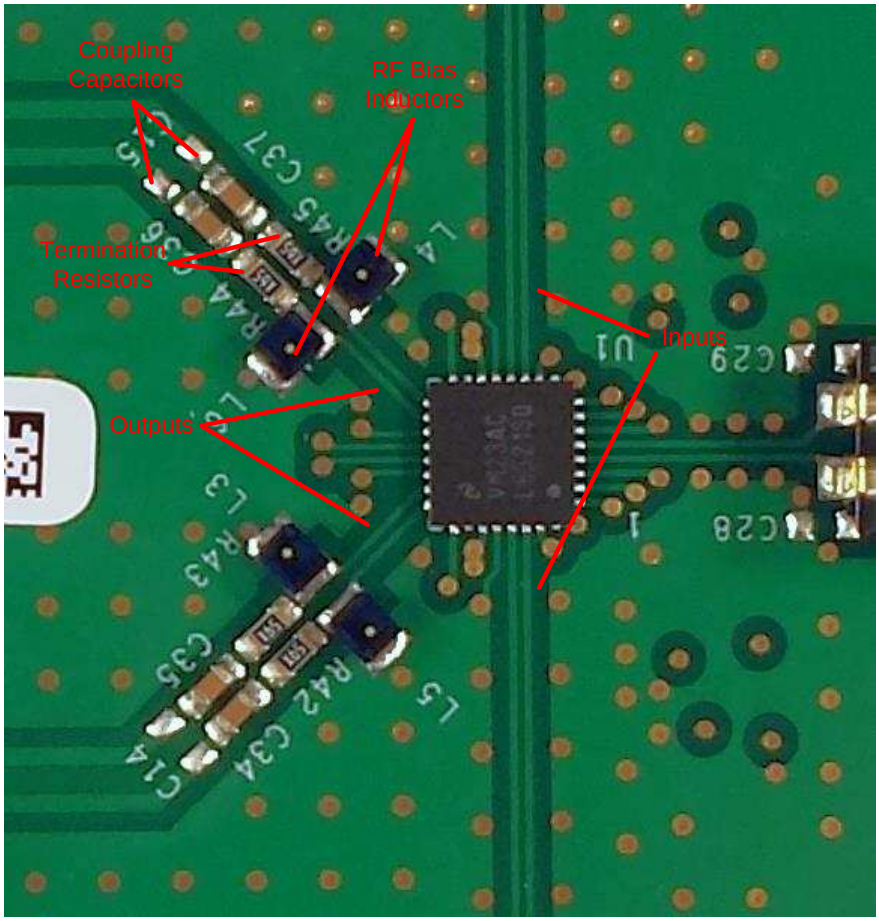


Figure 42. LMH6521 Layout Example

10.3 Thermal Considerations

The LMH6521 is packaged in a thermally enhanced WQFN package and features an exposed pad that is connected to the GND pins. TI recommends attaching the exposed pad directly to a large power supply ground plane for maximum heat dissipation. The thermal advantage of the WQFN package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board with the through vias planted underneath the thermal land. The thermal land can be connected to any ground plane within the PCB. However, it is also very important to maintain good high-speed layout practices when designing a system board.

The LMH6521EVAL evaluation board implemented an eight metal layer PCB with (a) 4 oz. copper inner ground planes (b) additonal through vias and (c) maximum bottom layer metal coverage to assist with device heat dissipation. These PCB design techniques assist with the heat dissipation of the LMH6521 to optimize distortion performance. See *AN–2045 LMH6521EVAL Evaluation Board* (SNOA551) for suggested layout techniques.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 《AN-2045 LMH6521EVAL 评估板》(SNOA551)
- 《SP16160CH1RB 参考设计电路板用户指南》(SNAU079)

11.2 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

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11.5 静电放电警告

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6521SQ/NOPB	Active	Production	WQFN (RTV) | 32	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6521SQ
LMH6521SQ/NOPB.A	Active	Production	WQFN (RTV) | 32	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6521SQ
LMH6521SQE/NOPB	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6521SQ
LMH6521SQE/NOPB.A	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6521SQ
LMH6521SQX/NOPB	Active	Production	WQFN (RTV) | 32	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6521SQ
LMH6521SQX/NOPB.A	Active	Production	WQFN (RTV) | 32	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6521SQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

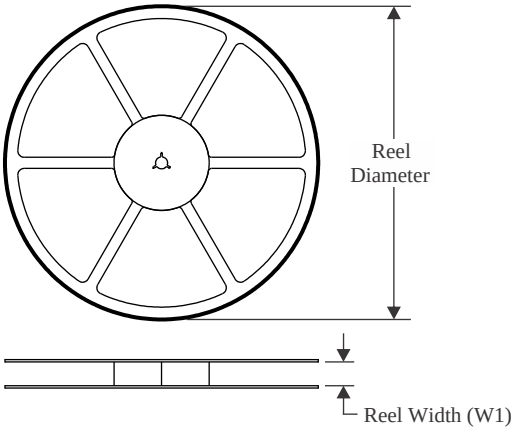
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

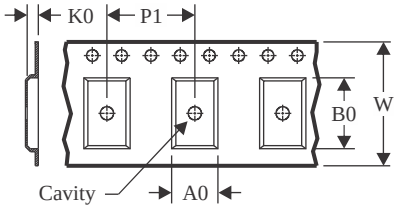
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

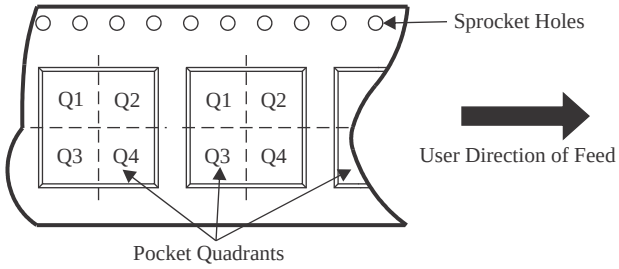


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

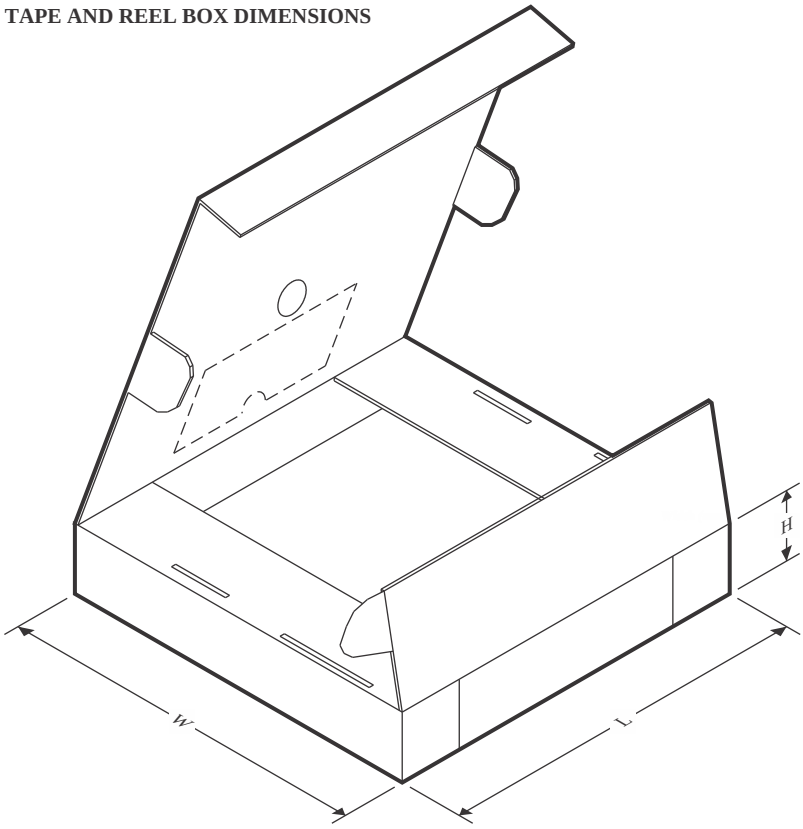
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6521SQ/NOPB	WQFN	RTV	32	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMH6521SQE/NOPB	WQFN	RTV	32	250	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMH6521SQX/NOPB	WQFN	RTV	32	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

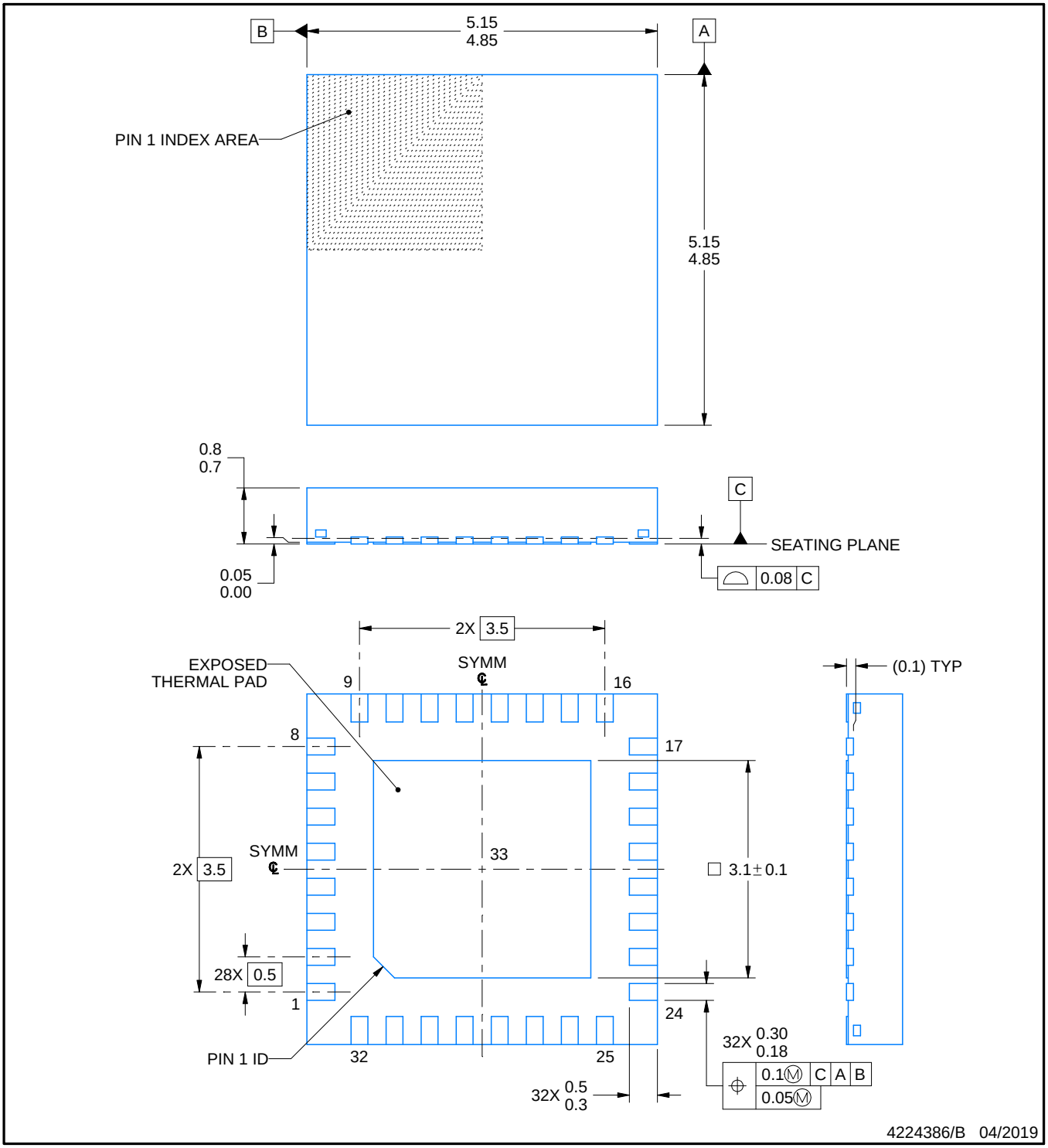
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6521SQ/NOPB	WQFN	RTV	32	1000	208.0	191.0	35.0
LMH6521SQE/NOPB	WQFN	RTV	32	250	208.0	191.0	35.0
LMH6521SQX/NOPB	WQFN	RTV	32	4500	356.0	356.0	36.0

PACKAGE OUTLINE

RTV0032A

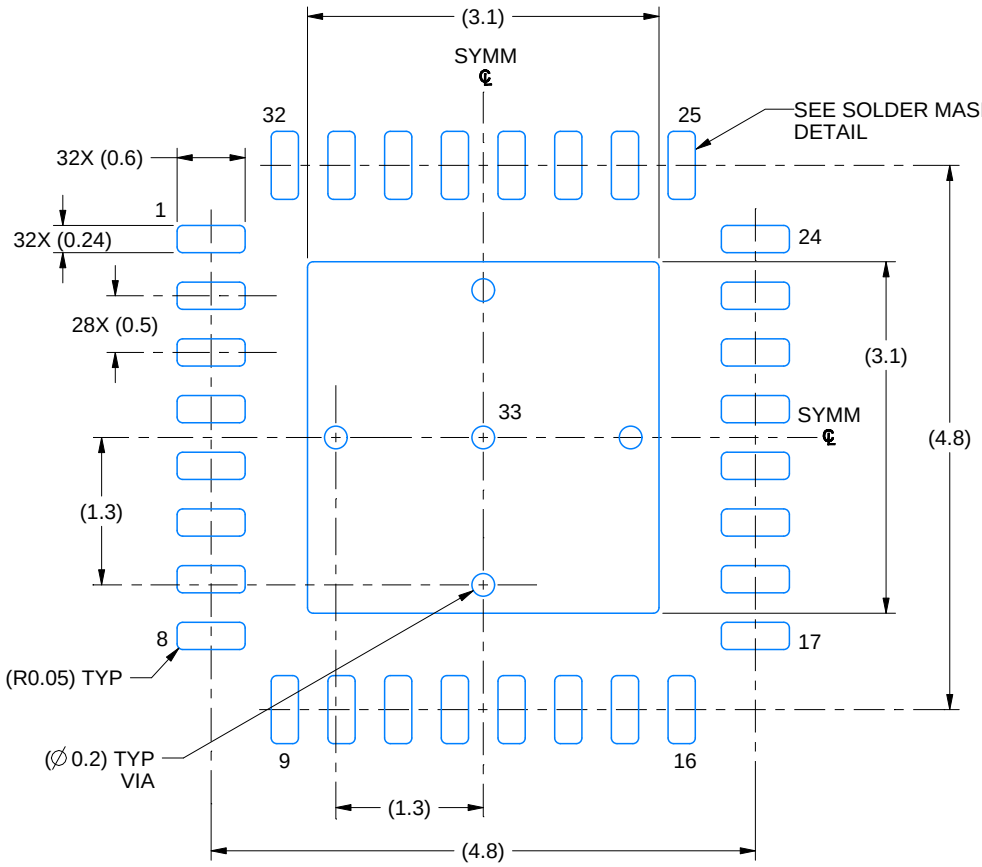
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

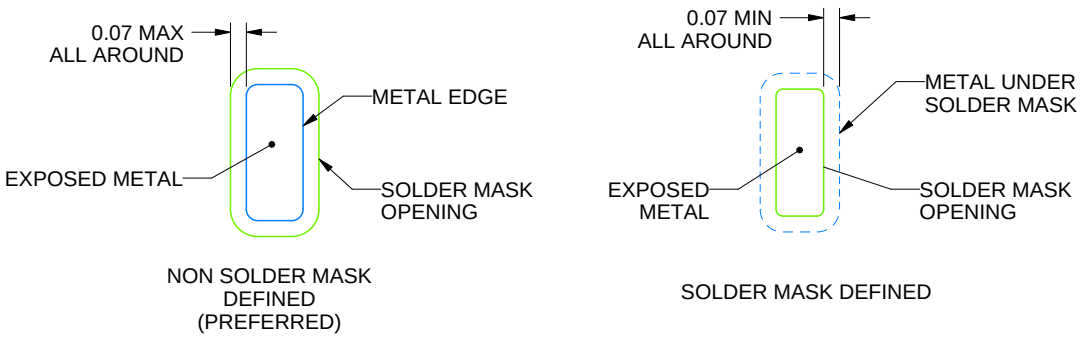


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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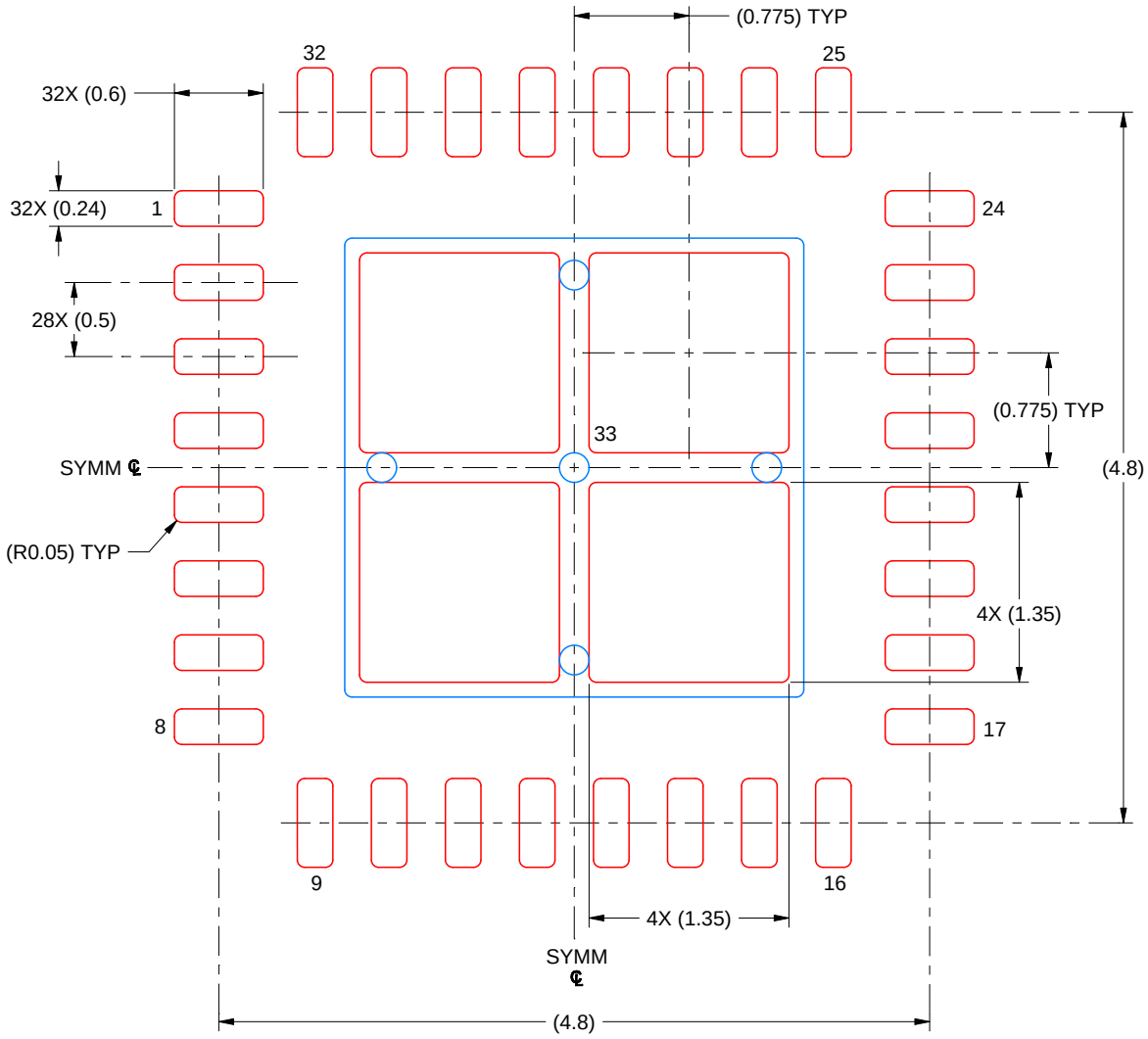
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224386/B 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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