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LMH1219

Reference

Design

ZHCSIC9D-APRIL 2016-REVISED JUNE 2018

# LMH1219 具有集成时钟恢复器的低功耗 12G UHD 自适应电缆均衡器

Technical

Documents

#### 特性 1

- 支持 ST-2082-1(12G)、ST-2081-1(6G)、ST-424 (3G)、ST-292(HD) 和 ST-259(SD)
- 支持适用于 SMPTE 2022-5/6 的 SFF8431 (SFP+)
- 兼容 DVB-ASI 和 AES10 (MADI)
- 集成的无基准时钟恢复器锁定至 SMPTE 和 10GbE 速率: 11.88Gbps、5.94Gbps、2.97Gbps、 1.485Gbps 或经 1.001 分频的子速率、270Mbps 和 10.3125Gbps
- 在输入 0 (IN0) 端具有自适应电缆均衡器
- 电缆长度 (Belden 1694A): •
  - 11.88Gbps (4Kp60 UHD) 时 75m
  - 5.94Gbps (UHD) 时 120m
  - 2.97Gbps (FHD) 时 200m
  - 1.485Gbps (HD) 时 280m
  - 270 Mbps (SD) 时 600m
- 输入1(IN1)上具有自适应电路板走线均衡器
- 低功耗: 250mW (典型值)
- 省电模式: 16mW
- 集成输入回波损耗网络
- 2:1 输入多路复用, 1:2 扇出输出, 具有去加重功能
- 支持信号分离器模式(-6dB 启动幅值)
- 片上回路滤波器电容和眼图监视器
- 由 2.5V 单电源或片上 1.8V 稳压器供电
- 可通过控制引脚、SPI 或者 SMBus 接口进行配置 •
- 4mm×4mm 24 引脚 QFN 封装
- 工作温度范围: -40℃ 至 +85℃ •
- 应用 2
- 兼容 SMPTE 的串行数字接口
- UHDTV/4K/8K/HDTV/SDTV 视频
- 广播视频路由器、交换机、分布式放大器和监视器
- 数字视频处理和编辑
- 10GbE SDI 媒体网关

## 3 说明

🥭 Tools &

Software

LMH1219 是一款具有集成时钟恢复器的低功耗双输入 双输出自适应均衡器。该器件支持高达 11.88Gbps 的 SMPTE 视频速率以及基于 IP 传输的 10GbE 视频, 能够应用于 4K/8K 超高清 (UHD) 应用至 RTN。INO 端 的远距离自适应电缆均衡器设计用于均衡通过 75Ω 同 轴电缆传输的数据,可在较宽的传输速率下运行,支持 的速率范围为 125Mbps 到 11.88Gbps。IN1 上的自适 应电路板走线均衡器与 SFF-8431 兼容,并且支持 SMPTE 和 10GbE 数据速率。

Support &

Community

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集成时钟恢复器可削弱高频抖动并且提供出色的信号完 整性。该器件的高输入抖动容差改善了时序裕度。时钟 恢复器内置有回路滤波器,运行时无需精准的输入基准 时钟。非破坏性眼图监视器支持实时测量串行数据,从 而简化系统调试并加速电路板调通。

凭借集成的 2:1 复用和 1:2 扇出电路,该器件能够灵活 输出多种视频信号。输出驱动器提供可编程的去加重功 能,用于补偿其输出端的电路板走线损失。集成式回波 损耗网络在所有数据传输速率下均可满足严格的 SMPTE 规范要求。LMH1219 典型的功耗值为 250mW。无输入信号时,功耗会进一步降至 16mW。

LMH1219 与 LMH1226(12G UHD 时钟恢复器) 以及 LMH0324(3G 自适应电缆均衡器)引脚兼容。

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器件型号	封装	封装尺寸(标称值)
LMH1219	QFN (24)	4.00mm × 4.00mm

如需了解所有可用封装,请参阅产品说明书末尾的可订购产品 (1) 附录。



#### 简化框图



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# 4 修订历史记录

Changes from Revision C (October 2017) to Revision D	Page
<ul> <li>首次公开发布的完整生产版产品说明书,添加 TI 参考设计顶部导航图标链接</li> </ul>	1
Moved LMH1219 and LMH0324 Compatibility to Application Information	40
Changes from Revision B (February 2017) to Revision C	Page
<ul> <li>添加封装图</li> </ul>	50
Changes from Revision A (May 2016) to Revision B	Page
Changed eq_en_bypass bit description from "Gain Stages 3 and 4" to "Gain Stages 2 and 3"	29
Changed bit location of IN1 Carrier Detect Power Down Control from Reg 0x13[5] to Reg 0x15[6]	29

#### Changes from Original (April 2016) to Revision A

С	hanges from Original (April 2016) to Revision A	Page
•	Deleted min and max VOD_DE amplitude specification when VOD_DE = Level F	9
•	Changed typical VOD_DE amplitude specifications for Levels F, R, and L	9
•	Changed DEM value and DEM register settings in Table 5 to match correct VOD_DE pin logic levels	20
•	已添加 new row for VOD = 5, DEM = 5 setting in 表 10	43



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# 5 Pin Configuration and Functions



#### **Pin Functions**

PIN		uo(1)	DESCRIPTION			
NAME	NO.	1/0 ( )	DESCRIPTION			
High Speed Differ	ential I/O'S					
IN0+	1	I, Analog	Single-ended complementary inputs, $75-\Omega$ internal termination from IN0+ or IN0- to			
INO-	2	I, Analog	internal common mode voltage and return loss compensation network. Requires external 4.7- $\mu$ F AC coupling capacitors. IN0+ is the 75- $\Omega$ input port for the adaptive cable equalizer in SMPTE video applications.			
IN1+	4	I, Analog	Differential complementary inputs with internal 100- $\Omega$ termination. Requires external			
IN1-	5	I, Analog	4.7-μF AC coupling capacitors for SMPTE and 10 GbE.			
OUT0+	18	O, Analog	Differential complementary outputs with $100-\Omega$ internal termination. Requires external			
OUT0-	17	O, Analog	4.7-µF AC coupling capacitors. Output driver OUT0± can be disabled under user control.			
OUT1+	15	O, Analog	Differential complementary outputs with $100-\Omega$ internal termination. Requires external			
OUT1-	14	O, Analog	4.7-μF AC coupling capacitors. Output driver OUT1± can be disabled under user control.			
Control Pins		•	•			
LOCK_N	12	O, LVCMOS, OD	LOCK_N is the reclocker lock indicator for the selected input. LOCK_N is pulled LOW when the reclocker has acquired locking condition. LOCK_N is an open drain output, 3.3 V tolerant, and requires an external 2-k $\Omega$ to 5-k $\Omega$ pull-up resistor to logic supply. LOCK_N pin can be re-configured to indicate CD_N (Carrier Detect) or INT_N (Interrupt) for IN0 or IN1 through register programming.			
IN_OUT_SEL	8	I, 4-LEVEL	IN_OUT_SEL selects the signal flow at input ports to output ports. See Table 2 for details. This pin setting can be overridden by register control.			
OUT_CTRL	19	I, 4-LEVEL	OUT_CTRL selects the signal flow from the selected IN port to OUT0± and OUT1±. It selects reclocked data, reclocked data and clock, bypassed reclocker data (equalized data to output driver), or bypassed equalizer and reclocker data. See Table 4 for details. This pin setting can be overridden by register control.			

(1) I = Input, O = Output, IO = Input or Output, OD = Open Drain, LVCMOS = 2-State Logic, 4-LEVEL = 4-State Logic

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Texas

# Pin Functions (continued)

PIN		u(a)(1)	DESCRIPTION		
NAME	NO.	1/0\''	DESCRIPTION		
VOD_DE	11	I, 4-LEVEL	VOD_DE selects the driver output amplitude and de-emphasis level for both OUT0 $\pm$ and OUT1 $\pm$ . See Table 5 for details. This pin setting can be overridden by register control.		
MODE_SEL	6	I, 4-LEVEL	MODE_SEL enables SPI or SMBus serial control interface. See Table 6 for details.		
Serial Control Inte	erface (SPI I	Mode), MODE_SEL =	F (Float)		
SS_N	7	I, LVCMOS	SS_N is the Slave Select. When SS_N is at logic Low, it enables SPI access to the LMH1219 slave device. SS_N is a LVCMOS input referenced to VDDIO.		
MISO	20	O, LVCMOS	MISO is the SPI control serial data output from the LMH1219 slave device. MISO is a LVCMOS output referenced to VDDIO.		
MOSI	10	I, LVCMOS	MOSI is used as the SPI control serial data input to the LMH1219 slave device. MOSI is LVCMOS input referenced to VDDIO.		
SCK	21	I, LVCMOS	SCK is the SPI serial input clock to the LMH1219 slave device. SCK is LVCMOS referenced to VDDIO.		
Serial Control Interface (SMBus MODE) , MODE_SEL = L (1 k $\Omega$ to VSS)					
ADDR0	7	Strap, 4-LEVEL	ADDR[1:0] are SMBus address straps to select one of the 16 supported SMBus		
ADDR1	20	Strap, 4-LEVEL	addresses. ADDR[1:0] are 4-level straps and are read into the device at power up		
SDA	10	IO, LVCMOS, OD	SDA is the SMBus bi-directional open drain SDA data line to or from the LMH1219 slave device. SDA is an open drain IO and tolerant to 3.3 V. SDA requires an external 2-k $\Omega$ to 5-k $\Omega$ pull-up resistor to the SMBus termination voltage.		
SCL	21	I, LVCMOS, OD	SCL is the SMBus input clock to the LMH1219 slave device. It is driven by a LVCMOS open drain driver from the SMBus master. SCL is tolerant to 3.3 V and requires an external 2-k $\Omega$ to 5-k $\Omega$ pull up resistor to the SMBus termination voltage.		
Power					
VSS	3, 9, 16	I, Ground	Ground reference.		
VIN	24	I, Power	VIN is connected to an external power supply. It accepts either 2.5 V $\pm$ 5% or 1.8 V $\pm$ 5%. When VIN is powered from 2.5 V, VDD_LDO is the output of an on-chip LDO regulator. For lower power operation, both VIN and VDD_LDO should be connected to a 1.8 V supply.		
VDDIO	22	I, Power	VDDIO powers the LVCMOS IO and 4-level input logic and connects to 2.5 V $\pm$ 5%.		
VDD_LDO	23	IO, Power	VDD_LDO is the output of the internal 1.8 V LDO regulator when VIN is connected to a 2.5 V supply. VDD_LDO output requires external 1-µF and 0.1-µF bypass capacitors to VSS. The internal LDO is designed to power internal circuitry only. VDD_LDO is an input when VIN is powered from 1.8 V for lower power operation. When VIN is connected to a 1.8 V supply, both VIN and VDD_LDO should be connected to a 1.8 V supply.		
VDD_CDR	13	I, Power	VDD_CDR powers the reclocker circuitry and connects to 2.5 V $\pm$ 5% supply.		
EP		I, Ground	EP is the exposed pad at the bottom of the QFN package. The exposed pad must be connected to the ground plane through a via array. See 🕄 41 for details.		



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## 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
Supply Voltage for 2.5 V Mode (VDD_CDR, VIN, VDDIO)	-0.5	2.75	V
Supply Voltage for 1.8 V Mode (VIN, VDD_LDO)	-0.5	2.0	V
4-Level Input/Output Voltage (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL, ADDR0, ADDR1)	-0.5	2.75	V
SMBus Input/Output Voltage (SDA, SCL)	-0.5	4.0	V
SPI Input/Output Voltage (SS_N, MISO, MOSI, and SCK)	-0.5	2.75	V
Input Voltage (IN0±, IN1±)	-0.5	2.75	V
Input Current (IN0±, IN1±)	-30	30	mA
Junction Temperature		125	°C
Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) For soldering specifications, see application note SNOA549.

## 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Flaatraatatia diaabaraa	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4500	V
	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	v

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions. Pins listed as ±4500 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions. Pins listed as ±1500 V may actually have higher performance.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Single Supply Mode <sup>(1)</sup>	VIN, VDDIO, VDD_CDR to VSS		2.375	2.5	2.625	V
Dual Supply	VIN, VDD_LDO to VSS		1.71	1.8	1.89	V
Mode <sup>(2)(3)</sup>	VDD_CDR, VDDIO to VSS		2.375	2.5	2.625	v
VDD <sub>SMBUS</sub>	SMBus: SDA, SCL Open Drain Termination	Voltage	2.375		3.6	V
	Source Launch Amplitude before coaxial cable	Normal mode	0.72	0.8	0.88	Vp-p
VIN0_LAUNCH		Splitter mode	0.36	0.4	0.44	
	Source Differential Launch Amplitude	before 5-inch board trace	300		850	mVp-p
VIN1_LAUNCH		before 20-inch board trace	650		1000	
T <sub>JUNCTION</sub>	Operating Junction Temperature				100	°C
T <sub>AMBIENT</sub>	Ambient Temperature		-40	25	85	°C
NTps <sub>max</sub> <sup>(4)</sup>	Maximum Supply Noise Tolerance	50 Hz to 1 MHz, sinusoidal		<20		mVp-p
		1.1 MHz to 6 GHz, sinusoidal		<10		

(1) In Single Supply Mode, the VIN, VDDIO and VDD\_CDR supplies are 2.5 V. The VDD\_LDO is the 1.8 V LDO output of an internal LDO regulator, the VDD\_LDO pin should not be connected to any external supply voltage.

(2) In Dual Supply Mode, the VIN and VDD\_LDO are connected to a 1.8 V supply, while the VDD\_CDR and VDDIO supplies are 2.5 V.

(3) In Dual Supply Mode, the VDDIO and VDD\_CDR supply should be powered before or at the same time as VIN and VDD\_LDO = 1.8 V.

(4) The sum of the DC supply voltage and AC supply noise should not exceed the recommended supply voltage range.

## 6.4 Thermal Information

		LMH1219	
	THERMAL METRIC <sup>(1)(2)</sup>	RTW (QFN)	UNIT
		24 PINS	
$R_{\thetaJA}$	Junction-to-ambient thermal resistance	33.2	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.2	°C/W
TLΨ	Junction-to-top characterization parameter	0.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	11.3	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).

(2) No heat sink is assumed for these estimations. Depending on the application, a heat sink, faster air flow, and/or reduced ambient temperature (< 85°C) may be required to maintain the maximum junction temperature specified in *Electrical Characteristics*.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

P	ARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD <sub>DUAL</sub>	Power Dissipation, Dual Supply Mode	Measured with PRBS-10, Locked to 11.88 Gbps at IN0+, VOD = default, only OUT0 enabled		250		mW
PD <sub>Z_DUAL</sub>	Power Dissipation, Dual Supply Mode	Power Save Mode, no input signal		16		mW
PD <sub>SINGLE</sub>	Power Dissipation, Single Supply Mode	Measured with PRBS-10, Locked to 11.88 Gbps at IN0+, VOD = default, only OUT0 enabled		290		mW
PD <sub>Z_SINGLE</sub>	Power Dissipation, Single Supply Mode	Power Save Mode, no input signal		27		mW
IDD <sub>DUAL</sub>	Current Consumption, Dual Supply Mode	Measured at 2.5 V supply with PRBS-10, Locked to 11.88 Gbps at IN0+, VOD = Default, only OUT0 enabled		64	70	mA
		Measured at 1.8 V supply with PRBS-10, Locked to 11.88 Gbps at IN0+, VOD = Default, only OUT0 enabled		50	62	
IDD <sub>Z_DUAL</sub>	Current Consumption, Dual Supply Mode	Forced Power Save Mode, MODE_SEL = LEVEL-H, Measured at 2.5 V supply		4	5	~^^
		Forced Power Save Mode, MODE_SEL = LEVEL-H, Measured at 1.8 V supply		3	9	ША
	Current Consumption, Dual Supply Mode Acquiring Lock, HEO/VEO Lock Monitor Disabled	Measured at 2.5 V supply with PRBS-10, IN1±, Acquiring Lock VOD = Default, OUT0 and OUT1 enabled		90	101	<b>m</b> 4
TRANS_DUAL		Measured at 1.8 V supply with PRBS-10, IN1±, Acquiring Lock VOD = Default, OUT0 and OUT1 enabled		30	37	ШA
VDD <sub>LDO</sub>	LDO 1.8 V Output Voltage	VIN = 2.5 V, Single Supply Mode	1.71	1.8	1.89	V



# **Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

I	PARAMETER	CONDITIONS	MIN	TYP MA	X UNIT
LVCMOS DC	SPECIFICATIONS				
		2-Level Input (SS_N, SCK, MOSI), VDDIO = 2.5 V	0.7 × VDDIO	VDDIO + 0	.3
VIH	High Level Input Voltage	2-Level Input (SCL, SDA), VDDIO = 2.5 V	0.7 × VDDIO	3	.6
		2-Level Input (SS_N, SCK, MOSI), VDDIO = 2.5 V	-0.3	0.3 × VDD	0
VIL	Low Level Input Voltage	2-Level Input (SCL, SDA), VDDIO = 2.5 V	0	0.3 × VDD	0
V <sub>OH</sub>	High Level Output Voltage	$I_{OH} = -2$ mA, (MISO), VDDIO = 2.5 V	0.8 × VDDIO	VDD	o v
	Low Level Output	$I_{OL}$ = 2 mA, (MISO), VDDIO = 2.5 V	0	0.2 × VDD	0
VOL	Voltage	$I_{OL}$ = 3 mA, (LOCK_N, SCL, SDA), VDDIO = 2.5 V		C	.4
	Input High Lookogo	SPI Mode: LVCMOS (SS_N, SCK, MOSI), Vinput = VDDIO			5
IIH	Current	SMBus Mode: LVCMOS (LOCK_N, SCL, SDA), Vinput = VDDIO			μΑ 0
		SPI Mode: LVCMOS (SS_N), Vinput = VSS	-40		
Input Low Leaka I <sub>IL</sub> Current	Input Low Leakage	SPI Mode: LVCMOS (SCK, MOSI), Vinput = VSS	-15		μA
	Guneni	SMBus Mode: LVCMOS (LOCK_N, SCL, SDA), Vinput = VSS	-10		
4-LEVEL LOG	IC DC SPECIFICATIONS (F	REFERENCE TO VDDIO, APPLY TO	ALL 4-LEVEL IN	IPUT CONTROL PINS)	
V <sub>4_LVL_H</sub>	LEVEL-H Input Voltage	Pull-up 1 kΩ to VDDIO		VDDIO	V
$V_{4\_LVL\_F}$	LEVEL-F Default Voltage	Float, VDDIO = 2.5 V		2/3 × VDDIO	V
V <sub>4_LVL_R</sub>	LEVEL-R Input Voltage	External Pull-down 20 k $\Omega$ to VSS, VDDIO = 2.5 V		1/3 × VDDIO	V
V <sub>4_LVL_L</sub>	LEVEL-L Input Voltage	External Pull-down 1 k $\Omega$ to VSS		0	V
Іатугін	Input High Leakage	4-Levels (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL), Vinput = VDDIO	20	45 8	30 µA
	Current	SMBus Mode: 4-Levels (ADDR0, ADDR1), Vinput = VDDIO	20	45 8	30
I4 LVL IL	Input Low Leakage	4-Levels (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL), Vinput = VSS	-160	-93 -4	μA
Current		SMBus Mode: 4-Levels (ADDR0, ADDR1), Vinput = VSS	-160	-93 -4	10
RECEIVER SPECIFICATIONS (IN0+)					
R <sub>IN0_TERM</sub>	DC Input Termination	IN0+ and IN0- to VSS	63	75 8	37 Ω
		S11, 5 MHz to 1.485 GHz		-20	
RI wa ave	Input Return Loss	S11, 1.485 GHz to 3 GHz		-18	dB
INU_S11	Reference to 75 $\Omega^{(1)}$	S11, 3 GHz to 6 GHz		–13	uВ
		S11, 6 GHz to 12 GHz		-6.5	
V <sub>IN0_CM</sub>	IN0 DC Common Mode Voltage	Input common mode voltage at IN0+ or IN0- to VSS		1.4	V

(1) This parameter was measured with an LMH1219EVM.



# **Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

F	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNIT
	Input DC Wonder	SD, signal at IN0+, Input launch amplitude = 0.8 Vp-p		100		m\/n-n
VWANDER	input DC wander	HD, 3G, 6G, 12G, signal at IN0+, Input launch amplitude = 0.8 Vp-p		50		шүр-р
RECEIVER SF	PECIFICATIONS (IN1±)					
R <sub>IN1_TERM</sub>	DC Input Differential Termination	Measured across IN1+ to IN1-	80	100	120	Ω
		SDD11, 10 MHz - 2.8 GHz		-21		
RL <sub>IN1_SDD11</sub>	Input Differential Return	SDD11, 2.8 GHz - 6 GHz		-17		dB
2033	2000	SDD11, 6 GHz - 11.1 GHz		8		
RL <sub>IN1_SCD11</sub>	Differential to Common Mode Conversion <sup>(1)</sup>	SCD11, 10 MHz to 11.1 GHz		-23		dB
V <sub>IN1_CM_TOL</sub>	Input AC Common Mode Voltage Tolerance			15		mV (rms)
V <sub>IN1_CM</sub>	IN1 DC Common Mode Voltage	Input common mode voltage at IN1+ or IN1- to VSS		2.06		V
	CD N = LOW Carrier	10.3125 Gbps, 1010 Clock Pattern		39		
	Detect (Default) Assert	10.3125 Gbps, PRBS-31 Pattern		25		mVn-n
ON Threshold Level for input voltage	11.88 Gbps, EQ and PLL Pathological Pattern		20			
	CD N = HIGH, Carrier	10.3125 Gbps, 1010 Clock Pattern		15		
	Detect (Default) De-	10.3125 Gbps, PRBS-31 Pattern		15		m\/n-n
	Assert OFF Threshold Level	11.88 Gbps, EQ and PLL Pathological Pattern		18		



# **Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

I	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTE	R OUTPUT (OUT0± AND O	UT1±)				
		8T pattern, VOD_DE = LEVEL-H, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		410		
	Output Differential	8T pattern, VOD_DE = LEVEL-F, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE	485	560	620	<ul> <li>UNIT</li> <li>mVp-p</li> <li>mVp-p</li> <li>mVp-p</li> <li>dB</li> </ul>
	Voltage <sup>(2)</sup>	8T pattern, VOD_DE = LEVEL-R, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		635		
		8T pattern, VOD_DE = LEVEL-L, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		810		
De-emphasized		8T pattern, VOD_DE = LEVEL-H, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		410		
	De-emphasized Output	8T pattern, VOD_DE = LEVEL-F, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		500		
VOD <sub>DE</sub>	Differential Voltage <sup>(2)</sup>	8T pattern, VOD_DE = LEVEL-R, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		480		шүр-р
		8T pattern, VOD_DE = LEVEL-L, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		480		
R <sub>OUT_TERM</sub>	DC Output Differential Termination	Measured across OUTn+ and OUTn-	80	100	120	Ω
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time (3)	20% - 80% using 8T Pattern SD, HD, 3G, 6G, 12G and 10 GbE, measured after 1 inch trace		45		ps
	Output Differential	SDD22, 10 MHz - 2.8 GHz		-17		
RI TV ODDOO	Return Loss Measured	SDD22, 2.8 GHz - 6 GHz		-15		dB
RLTX-SDD22	Up and Outputs a 10- MHz Clock Signal <sup>(3)</sup>	SDD22, 6 GHz - 11.1 GHz		-15		ŭD
	Output Common Mode	SCC22, 10 MHz - 4.75 GHz		-12		
RL <sub>TX-SCC22</sub>	Return Loss Measured with the Device Powered Up and Outputs a 10- MHz Clock Signal <sup>(3)</sup>	SCC22, 4.75 GHz - 11.1 GHz		-12		dB
V <sub>TX_CM</sub>	AC Common Mode Voltage <sup>(3)</sup>	Default Setting, PRBS-31, 10.3125 Gbps		5		mV (rms)

(2) ATE production tested with DC method.(3) This parameter was measured with an LMH1219EVM.



# **Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNIT
OUTPUT JIT	TER					
		11.88 Gbps, PRBS-10, TX launch amplitude = 720 mV, 75 m Belden 1694A at IN0+		0.11	0.15	UI
		5.94 Gbps, PRBS-10, TX launch amplitude = 720 mV, 120 m Belden 1694A at IN0+		0.106		UI
	Total littar (PEPc1a 12)	2.97 Gbps, PRBS-10, TX launch amplitude = 720 mV, 200 m Belden 1694A at IN0+		0.075		UI
TJ	Reclocked Output <sup>(4)</sup>	1.485 Gbps, PRBS-10, TX launch amplitude = 720 mV, 300 m Belden 1694A at IN0+		0.07		UI
		270 Mbps, PRBS-10, TX launch amplitude = 720 mV, 600 m Belden 1694A at IN0+		0.07		UI
		10.3125 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.09	0.15	UI
	Devide as l'iter	11.88 Gbps, PRBS-10, TX launch amplitude = 720 mV, 75 m Belden 1694A at IN0+		5.7		mUI (rms)
RJ	Reclocked Output	10.3125 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		4.1	mUI	mUI (rms)
DJ	Datarministia littar	11.88 Gbps, PRBS-10, TX launch amplitude = 720 mV, 75 m Belden 1694A at IN0+		40		mUI
	Reclocked Output	10.3125 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		34		mUl
TJ <sub>RAW</sub>	Total Jitter (BER≤1e-12), RAW (Reclocker	125 Mbps, PRBS-10, TX launch amplitude = 800 mV, 600 m Belden 1694A at IN0+		0.17		111
	Bypassed)	1.25 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1 $\pm$		0.17		0

(4) These limits are ensured by bench characterization and are not production tested.



### **Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

F	PARAMETER	CONDITIONS	MIN TYP	MAX	UNIT
CLOCK AND	DATA RECOVERY		·		
		SMPTE 12G, /1	11.88		Gbps
		SMPTE 12G, /1.001	11.868		Gbps
		SMPTE 6G, /1	5.94		Gbps
		SMPTE 6G, /1.001	5.934		Gbps
	IN0+ Reclocker Lock	SMPTE 3G, /1	2.97		Gbps
LOCK <sub>RATE</sub>	Data Natos	SMPTE 3G, /1.001	2.967		Gbps
		SMPTE HD, /1	1.485		Gbps
		SMPTE HD, /1.001	1.4835		Gbps
		SMPTE SD, /1	270		Mbps
	IN1± Reclocker Lock Data Rate	10 GbE	10.3125		Gbps
DVDASS	IN0+ Bypass Reclocker Data Rate	MADI	125		Mbps
BYPASSRATE	IN1± Bypass Reclocker Data Rate	1 GbE	1.25		Gbps
		Measured with 0.2 UI SJ at –3 dB, 10.3125 Gbps	8		
BW <sub>PLL</sub> P	PLL Bandwidth	Measured with 0.2 UI SJ at –3 dB, 11.88 Gbps	13		MHz
		Measured with 0.2 UI SJ at –3 dB, 5.94 Gbps	7		
		Measured with 0.2 UI SJ at –3 dB, 2.97 Gbps	5		
		Measured with 0.2 UI SJ at -3 dB, 1.485 Gbps	3		
		Measured with 0.2 UI SJ at –3 dB, 270 Mbps	1		
J <sub>PEAKING</sub>	PLL Jitter Peaking	SD, HD, 3G, 6G, 12G (IN0+), and 10 GbE (IN1±)	0.3		dB
J <sub>TOL_IN1</sub>	IN1 Input Jitter Tolerance per SFF-8431 Appendix D.11	Total jitter tolerance combination of Dj, Pj, and Rj at 10 GbE, with RX stress eye mask Y1, Y2 limits	>0.7		UI
J <sub>TOL_IN0</sub>	IN0 Input Jitter Tolerance with SJ	IN0+ EQ bypassed, Sinusoidal jitter, tested at 3G, 6G and 12G; SJ amplitude low to high sweep, tested at BER ≤ 1e-12	0.65		UI
T <sub>LOCK</sub>	Reclocker Lock Time	All supported data rates, disable HEO/VEO monitor, IN0 EQ bypassed	5		ms
T <sub>ADAPT</sub>	EQ Adapt Time	Adaptation Time for EQ at IN0	5		ms
TEMP <sub>LOCK</sub>	VCO Lock with Temp Ramp	Lock Temperature Range (5°C per min, ramp up and down), -40°C to 85°C operating range, at 10.3125 Gbps and 11.88 Gbps	125		°C
T	Poelockor Latonov <sup>(6)</sup>	Adapt mode 0, All supported data rates, disable HEO/VEO monitor, IN0 EQ bypassed	1.5 UI + 220		00
T <sub>LATENCY</sub>		Adapt mode 0, All supported data rates, disable HEO/VEO monitor, IN1± EQ = default	1.5 UI + 190		μs

(5) IN1± can also be configured to lock to SMPTE data rates via register override control. For more information, refer to the LMH1219 Programming Guide.

(6) This parameter is data rate dependent. For example, at 11.88 Gbps, 1.5 UI =  $1.5 \times 84.17 \text{ ps} = 126.25 \text{ ps}$ . Therefore, T<sub>Latency</sub> = (126.25 + 220) ps = 346.25 ps.

### **Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	MIN TY	P MAX	UNIT
T <sub>PD-RAW</sub> Propa (reclo	Propagation Delay, RAW	All supported data rates, IN0 EQ bypassed	30	)	20
	(reclocker bypassed)	Raw Data (reclocker bypassed), IN1± EQ = default	25	)	ps
FCLK <sub>OUT</sub>		Operating at 11.88 Gbps	29	7	MHz
	Output Clock Frequency	Operating at 5.94 Gbps	29	7	MHz
	OUT1 Programmed to	Operating at 2.97 Gbps	2.9	7	GHz
	Output Recovered Clock	Operating at 1.485 Gbps	1.48	5	GHz
		Operating at 270 Mbps	27	)	MHz

## 6.6 Recommended SMBus Interface AC Timing Specifications

over recommended operating supply and temperature ranges (unless otherwise specified)<sup>(1)(2)(3)</sup>

	PARAMETER	TEST CONDITIONS	MIN	NOM MAX	UNIT
F <sub>SCL</sub>	SMBus SCL Frequency		10	400	kHz
T <sub>BUF</sub>	Bus Free Time Between Stop and Start Condition		1.3		μs
T <sub>HD:STA</sub>	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.		0.6		μs
T <sub>SU:STA</sub>	Repeated Start Condition Setup Time		0.6		μs
T <sub>SU:STO</sub>	Stop Condition Setup Time		0.6		μs
T <sub>HD:DAT</sub>	Data Hold Time		0		ns
T <sub>SU:DAT</sub>	Data Setup Time		100		ns
T <sub>LOW</sub>	Clock Low Period		1.3		μs
T <sub>HIGH</sub>	Clock High Period		0.6		μs
T <sub>R</sub>	Clock/Data Rise Time			300	ns
T <sub>F</sub>	Clock/Data Fall Time			300	ns

(1) These parameters support SMBus 2.0 specifications.

(2) These parameters are not production tested.(3) See Figure 1 for timing diagrams.



## 6.7 Serial Parallel Interface (SPI) AC Timing Specifications

over recommended operating supply and temperature ranges (unless otherwise specified) <sup>(1)</sup>

	1 0 11 3	<b>U</b> (	1 /		
	PARAMETER	TEST CONDITIONS	MIN	NOM MA	X UNIT
F <sub>SCK</sub>	SPI SCK Frequency			10 2	0 MHz
Т <sub>SCK</sub>	SCK Period		50		ns
T <sub>PH</sub>	SCK Pulse Width High		0.40 x T <sub>SCK</sub>		ns
T <sub>PL</sub>	SCK Pulse Width Low		0.40 x T <sub>SCK</sub>		ns
T <sub>SU</sub>	MOSI Setup Time		4		ns
Т <sub>Н</sub>	MOSI Hold Time		4		ns
T <sub>SSSU</sub>	SS_N Setup Time		14		ns
T <sub>SSH</sub>	SS_N Hold Time		4		ns
T <sub>SSOF</sub>	SS_N Off Time		1		μs
T <sub>ODZ</sub>	MISO Driven-to-Tristate Time			20	ns
T <sub>OZD</sub>	MISO Tristate-to-Driven Time			10	ns
T <sub>OD</sub>	MISO Output Delay Time			15	ns

(1) See Figure 2 for timing diagrams.



#### Figure 1. SMBus Timing Parameters



## Figure 2. SPI Timing Parameters

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### 6.8 Typical Characteristics

 $T_A = 25^{\circ}C$  and VIN = VDDIO = VDD\_CDR = 2.5 V (unless otherwise noted)





## **Typical Characteristics (continued)**

 $T_A = 25^{\circ}C$  and VIN = VDDIO = VDD\_CDR = 2.5 V (unless otherwise noted)



## 7 Detailed Description

### 7.1 Overview

The LMH1219 is a SMPTE compatible, low-power UHD adaptive cable equalizer with integrated reclocker. The LMH1219 has two inputs: a 75- $\Omega$  cable equalizer and a 100- $\Omega$  PCB (printed circuit board) equalizer. The 75- $\Omega$  cable equalizer input features an internal 75- $\Omega$  termination and compensation network for meeting stringent SMPTE return loss requirements. The 100- $\Omega$  PCB equalizer input supports high speed signals across differential PCB traces that connect to an external SFF-8431 optical module or on-board FPGA. An internal 2:1 input mux allows users to select between the 75- $\Omega$  cable equalizer and the 100- $\Omega$  PCB equalizer. The selected input then passes through a multi-rate reclocker with a built-in loop-filter. The multi-rate reclocker is compatible with SMPTE data rates (11.88, 5.94, 2.97, 1.485 Gbps, 270 Mbps) and their divide-by-1.001 sub-rates. It is also compatible with the 10 GbE data rate (10.3125 Gbps). After the reclocker, an internal 1:2 fan-out mux allows users to select the data or clock content for each output. At both outputs, the LMH1219 has 100- $\Omega$  drivers with de-emphasis. The de-emphasis feature of the drivers is designed to compensate for insertion loss caused by output PCB traces.

The operating mode of the LMH1219 can be set by 4-level control pins, SPI, or SMBus serial control interface. The LMH1219 can be powered from a single 2.5 V supply or dual 2.5 V/1.8 V supplies for lower power consumption. The LMH1219 is offered in a small 4 mm x 4 mm 24-lead QFN package.



### 7.2 Functional Block Diagram



### 7.3 Feature Description

The LMH1219 consists of several key blocks:

- 4-Level Input Configuration Pins
- Input Carrier Detect
- -6 dB Splitter Mode Launch Amplitude for IN0
- Continuous Time Linear Equalizer (CTLE)
- Input-Output Mux Selection
- Clock and Data Recovery (CDR) Reclocker
- Internal Eye Opening Monitor (EOM)
- Output Function Control
- Output Driver Amplitude and De-Emphasis Control
- Status Indicators and Interrupts

#### 7.3.1 4-Level Input Configuration Pins

The 4-level input configuration pins use a resistor divider to provide four logic states for each control pin. There is an internal  $30-k\Omega$  pull-up and a  $60-k\Omega$  pull-down connected to the control pin that sets the default voltage at 2/3 x VDDIO. These resistors, together with the external resistor, combine to achieve the desired voltage level. By using the 1-k $\Omega$  pull-down, 20-k $\Omega$  pull-down, no connect, and 1-k $\Omega$  pull-up, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

#### **Table 1. 4-Level Control Pin Settings**

LEVEL	SETTING	RESULTING PIN VOLTAGE
Н	Tie 1 kΩ to VDDIO	VDDIO
F	Float (leave pin open)	2/3 × VDDIO
R	Tie 20 k $\Omega$ to VSS	1/3 × VDDIO
L	Tie 1 kΩ to VSS	0

Typical 4-Level Input Thresholds:

- Internal Threshold between L and R = 0.2 × VDDIO
- Internal Threshold between R and F = 0.5 × VDDIO
- Internal Threshold between F and H = 0.8 × VDDIO

#### 7.3.2 Input Carrier Detect

Both inputs of the LMH1219 have a Carrier Detect circuit to monitor the presence or absence of the input signal. When the input signal amplitude for the selected input (determined by IN\_OUT\_SEL pin) surpasses the Carrier Detect assert threshold, the LMH1219 operates in normal mode.

In the absence of an input signal, the LMH1219 automatically goes into Power Save Mode to conserve power consumption. When a valid signal is detected, the LMH1219 automatically exits Power Save Mode and returns to the normal operating mode.

#### 7.3.3 -6 dB Splitter Mode Launch Amplitude for IN0

The LMH1219 is designed to equalize data transmitted through a coaxial cable driven by a SMPTE compatible cable driver with launch amplitude of 800 mVp-p  $\pm$  10%. In applications where a 1:2 passive splitter is used, the signal amplitude is reduced by half due to the 6 dB insertion loss of the splitter. The LMH1219 is designed to support -6 dB splitter mode for INO, enabled by SPI or SMBus serial interface. For more information, refer to the LMH1219 Register Map and the Programming Guide.

#### 7.3.4 Continuous Time Linear Equalizer (CTLE)

The LMH1219 has two Continuous Time Linear Equalizer (CTLE) blocks, one for each input. The CTLE compensates for frequency-dependent loss due to the transmission media prior to the device input. The CTLE accomplishes this by applying variable gain to the input signal, thereby boosting higher frequencies more than lower frequencies.



Only one CTLE is enabled at a time, in accordance with the input channel selected by the input mux. If IN0 is selected, the IN0 cable CTLE is powered on and the IN1 PCB CTLE is powered off. Alternatively, the two CTLEs can be bypassed either by using the OUT\_CTRL pin or via register control.

#### 7.3.4.1 Adaptive Cable Equalizer (IN0+)

If IN0 is selected, adaptive cable equalization is enabled by default. IN0 has an on-chip 75- $\Omega$  termination to the input common mode voltage and includes a series return loss compensation network for meeting stringent SMPTE return loss requirements. It is designed for AC coupling, requiring a 4.7- $\mu$ F AC coupling capacitor for minimizing base-line wander due to the rare-occurring pathological bit pattern. The cable equalizer is designed with high gain and low noise circuitry to compensate for the insertion loss of a coaxial cable, such as Belden 1694A, which is widely used in broadcast video infrastructures.

Internal control loops are used to monitor the input signal quality and automatically select the optimum equalization boost and DC offset compensation. The LMH1219 is designed to handle the stringent pathological pattern defined in the SMPTE RP 198 and SMPTE RP 178 standards.

#### 7.3.4.2 Adaptive PCB Trace Equalizer (IN1±)

The IN1 PCB equalizer has an on-chip  $100-\Omega$  termination and is designed for AC coupling, requiring a 4.7- $\mu$ F AC coupling capacitor for minimizing base-line wander due to the rare-occurring pathological bit pattern. The PCB equalizer can compensate up to 20 inches of board trace at data rates up to 11.88 Gbps. There are two adapt modes for IN1: AM0 manual mode and AM1 adaptive mode. In AM0 manual mode, fixed EQ boost settings are applied through user-programmable register control, whereas in AM1 adaptive mode, state machines automatically find the optimal equalization setting from a set of 16 pre-determined settings defined in Registers 0x40-0x4F.

If IN1 is selected, AM1 adaptive mode is enabled at the 10 GbE data rate by default. The PCB equalizer is able to adapt at 10.3125 Gbps (10 GbE) and 2.97 Gbps, 5.94 Gbps, and 11.88 Gbps (SMPTE) data rates. At 1.485 Gbps and 270 Mbps data rates, the equalization is fixed at 0x00 (minimum EQ boost). This fixed EQ value can be changed via register control. For more details, refer to the LMH1219 Register Map and Programming Guide.

#### 7.3.5 Input-Output Mux Selection

By default, the LMH1219 input-to-output signal flow and data rate selection are configured by the IN\_OUT\_SEL pin logic settings shown in Table 2. These settings can be overridden via register control by applying the appropriate override bit values. For more information, refer to the LMH1219 Register Map and Programming Guide.

LEVEL	LEVEL DEFINITION	
Н	SMPTE Data Rates: IN0 to OUT0 and OUT1	
F	SMPTE Data Rates: IN0 to OUT0 (OUT1 disabled)	
R	10 GbE Data Rate: IN1 to OUT1 (OUT0 disabled)	
L	10 GbE Data Rate: IN1 to OUT0 and OUT1	

Table 2. IN\_OUT\_SEL Pin Settings

#### 7.3.6 Clock and Data Recovery (CDR) Reclocker

After the input signal passes through the CTLE, the equalized data is fed into the clock and data recovery (CDR) block. Using an internal PLL, the CDR locks to the incoming equalized data and recovers a clean internal clock to re-sample the equalized data. The LMH1219 CDR is able to tolerate high input jitter, tracking low frequency input jitter below the PLL bandwidth while reducing high frequency input jitter above the PLL bandwidth.

The supported data rates are listed in Table 3. By default, IN0 locks to SMPTE data rates and IN1 locks to the 10 GbE data rate, according to the IN\_OUT\_SEL pin logic shown previously in Table 2. IN1 can be programmed to lock to SMPTE data rates via register control by applying the appropriate override bit values. For more information, refer to the LMH1219 Register Map and Programming Guide.



#### Table 3. Supported Data Rates

INPUT	DATA RATE	RECLOCKER MODE
IN0+	11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps, 270 Mbps <sup>(1)</sup>	Reclocker Enabled
	125 Mbps	Reclocker Disabled (CDR Bypassed)
INIA .	10.3125 Gbps	Reclocker Enabled
IN1±	1.25 Gbps	Reclocker Disabled (CDR Bypassed)

(1) Divide-by-1.001 lock rates available only for 11.88 Gbps, 5.94 Gbps, 2.97 Gbps, and 1.485 Gbps.

#### NOTE

If the selected data rate (SMPTE or 10 GbE) is changed while the device is operating with active data, a CDR reset and release is required for the CDR to re-acquire lock. If the input data signal is toggled off and on after the selected data rate is changed, the Carrier Detect circuit will reset the CDR. In this case, no register write is needed for the CDR to re-acquire lock.

#### 7.3.7 Internal Eye Opening Monitor (EOM)

The LMH1219 has an on-chip eye opening monitor (EOM) that can be used to analyze, monitor, and diagnose the post-equalized waveform, just prior to the CDR reclocker. The EOM is operational for 2.97 Gbps and higher data rates.

The EOM monitors the post-equalized waveform in a time window that spans one unit interval and a configurable voltage range that spans up to  $\pm 400 \text{ mV}$  differential. The time window and voltage range are divided into 64 steps, so the result of the eye capture is a 64 × 64 matrix of *hits*, where each point represents a specific voltage and phase offset relative to the main data sampler. The number of *hits* registered at each point needs to be taken in context with the total number of bits observed at that voltage and phase offset in order to determine the corresponding probability for that point. The number of bits observed at each point is configurable.

The resulting 64 × 64 matrix produced by the EOM can be processed by software and visualized in a number of ways. Two common ways to visualize this data are shown in Figure 11 and Figure 12. These diagrams depict examples of eye monitor plots implemented by software. The first plot is an example using the EOM data to plot a basic eye using ASCII characters, which can be useful for simple diagnostic software. The second plot shows the first derivative of the EOM data, revealing the density of hits and the actual waveforms and crossings that comprise the eye.



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A common measurement performed by the EOM is the horizontal and vertical eye opening. The horizontal eye opening (HEO) represents the width of the post-equalized eye at 0-V differential amplitude, measured in unit intervals or picoseconds (ps). The vertical eye opening (VEO) represents the height of the post-equalized eye, measured midway between the mean zero crossing of the eye. This position in time approximates the CDR sampling phase.

#### 7.3.8 Output Function Control

By default, the LMH1219 output function control for OUT0 and OUT1 is configured by the OUT\_CTRL pin logic settings shown in Table 4. These settings can be overridden via register control by applying the appropriate override bit values. For more information, refer to the LMH1219 Register Map and Programming Guide.

LEVEL	DEFINITION
Н	OUT0 and OUT1: Raw Data, Both EQ and Reclocker Bypassed
F	OUT0 and OUT1: Recovered Data, Both EQ and Reclocker Enabled
R	OUT0: Recovered Data, EQ and Reclocker Enabled OUT1: Full-Rate Recovered Clock if Data Rate ≤ 3 Gbps. 297 MHz Recovered Clock if Data Rate > 3 Gbps <sup>(1)</sup>
L	OUT0 and OUT1: Equalized Data, EQ Enabled, Reclocker Bypassed

Table 4			Pin	Settings
---------	--	--	-----	----------

(1) This setting is only valid for SMPTE data rates. It is not supported for the 10 GbE data rate.

#### 7.3.9 Output Driver Amplitude and De-Emphasis Control

5

The VOD\_DE control pin selects the output amplitude and de-emphasis settings for both OUT0 and OUT1. It offers users the capability to select higher output amplitude and de-emphasis levels for longer board trace that connects the drivers to their downstream receivers. Driver de-emphasis provides transmitter equalization to reduce the ISI caused by the board trace.

By default, the output driver VOD and de-emphasis settings are configured by the VOD\_DE pin logic settings shown in Table 5. These settings can be overridden via register control by applying the appropriate override bit values. When these parameters are controlled by registers, the VOD and de-emphasis levels for each channel can be programmed independently. For more information, refer to the LMH1219 Register Map and the Programming Guide.

		- 0	0			•
VOD_DE LEVEL	VOD REG SETTING OUT0±: 0x30[5]=1, 0x30[2:0] OUT1±: 0x32[5]=1, 0x32[2:0]	DEM REG SETTING OUT0±: 0x31[6]=1, 0x31[2:0] OUT1±: 0x33[6]=1, 0x33[2:0]	VOD (mVpp) <sup>(2)</sup>	VOD <sub>DE</sub> (mVpp) <sup>(2)</sup>	DEM (dB)	FR4 TRACE LENGTH (inches)
Н	0	0	410	410	0	0 - 1
F	2	2	560	500	-0.9	2 – 4
R	3	3	635	480	-2.4	5 – 6

Table 5. Recommended VOD\_DE Pin and Register Settings for Different FR4 Trace Lengths<sup>(1)</sup>

(1) The output drivers are capable of providing higher VOD and DEM levels (max settings are 7). For more VOD and de-emphasis levels, refer to 表 10.

810

480

5

(2) See Figure 13.

L



Figure 13. VOD and VOD<sub>DE</sub> Levels

-6.1

7 – 8



#### 7.3.10 Status Indicators and Interrupts

#### 7.3.10.1 LOCK\_N (Lock Indicator)

The LOCK\_N pin is a 3.3 V tolerant, active-low open drain output. An external resistor to the logic supply is required. By default, LOCK\_N is the reclocker lock indicator, and this pin asserts low when the LMH1219 achieves lock to a valid SMPTE or 10 GbE data rate. The LOCK\_N pin functionality can also be configured via register control to indicate CD\_N (Carrier Detect) or INT\_N (Interrupt) events. For more information about how to reconfigure the LOCK\_N pin functionality, refer to the LMH1219 Register Map and the Programming Guide.

#### 7.3.10.2 CD\_N (Carrier Detect)

The LOCK\_N pin can be reconfigured via register control to indicate a CD\_N (Carrier Detect) event. When configured as a CD\_N output, the pin asserts low at the end of adaptation after a valid signal is detected by the Carrier Detect circuit of the selected input. Under register control, this pin can be reconfigured to indicate CD\_N for IN0 or IN1. For more information about how to configure the LOCK\_N pin for CD\_N functionality, refer to the LMH1219 Register Map and the Programming Guide.

#### 7.3.10.3 INT\_N (Interrupt)

The LOCK\_N pin can be configured to indicate an INT\_N (Interrupt) event. When configured as an INT\_N output, the pin asserts low when an interrupt occurs, according to the programmed interrupt masks. Seven separate masks can be programmed via register control as interrupt sources:

- If there is a Loss of Signal (LOS) event on IN0, irrespective of the input channel selected (2 separate masks).
- If there is a Loss of Signal (LOS) event on IN1, irrespective of the input channel selected (2 separate masks).
- If HEO or VEO falls below a certain threshold after CDR is locked (1 mask).
- If a CDR Lock event has occurred (2 separate masks).

INT\_N is a sticky bit, meaning that it will flag after an interrupt occurs and will not clear until read back. Once the Interrupt Status Register is read, the INT\_N pin will assert high again. For more information about how to configure the LOCK\_N pin for INT\_N functionality, refer to the LMH1219 Register Map and the Programming Guide.

#### 7.3.11 Additional Programmability

The LMH1219 supports extended programmability through the use of an SPI or SMBus serial control interface. Such added programmability includes:

- Cable Length Indicator (CLI)
- Digital MUTE<sub>REF</sub>

#### 7.3.11.1 Cable Length Indicator (CLI)

The Cable Length Indicator (CLI) indicates the length of the coax cable attached to IN0+. CLI is accessible through CableEQ/Driver Page Reg 0x25[5:0]. The 6-bit setting ranges in decimal value from 0 to 55 (000000'b to 110111'b in binary), corresponding to approximately 0 to 600 m of Belden 1694A cable.

#### 7.3.11.2 Digital MUTE<sub>REF</sub>

Digital  $MUTE_{REF}$  CableEQ/Driver Page Reg 0x03[5:0] sets the threshold for the maximum cable length at IN0+ to be equalized before muting the outputs. The  $MUTE_{REF}$  register value is directly proportional to the cable length being equalized.  $MUTE_{REF}$  is data rate dependent. Follow the steps below to set the  $MUTE_{REF}$  register setting for any desired SDI rate:

- 1. Connect the desired input cable length at which the driver output needs to be muted.
- 2. Send video patterns to IN0+ at the SD rate (270 Mbps). At SD, the Cable Length Indicator (CLI) has the largest dynamic range.
- 3. Read back Cable EQ/Driver Page Reg 0x25[5:0] to record the CLI value.
- 4. Copy the CLI value, and write this value to Digital MUTE<sub>REF</sub> Cable EQ/Driver Page Reg 0x03[5:0].



## 7.4 Device Functional Modes

The LMH1219 operates in one of two modes: System Management Bus (SMBus) or Serial Peripheral Interface (SPI) mode. In order to determine the mode of operation, the proper setting must be applied to the MODE\_SEL pin at power-up, as detailed in Table 6.

LEVEL	DEFINITION				
Н	Forced Power Save Mode, only SPI is enabled (all other circuitry powered down)				
F	Select SPI Interface for register access				
R	Reserved for factory testing – do not use				
L	Select SMBus Interface for register access				

#### Table 6. MODE\_SEL Pin Settings

		_
N	nτ	E
	UI.	

Changing logic states between LEVEL-L and LEVEL-H after power up is not allowed.

#### 7.4.1 System Management Bus (SMBus) Mode

If MODE\_SEL = L, the LMH1219 is in SMBus mode. In SMBus mode, Pins 10 and 21 are configured as SDA and SCL. Pins 7 and 20 act as 4-level address straps for ADDR0 and ADDR1 at power up to determine the 7-bit slave address of the LMH1219, as shown in Table 7.

ADDR0 (LEVEL)	ADDR1 (LEVEL)	7-BIT SLAVE ADDRESS [HEX]	8-BIT WRITE COMMAND [HEX]					
L	L	1D	3A					
L	R	1E	3C					
L	F	1F	3E					
L	Н	20	40					
R	L	21	42					
R	R	22	44					
R	F	23	46					
R	Н	24	48					
F	L	25	4A					
F	R	26	4C					
F	F	27	4E					
F	Н	28	50					
Н	L	29	52					
Н	R	2A	54					
Н	F	2B	56					
Н	Н	2C	58					

### Table 7. SMBus Device Slave Addresses<sup>(1)</sup>

(1) The 8-bit write command consists of the 7-bit slave address (Bits 7:1) with 0 appended to the LSB to indicate an SMBus write. For example, if the 7-bit slave address is 0x1D (001 1101'b), the 8-bit write command is 0x3A (0011 1010'b).



#### 7.4.1.1 SMBus Read and Write Transactions

SMBus is a two-wire serial interface through which various system component chips can communicate with the master. Slave devices are identified by having a unique device address. The two-wire serial interface consists of SCL and SDA signals. SCL is a clock output from the master to all of the slave devices on the bus. SDA is a bidirectional data signal between the master and slave devices. The LMH1219 SMBus SCL and SDA signals are open drain and require external pull-up resistors.

#### Start and Stop:

The master generates start and stop patterns at the beginning and end of each transaction.

- Start: High to low transition (falling edge) of SDA while SCL is high.
- Stop: Low to high transition (rising edge) of SDA while SCL is high.



Figure 14. Start and Stop Conditions

The master generates nine clock pulses for each byte transfer. The 9th clock pulse constitutes the ACK cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is recorded when the device pulls SDA low, while a NACK is recorded if the line remains high.



Figure 15. Acknowledge (ACK)

#### 7.4.1.1.1 SMBus Write Operation Format

Writing data to a slave device consists of three parts, as illustrated in Figure 16:

- 1. The master begins with a start condition, followed by the slave device address with the R/W bit set to 0'b.
- 2. After an ACK from the slave device, the 8-bit register word address is written.
- 3. After an ACK from the slave device, the 8-bit data is written, followed by a stop condition.



Figure 16. SMBus Write Operation

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#### 7.4.1.1.2 SMBus Read Operation Format

Reading data from a slave device consists of four parts, as illustrated in Figure 17:

- 1. The master begins with a start condition, followed by the slave device address with the  $R/\overline{W}$  bit set to 0'b.
- 2. After an ACK from the slave device, the 8-bit register word address is written.
- 3. After an ACK from the slave device, the master initiates a re-start condition, followed by the slave address with the R/W bit set to 1'b.
- 4. After an ACK from the slave device, the 8-bit data is read back. The last ACK is high if there are no more bytes to read, and the last read is followed by a stop condition.



Figure 17. SMBus Read Operation

#### 7.4.2 Serial Peripheral Interface (SPI) Mode

If  $MODE\_SEL = F$  or H, the LMH1219 is in SPI mode. In SPI mode, the following pins are used for SPI bus communication:

- MOSI (pin 10): Master Output Slave Input
- MISO (pin 20): Master Input Slave Output
- SS\_N (pin 7): Slave Select (active low)
- SCK (pin 21): Serial clock (input to the LMH1219 slave device)

#### 7.4.2.1 SPI Read and Write Transactions

Each SPI transaction to a single device is 17 bits long and is framed by SS\_N when asserted low. The MOSI input is ignored, and the MISO output is floated whenever SS\_N is de-asserted (high).

The bits are shifted in left-to-right. The first bit is R/W, which is 1'b for "read" and 0'b for "write." Bits A7-A0 are the 8-bit register address, and bits D7-D0 are the 8-bit read or write data. The previous SPI command, address, and data are shifted out on MISO as the current command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously when SS\_N asserts low. The contents of a single MOSI or MISO transaction frame are shown in Table 8.

#### Table 8. 17-Bit Single SPI Transaction Frame

_	
R/W A7 A6 A5 A4 A3 A2 A1 A0 D7 D6	6 D5 D4 D3 D2 D1 D0

#### 7.4.2.1.1 SPI Write Transaction Format

For SPI writes, the R/W bit is 0'b. SPI write transactions are 17 bits per device, and the command is executed on the rising edge of SS\_N. The SPI transaction always starts on the rising edge of the clock.

The signal timing for a SPI Write transaction is shown in Figure 18. The "prime" values on MISO (for example, A7') reflect the contents of the shift register from the previous SPI transaction and are *don't-care* for the current transaction.





Figure 18. Signal Timing for a SPI Write Transaction

#### 7.4.2.1.2 SPI Read Transaction Format

A SPI read transaction is 34 bits per device and consists of two 17-bit frames. The first 17-bit read transaction frame shifts in the address to be read, followed by a dummy transaction second frame to shift out 17-bit read data. The R/W bit is 1'b for the read transaction, as shown in Figure 19.

The first 17 bits from the read transaction specifies 1-bit of R/W and 8-bits of address A7-A0 in the first 8 bits. The eight 1's following the address are ignored. The second dummy transaction acts like a read operation on address 0xFF and needs to be ignored. However, the transaction is necessary in order to shift out the read data D7-D0 in the last 8 bits of the MISO output. As with the SPI Write, the "prime" values on MISO during the first 16 clocks are *don't-care* for this portion of the transaction. The values shifted out on MISO during the last 17 clocks reflect the read address and 8-bit read data for the current transaction.



Figure 19. Signal Timing for a SPI Read Transaction

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#### 7.4.2.2 SPI Daisy Chain

The LMH1219 supports SPI daisy-chaining among multiple devices, as shown in Figure 20.



Figure 20. Daisy-Chain Configuration

Each LMH1219 device is directly connected to the SCK and SS\_N pins of the host. The first LMH1219 device in the chain is connected to the host's MOSI pin, and the last device in the chain is connected to the host's MISO pin. The MOSI pin of each intermediate LMH1219 device in the chain is connected to the MISO pin of the previous LMH1219 device, thereby creating a serial shift register. In a daisy-chain configuration of N x LMH1219 devices, the host conceptually sees a shift register of length 17 x N for a basic SPI transaction, during which SS\_N is asserted low for 17 x N clock cycles.



#### 7.5 LMH1219 Register Map

The LMH1219 register map is divided into three register pages. These register pages are used to control different aspects of the LMH1219 functionality. A brief summary of the pages is shown below:

- 1. **Share Register Page**: This page corresponds to global parameters, such as LMH1219 device ID and LOCK\_N status configuration. This is the default page at start-up.
- 2. **CTLE/CDR Register Page**: This page corresponds to IN1 PCB CTLE, input and output mux settings, CDR settings, and output interrupt overrides. Access this page by setting Reg 0xFF[2:0] = 100'b.
- 3. **CableEQ/Drivers Register Page**: This page corresponds to IN0 Cable EQ and both OUT0 and OUT1 driver output settings. Access this page by setting Reg 0xFF[2:0] = 101'b.

For typical device configurations and proper register reset sequencing, reference the appropriate sections of the LMH1219 Programming Guide.

Please note the following about the LMH1219 default register values in the register map:

- Default register values were read after power-up with no active inputs applied to IN0 or IN1.
- Default register values for Reserved "Read-Only" bits may vary dynamically from part to part.

#### 7.5.1 Share Register Page

Address	Register Name	Bit	Field	Default	Туре	Description
0x00	Reserved	7:0	Reserved	0x00	R	Reserved
0x01	Reserved	7:0	Reserved	0x40	R	Reserved
0x02	Reserved	7:0	Reserved	0x02	RW	Reserved
0x03	Reserved	7:0	Reserved	0x00	RW	Reserved
0x04	Reserved	7:0	Reserved	0x01	RW	Reserved
0x05	Reserved	7:0	Reserved	0x00	RW	Reserved
0x06	Reserved	7:0	Reserved	0x00	RW	Reserved
0x07	Reserved	7:0	Reserved	0x04	RW	Reserved
0x08	Reserved	7:0	Reserved	0x11	RW	Reserved
0x09	Reserved	7:0	Reserved	0x00	R	Reserved
		7:5	Reserved		R	Reserved
0vF2	Reset	4	reset_done		R	<ul><li>0 = Internal state machine register initialization not done.</li><li>1 = Internal state machine register initialization done.</li></ul>
UXEZ	Regs	3:1	Reserved	0.00	RW	Reserved
	0	0	reset_init		RW	1 = Initialize internal state machine register settings. Refer to the LMH1219 Programming Guide for details.
0xF0	Device Revision	7:0	Version	0x02	R	Device Revision
0xF1	Device ID	7:0	Device_ID	0x80	R	For LMH1219, Device ID = 0x80

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Address	Register Name	Bit	Field	Default	Туре	Description
Register 0xFF Communication Control		7:6	lock_output_ctrl		RW	Controls the output on LOCK pin if Reg 0xFF[5:4] = 01'b 00 = Lock status from Reclocker 01 = CableEQ/Driver Reg 0x00[7] status output 10 = Logical OR of LOCK status from Reclocker and CableEQ/Driver Reg 0x00[7] status 11 = Logical AND of LOCK status from Reclocker and CableEQ/Driver Reg 0x00[7] status
	5:4	los_int_bus_sel	0x00	RW	Controls the output on LOCK_N pin 00 = Default behavior (LOCK_N outputs lock status from reclocker) 01 = LOCK_N pin output status determined by Reg 0xFF[7:6] 10 = LOS of selected input (IN0 or IN1) 11 = Interrupts are output on LOCK_N pin, as determined by CTLE/CDR Page Reg 0x56[6:0]	
		3	Reserved		RW	Reserved
		2	page_select_enable		RW	0 = The shared registers are enabled. 1 = Enables communication access to the Register Page specified in Reg 0xFF[1:0].
		1:0	page_select		RW	Enable communication access to a specific Register Page 00 = CTLE/CDR Register Page 01 = CableEQ/Drivers Register Page Other values are invalid.

## 7.5.2 CTLE/CDR Register Page

Address	Register Name	Bit	Field	Default	Туре	Description
		7:3	Reserved		RW	Reserved
0x00	Reset CTLE/CDR Registers	2	rst_CTLE/CDR_regs	0x00	RW	Reset registers (self-clearing) 0 = Normal Operation 1 = Reset CTLE/CDR Registers. Register re-initialization procedure required after resetting the CTLE/CDR Registers.
		1:0	Reserved		RW	Reserved
		7:2	Reserved		RW	Reserved
0x01	LOS Status	1	LOS1	0x03	R	0 = Signal Present on IN1 1 = Loss of Signal on IN1
		0	Reserved		R	Reserved
0x02	CDR_Status	7:0	CDR_Status	0x41	R	CDR status indicator. See "Lock Data Rate Indication" subsection in the LMH1219 Programming Guide for more information.
		7:6	eq_BST0		RW	Used for setting manual EQ value for IN1 when Reg 0x2D[3]
0x03 IN1 Manual EQ Boost	5:4	eq_BST1		RW	= 1. EQ boost value can be read back on CTLE/CDR Page	
	IN1 Manual EQ Boost	3:2	eq_BST2	0x80	RW	[7:6]: 2-bit control for Stage 0 of the CTLE.
	Doost	1:0	eq_BST3		RW	<ul><li>[5:4]: 2-bit control for Stage 1 of the CTLE.</li><li>[3:2]: 2-bit control for Stage 2 of the CTLE.</li><li>[1:0]: 2-bit control for Stage 3 of the CTLE.</li></ul>
0x04	Reserved	7:0	Reserved	0x00	RW	Reserved
0x05	Reserved	7:0	Reserved	0x00	RW	Reserved
0x06	Reserved	7:0	Reserved	0x00	RW	Reserved
0x07	Reserved	7:0	Reserved	0x00	RW	Reserved
0x08	Reserved	7:0	Reserved	0x00	RW	Reserved
		7:6	Reserved		RW	Reserved
0x09	Output Mux Override Control	5	reg_out_control_ov	0x00	RW	Output Mux Override Control 0 = Reg 0x1C[3:2] determines the output selection for both OUT0 and OUT1 1 = Enable individual output mux control based on values from Reg 0x1C[7:5] and Reg 0x1E[7:5]
		4:3	Reserved	ļ	RW	Reserved
		2:0	Reserved		RW	Reserved

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Address	Register Name	Bit	Field	Default	Туре	Description
		7:4	Reserved		RW	Reserved
0×04	CDR Reset	3	reg_cdr_reset_ov	0.450	RW	0 = Disables CDR Reset (Normal Operating Mode) 1 = Enables Reg 0x0A[2] to control CDR Reset
UXUA	0x0A Control	2	reg_cdr_reset	0x50	RW	0 = No CDR Reset if Reg 0x0A[3] = 1 1 = CDR Reset if Reg 0x0A[3] = 1
		1:0	Reserved		RW	Reserved
0x0B	Reserved	7:0	Reserved	0x1F	RW	Reserved
0x0C	CDR Output Status Control	7:4	reg_sh_status_control	0x08	RW	Value determines what CDR status outputs are displayed in CTLE/CDR Page Reg 0x02. See "Lock Data Rate Indication" subsection in the LMH1219 Programming Guide for more information.
		3:0	Reserved		RW	Reserved
0x0D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x0E	Reserved	7:0	Reserved	0x93	RW	Reserved
0x0F	Reserved	7:0	Reserved	0x69	RW	Reserved
0x10	Reserved	7:0	Reserved	0x27	RW	Reserved
0x11	EOM Voltage Range Control	7:6	eom_sel_vrange	0xE0	RW	Sets the expected incoming eye diagram vertical eye opening interval if Reg 0x2C[6] = 0 $00 = 3.125 \text{ mV} (3.125 \text{ mV x } 64 = 200 \text{ mV}; \pm 100 \text{ mV} range)$ $01 = 6.25 \text{ mV} (6.25 \text{ mV x } 64 = 400 \text{ mV}; \pm 200 \text{ mV} range)$ $10 = 9.375 \text{ mV} (9.375 \text{ mV x } 64 = 600 \text{ mV}; \pm 300 \text{ mV} range)$ $11 = 12.5 \text{ mV} (12.5 \text{ mV} \text{ x } 64 = 800 \text{ mV}; \pm 400 \text{ mV} range)$
		5	eom_PD		RW	0 = EOM is always powered up 1 = Power down EOM when not in use
		4:0	Reserved		RW	Reserved
0x12	Reserved	7:0	Reserved	0xA0	RW	Reserved
		7:4	Reserved		RW	Reserved
0x13	IN1 CTLE Control	3	eq_PD_EQ		RW	IN1 CTLE Power-Down Control 0 = Powers up EQ of IN1 1 = Powers down EQ of IN1 Note: The un-selected channel is always powered-down.
0.0		2	Reserved	UNCC.	RW	Reserved
		1	eq_en_bypass		RW	0 = Enable Gain Stages 2 and 3 of IN1 CTLE 1 = Bypass Gain Stages 2 and 3 of IN1 CTLE
		0	Reserved		RW	Reserved
0x14	Reserved	7:0	Reserved	0x00	RW	Reserved
		7	Reserved		RW	Reserved
	IN1 Carrier	6	cd_1_PD		RW	IN1 Carrier Detect Power Down Control 0 = Power Up IN1 Carrier Detect 1 = Power Down IN1 Carrier Detect
0x15	Detect Control	5:4	cd_1_refa_sel	0x00	RW	Controls IN1 Carrier Detect Assert and De-Assert Thresholds
and Threshold Setting	Setting	3:2	cd_1_refd_sel		RW	0000 = Default levels (nominal) 0101 = Nominal - 2 mV 1010 = Nominal + 5 mV 1111 = Nominal + 3 mV
		1:0	Reserved		RW	Reserved
0x16	Reserved	7:0	Reserved	0x25	RW	Reserved
0x17	Reserved	7:0	Reserved	0x25	RW	Reserved
0x18	Reserved	7:0	Reserved	0x40	RW	Reserved
0x19	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1A	Reserved	7:0	Reserved	0xA0	RW	Reserved
0x1B	Reserved	7:0	Reserved	0x03	RW	Reserved

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Address	Register Name	Bit	Field	Default	Туре	Description
	7:5	out_sel0_data_mux		RW	In normal operating mode, Reg 0x1C[7:5] returns the mux select value applied at OUT0. When Reg 0x09[5] = 1, OUT0 mux selection is controlled by Reg 0x1C[7:5] as follows: 000 = Mute 001 = 10 MHz Clock 010 = Raw Data (EQ Only) 100 = Retimed Data Other Settings are invalid.	
0x1C	OUT Mux	4	VCO_Div40	0x58	RW	When Reg 0x09[5] = 1 and Reg 0x1E[7:5] = 101'b, OUT1 clock selection can be controlled by Reg 0x1C[4] as follows: 0 = OUT1 outputs 10 MHz clock 1 = OUT1 outputs VCO divide-by-40
Select_0	3:2	drv_out_ctrl		RW	Controls output mux selection for both OUT0 and OUT1 if Reg 0x3F[3] = 1 to override the OUT_CTRL pin 00 = Mute both OUT0 and OUT1 01 = When CDR is locked, output reclocked data on OUT0 and output clock on OUT1. If locked data rate is $\leq$ 3G, OUT1 = VCO. If locked data rate is $>$ 3G, OUT1 = VCO/40. When unlocked, output raw data on OUT0 and mute OUT1. 10 = When locked, output retimed data on both OUT0 and OUT1. When unlocked, output raw data on both OUT0 and OUT1. This is the default setting. 11 = Output raw data on both OUT0 and OUT1.	
		1:0	Reserved		RW	Reserved
0x1D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1E	OUT Mux Select_1	7:5	out_sel1_data_mux	0x09	RW	In normal operating mode, Reg 0x1E[7:5] returns the mux select value applied at OUT1. When Reg 0x09[5] = 1, OUT1 mux selection is controlled by Reg 0x1E[7:5] as follows: 000 = Raw Data (EQ Only) 001 = Retimed Data 010 = Full Rate VCO clock 101 = 10 MHz Clock if Reg 0x1C[4] = 0 and VCO/40 clock if Reg 0x1C[4] = 1 111 = Mute Other Settings are invalid
		4:0	Reserved		RW	Reserved
0x1F	OUT1 Polarity	7	sel_inv_out1	0x10	RW	0 = OUT1 normal polarity 1 = Inverts OUT1 driver polarity Note: No polarity inversion for OUT0
		6:0	Reserved		RW	Reserved
0x20	Reserved	7:0	Reserved	0x00	RW	Reserved
0x21	Reserved	7:0	Reserved	0x00	RW	Reserved
0x22	Reserved	7:0	Reserved	0x00	RW	Reserved
0x23	HEO_VEO_OV	7	eom_get_heo_ veo_ov	0x40	RW	0 = Disable HEO/VEO Acquisition override. 1 = Enable HEO/VEO Acquisition override. Value determined by Reg 0x24[1].
		6:0	Reserved			Reserved
		7	fast_eom		RW	0 = Disable Fast EOM mode 1 = Enable Fast EOM mode
	6	Reserved	-	R	Reserved	
	FOM Constral	5	get_heo_veo_error_ no_hits	010	R	Zero Crossing Error Detector Status 0 = Zero crossing errors in the eye diagram observed 1 = No zero crossing errors in the eye diagram observed
UX24		4	get_heo_veo_error_ no_opening	UX4U	R	Vertical Eye Closure Detector Status 0 = Open eye diagram detected 1 = Eye diagram completely closed
		3:2	Reserved		R	Reserved
	1	eom_get_heo_veo		RW	1 = Acquire HEO and VEO (self-clearing) if Reg 0x23[7] = 1	

RW

1 = Start EOM counter (self-clearing)



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0

eom\_start



Address	Register Name	Bit	Field	Default	Туре	Description
0x25	EOM_MSB	7:0	eom_count_msb	0x00	R	MSBs of EOM counter
0x26	EOM_LSB	7:0	eom_count_lsb	0x00	R	LSBs of EOM counter
0x27	HEO	7:0	heo	0x00	R	HEO value. This is measured in 0-63 phase settings. To get HEO in UI, read HEO, convert hex to dec, then divide by 64.
0x28	VEO	7:0	veo	0x00	R	VEO value. This is measured in 0-63 vertical steps. To get VEO in mV, convert hex to dec, then multiply by the EOM Voltage Range defined in Reg 0x29[6:5].
		7	Reserved		RW	Reserved
0x29	Auto EOM Voltage Range	6:5	eom_vrange_setting	0x00	R	Readback of automatic EOM Voltage Range granularity. 00 = 3.125 mV 01 = 6.25 mV 10 = 9.375 mV 11 = 12.5 mV
		4:0	Reserved		RW	Reserved
0x2A	EOM_timer_thr	7:0	eom_timer_thr	0x30	RW	EOM timer for how long to check each phase/voltage setting.
0x2B	Reserved	7:0	Reserved	0x00	RW	Reserved
		7	Reserved	+	RW	Reserved
0x2C	VEO Scale	6	veo_scale	0x72	RW	0 = VEO scaling based on manual Voltage Range settings (see Reg 0x11[7:6]) 1 = Enable Auto VEO scaling
		5:0	Reserved		RW	Reserved
		7:4	Reserved		RW	Reserved
0x2D	CTLE Boost Override	3	reg_eq_bst_ov	0x00	RW	IN1 EQ Boost Override Control 0 = Disable IN1 EQ boost override 1 = Override the internal IN1 EQ boost settings with values in Reg 0x03[7:0]
		2:0	Reserved		RW	Reserved
0x2E	Reserved	7:0	Reserved	0x24	RW	Reserved
0x2F	Rate Overrides	7:6	refn_rate	0x06	RW	Reference Rate Selection for CDR Lock if Reg 0x3F[2] = 1 00 = Select SMPTE rates 01 = Select 10G Ethernet rate Other settings are Invalid
		5:0	Reserved		R	Reserved
0x30	Reserved	7:0	Reserved	0x00	RW	Reserved
		7	Reserved		RW	Reserved
	IN1 Adaptation	6:5	adapt_mode		RW	Adapt Mode Override Value if Reg 0x3F[5] = 1 00 = Manual CTLE for IN1. Set CTLE/CDR Page Reg 0x2D[3] = 1 to enable IN1 EQ boost settings with values in Reg 0x03[7:0]. 01 = Automatic CTLE Adaptation for IN1.
0x31	Mode and Input	4:2	Reserved	0x00	RW	Reserved
Mux Select	Mux Select	1:0	input_mux_ch_sel		RW	Input Mux Selection if Reg $0x3F[4] = 1$ to override IN_OUT_SEL pin 00 = IN0 to OUT0 and OUT1 01 = IN0 to OUT0 only 10 = IN1 to OUT1 only 11 = IN1 to OUT0 and OUT1
0x32	HEO/VEO	7:4	heo_int_thresh	0x11	RW	Compares HEO value, Reg 0x27[7:0] vs. threshold from Reg 0x32[7:4] x 4.
0x32 Interrupt Threshold	3:0	veo_int_thresh	0.11	RW	Compares VEO value. Reg 0x28[7:0] vs. threshold from Reg 0x32[3:0] x 4.	
0x33	Reserved	7:0	Reserved	0x88	RW	Reserved
0x34	Reserved	7:0	Reserved	0x3F	RW	Reserved
0x35	Reserved	7:0	Reserved	0x1F	RW	Reserved
0x36	Reserved	7:0	Reserved	0x11	RW	Reserved
0x37	Reserved	7:0	Reserved	0x00	R	Reserved
0x38	Reserved	7:0	Reserved	0x00	R	Reserved

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Address	Register Name	Bit	Field	Default	Туре	Description		
0x39	Reserved	7:0	Reserved	0x00	R	Reserved		
		7:6	fixed_eq_BST0		RW	Fixed IN1 CTLE setting for 270M and 1.5G SMPTE rates. If		
		5:4	fixed_eq_BST1		RW	Reg 0x3F[0] = 0, Reg 0x3A fixed IN1 CTLE setting is also used for 3G rate		
0x3A	Low Data Rate	3:2	fixed_eq_BST2	0x00	RW	[7:6]: 2-bit control for Stage 0 of the CTLE		
		1:0	fixed_eq_BST3		RW	<ul><li>[5:4]: 2-bit control for Stage 1 of the CTLE.</li><li>[3:2]: 2-bit control for Stage 2 of the CTLE.</li><li>[1:0]: 2-bit control for Stage 3 of the CTLE.</li></ul>		
0x3B	Reserved	7:0	Reserved	0x96	R	Reserved		
0x3C	Reserved	7:0	Reserved	0x90	R	Reserved		
0x3D	Reserved	7:0	Reserved	0x00	RW	Reserved		
0x3E HEO_VEO Lock Monitor Enable	HEO_VEO Lock Monitor Enable	7	heo_veo_lockmon_en	0x80	RW	Enable HEO/VEO lock monitoring. Once the lock and adaptation processes are complete, HEO/VEO monitoring is performed once per the interval determined by Reg 0x69[3:0].		
		6:0	Reserved		RW	Reserved		
		7:6	Reserved		RW	Reserved		
		5	mr_adapt_mode_ov		RW	0 = Normal Behavior (Automatic Adaptation when IN1 is selected) 1 = Override Automatic Adaptation for IN1. Adaptation behavior is controlled by Reg 0x31[6:5].		
	Pin Override Register Control	4	mr_in_out_sel_ov		RW	0 = Input channel selection determined by IN_OUT_SEL pin 1 = Override input channel selection pin settings. Input selection is controlled by Reg 0x31[1:0].		
0x3F		3	mr_out_ctrl_ov	0x01	RW	0 = Output mux settings determined by OUT_CTRL pin 1 = Override output mux pin settings. Output mux is controlled by Reg 0x1C[3:2].		
0x3F		2	mr_refn_rate_ov		RW	0 = SMPTE or 10 GbE reference rates determined by IN_OUT_SEL pin 1 = Override reference rate pin settings. Reference rates for CDR lock are controlled by Reg 0x2F[7:6].		
		1	mr_eqbst_pin_ov		RW	0 = IN1 EQ boost Bypass is controlled by OUT_CTRL pin behavior 1 = Override IN1 EQ boost pin control. IN1 EQ boost bypass characteristics are controlled by settings in Reg 0x2D[3] and Reg 0x03[7:0].		
		0	mr_en_3G_divsel_eq		RW	0 = Disables IN1 EQ Adaptation for 3G data rate 1 = Enables IN1 EQ Adaptation for 3G data rate		
		7:6	EQ_index_0_BST0	-	RW	Index 0 Boost		
0x40	IN1 Index 0 Boost for	5:4	EQ_index_0_BST1	0x00	RW	[7:6]: 2-bit control for Stage 0 of the CTLE		
0,110	Adaptation	3:2	EQ_index_0_BST2	ence	RW	[3:2]: 2-bit control for Stage 2 of the CTLE.		
		1:0	EQ_index_0_BST3		RW	[1:0]: 2-bit control for Stage 3 of the CTLE.		
		7:6	EQ_index_1_BST0	+	RW	Index 1 Boost		
0x41	Boost for	5:4	EQ_index_1_BST1	0x40	RW	[7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE.		
	Adaptation	3:2	EQ_index_1_BST2	ł	RW	[3:2]: 2-bit control for Stage 2 of the CTLE.		
		1:0	EQ_index_1_BST3		RW	[1:0]: 2-bit control for Stage 3 of the CTLE.		
	IN1 Index 2	7:6	EQ_index_2_BST0	+	RW	Index 2 Boost		
0x42	Boost for	5:4	EQ_index_2_BST1	0x80	RW	[5:4]: 2-bit control for Stage 0 of the CTLE		
	Adaptation	3:2	EQ_index_2_BST2	0,00	RW	[3:2]: 2-bit control for Stage 2 of the CTLE.		
		1:0	EQ_index_2_BST3		RW	[1.0]. 2-bit control for Stage 3 of the CTLE.		
	IN1 Index 3	1:6	EQ_INDEX_3_BS10	ł	KW	Index 3 Boost [7:6]: 2-bit control for Stage 0 of the CTLE		
0x43	Boost for	5:4 2·2	EQ_INDEX_3_BOT1	0x50		[5:4]: 2-bit control for Stage 1 of the CTLE.		
	Adaptation	1:0	FQ index 3 BST3	ł	RW	[3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.		



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Address	Register Name	Bit	Field	Default	Туре	Description
		7:6	EQ_index_4_BST0		RW	Index 4 Boost
	IN1 Index 4	5:4	EQ_index_4_BST1		RW	[7:6]: 2-bit control for Stage 0 of the CTLE
0x44	Boost for Adaptation	3:2	EQ_index_4_BST2	0xC0	RW	[5:4]: 2-bit control for Stage 1 of the CTLE.
	/	1:0	EQ_index_4_BST3	†	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_5_BST0		RW	Index 5 Boost
045	IN1 Index 5	5:4	EQ_index_5_BST1	000	RW	[7:6]: 2-bit control for Stage 0 of the CTLE
0x45	Adaptation	3:2	EQ_index_5_BST2	0x90	RW	[3:2]: 2-bit control for Stage 2 of the CTLE.
		1:0	EQ_index_5_BST3	Ī	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_6_BST0		RW	Index 6 Boost
0.46	IN1 Index 6	5:4	EQ_index_6_BST1	0.454	RW	[7:6]: 2-bit control for Stage 0 of the CTLE
0x40	Adaptation	3:2	EQ_index_6_BST2	0x54	RW	[3:2]: 2-bit control for Stage 2 of the CTLE.
		1:0	EQ_index_6_BST3		RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_7_BST0		RW	Index 7 Boost
IN1 Index 7	IN1 Index 7	5:4	EQ_index_7_BST1	0.40	RW	[7:6]: 2-bit control for Stage 0 of the CTLE
0x47	Adaptation	3:2	EQ_index_7_BST2	UXAU	RW	[3:2]: 2-bit control for Stage 2 of the CTLE.
		1:0	EQ_index_7_BST3	Ī	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_8_BST0		RW	Index 8 Boost
010	IN1 Index 8	5:4	EQ_index_8_BST1	0xB0	RW	[7:6]: 2-bit control for Stage 0 of the CTLE
0X48	Boost for Adaptation	3:2	EQ_index_8_BST2		RW	[5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE.
		1:0	EQ_index_8_BST3	Ī	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_9_BST0	0.05	RW	Index 9 Boost
0.40	IN1 Index 9	5:4	EQ_index_9_BST1		RW	[7:6]: 2-bit control for Stage 0 of the CTLE
0x49	Adaptation	3:2	EQ_index_9_BST2	0x95	RW	[5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE.
		1:0	EQ_index_9_BST3	Ť	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
	7:6	EQ_index_10_BST0		RW	Index 10 Boost	
0	IN1 Index 10	5:4	EQ_index_10_BST1	0.00	RW	[7:6]: 2-bit control for Stage 0 of the CTLE
UX4A	Adaptation	3:2	EQ_index_10_BST2	0x69	RW	[3:2]: 2-bit control for Stage 1 of the CTLE.
	, captation	1:0	EQ_index_10_BST3	Ī	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_11_BST0		RW	Index 11 Boost
0.40	IN1 Index 11	5:4	EQ_index_11_BST1		RW	[7:6]: 2-bit control for Stage 0 of the CTLE
UX4B	Adaptation	3:2	EQ_index_11_BST2	UXD5	RW	[3:2]: 2-bit control for Stage 1 of the CTLE.
		1:0	EQ_index_11_BST3	Ī	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_12_BST0		RW	Index 12 Boost
040	IN1 Index 12	5:4	EQ_index_12_BST1	000	RW	[7:6]: 2-bit control for Stage 0 of the CTLE
UX4C	Adaptation	3:2	EQ_index_12_BST2	0x99	RW	[3:2]: 2-bit control for Stage 1 of the CTLE.
		1:0	EQ_index_12_BST3		RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_13_BST0		RW	Index 13 Boost
0.40	IN1 Index 13	5:4	EQ_index_13_BST1	0.45	RW	[7:6]: 2-bit control for Stage 0 of the CTLE
UX4D	Adaptation	3:2	EQ_index_13_BST2	UXAS	RW	[3:2]: 2-bit control for Stage 1 of the CTLE.
		1:0	EQ_index_13_BST3	Ī	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_14_BST0		RW	Index 14 Boost
0.45	IN1 Index 14	5:4	EQ_index_14_BST1	0	RW	[7:6]: 2-bit control for Stage 0 of the CTLE
0x4E	Adaptation	3:2	EQ_index_14_BST2	0xE6	RW	[3:2]: 2-bit control for Stage 1 of the CTLE.
	•	1:0	EQ_index_14_BST3		RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
		7:6	EQ_index_15_BST0		RW	Index 15 Boost
	IN1 Index 15 Boost for	5:4	EQ_index_15_BST1		RW	[7:6]: 2-bit control for Stage 0 of the CTLE
UX4F	Adaptation	3:2	EQ_index_15_BST2	UXF9	RW	[3:2]: 2-bit control for Stage 2 of the CTLE.
		1:0	EQ_index_15_BST3	Ī	RW	[1:0]: 2-bit control for Stage 3 of the CTLE.
0x50	Reserved	7:0	Reserved	0x00	RW	Reserved

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Address	Register Name	Bit	Field	Default	Туре	Description		
0x51	Reserved	7:0	Reserved	0x00	RW	Reserved		
0x52	IN1 Active EQ Readback	7:0	eq_bst_to_ana	0x00	R	IN1 CTLE boost setting readback from Active CTLE Adaptation.		
0x53	Reserved	7:0	Reserved	0x00	R	Reserved		
		7	cardet		R	0 = Carrier Detect from the selected input de-asserted 1 = Carrier Detect from the selected input asserted Note: Clears when Reg 0x54 is read-back.		
		6	cdr_lock_int		R	0 = No interrupt from CDR Lock 1 = CDR Lock Interrupt Note: Clears when Reg 0x54 is read-back.		
		5	carrier_det1_int		R	0 = No interrupt from IN1 Carrier Detect 1 = IN1 Carrier Detect Interrupt Note: Clears when Reg 0x54 is read-back.		
0x54	Interrupt Status	4	carrier_det0_int	0×00	R	0 = No interrupt from IN0 Carrier Detect 1 = IN0 Carrier Detect Interrupt Note: Clears when Reg 0x54 is read-back.		
	Register	3	heo_veo_int	0x00	R	0 = No interrupt from HEO/VEO 1 = HEO/VEO Threshold Reached Interrupt Note: Clears when Reg 0x54 is read-back.		
		2	cdr_lock_loss_int		R	0 = No interrupt from CDR Lock 1 = CDR Loss of Lock Interrupt Note: Clears when Reg 0x54 is read-back.		
		1	carrier_det1_loss_int		R	0 = No interrupt from IN1 Carrier Detect 1 = IN1 Carrier Detect Loss Interrupt Note: Clears when Reg 0x54 is read-back.		
		0	carrier_det0_loss_int		R	0 = No interrupt from IN0 Carrier Detect 1 = IN0 Carrier Detect Loss Interrupt Note: Clears when Reg 0x54 is read-back.		
0x55	Reserved	7:0	Reserved	0x02	R	Reserved		
		7	Reserved		RW	Reserved		
		6	cdr_lock_int_en		RW	0 = Disable interrupt if CDR lock is achieved 1 = Enable interrupt if CDR lock is achieved		
		5	carrier_det1_int_en		RW	0 = Disable interrupt if IN1 Carrier Detect is asserted 1 = Enable interrupt if IN1 Carrier Detect is asserted		
	Interrupt Control	4	carrier_det0_int_en		RW	0 = Disable interrupt if IN0 Carrier Detect is asserted 1 = Enable interrupt if IN0 Carrier Detect is asserted		
0x56	Register	3	heo_veo_int_en	0x00	RW	0 = Disable interrupt if HEO/VEO threshold is reached 1 = Enable interrupt if HEO/VEO threshold is reached		
		2	cdr_lock_loss_int_en		RW	0 = Disable interrupt if CDR loses lock 1 = Enable interrupt if CDR loses lock		
		1	carrier_det1_loss_int_ en		RW	0 = Disable interrupt if there is loss of signal (LOS) on IN1 1 = Enable interrupt if there is loss of signal (LOS) on IN1		
		0	carrier_det0_loss_int_ en		RW	0 = Disable interrupt if there is loss of signal (LOS) on IN0 1 = Enable interrupt if there is loss of signal (LOS) on IN0		
0x60	Reserved	7:0	Reserved	0x26	RW	Reserved		
0x61	Reserved	7:0	Reserved	0x31	RW	Reserved		
0x62	Reserved	7:0	Reserved	0x70	RW	Reserved		
0x63	Reserved	7:0	Reserved	0x3D	RW	Reserved		
0x64	Reserved	7:0	Reserved	0xFF	RW	Reserved		
0x65	Reserved	7:0	Reserved	0x00	RW	Reserved		
0x66	Reserved	7:0	Reserved	0x00	RW	Reserved		

RW

RW

0x00

0x00

Reserved

Reserved



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0x67

0x68

7:0

7:0

Reserved

Reserved

Reserved

Reserved



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Address	Register Name	Bit	Field	Default	Туре	Description
		7:4	Reserved		RW	Reserved
0x69	HEO_VEO Lock Monitor	3:0	hv_lckmon_cnt_ms	0x0A	RW	While monitoring lock, these bits set the amount of interval times to monitor HEO or VEO lock. Each interval is 6.5 ms. Therefore, by default, Reg 0x69[3:0] = 1010'b causes HEO_VEO lock monitor to occur once every 65 ms.
0.46.4	HEO and VEO	7:4	veo_lck_thrsh	0×44	RW	HEO/VEO lock thresholds. Lock will not be declared until
UX6A	Lock Threshold	3:0	heo_lck_thrsh	0x44	RW	HEO $\geq$ (heo_lck_thrsh x 4) and VEO $\geq$ (veo_lck_thrsh x 4).
0x6B	Reserved	7:0	Reserved	0x40	RW	Reserved
0x6C	Reserved	7:0	Reserved	0x00	RW	Reserved
0x6D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x6E	Reserved	7:0	Reserved	0x00	RW	Reserved
0x6F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x70	Reserved	7:0	Reserved	0x03	RW	Reserved
0x71	Reserved	7:0	Reserved	0x20	R	Reserved
0x72	Reserved	7:0	Reserved	0x00	RW	Reserved
0x73	Reserved	7:0	Reserved	0x00	RW	Reserved
0x74	Reserved	7:0	Reserved	0x00	RW	Reserved
0x75	Reserved	7:0	Reserved	0x00	RW	Reserved
0x77	Reserved	7:0	Reserved	0x00	RW	Reserved
0x80	Reserved	7:0	Reserved	0x50	RW	Reserved
0x81	Reserved	7:0	Reserved	0x00	RW	Reserved
0x82	Reserved	7:0	Reserved	0x80	RW	Reserved
0x83	Reserved	7:0	Reserved	0x70	RW	Reserved
0x84	Reserved	7:0	Reserved	0x04	RW	Reserved
0x85	Reserved	7:0	Reserved	0x00	RW	Reserved
0x87	Reserved	7:0	Reserved	0x00	RW	Reserved
0x90	Reserved	7:0	Reserved	0xA5	RW	Reserved
0x91	Reserved	7:0	Reserved	0x23	RW	Reserved
0x92	Reserved	7:0	Reserved	0x2C	RW	Reserved
0x93	Reserved	7:0	Reserved	0x32	RW	Reserved
0x94	Reserved	7:0	Reserved	0x37	RW	Reserved
0x95	Reserved	7:0	Reserved	0x3E	RW	Reserved
0x98	Reserved	7:0	Reserved	0x3F	RW	Reserved
0x99	Reserved	7:0	Reserved	0x04	RW	Reserved
0x9A	Reserved	7:0	Reserved	0x04	RW	Reserved
0x9B	Reserved	7:0	Reserved	0x04	RW	Reserved
0x9C	Reserved	7:0	Reserved	0x06	RW	Reserved
0x9D	Reserved	7:0	Reserved	0x04	RW	Reserved
0x9E	Reserved	7:0	Reserved	0x04	RW	Reserved
		7:5	Reserved	+	RW	Reserved
		4	dvb_enable	-	RW	0 = Disable CDR Lock to 270 Mbps 1 = Enable CDR Lock to 270 Mbps
	SMPTE Data	3	hd_enable	-	RW	0 = Disable CDR Lock to 1.485/1.4835 Gbps 1 = Enable CDR Lock to 1.485/1.4835 Gbps
0xA0	Rate Lock Enable	2	3G_enable	0x1F	RW	0 = Disable CDR Lock to 2.97/2.967 Gbps 1 = Enable CDR Lock to 2.97/2.967 Gbps
		1	6G_enable		RW	0 = Disable CDR Lock to 5.94/5.934 Gbps 1 = Enable CDR Lock to 5.94/5.934 Gbps
		0	12G_enable		RW	0 = Disable CDR Lock to 11.88/11.868 Gbps 1 = Enable CDR Lock to 11.88/11.868 Gbps



# 7.5.3 CableEQ/Drivers Register Page

Address	Register Name	Bit	Field	Default	Туре	Description			
		7	adapt_cd		RW	LOCK_N pin status 0 = LOCK_N indicates when Coarse Adaptation for IN0 is done 1 = LOCK_N indicates carrier detect (CD_N) for IN0			
		6	Reserved		RW	Reserved			
		5	reg_power_save_ov		RW	<ul> <li>IN0 Power Save Override Control for Cable EQ</li> <li>0 = Disable Power Save Mode override. Automatic Power Save when no input signal detected.</li> <li>1 = Enable Power Save Mode override. Power Save mode control set by value in Reg 0x00[4:3].</li> <li>Note: Unused input is always powered down automatically.</li> </ul>			
0x00	Reset CableEQ/Drivers Registers	4:3	reg_power_save	0x08	RW	INO Auto Power Save Mode control for Cable EQ if Reg 0x00[5] = 1 00 = Enable Power Save Mode when no input signal is detected 01 = Disable auto Power Save Mode (disable power down) 10 = Reserved 11 = Force Power Save Mode Note: Unused input is always powered down automatically.			
		2	rst_cableEQ/Drivers_ regs		RW	Reset registers (self-clearing) 0 = Normal operation 1 = Reset CableEQ/Drivers Registers. Register re- initialization procedure required after resetting the CableEQ/Drivers Registers. Refer to the LMH1219 Programming Guide for details.			
			Reserved		RW	Reserved			
	EQ Observation	7:1	Reserved		R	Reserved			
0x01	Status	0	adaptation_status	0x80	R	0 = Adaptation not completed 1 = Adaptation completed			
		7	Reserved		R	Reserved			
		6	IN0 Carrier Detect		R	Carrier Detect Status of IN0 0 = No signal present at IN0 1 = Signal present at IN0			
		5:3	freq_rate_det		R	Readback of rate detected 001 = 125M-270M 010 = 1.5G-3G 100 = 6G-12G			
0x02	Rate and Driver Observation	2	power_save_status	0x07	R	Observation Bit 0 = Power Save Mode is Inactive 1 = Power Save Mode is Active			
	Glatus	1	mute_tx1		R	Observation Bit 0 = OUT1 Driver is Active 1 = OUT1 Driver is in Mute Note: When muted, driver output remains at common mode voltage.			
		0	mute_tx0		R	Observation Bit 0 = OUT0 Driver is Active 1 = OUT0 Driver is in Mute Note: When muted, driver output remains at common mode voltage.			
		7:6	Reserved		RW	Reserved			
0x03	MUTERef Control	5:0	MUTERef	0x3F	RW	Digital MUTERef sets the threshold at which the output will be muted. See the "Digital MUTE <sub>REF</sub> " subsection of the LMH1219 datasheet for more information.			
0x04	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x05	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x06	Reserved	7:0	Reserved	0xA0	RW	Reserved			
0x07	Reserved	7:0	Reserved	0x24	RW	Reserved			
0x08	Reserved	7:0	Reserved	0x27	RW	Reserved			



Address	Register Name	Bit	Field	Default	Type	Description			
0x09	Reserved	7:0	Reserved	0x01	RW	Reserved			
0x0A	Reserved	7:0	Reserved	0x05	RW	Reserved			
0x0B	Reserved	7:0	Reserved	0x37	RW	Reserved			
0x0C	Reserved	7:0	Reserved	0x01	RW	Reserved			
0x0D	Reserved	7:0	Reserved	0x25	RW	Reserved			
0x0E	Reserved	7:0	Reserved	0x37	RW	Reserved			
0x0F	Reserved	7:0	Reserved	0x02	RW	Reserved			
0x10	Reserved	7:0	Reserved	0x0A	RW	Reserved			
0x11	Reserved	7:0	Reserved	0x02	RW	Reserved			
0x12	Reserved	7:0	Reserved	0x08	RW	Reserved			
0x13	Reserved	7:0	Reserved	0x04	RW	Reserved			
0x14	Reserved	7:0	Reserved	0x3C	RW	Reserved			
0x15	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x16	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x17	Reserved	7:0	Reserved	0x08	RW	Reserved			
0x18	Reserved	7:0	Reserved	0x01	RW	Reserved			
0x19	Reserved	7:0	Reserved	0x08	RW	Reserved			
0x1A	Reserved	7:0	Reserved	0x01	RW	Reserved			
0x1B	Reserved	7:0	Reserved	0xA7	RW	Reserved			
0x1C	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x1D	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x1E	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x1F	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x20	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x21	Reserved	7:0	Reserved	0xC0	RW	Reserved			
0x22	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x23	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x24	Reserved	7:0	Reserved	0x00	RW	Reserved			
		7:6	Reserved	+	R	Reserved			
0x25	Cable Length Indicator	5:0	CLI	0x00	R	Readback of Cable Length Indicator (CLI) after adaptation. See the "Cable Length Indicator (CLI)" subsection of the LMH1219 datasheet for more information.			
0x26	Reserved	7:0	Reserved	0x05	R	Reserved			
		7:4	Reserved	+	RW	Reserved			
0x27	EQ Bypass	3	eq_bypass_ov	0x00	RW	Override eq_bypass value to analog core 0 = Disable EQ Bypass override 1 = Enable EQ Bypass override. Value of EQ Bypass Control determined by Reg 0x27[2].			
	Override	2	eq_bypass_val		RW	Override value of eq_bypass 0 = Do not Bypass Cable EQ. Use Adaptive EQ 1 = Bypass Cable EQ			
		1:0	Reserved		RW	Reserved			
0x28	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x29	Reserved	7:0	Reserved	0x20	R	Reserved			
0x2A	Reserved	7:0	Reserved	0x40	RW	Reserved			
0x2B	Reserved	7:0	Reserved	0x89	RW	Reserved			
0x2C	Reserved	7:0	Reserved	0x0B	RW	Reserved			
0x2D	Reserved	7:0	Reserved	0x20	RW	Reserved			
0x2E	Reserved	7:0	Reserved	0x00	R	Reserved			
0x2F	Reserved	7:0	Reserved	0x00	RW	Reserved			

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Address	Register Name	Bit	Field	Default	Туре	Description			
		7	tx0_mute_ov		RW	OUT0 Mute Override Control 0 = Disable OUT0 Mute Override Control 1 = Enable OUT0 Mute Override Control by value in Reg 0x30[6].			
		6	tx0_mute_val		RW	0 = Normal Operation 1 = Mute OUT0 if Reg 0x30[7] = 1			
0x30	OUT0 Output Control	5	tx0_vod_ov	0x0A	RW	OUT0 VOD Override Control 0 = VOD settings for OUT0 determined by VOD_DE pin 1 = Override VOD pin settings for OUT0. VOD settings for OUT0 are controlled by Reg 0x30[2:0]			
		4:3	Reserved		RW	Reserved			
		2:0	tx0_vod		RW	VOD settings for OUT0 if Reg 0x30[5] = 1. See the "Output Amplitude vs. VOD Register Settings" graph in the Typical Characteristics subsection of the LMH1219 datasheet for more information.			
		7	Reserved		RW	Reserved			
0x31		6	6 tx0_dem_ov RW OUT0 De-Emphasis Override Control 0 = De-emphasis for OUT0 determined by 1 = Override De-emphasis settings for OU settings for OUT0 are controlled by Reg 0:		OUT0 De-Emphasis Override Control 0 = De-emphasis for OUT0 determined by VOD_DE pin 1 = Override De-emphasis settings for OUT0. De-emphasis settings for OUT0 are controlled by Reg 0x31[2:0]				
	OUT0 De-Emphasis Control	5	tx0_PD_ov	0x01	RW	OUT0 Power Down Override Control 0 = Disable OUT0 Power Down Override Control 1 = Enable OUT0 Power Down Override Control by value in Reg 0x31[4]			
		4	tx0_PD		RW	0 = Normal Operation 1 = Power Down OUT0 if Reg 0x31[5] = 1			
		3	Reserved		RW	Reserved			
		2:0	tx0_dem		RW	De-emphasis settings for OUT0 if Reg 0x31[6] = 1. See the "Output De-emphasis vs. VOD Register Settings" graph in the Typical Characteristics subsection of the LMH1219 datasheet for more information.			
		7	tx1_mute_ov		RW	OUT1 Mute Override Control 0 = Disable OUT1 Mute Override Control 1 = Enable OUT1 Mute Override Control by value in Reg 0x32[6].			
		6	tx1_mute_val		RW	0 = Normal Operation 1 = Mute OUT1 if Reg 0x32[7] = 1			
0x32	OUT1 Output Control	5	tx1_vod_ov	0x0A	0x0A	RW	OUT1 VOD Override Control 0 = VOD settings for OUT1 determined by VOD_DE pin 1 = Override VOD pin settings for OUT1. VOD settings for OUT1 are controlled by Reg 0x32[2:0]		
		4:3	Reserved		RW	Reserved			
		2:0	tx1_vod		RW	VOD settings for OUT0 if Reg 0x32[5] = 1. See the "Output Amplitude vs. VOD Register Settings" graph in the Typical Characteristics subsection of the LMH1219 datasheet for more information.			



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Address	Register Name	Bit	Field	Default	Туре	Description			
		7	Reserved		RW	Reserved			
		6	tx1_dem_ov		RW	OUT1 De-Emphasis Override Control 0 = De-emphasis for OUT1 determined by VOD_DE pin 1 = Override De-emphasis settings for OUT1. De-emphasis settings for OUT1 are controlled by Reg 0x33[2:0]			
0x33	OUT1 De-Emphasis Control	5	tx1_PD_ov	0x11	RW	OUT1 Power Down Override Control 0 = Disable OUT1 Power Down Override Control 1 = Enable OUT1 Power Down Override Control by value in Reg 0x33[4].			
	Control	4	tx1_PD	RW		0 = Normal Operation 1 = Power Down OUT1 if Reg 0x33[5] = 1			
		3	Reserved		RW	Reserved			
		2:0	tx1_dem		RW	De-emphasis settings for OUT1 if Reg 0x33[6] = 1. See the "Output De-emphasis vs. VOD Register Settings" graph in the Typical Characteristics subsection of the LMH1219 datasheet for more information.			
0x34	Splitter_Reg	7	hi_gain_mode	0x17	RW	-6 dB Launch Amplitude Adaptation Mode 0 = Enable EQ adaptation with nominal 800 mV launch amplitude 1 = Enable EQ adaptation with 400 mV launch amplitude			
		6:0	Reserved			Reserved			
0x35	Reserved	7:0	Reserved	0x61	RW	Reserved			
0x36	Reserved	7:0	Reserved	0x02	RW	Reserved			
0x37	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x38	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x39	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x3A	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x3B	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x3C	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x3D	Reserved	7:0	Reserved	0x7F	RW	Reserved			
0x3E	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x3F	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x40	Reserved	7:0	Reserved	0x00	R	Reserved			
0x41	Reserved	7:0	Reserved	0x00	R	Reserved			
0x42	Reserved	7:0	Reserved	0x00	R	Reserved			
0x43	Reserved	7:0	Reserved	0x00	R	Reserved			
0x44	Reserved	7:0	Reserved	0x00	R	Reserved			
0x45	Reserved	7:0	Reserved	0x00	R	Reserved			
0x46	Reserved	7:0	Reserved	0x00	R	Reserved			
0x47	Reserved	7:0	Reserved	0x00	R	Reserved			
0x48	Reserved	7:0	Reserved	0x00	R	Reserved			
0x49	Reserved	7:0	Reserved	0x01	R	Reserved			
0x4A	Reserved	7:0	Reserved	0x00	R	Reserved			
0x4B	Reserved	7:0	Reserved	0x00	R	Reserved			
0x4C	Reserved	7:0	Reserved	0x00	R	Reserved			
	Reserved	7:0	Reserved	0x00	RW	Reserved			
0x4E	Reserved	7.0	Reserved	0000	RW	Reserved			
	Reserved	7:0	Reserved	0x00		Posoniod			
0x50	Reserved	7.0	Posserved	0x00		Posoniod			
0723	Reserved	7.0	Reserved	0x00		Pesenved			
072	Record	7.0 7.0	Reserved	0,00		Pesenved			
0,00	People	7.0	Peopled			Posoniod			
0304	ILESEIVEU	1.0	<b>Neseive</b> ü	UXUF	л	IVESCIVEU			

## 8 Application and Implementation

#### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

## 8.1.1 General Guidance for SMPTE and 10 GbE Applications

SMPTE specifies the requirements for the Serial Digital Interface to transport digital video over coaxial cables. One of the requirements is meeting return loss, which specifies how closely the port resembles 75- $\Omega$  impedance across a specified frequency band. The SMPTE specifications also defines the use of AC coupling capacitors for transporting uncompressed serial data streams with heavy low frequency content. The use of 4.7- $\mu$ F AC coupling capacitors is recommended to avoid low frequency DC wander. SFF-8431 (SFP+) requires the 100- $\Omega$  transmit signal to meet the electrical, return loss, jitter, and eye mask specifications. TI recommends placing the LMH1219 as close as possible to the 75- $\Omega$  BNC and 100- $\Omega$  SFP+ optical module in order to meet the specifications for SMPTE and SFF-8431. Refer to  $\frac{1}{2}$  9 for design guidelines.

#### 8.1.2 Optimizing Time to Adapt and Lock

When carrier detect is asserted the LMH1219 continuously adapts the cable equalizer to the optimal gain and bandwidth. The time required to adapt the equalizer and achieve lock to the incoming signal can be optimized by manually programming the highest data rate expected in the application. Refer to LMH1219 programming guide for more details.

### 8.1.3 LMH1219 and LMH0324 Compatibility

The LMH1219 is pin compatible with the LMH0324 (3 Gbps adaptive cable equalizer) when the LMH0324 RSV\_L pin is tied to 2.5 V. This pin compatibility allows users to upgrade easily from a 3 Gbps equalizer to a 12 Gbps UHD equalizer with integrated reclocker. See 🛽 21 for details.



图 21. Pin Connections for LMH1219 and LMH0324 Compatibility

## 8.2 Typical Application

The LMH1219 is a low-power cable equalizer with integrated reclocker that supports SDI data rates up to 11.88 Gbps and 10 GbE. 2 2 shows a typical implementation of the LMH1219 as a SDI adaptive cable equalizer at IN0+. Signal attenuated by a long coax cable is applied to the LMH1219 at the BNC port. Signal from a 10 GbE optical module is connected to the input port at IN1±. Equalized and reclocked data is output at OUT0± and OUT1± to a downstream video processor.



# Typical Application (接下页)





### 8.2.1 Design Requirements

#### 表 9. LMH1219 Design Requirements

DESIGN PARAMETER	REQUIREMENTS
IN0+ Input AC coupling capacitor	AC Coupling capacitor at IN0+ should be a 4.7- $\mu$ F capacitor. Choose a small 0402 surface mount ceramic capacitor. IN0- should be AC terminated with 4.7 $\mu$ F and 75 $\Omega$ to VSS.
IN1± Input AC coupling capacitors	AC Coupling capacitors at IN1 $\pm$ should be 4.7- $\mu$ F capacitors. Choose small 0402 surface mount ceramic capacitors. This allows both SMPTE and 10 GbE data traffic.
Output AC coupling capacitors	Both OUT0 $\pm$ and OUT1 $\pm$ require AC coupling capacitors. Choose small 0402 surface mount ceramic capacitors. 4.7- $\mu$ F AC coupling capacitors are recommended.
DC power supply decoupling capacitors	Decoupling capacitors are required to minimize power supply noise. Place $10-\mu F$ and $1-\mu F$ bulk capacitors close to each device. Place a $0.1-\mu F$ capacitor close to each supply pin.
VDD_LDO decoupling capacitors	Place 1- $\mu$ F and 0.1- $\mu$ F surface mount ceramic capacitors as close as possible to the device VDD_LDO pin.
High speed board trace for IN0	IN0+ and IN0- should be routed with uncoupled board traces with 75- $\Omega$ characteristic impedance.
High Speed IN1, OUT0, and OUT1 trace impedance	IN1±, OUT0± and OUT1± should be routed with coupled board traces with 100- $\Omega$ differential impedance.
SMPTE return loss	Place BNC within 1 inch of the LMH1219 and consult BNC vendor for recommended BNC landing pattern to meet SMPTE requirements.
IN0+ and IN1± cross talk	When a long length coax cable is connected to IN0+, the signal amplitude at IN0+ can be just a few mVp-p. Layout precautions must be taken to minimize crosstalk from adjacent devices or from adjacent input port IN1 $\pm$ . To reduce cross coupling effects, keep IN1 $\pm$ traces as far from IN0 $\pm$ as possible. When IN1 $\pm$ is not used, it is recommended to turn off the signal source to IN1 $\pm$ for best results.
Use of SPI or SMBus interface	Set MODE_SEL to Level-F (pin unconnected) for SPI. Set MODE_SEL to Level-L (connect 1 $k\Omega$ to VSS) for SMBus. SMBus is 3.3 V tolerant.

#### 8.2.2 Detail Design Procedure

The following general design procedure is recommended:

- 1. Select a suitable power supply voltage for the LMH1219. See Power Supply Recommendations for details.
- 2. Check that the power supply meets the DC and AC requirements in Recommended Operating Conditions.
- 3. Select the proper pull-high or pull-low resistors for IN\_OUT\_SEL and OUT\_CTRL for setting the signal path.



- 4. If -6 dB launch amplitude or other expanded programmable features are needed, select the use of SPI or SMBus by setting Level-F or Level-L for MODE\_SEL, respectively.
- 5. Choose a high quality  $75-\Omega$  BNC that is capable of supporting 11.88 Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended footprint for meeting SMPTE return loss.
- Depending on the length and insertion loss of the output traces for OUT0± and OUT1±, select the proper pull-high or pull-low resistors for VOD\_DE to set the output amplitude and de-emphasis settings. Refer to Table 5 for details.
- 7. Follow all design requirements detailed in  $\frac{1}{5}$  9 to optimize LMH1219 performance.
- 8. For additional layout recommendations, refer to PCB Layout Guidelines.

#### 8.2.3 Recommended VOD and DEM Register Settings

表 10 shows recommended output amplitude and de-emphasis register settings for most applications.



表 1	0. V	'OD	and	DEM	Register	Settings
-----	------	-----	-----	-----	----------	----------

VOD REG SETTING OUT0±: 0x30[5]=1, 0x30[2:0] OUT1±: 0x32[5]=1, 0x32[2:0]	DEM REG SETTING OUT0±: 0x31[6]=1, 0x31[2:0] OUT1±: 0x33[6]=1, 0x33[2:0]	VOD (mVpp)	DEM (dB)
0	0	410	0
1	1	486	-0.1
2	1	560	-0.1
2	2	560	-0.9
3	1	635	-0.3
3	2	635	-1.3
3	3	635	-2.4
4	1	716	-0.5
4	2	716	-1.8
4	3	716	-3.0
4	4	716	-4.0
5	1	810	-0.8
5	2	810	-2.4
5	3	810	-3.6
5	4	810	-4.6
5	5	810	-6.1
6	1	880	-1.0
6	2	880	-2.7
6	3	880	-4.0
6	4	880	-5.0
6	5	880	-6.5
7	1	973	-1.2
7	2	973	-3.1
7	3	973	-4.6
7	4	973	-5.7
7	5	973	-7.1

#### 8.2.4 Application Performance Plots

Depending on the selected input, the LMH1219 performance was measured with the test setups shown in 图 23 and 图 24.



图 23. Test Setup for LMH1219 Cable Equalizer (IN0+)



图 24. Test Setup for LMH1219 PCB Equalizer (IN1±)

The eye diagrams in this subsection show how the LMH1219 improves overall signal integrity in the data path for 75- $\Omega$  coax cable input length (CC) when IN0 is selected and 100- $\Omega$  differential FR4 PCB trace when IN1 is selected.

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#### 9 Power Supply Recommendations

The LMH1219 is designed to provide flexibility in supply rails. There are two ways to power the LMH1219:

- Single Supply Mode (2.5 V): This mode offers ease of use, with the internal circuitry receiving power from the on-chip 1.8 V regulator. In this mode, 2.5 V is applied to VDD\_CDR, VIN, and VDDIO. See 图 39 for more details.
- Dual Supply Mode (2.5 V and 1.8 V): This mode provides lower power consumption. In this mode, 1.8 V is connected to both VIN and VDD\_LDO. VDD\_CDR, and VDDIO are powered from a 2.5 V supply. See 图 40 for more details.
- When Dual Supply Mode is used, the 2.5 V supply for VDD\_CDR and VDDIO should be powered *before or at the same time as* the 1.8 V supply that powers VIN and VDD\_LDO.



图 39. Typical Connection for Single 2.5 V Supply



图 40. Typical Connection for Dual 2.5 V and 1.8 V Supply

For power supply de-coupling, 0.1- $\mu$ F surface-mount ceramic capacitors are recommended to be placed close to each VDD\_CDR, VIN, VDD\_LDO, and VDDIO supply pin to VSS. Larger bulk capacitors (for example, 10  $\mu$ F and 1  $\mu$ F) are recommended for VDD\_CDR and VIN. Good supply bypassing requires low inductance capacitors. This can be achieved through an array of multiple small body size surface-mount bypass capacitors in order to keep low supply impedance. Better results can be achieved through the use of a buried capacitor formed by a VDD and VSS plane separated by 2-4 mil dielectric in a printed circuit board.

## 10 Layout

#### 10.1 PCB Layout Guidelines

The following guidelines are recommended for designing the board layout for the LMH1219:

1. Choose a suitable board stack-up that supports  $75 \cdot \Omega$  single-ended trace and  $100 \cdot \Omega$  differential trace routing on the board's top layer. This is typically done with a Layer 2 ground plane reference for the  $100 \cdot \Omega$ 



## PCB Layout Guidelines (接下页)

differential traces and a second ground plane at Layer 3 reference for the 75- $\Omega$  single end traces.

- 2. Use single-ended uncoupled trace designed with 75- $\Omega$  impedance for signal routing to IN0+ and IN0-. The trace width is typically 8-10 mil reference to a ground plane at Layer 3.
- 3. Place anti-pad (ground relief) on the power and ground planes directly under the 4.7-µF AC coupling capacitor and IC landing pads to minimize parasitic capacitance. The size of the anti-pad depends on the board stack-up and can be determined by a 3-dimension electromagnetic simulation tool.
- 4. Use a well-designed BNC footprint to ensure the BNC's signal landing pad achieves 75-Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
- 5. Keep trace length short between the BNC and IN0+. The trace routing for IN0+ and IN0- should be symmetrical, approximately equal lengths and equal loading.
- 6. Use coupled differential traces with  $100-\Omega$  impedance for signal routing to IN1±, OUT0± and OUT1±. They are usually 5-8 mil trace width reference to a ground plane at Layer 2.
- 7. The exposed pad EP of the package should be connected to the ground plane through an array of vias. These vias are solder-masked to avoid solder flowing into the plated-through holes during the board manufacturing process.
- 8. Connect each supply pin (VDD\_CDR, VIN, VDDIO, VDD\_LDO) to the power or ground planes with a short via. The via is usually placed tangent to the supply pins' landing pads with the shortest trace possible.
- 9. Power supply bypass capacitors should be placed close to the supply pins. They are commonly placed at the bottom layer and share the ground of the EP.



### 10.2 Layout Example

The following example demonstrates the high speed signal trace routing to the LMH1219.

- 1. BNC footprint and anti-pad: Consult BNC manufacturer for proper size.
- 2. Anti-pad under passive components.
- 3. 75- $\Omega$  single ended trace. Trace width should be similar to that of the IC landing pad (10 mil).
- 4. 100- $\Omega$  coupled trace.
- 5. Vias with solder mask.





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#### 11 器件和文档支持

#### 11.1 接收文档更新通知

要接收文档更新通知,请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册,即可每周接收产品信息更改摘要。有关更改的详细信息,请查看任何已修订文档中包含的修订历史记录。

#### 11.2 社区资源

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ESD 的损坏小至导致微小的性能降级,大至整个器件故障。精密的集成电路可能更容易受到损坏,这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

#### 11.5 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更, 恕不另行通知, 且 不会对此文档进行修订。如需获取此产品说明书的浏览器版本, 请参阅左侧的导航栏。



## **PACKAGING INFORMATION**

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
LMH1219RTWR	Active	Production	WQFN (RTW)   24	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L1219A2
LMH1219RTWR.A	Active	Production	WQFN (RTW)   24	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L1219A2
LMH1219RTWR.B	Active	Production	WQFN (RTW)   24	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L1219A2
LMH1219RTWT	Active	Production	WQFN (RTW)   24	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L1219A2
LMH1219RTWT.A	Active	Production	WQFN (RTW)   24	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L1219A2
LMH1219RTWT.B	Active	Production	WQFN (RTW)   24	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L1219A2

<sup>(1)</sup> **Status:** For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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# PACKAGE OPTION ADDENDUM

23-May-2025



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STRUMENTS

## TAPE AND REEL INFORMATION





#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1219RTWR	WQFN	RTW	24	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH1219RTWT	WQFN	RTW	24	250	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1



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# PACKAGE MATERIALS INFORMATION

1-Aug-2025



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1219RTWR	WQFN	RTW	24	3000	356.0	356.0	36.0
LMH1219RTWT	WQFN	RTW	24	250	208.0	191.0	35.0

# **RTW0024A**



# **PACKAGE OUTLINE**

# WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



# **RTW0024A**

# **EXAMPLE BOARD LAYOUT**

# WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



# **RTW0024A**

# **EXAMPLE STENCIL DESIGN**

# WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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