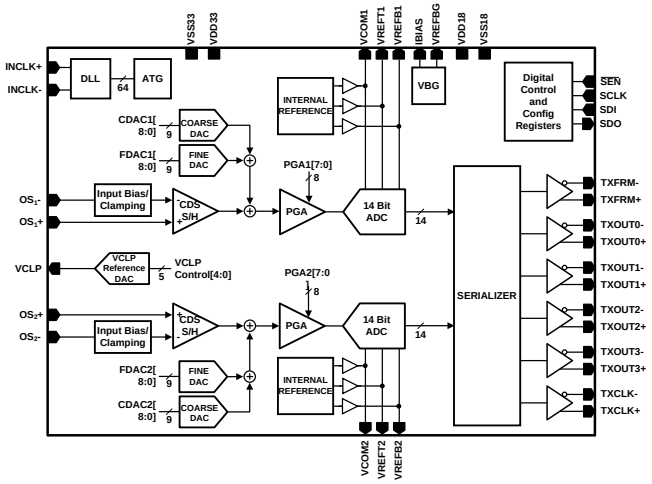
具有 LVDS 输出的 LM98640QML-SP 抗辐射加固 (RHA) 型、双通道、14 位、40MSPS 模拟前端

1 特性

- 耐辐射
  - TID 100krad(Si)
  - 单粒子锁定 (SEL) 对于 LET 的抗扰度 = 120MeV-cm^2/mg
  - 在高达 120MeV-cm^2/mg 的条件下无单粒子功能中断 (SEFI)
  - SMD 5962R1820301VXC
- ADC 分辨率：14 位
- ADC 采样速率：5MSPS 至 40MSPS
- 输入电平：2.85V
- 电源电压 3.3V 和 1.8V（标称值）
  - 15MSPS 时的每通道功耗为 125mW
  - 40MSPS 时的每通道功耗为 178mW
- 针对 CCD 或 CIS 传感器的 CDS 或 S/H 处理
  - CDS 或 S/H 增益为 0dB 或 6dB
- 每个通道具有可编程模拟增益
  - 256 步；范围 –3dB 至 18dB
- 可编程模拟失调电压校正
  - 精细和粗略 DAC 分辨率 ±8 位
  - 精细 DAC 范围 ±5mV
  - 粗略 DAC 范围 ±250mV
- 可编程输入钳位电压
- 可编程采样边沿：1/64 像素周期
- 15MHz 时的 INL：±3.5LSB
- 本底噪声：–79dB
- 串扰：–80dB
- 工作温度：–55°C 至 125°C



2 应用

- 太空卫星科学 应用
  - 焦平面电子学
  - 成像姿态控制系统
  - 地球成像

3 说明

LM98640QML-SP 是一种完全集成的高性能 14 位 5MSPS 至 40MSPS 信号处理解决方案。串行 LVDS 输出格式在单粒子曝光期间表现良好，可防止数据丢失。LM98640QML-SP 具有自适应功率调节功能，可根据工作频率和所需增益量优化功耗。借助创新型架构，并利用相关双采样 (CDS) 技术 - 通常用于 CCD 阵列或采样保持 (S/H) 输入（用于 CIS 和 CMOS 图像传感器），可实现高速信号吞吐量。采样边沿可编程为 1/64 像素周期的分辨率。CDS 和 S/H 都具有 0dB 或 6dB 的可编程增益。信号路径使用两个 ±8 位失调电压校正 DAC 进行粗略和精细的失调电压校正，并使用可为每个输入独立编程的 8 位可编程增益放大器 (PGA)。然后，信号将传送至两个片上 14 位 40MHz 高性能模数转换器 (ADC)。全差分处理通道提供卓越的抗噪能力，在 1 倍增益下具有 –79dB 的极低本底噪声。

器件信息(1)

器件型号	等级	封装
5962R1820301VXC	QMLV RHA（SMD 器件）[100krad(Si)]	CQFP (68)
LM98640W-MLS	飞行 RHA（非 SMD 器件）[100krad(Si)]	CQFP (68)
LM96840W-MPR	工程样片(2)	CQFP (68)
LM98640CVAL	陶瓷评估板	EVM

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 这些部件仅适用于工程评估。部件按照不合规的流程进行加工处理。这些部件不适用于质检、生产、辐射测试或飞行。无法在 –55°C 至 125°C 的完整 MIL 额定温度范围内或运行寿命中保证这些器件的性能。

目录

4 修订历史记录

Changes from Revision F (October 2018) to Revision G **Page**

- Changed pin diagram in *Pin Configuration and Functions* section to correct typographical error ... 4

Changes from Revision E (December 2017) to Revision F **Page**

- 已删除 运行寿命测试 Delta 参数表 ... 1
- 更新*特性* 部分的列表项以包含 SMD 信息 ... 1
- 更新*应用* 部分 ... 1
- 已添加 向“器件信息”表中添加新的可订购器件 ... 1
- 已添加 工程样片脚注 ... 1
- 已删除 “器件信息”表中的 LM98640-MDR 和 LM9864-MDP ... 1
- Updated thermal metrics ... 8
- Deleted 15 MHz and 25 MHz min/max spec ... 11
- Changed ENOB typical for subgroup 6 at 25 MHz ... 16
- Added minimum spec value for ENOB subgroups 4,5 at 40 MHz ... 16
- Changed pulses to windows ... 23
- Updated wording in CDS Mode CLAMP/SAMPLE Adjust section ... 23
- Updated wording in Input Bias and Clamping section ... 24

Changes from Revision D (September 2015) to Revision E **Page**

- 已更改 在“器件信息”表中将 64 引线更改为 68 引线 ... 1

Changes from Revision C (April 2013) to Revision D **Page**

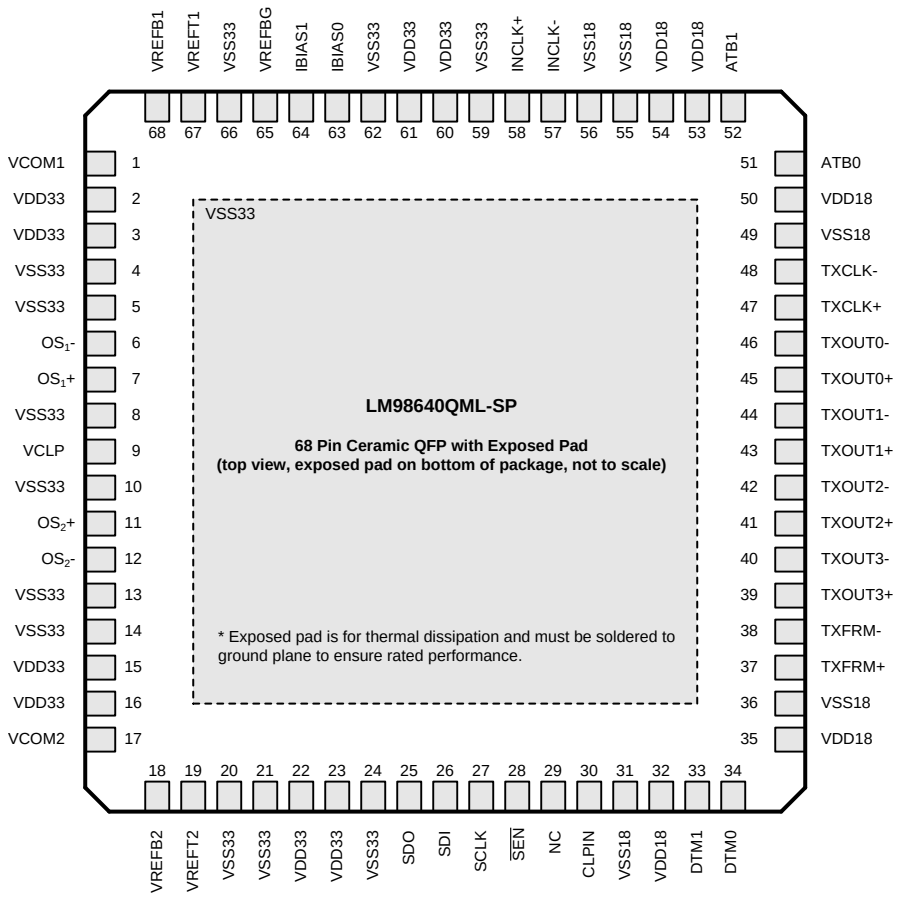
- 根据新的数据表标准添加、更新或修订以下部分：*说明*、*引脚配置和功能*、*规格*、*详细 说明*、*应用和实施*、*电源建议*、*布局*、*器件和文档支持*、*机械*、*封装和订购信息* 1
- Changed CLPIN I_{IH} from 44 to 100 µA 9
- Changed $\overline{SEN}$ I_{IH} from 28 to 100 µA 9
- Changed $\overline{SEN}$ I_{IL} from –70 to –100 µA 9
- Changed INCLK I_{IHL} from 36 to 100 µA 9
- Added mininum limits for t_{DSO}, t_{DSE}, t_{QSR} and t_{QHF} and deleted maximum limits 17
- Added details on register write. 34
- Changed Device Revision ID from x01 to x48 37
- Changed Device Revision ID from x01 to x48 45
- Added TID test and ELDRS-free information 46

Changes from Revision B (January 2011) to Revision C **Page**

- 将美国国家半导体数据表的布局更改为 TI 格式 1

5 Pin Configuration and Functions

68-Pin QFP
Package NBB0068D
Top View



Pin Functions

PIN	NAME	I/O(1)	TYP	RES	DESCRIPTION
1	VCOM1	O	A		Common mode of ADC reference. Bypass with 0.1-µF capacitor to VSS33.
2	VDD33		P		Analog power supply. Decouple with minimum 0.1-µF capacitor to VSS33 plane.
3	VDD33		P		Analog power supply. Decouple with minimum 0.1-µF capacitor to VSS33 plane.
4	VSS33		P		Analog supply return.
5	VSS33		P		Analog supply return.
6	OS1-	I	A		Analog input signal.
7	OS1+	I	A		Sample/Hold Mode Reference Level. Bypassed with a 0.1-µF to ground in CDS mode.
8	VSS33		P		Analog supply return.
9	VCLP	O	A		Programmable Clamp Voltage output. Normally bypassed with a 0.1-µF capacitor to VSS33.
10	VSS33		P		Analog supply return.
11	OS2+	I	A		Sample/Hold Mode Reference Level. Bypassed with a 0.1-µF to ground in CDS mode.
12	OS2-	I	A		Analog input signal.
13	VSS33		P		Analog supply return.
14	VSS33		P		Analog supply return.
15	VDD33		P		Analog power supply. Decouple with minimum 0.1-µF capacitor to VSS33 plane.
16	VDD33		P		Analog power supply. Decouple with minimum 0.1-µF capacitor to VSS33 plane.
17	VCOM2	O	A		Common mode of ADC reference. Bypass with 0.1-µF capacitor to ground.
18	VREFB2	O	A		Bottom of ADC reference. Bypass with a 0.1-µF capacitor to ground.
19	VREFT2	O	A		Top of ADC reference. Bypass with a 0.1-µF capacitor to ground.
20	VSS33		P		Analog supply return.
21	VSS33		P		Analog supply return.
22	VDD33		P		Analog power supply. Decouple with minimum 0.1-µF capacitor to VSS33 plane.
23	VDD33		P		Analog power supply. Decouple with minimum 0.1-µF capacitor to VSS33 plane.
24	VSS33		P		Analog supply return.
25	SDO	O	D		Serial Interface Data Output. (Tri-State when $\overline{SEN}$ is high)
26	SDI	I	D		Serial Interface Data Input. (Tri-State when $\overline{SEN}$ is high)
27	SCLK	I	D	PD	Serial Interface shift register clock. (Tri-State when $\overline{SEN}$ is high)
28	$\overline{SEN}$	I	D	PU	Active-low chip enable for the Serial Interface.
29	NC				No Connection. Can be connected to VSS18.
30	CLPIN	I	D		Input clamp signal.
31	VSS18		P		Digital supply return.
32	VDD18		P		Digital power supply. Decouple with minimum 0.1-µF capacitor to VSS18 plane.
33	DTM1	O	D		Digital Timing Monitor. If not used, can be connected to VDD18 through a 10-kΩ resistor.
34	DTM0	O	D		Digital Timing Monitor. If not used, can be connected to VDD18 through a 10-kΩ resistor.
35	VDD18		P		Digital power supply. Decouple with minimum 0.1-µF capacitor to VSS18 plane.
36	VSS18		P		Digital supply return.
37	TXFRM+	O	D		LVDS Frame+
38	TXFRM-	O	D		LVDS Frame-
39	TXOUT3+	O	D		LVDS Data Out3+
40	TXOUT3-	O	D		LVDS Data Out3-
41	TXOUT2+	O	D		LVDS Data Out2+
42	TXOUT2-	O	D		LVDS Data Out2-
43	TXOUT1+	O	D		LVDS Data Out1+
44	TXOUT1-	O	D		LVDS Data Out1-
45	TXOUT0+	O	D		LVDS Data Out0+

(1) (I = Input), (O = Output), (IO = Bi-directional), (P = Power), (D = Digital), (A = Analog), (PU = Pull Up with an internal resistor), (PD = Pull Down with an internal resistor.).

Pin Functions (continued)

PIN	NAME	I/O(1)	TYP	RES	DESCRIPTION
46	TXOUT0-	O	D		LVDS Data Out0-
47	TXCLK+	O	D		LVDS Clock+
48	TXCLK-	O	D		LVDS Clock-
49	VSS18		P		Digital supply return.
50	VDD18		P		Digital power supply. Decouple with minimum 0.1-µF capacitor to VSS18 plane.
51	ATB0	O	A		Analog Test Bus. If not used, can be connected to VSS18 through a 10-kΩ resistor.
52	ATB1	O	A		Analog Test Bus. If not used, can be connected to VSS18 through a 10-kΩ resistor.
53	VDD18		P		Digital power supply. Decouple with minimum 0.1-µF capacitor to VSS18 plane.
54	VDD18		P		Digital power supply. Decouple with minimum 0.1-µF capacitor to VSS18 plane.
55	VSS18		P		Digital supply return.
56	VSS18		P		Digital supply return.
57	INCLK-	I	D		Clock Input. Inverting input for LVDS clocks.
58	INCLK+	I	D		Clock Input. Non-Inverting input for LVDS clocks.
59	VSS33		P		Analog supply return.
60	VDD33		P		Analog power supply. Decouple with minimum 0.1-µF capacitor to VSS33 plane.
61	VDD33		P		Analog power supply. Decouple with minimum 0.1-µF capacitor to VSS33 plane.
62	VSS33		P		Analog supply return.
63	IBIAS0	I	A		Connect with external 10-kΩ 1% resistor to IBIAS1 pin.
64	IBIAS1	I	A		Connect with external 10-kΩ 1% resistor to IBIAS0 pin.
65	VREFBG	O	A		Band gap reference output. Bypass with a 0.1-µF capacitor to VSS33. Can be overdriven with external voltage source.
66	VSS33		P		Analog supply return.
67	VREFT1	O	A		Top of ADC reference. Bypass with a 0.1-µF capacitor to VSS33.
68	VREFB1	O	A		Bottom of ADC reference. Bypass with a 0.1-µF capacitor to VSS33.
	Exp Pad		P		Exposed pad must be soldered to ground plane to ensure rated performance.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

PARAMETER	MIN	MAX	UNIT
Supply Voltage (VDD33)		4.2	V
Supply Voltage (VDD18)		2.35	V
Voltage on any VDD33 Input Pin (Not to exceed 4.2 V)	–0.3	VDD33 + 0.3	V
Voltage on any VDD33 Output Pin (Not to exceed 4.2 V)	–0.3	VDD33 + 0.3	V
Voltage on any VDD18 Input or Output Pin (33 to 52) (Not to exceed 2.35 V)	–0.3	VDD18 + 0.3	V
Input Current at any pin other than Supply Pins(3)		±25	mA
Package Input Current (except Supply Pins)(3)		±50	mA
Maximum Junction Temperature (TA)		150	°C
Storage Temperature	–65	150	°C

(1) All voltages are measured with respect to VSS = 0 V, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the *Recommended Operating Conditions* is not recommended
(3) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < VSS or V_{IN} > VDD33), the current at that pin should be limited to 25 mA. The 50-mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.

6.2 ESD Ratings(1)

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±250	

(1) Human body model is 100-pF capacitor discharged through a 1.5-kΩ resistor. Machine model is 220-pF discharged through 0 Ω.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2500 V may actually have higher performance.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

6.3 Recommended Operating Conditions(1)

PARAMETER	MIN	MAX	UNIT
Operating Temperature (T_A)	–55	125	°C
VDD33(2)(3)	3.15	3.45	V
VDD18(2)(3)	1.7	1.9	V
| VSS33 - VSS18 |		100	mV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
(2) All voltages are measured with respect to VSS = 0 V, unless otherwise specified.
(3) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < VSS or V_{IN} > VDD33), the current at that pin should be limited to 25 mA. The 50-mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.

6.4 Thermal Information(1)

THERMAL METRIC(2)		LM98640QML-SP NBB (CFP) 68 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	
ψ_{JT}	Junction-to-top characterization parameter	1.7	
ψ_{JB}	Junction-to-board characterization parameter	7.2	
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	0.3	

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T^{JMAX} – T_A) / \theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided

(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

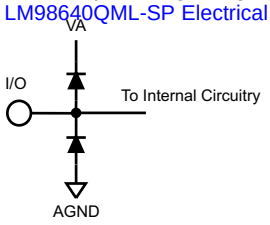
SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55
12	Setting time at	25
13	Setting time at	125
14	Setting time at	–55

6.6 LM98640QML-SP Electrical Characteristics[1][2]

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP[3]	MAX	UNIT
CMOS DIGITAL INPUT DC SPECIFICATIONS (SCLK, $\overline{SEN}$, SDI, CLPIN)								
V_{IH}	Logical “1” Input Voltage			1, 2, 3	2.0			V
V_{IL}	Logical “0” Input Voltage			1, 2, 3			0.8	V
I_{IH}	Logical “1” Input Current V_{IH} = VDD33	CLPIN		1, 2, 3		70	100	µA
		SCLK, SDI				40	300	nA
		$\overline{SEN}$				0.2	6	µA
I_{IL}	Logical “0” Input Current V_{IL} = VSS	CLPIN		1, 2, 3	–300	–85		nA
		SCLK, SDI			–300	–50		nA
		$\overline{SEN}$			–100	–70		µA
CMOS DIGITAL OUTPUT DC SPECIFICATIONS (SDO)								
V_{OH}	Logical "1" Output Voltage	I_{OUT} = –0.5 mA		1, 2, 3	1.8	1.93		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6 mA		1, 2, 3		0.05	0.2	V
I_{OH}	Output Leakage Current	V_{OUT} = V_{DD}		1, 2, 3		20	50	nA
I_{OL}	Output Leakage Current	V_{OUT} = V_{SS}		1, 2, 3	–50	–20		nA
LVDS CLOCK RECEIVER DC SPECIFICATIONS (INCLK+ and INCLK– Pins)								
V_{IHL}	Differential LVDS Clock High Threshold Voltage	R_L = 100 Ω V_{CM} (LVDS Input Common Mode Voltage) = 1.25 V		1, 2, 3		100	250	mV
V_{ILL}	Differential LVDS Clock Low Threshold Voltage	RL = 100 Ω V_{CM} (LVDS Input Common Mode Voltage) = 1.25 V		1, 2, 3	–250	–100		mV
I_{IHL}	Differential LVDS Clock Input Current	V_{IH} = VDD33		1, 2, 3		70	100	µA
I_{ILL}	Differential LVDS Clock Input Current	V_{IL} = VSS		1, 2, 3	–49	–34		µA

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per Note 2 under the LM98640QML-SP Electrical Characteristics[1][2]. However, input errors will be generated If the input goes above VDD33 and below VSS.



(2) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < VSS or V_{IN} > VDD33), the current at that pin should be limited to 25 mA. The 50-mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.

(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

LM98640QML-SP Electrical Characteristics[1][2] (continued)

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP[3]	MAX	UNIT
LVDS OUTPUT DC SPECIFICATIONS								
V_{OD}	Differential Output Voltage	LVDS Output Modes = 0000 x100 R_L = 100 Ω		1, 2, 3	210	275	410	mV
V_{OS}	LVDS Output Offset Voltage			1, 2, 3	1.05	1.19	1.3	V
V_{OD}	Differential Output Voltage	LVDS Output Modes = 0000 x101 R_L = 100 Ω		1, 2, 3	250	325	460	mV
V_{OS}	LVDS Output Offset Voltage			1, 2, 3	1.05	1.19	1.3	V
V_{OD}	Differential Output Voltage	LVDS Output Modes = 0000 x110 R_L = 100 Ω		1, 2, 3	300	377	535	mV
V_{OS}	LVDS Output Offset Voltage			1, 2, 3	0.95	1.1	1.2	V
V_{OD}	Differential Output Voltage	LVDS Output Modes = 0000 x111 R_L = 100 Ω		1, 2, 3	350	425	590	mV
V_{OS}	LVDS Output Offset Voltage			1, 2, 3	0.95	1.1	1.2	V
I_{OH}	LVDS Output Leakage Current			1, 2, 3		4.25	5	µA
I_{OL}	LVDS Output Leakage Current			1, 2, 3	–5	–4.29		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V, R_L = 100 Ω		1, 2, 3		40	50	mA

LM98640QML-SP Electrical Characteristics[1][2] (continued)

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP[3]	MAX	UNIT
POWER SUPPLY SPECIFICATIONS (see *Power Trimming* section for PGA and ADC Power Trimming register settings)								
IA	VDD33 Analog Supply Current **Dual Channel** Power optimized for **PGA Gain = 1-4x**	Powerdown Control Reg = 0x00						
		5 MHz		1, 2, 3		51.5	58	mA
		15 MHz				61.3		
		25 MHz				69.6		
		40 MHz		1, 2, 3		87.6	98	
	VDD33 Analog Supply Current **Dual Channel** Power optimized for **PGA Gain = 1-8x**	Powerdown Control Reg = 0x00						
		5 MHz		1, 2, 3		51.5	58	mA
		15 MHz				61.3		
		25 MHz				72.9		
		40 MHz		1, 2, 3		91.3	103	
	VDD33 Analog Supply Current **Single Channel** Power optimized for **PGA Gain = 1-4x**	Powerdown Control Reg = 0x15 (CH1 PD) or = 0x2A (CH2 PD)						
		5 MHz		1, 2, 3		29.5	35	mA
		15 MHz				36.1		
		25 MHz				42		
		40 MHz		1, 2, 3		53.7	60	
	VDD33 Analog Supply Current **Single Channel** Power optimized for **PGA Gain = 1-8x**	Powerdown Control Reg = 0x15 (CH1 PD) or = 0x2A (CH2 PD)						
		5 MHz		1, 2, 3		29.5	35	mA
		15 MHz				36.1		
		25 MHz				43.8		
		40 MHz		1, 2, 3		55.6	64	
	VDD33 Analog Supply Current **Powerdown**	Powerdown Control Reg = 0x80		1, 2, 3		2.85	3.85	mA
ID	VDD18 Digital Supply Current **LVDS Quad Lane Mode** LVDS Output Mode Reg = 0x0E	5 MHz				36		mA
		15 MHz				39		
		25 MHz				42		
		40 MHz				45		
	VDD18 Digital Supply Current	5 MHz		1, 2, 3		23.5	29	mA
		15 MHz				25.5		
		25 MHz				27.5		
		40 MHz		1, 2, 3		30.5	37	
	VDD18 Digital Supply Current **Powerdown**	Powerdown Control Reg = 0x80		1, 2, 3		1.2	3.0	mA
PWR	Average Power Dissipation Power optimized for PGA Gain = 1-4x Dual Channel LVDS Dual Lane Mode	5 MHz		1, 2, 3		212	244	mW
		15 MHz				250		
		25 MHz				280		
		40 MHz		1, 2, 3		345	390	
	Average Power Dissipation Power optimized for PGA Gain = 1-8x Dual Channel LVDS Dual Lane Mode	5 MHz		1, 2, 3		212	244	mW
		15 MHz				250		
		25 MHz				290		
		40 MHz		1, 2, 3		356	407	

LM98640QML-SP Electrical Characteristics[1][2] (continued)

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP[3]	MAX	UNIT
PSRR	Dynamic Power Supply Rejection Ratio CDS Gain = 1x PGA Gain = 1x	200 mVpp, 200 KHz	See[4]			–72.3		dB
		200 mVpp, 500 KHz				–72		
		200 mVpp, 1 MHz				–71		
		200 mVpp, 1.5 MHz				–68		
		200 mVpp, 2 MHz				–66		
INTERNAL REFERENCE SPECIFICATIONS								
V_{REFBG}	Reference Voltage		See[5]			1.218		V
	Reference Tolerance (chip to chip)		See[5]			±2%		
R_{REFBG}	Reference Impedance		See[5]			20		kΩ
V_{REFTC}	Temperature Coefficient	25°C to 125°C				80		ppm/°C
		–55°C to 25°C				50		
INPUT SAMPLING CIRCUIT SPECIFICATIONS								
V_{IN}	Input Voltage Level	CDS Gain = 1x, PGA Gain = 1x		1, 2, 3		2		Vp-p
		CDS Gain = 2x, PGA Gain= 1 x				1		
		CDS Gain = 1x, PGA Gain = 0.7x				2.85		
V_{RESET}	Reset Feed Through					500		mV
I_{IN_SH}	Sample and Hold Mode Input Leakage Current	CDS Gain = 1x	See[5]			384		µA
		OS_X = VDD33 (OS_X = VSS)						
		CDS Gain = 2x	See[5]			–475		µA
		OS_X = VDD33 (OS_X = VSS)						
C_{SH}	Sample/Hold Mode Equivalent Input Capacitance (see Figure 20)	CDS Gain = 1x	See[5]			4		pF
		CDS Gain = 2x	See[5]			8		pF
I_{IN_CDS}	CDS Mode Input Leakage Current	OS_X = VDD33 (OS_X = VSS)	See[5]			300		nA
R_{CLPIN}	CLPIN Switch Resistance (OS_X to VCLP Node in Figure 17)		See[5]			16		Ω

(4) Dynamic Power Supply Rejection Ratio is performed by injecting a 200-mVpp sine wave ac coupled to the analog supply pin. The LM98640QML-SP inputs are left floating in CDS mode and an FFT is captured. The spur ensured by the injected signal is recorded.
(5) This parameter is ensured by design and/or characterization and is not tested.

LM98640QML-SP Electrical Characteristics[1][2] (continued)

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP[3]	MAX	UNIT
VCLP REFERENCE CIRCUIT SPECIFICATION								
	VCLP DAC Resolution			1, 2, 3	5	5		Bits
	VCLP DAC Step Size			1, 2, 3	96	98	102	mV
V_{VCLP}	VCLP DAC Voltage Min Output	VCLP Control Register = 0110 0000		1, 2, 3	194	224	298	mV
	VCLP DAC Voltage Max Output	VCLP Control Register = 0111 1101		1, 2, 3	2.99	3.07	3.11	V
I_{SC}	VCLP DAC Short Circuit Output Current	VCLP Control Register = 011x xxxx				33		mA
COARSE ANALOG OFFSET DAC SPECIFICATIONS								
	Resolution					±8		Bits
	Offset Adjustment Range Referred to AFE Input CDS Gain = 1x	Minimum DAC Code = 0x000		1, 2, 3	–264	–262	–251	mV
		Maximum DAC Code = 0x1FF			251	263	266	
	Offset Adjustment Range Referred to AFE Input CDS Gain = 2x	Minimum DAC Code = 0x000		1, 2, 3	–132	–131	–126	mV
		Maximum DAC Code = 0x1FF			126	131	133	
	Offset Adjustment Range Referred to AFE Output	Minimum DAC Code = 0x000		1, 2, 3	–2162	–2146	–2058	LSB
		Maximum DAC Code = 0x1FF			2058	2154	2176	
	DAC Step Size CDS Gain = 1x	Input Referred				1		mV
	DAC Step Size CDS Gain = 1x	Output Referred				8		LSB
DNL	Differential Non-Linearity	CDS Gain = 1x or 2x 40 MHz		1, 2, 3	–1.1	±0.97	1.1	LSB
INL	Integral Non-Linearity	CDS Gain = 1x or 2x 40 MHz		1, 2, 3	–2.8	±1.5	2.80	LSB
FINE ANALOG OFFSET DAC SPECIFICATIONS								
	Resolution					±8		Bits
	Offset Adjustment Range Referred to AFE Input CDS Gain = 1x	Minimum DAC Code = 0x000		1, 2, 3	–5.9	–4.6	–3.1	mV
		Maximum DAC Code = 0x1FF			4.3	5.3	6.8	
	Offset Adjustment Range Referred to AFE Input CDS Gain = 2x	Minimum DAC Code = 0x000		1, 2, 3	–2.9	–2.3	–1.5	mV
		Maximum DAC Code = 0x1FF			2.1	2.6	3.4	
	Offset Adjustment Range Referred to AFE Output	Minimum DAC Code = 0x000		1, 2, 3	–48	–38	–25	LSB
		Maximum DAC Code = 0x1FF			35	43	56	
	DAC Step Size CDS Gain = 1x	Input Referred				20		uV
	DAC Step Size CDS Gain = 1x	Output Referred				0.16		LSB
DNL	Differential Non-Linearity					±1		LSB
INL	Integral Non-Linearity					±2.2		LSB

LM98640QML-SP Electrical Characteristics[1][2] (continued)

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP[3]	MAX	UNIT
PGA SPECIFICATIONS								
	Gain Resolution			1, 2, 3			8	Bits
	Monotonicity		See[5]					
	Maximum Gain	CDS Gain = 1x		1, 2, 3	7.92	8.3	8.78	V/V
		CDS Gain = 1x		1, 2, 3	17.99	18.4	18.88	dB
	Minimum Gain	CDS Gain = 1x		1, 2, 3	0.62	0.64	0.66	V/V
		CDS Gain = 1x		1, 2, 3	–4.15	–3.8	–3.54	dB
	PGA Function	Gain (V/V) = (180/(277-PGA Code))						
		Gain (dB) = 20LOG10(180/(277-PGA Code))						
	Channel Matching	Minimum PGA Gain		1, 2	95.2%	99.0%		
				3	94.0%	99.0%		
		Maximum PGA Gain		1, 2	95.2%	99.0%		
				3	94.0%	99.0%		
ADC SPECIFICATIONS								
V_{REFT}	Top of Reference					2.0		V
V_{REFB}	Bottom of Reference					1.0		V
V_{REFT} - V_{REFB}	Differential Reference Voltage					1.0		V
	Overrange Output Code			1, 2, 3	16383	16383		Code
	Underrange Output Code			1, 2, 3		0	0	Code
FULL CHANNEL PERFORMANCE SPECIFICATIONS								
DNL	Differential Non-Linearity	5 MHz		1, 2, 3	–1.03	0.78	1.53	LSB
		5 MHz CDS		1, 2, 3	–1.20	1.0	2.24	
		15 MHz				0.78		
		25 MHz				0.78		
		40 MHz		1, 2, 3	–1.03	0.78	1.45	
INL	Integral Non-Linearity	5 MHz		1, 2, 3	–5.38	1.7	4.38	LSB
		5 MHz CDS		1, 2, 3	–3.41	1.7	5.15	
		15 MHz				1.9		
		25 MHz				2.4		
		40 MHz		1, 2, 3	–9.9	6.0	7.34	

LM98640QML-SP Electrical Characteristics[1][2] (continued)

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP[3]	MAX	UNIT
Noise	Noise Floor CDS Gain = 1x PGA Gain = FE	5 MHz		1, 2		–66.0	–64.6	dB
				3		–65.0	–62.5	
		15 MHz				–66.0		dB
						–66.0		
		25 MHz				–66.0		dB
						–65.0		
		40 MHz		1, 2		–66.0	–64.6	dB
				3		–66.5	–65.7	
	Noise Floor CDS Gain = 1x PGA Gain = FE	5 MHz		1, 2		8.20	9.6	LSB
				3		9.15	11.9	
		15 MHz				8.20		LSB
						8.20		
		25 MHz				8.20		LSB
						9.15		
		40 MHz		1, 2		8.20	9.45	LSB
				3		7.70	8.5	
	Noise Floor CDS Gain = 1x PGA Gain = 61	5 MHz		1, 2, 3		–79	–78	dB
		15 MHz				–79		dB
		25 MHz				–79		dB
		40MHz		1, 2, 3		–79	–78	dB
	Noise Floor CDS Gain = 1x PGA Gain = 61	5 MHz		1, 2, 3		1.8	2.05	LSB
		15 MHz				1.8		LSB
		25 MHz				1.8		LSB
		40 MHz		1, 2, 3		1.8	2.05	LSB
	Channel to Channel Crosstalk	5 MHz		4, 5, 6		–79	–77	dB
		15 MHz				–86		
		25 MHz				–79		
		40 MHz		4, 5, 6		–76	–74	
BMD	CDS Mode Bimodal Offset CDS Gain = 1x PGA Gain = 8x	5 MHz		1, 2, 3		2.2	6.0	mV
		15 MHz				2.1		
		25 MHz				2.2		
		40 MHz		1, 2, 3		2.3	6.0	
	CDS Mode Bimodal Offset CDS Gain = 1x PGA Gain = 1x	5 MHz		1, 2, 3		0.35	1	mV
		15 MHz				0.29		
		25 MHz				0.33		
		40 MHz		1, 2, 3		0.4	1.05	
SNR	Signal-to-Noise Ratio	5 MHz		4, 5	66.0	67.4		dB
				6	63.0	64.2		
		15 MHz				68.0		dB
						64.2		
		25 MHz				68.5		dB
						64.2		
		40 MHz		4, 5	66.5	68.5		dB
				6	62.0	64.0		

LM98640QML-SP Electrical Characteristics[1][2] (continued)

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP[3]	MAX	UNIT
THD	Total Harmonic Distortion	5 MHz		4, 5		–71.4	–69.0	dB
				6		–69.9	–67.8	
		15 MHz				–75.1		dB
						–73.9		
		25 MHz				–68.9		dB
						–68.2		
		40 MHz		4, 5		–62.0	–60.0	dB
				6		–62.0	–60.0	
SFDR	Spurious-Free Dynamic Range	5 MHz		4, 5	69.4	71.5		dB
				6	68.4	70.4		
		15 MHz				76.0		dB
						76.0		
		25 MHz				69.0		dB
						69.0		
		40 MHz		4, 5	60.0	62.0		dB
				6	60.0	62.0		
SINAD	Signal-to-Noise Plus Distortion Ratio	5 MHz		4, 5	65.0	67.0		dB
				6	62.0	64.5		
		15 MHz				68.0		dB
						64.5		
		25 MHz				66.0		dB
						64.5		
		40 MHz		4, 5	59.0	61.0		dB
				6	59.0	60.5		
ENOB	Effective Number of Bits	5 MHz		4, 5	10.5	10.8		Bits
				6	10.0	10.4		
		15 MHz				11.0		Bits
						10.4		
		25 MHz				10.7		Bits
						10.5		
		40 MHz		4, 5	9.5	9.8		Bits
				6	9.5	9.8		

6.7 AC Timing Specifications

The following specifications apply for VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 15 MHz unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP(1)	MAX	UNIT
INPUT CLOCK TIMING SPECIFICATIONS								
f_{INCLK}	Input clock frequency	INCLK = ADCCLK (ADC Rate Clock)		9, 10, 11	5		40	MHz
T_{dc}	Input clock duty cycle			9, 10, 11	40/60%	50/50%	60/40%	
t_{LAT}	Pipeline latency		See(2)				10	T_{ADC}
LVDS OUTPUT TIMING SPECIFICATIONS								
t_{DOD}	Data output delay	f_{INCLK} = 40 MHz INCLK = ADCCLK (ADC Rate Clock) LVDS Output Specifications not tested in production. Min/Max ensured by design, characterization and statistical analysis.		9, 10, 11		6.44	7.50	ns
t_{DSO}	Dual lane mode Odd data setup			9, 10, 11	0.45	0.69		ns
t_{DSE}	Dual lane mode Even data setup			9, 10, 11	0.45	0.89		ns
t_{QSR}	Quad lane mode Data to rising clock setup			9, 10, 11	0.45	0.63		ns
t_{QHF}	Quad lane mode Falling clock to data hold			9, 10, 11	0,45	0.53		ns
SERIAL INTERFACE TIMING SPECIFICATIONS								
f_{SCLK}	Input clock frequency	f_{SCLK} <= f_{INCLK} INCLK = ADCCLK (ADC Rate Clock)		9, 10, 11	1		20	MHz
	SCLK duty cycle			9, 10, 11	40/60	50/50	60/40	ns
t_{IH}	Input hold time			9, 10, 11	2.5	1		ns
t_{IS}	Input setup time			9, 10, 11	2.5	1		ns
t_{SENSC}	SCLK start time after $\overline{SEN}$ low			9, 10, 11	1.5	1		ns
t_{SCSEN}	$\overline{SEN}$ high after last SCLK rising edge			9, 10, 11	2.5	2		ns
t_{SENW}	$\overline{SEN}$ pulse width			9, 10, 11	8	6		ns
t_{OD}	Output delay time			9, 10, 11		10.54	11.6	ns
t_{HZ}	Data output to high Z			9, 10, 11		1.2	1.23	T_{SCLK}

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(2) This parameter is ensured by design and/or characterization and is not tested.

6.8 Typical Performance Characteristics

T_A = 25°C, F_S = 15 MHz, PGA Gain = 1x, CDS Gain = 1x, Dual Lane Output Mode, F_{IN} = 7.48 MHz unless otherwise stated.

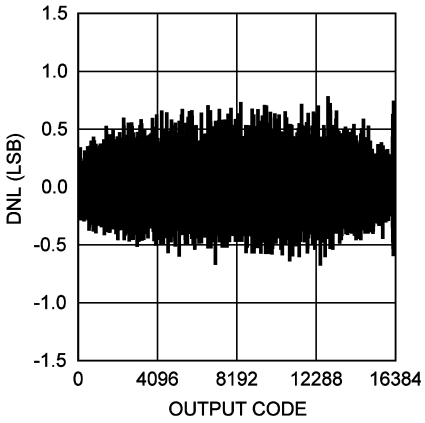


Figure 1. DNL vs Output Code

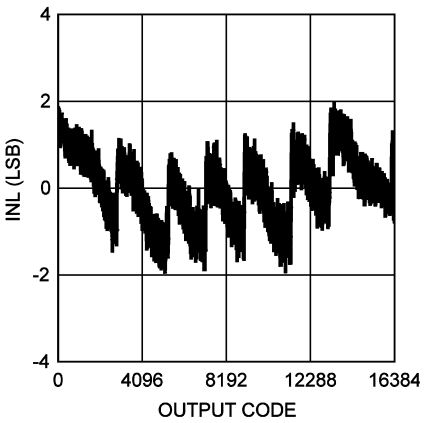


Figure 2. INL vs Output Code

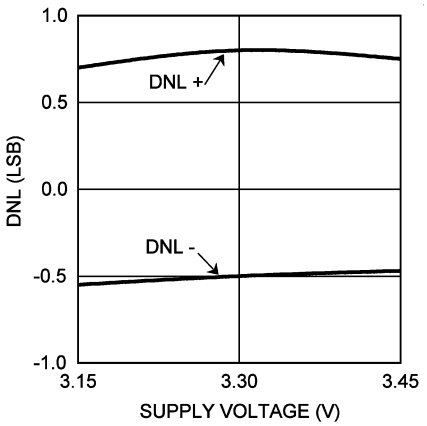


Figure 3. DNL vs Voltage

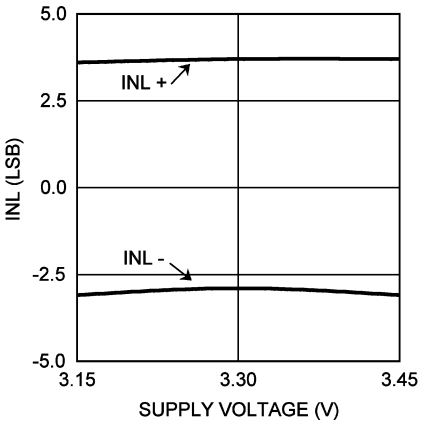


Figure 4. INL vs Voltage

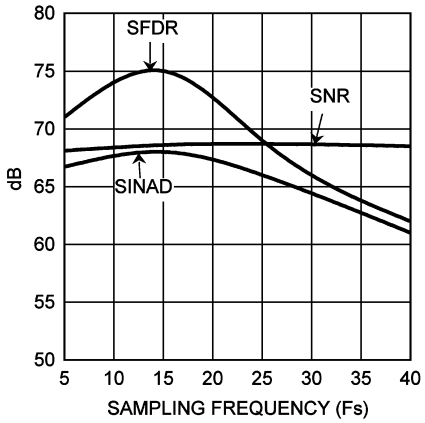


Figure 5. SNR, SFDR and SINAD vs F_S

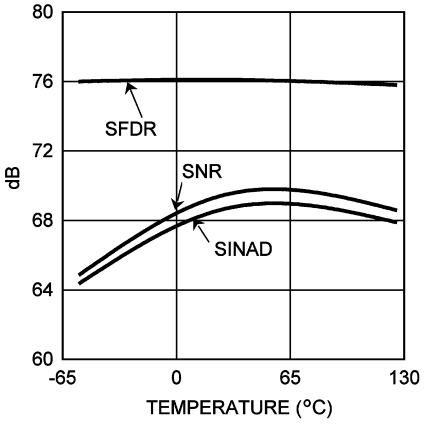


Figure 6. SNR, SFDR and SINAD vs Temperature

Typical Performance Characteristics (continued)

T_A = 25°C, F_S = 15 MHz, PGA Gain = 1x, CDS Gain = 1x, Dual Lane Output Mode, F_{IN} = 7.48 MHz unless otherwise stated.

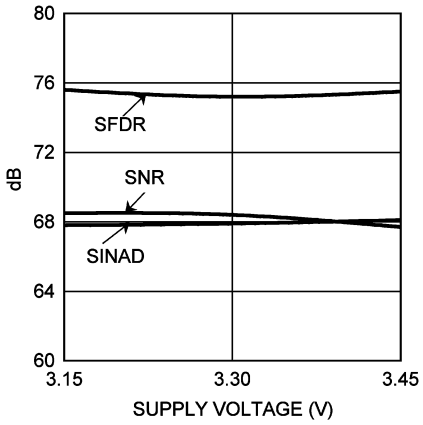


Figure 7. SNR, SFDR and SINAD vs Voltage

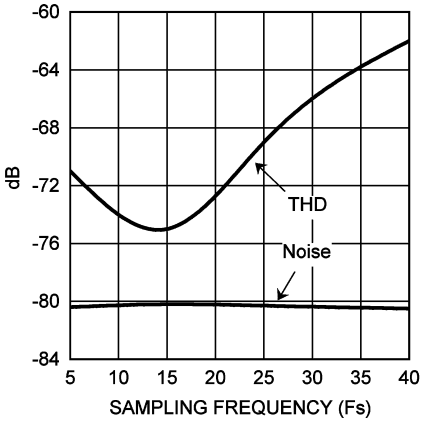


Figure 8. THD and Noise vs F_S

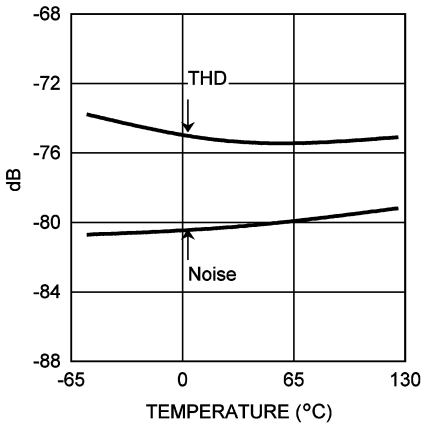


Figure 9. THD and Noise vs Temperature

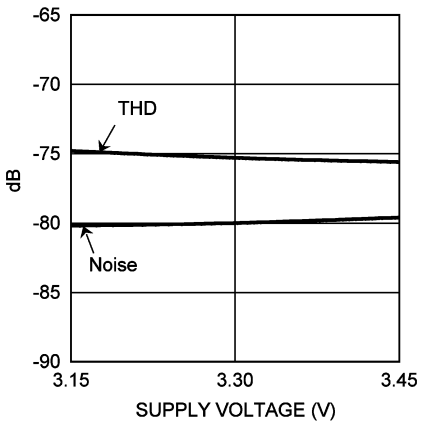


Figure 10. THD and Noise vs Voltage

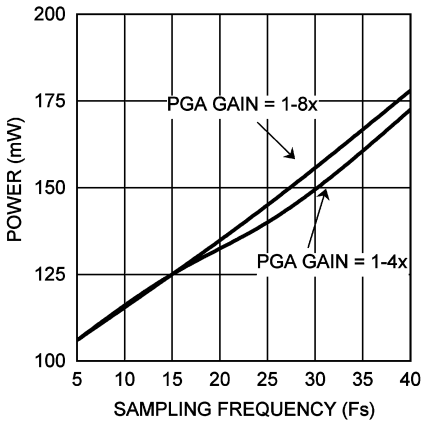


Figure 11. Power vs F_S

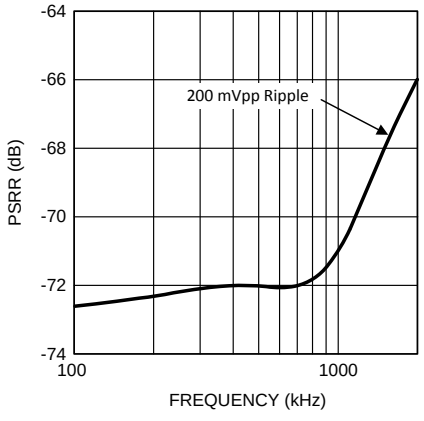


Figure 12. Dynamic PSRR vs Power Supply Frequency

7 Detailed Description

7.1 Overview

The LM98640QML-SP is a 14-bit, 5-MSPS to 40-MSPS, dual channel, complete Analog Front End (AFE) for digital imaging applications. The system block diagram of the LM98640QML-SP, shown in Figure 29 highlights the main features of the device. Each input has its own Input Bias and Clamping Network and Correlated Double Sample (CDS) amplifier (which can also be configure to operate in Sample/Hold Mode). Two ±8-Bit Offset DACs apply independent coarse and fine offset correction for each channel. A –3 to 18-dB Programmable Gain Amplifier (PGA) applies independent gain correction for each channel. The signals are digitized using two independent on chip high performance 14-bit, 40-MHz analog-to-digital converters. The data is finally output using a unique Serial LVDS output format that is tolerant to upsets preventing data loss.

7.2 Functional Block Diagram

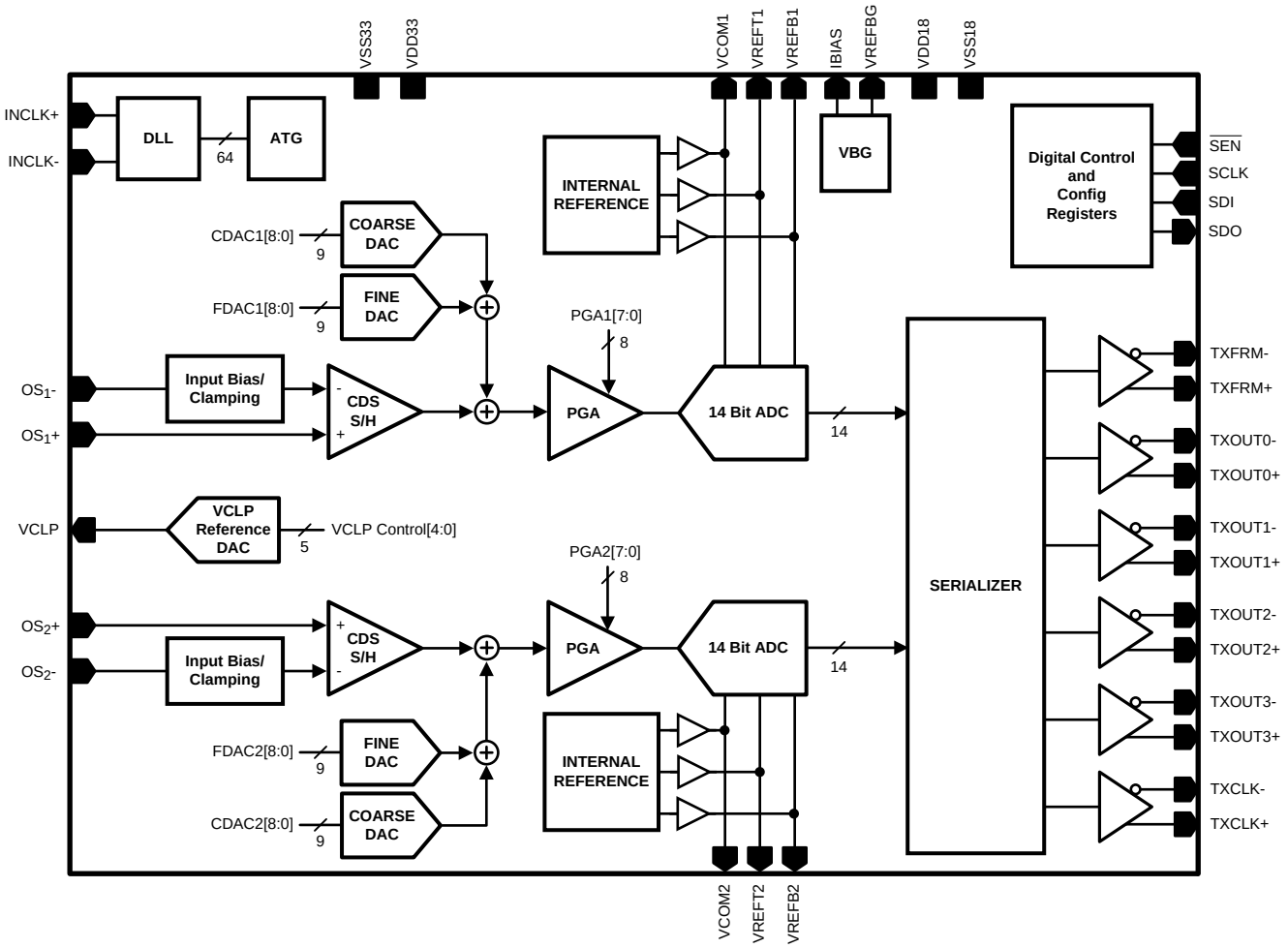


Figure 13. Chip Block Diagram

Functional Block Diagram (continued)

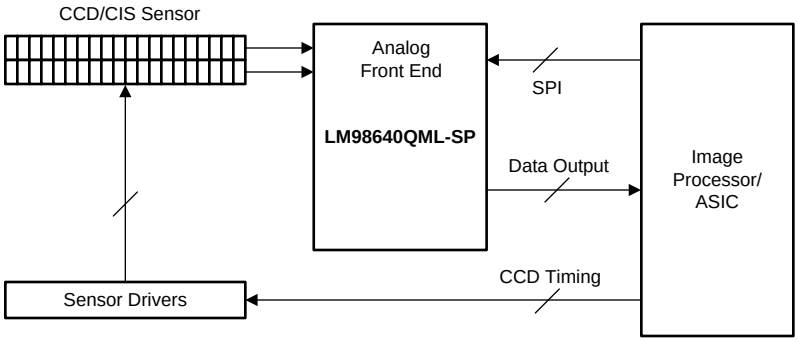


Figure 14. Typical CCD System

7.3 Feature Description

7.3.1 Input Sampling Modes

The LM98640QML-SP provides two input sampling modes, Sample & Hold mode and Correlated Double Sample (CDS) mode. The following sections describe these two input sampling modes.

7.3.1.1 Sample & Hold Mode

In Sample/Hold mode, a Video Level signal and a Reference Level signal need to be presented to the LM98640QML-SP. The Reference Level signal must be connected to the OS_X+ pin, and the Video Level signal connected to the OS_X- pin. The output code will then be OS_X+ minus OS_X-, or the difference between the Reference Level and Video Level. A minimum code represents zero deviation between the Reference and Video Levels and a maximum code represents a 2-V deviation between the Reference and Video Levels with CDS and PGA gains of 1x.

The Reference Level signal can be either an external signal from the image sensor, or the VCLP pin can be externally connected to the OS_X+ pin. In order to fully utilize the range of the input circuitry it is desirable to cause the Black Level signal voltage to be as close to the Reference Level voltage as possible, resulting in a near zero scale output for Black Level pixels. The LM98640QML-SP provides several methods for ensuring the Black Level signal and Reference Level are matched, these are described in the *Input Bias and Clamping* section.

To place the LM98640QML-SP in Sample & Hold Mode from power up, first write the baseline configuration to the registers as shown in Table 5. This configuration has Sample & Hold mode enabled by default. Next, the SAMPLE pulse must be properly positioned over the input signal using the CLAMP/SAMPLE Adjust.

7.3.1.1.1 Sample & Hold Mode CLAMP/SAMPLE Adjust

For accurate sampling of the input signals the LM98640QML-SP allows for full adjustment of the internal SAMPLE pulse to align it to the proper positions over the input signal. In Sample & Hold mode the SAMPLE pulse should be placed over the pixel output period of the image sensor. Only the Sample Start and Sample End Registers (0x22,0x23) need to be configured, the Clamp Start and Clamp End Registers (0x20,0x21) are not valid in Sample & Hold Mode. Internally the input clock is divided into 64 edges per clock period, the Sample Start and Sample End Registers correspond to the internal edge number the SAMPLE pulse will start and end. To adjust the SAMPLE pulse, first send the CLAMP and SAMPLE signals to the DTM pins by writing **10** to bits[4:3] of the Clock Monitor Register (0x09). This will allow the user to observe the SAMPLE pulse on pin DTM1 along with the image sensor output using an oscilloscope. Then, using the Sample Start and End Registers, adjust the SAMPLE pulse to align it over the Video Level portion of the image sensor output. To allow for settling and to reduce noise, the SAMPLE pulse should be made as wide as possible and fill the entire Video Level portion of the input signal.

Feature Description (continued)

Figure 15 shows some examples of an input waveform and where the SAMPLE pulse should be placed. Ideally the image sensor output would line up directly with the input clock at the AFE inputs, but due to trace delays in the system the image sensor output is delayed relative to the input clock. In the delayed image sensor waveform the Sample Start value is higher than the Sample End value. In this situation the SAMPLE pulse will start in one clock period and wraps around to the next. This allows the LM98640QML-SP to adjust for the delay in the image sensor waveform. Notice that edge zero of the internal clock does not line up with the rising edge of the input clock. This is due to internal delays of the clock signals. The amount of delay can be calculated from operating frequency using the following formula: t_{DCLK} = 6.0 ns + 3 / 64 × T_{INCLK}

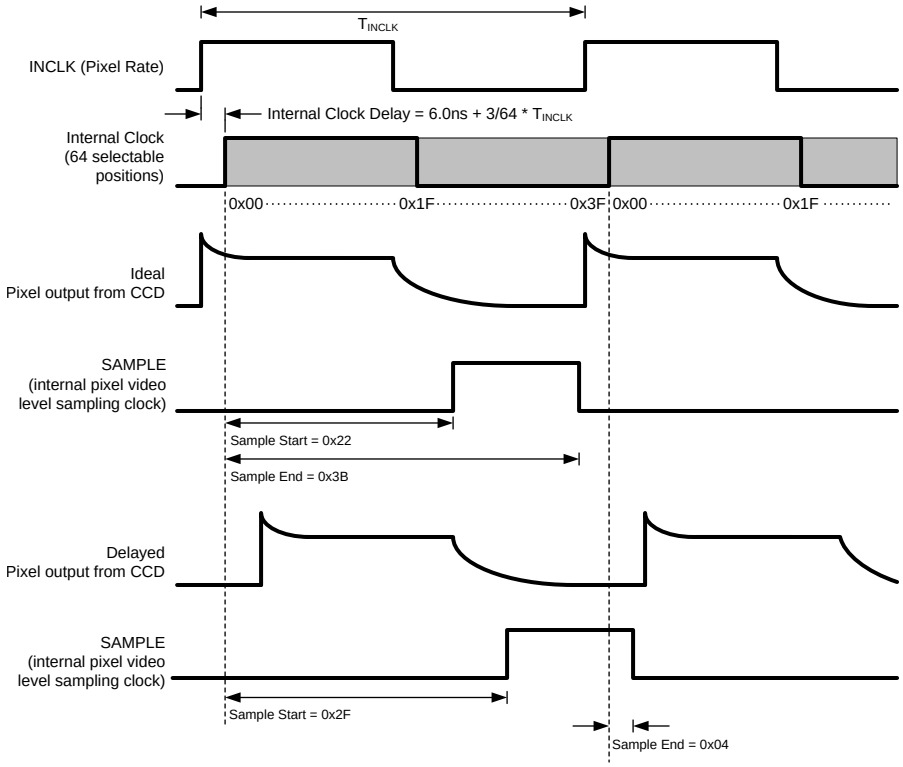


Figure 15. S/H Mode CLAMP/SAMPLE Adjust

7.3.1.2 CDS Mode

In CDS mode, both the Reference Level and Video Level are presented to the LM98640QML-SP on the OS_X– pin. The OS_X+ pin should be bypassed to ground with a 0.1-µF capacitor. The CLAMP pulse is then used to sample the Reference Level and the SAMPLE pulse is used to sample the Video Level. The output code will then be the Reference Level minus the Video Level, or the difference between the Reference Level and Video Level. A minimum code represents zero deviation between the Reference and Video Levels and a maximum code represents a 2-V deviation between the Reference and Video Levels with CDS and PGA gains of 1x.

To place the LM98640QML-SP in CDS Mode from power up, first write the baseline configuration to the registers as shown in Table 5. Then ensure S/H mode is disabled by clearing bit[7] of the Sample & Hold Register (0x06), then enable CDS mode by setting bit[0] of the Main Configuration Register (0x00). Next the CLAMP and SAMPLE pulses need to be positioned correctly over the reference and video levels respectively using the CLAMP/SAMPLE Adjust.

7.3.1.2.1 CDS Mode Bimodal Offset

In CDS mode, the input sampling amplifier has two physical paths through which a particular pixel will be sampled. These two sampling paths are a requirement in the Correlated Double Sampling architecture. The sampling of the one pixel will travel the first path (arbitrarily called an even pixel), and the sampling of the next pixel will travel the second path (called an odd pixel). The sampling will continue in an even/odd/even/odd fashion for all pixels processed in a particular channel. Due to slight variances in the sampling paths (most

Feature Description (continued)

commonly a difference in switched capacitor matching), the processing of identical pixels through the two different paths may result in a small offset in ADC output data between the two paths. To correct this, a simple digital offset can be applied in post processing to either the even pixel data or the odd pixel data. To simplify this action, the LM98640QML-SP will indicate (with the TXFRM signal) whether the pixel traveled the even path or the odd path. For all "Odd" pixels, the TXFRM signal is high for three TXCLK periods. For "Even" pixels, the TXFRM signal is high for two TXCLK periods. In Sample and Hold Mode there is only one sampling path, therefore there is no need to indicate an even or odd pixel. As a result, the TXFRM signal is the same for every pixel in Sample and Hold mode (i.e. high for three TXCLK periods).

7.3.1.2.2 CDS Mode CLAMP/SAMPLE Adjust

In CDS mode, the LM98640QML-SP utilizes two input networks, alternating between them every pixel, to increase throughput speeds. Because of this, there are two sets of CLAMP and SAMPLE windows defined in Table 8, one for even pixels and one for odd. Sample Start and Sample End Registers (0x22,0x23) along with the Clamp Start and Clamp End Registers (0x20,0x21) control both the even and odd CLAMP and SAMPLE pulses. To adjust the CLAMP and SAMPLE pulses, first send the $CLAMP_{ODD}$ and $SAMPLE_{ODD}$ signals to the DTM pins by writing **10** to bits[4:3] of the Clock Monitor Register (0x09). This will allow the user to observe the $CLAMP_{ODD}$ and $SAMPLE_{ODD}$ pulses on pins DTM0 and DTM1 along with the image sensor output using an oscilloscope. The CLAMP and SAMPLE pulses will only be shown for every other pixel because of the even odd architecture, but the positions of the even CLAMP and SAMPLE pulses will be identically defined to that of the odd CLAMP and SAMPLE; however, odd and even path mismatch could result in a slightly different position of the pulses. Then, using the Clamp Start/End and Sample Start/End registers, adjust the positions of the CLAMP and SAMPLE pulses to align them over the Reference and Video Levels of the input signal. To allow for settling and to reduce noise, the CLAMP and SAMPLE pulses should be made as wide as possible and placed near the far edge of their respective input levels.

The following figure shows some examples of input CCD waveforms and placement of the CLAMP and SAMPLE positions for each. Ideally the CCD output would line up directly with the input clock at the AFE inputs, but due to trace delays in the system the CCD output is delayed relative to the input clock. In the Delayed CCD waveform the Sample Start/End Register values are lower than the Clamp Start/End Register Values. In this situation the sample pulse is not generated until the next clock period, which allows it to be correctly placed in the Video Level of the input signal. Notice that edge zero of the internal clock does not line up with the rising edge of the input clock. This is due to internal delays of the clock signals. The amount of delay can be calculated from operating frequency using the following formula: $t_{DCLK} = 6.0\ ns + 3 / 64 \times T_{INCLK}$

Feature Description (continued)

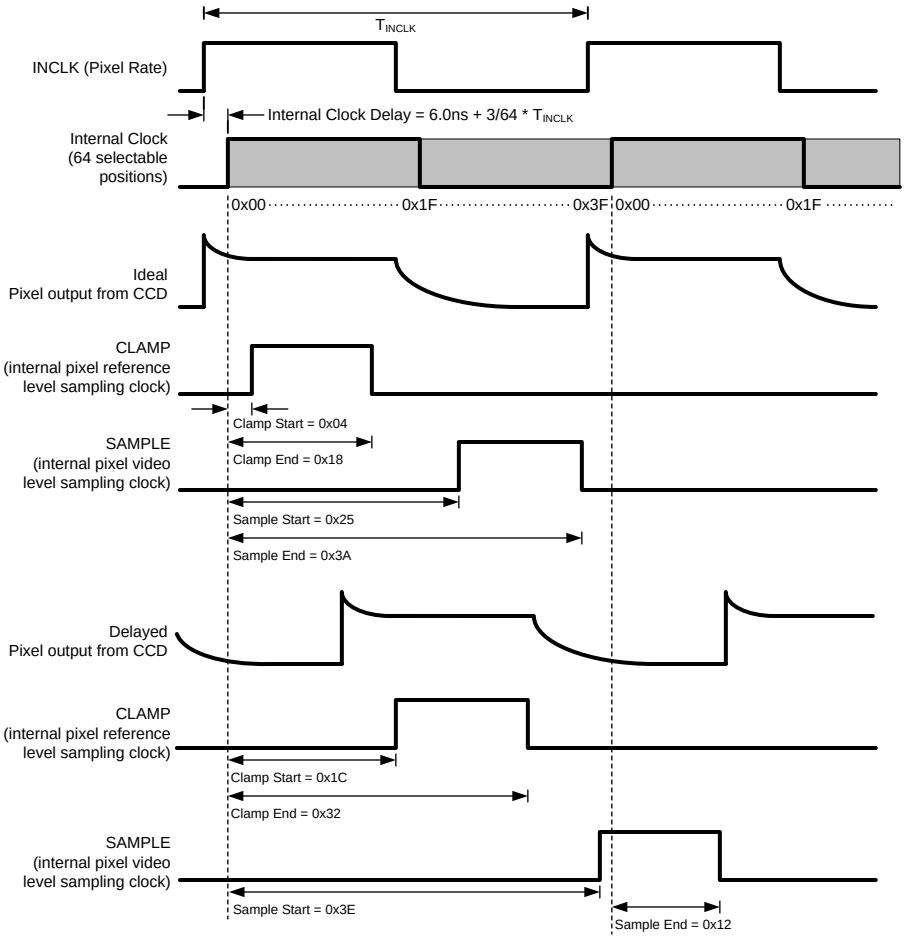


Figure 16. CDS Mode CLAMP/SAMPLE Adjust

7.3.2 Input Bias and Clamping

The inputs to the LM98640QML-SP are typically AC coupled in Correlated Double Sampling Mode (CDS Mode) because of the switching between two signals. In Sample and Hold Mode (S/H Mode), DC coupling or AC coupling is possible depending on the signal type. The circuit of Figure 17 shows the input structure of the LM98640QML-SP. The DC bias point for the LM98640QML-SP side of the AC coupling capacitor can to be set using an external DC bias resistor network, by using the CLPIN configuration, or by using the BITCLP configuration. A typical CCD waveform is shown in Figure 18. Also shown in Figure 18 is an internal signal “CLAMP” which can be used to “gate” the CLPIN signal so that it only occurs during the “pedestal” portion of the CCD pixel waveform.

Feature Description (continued)

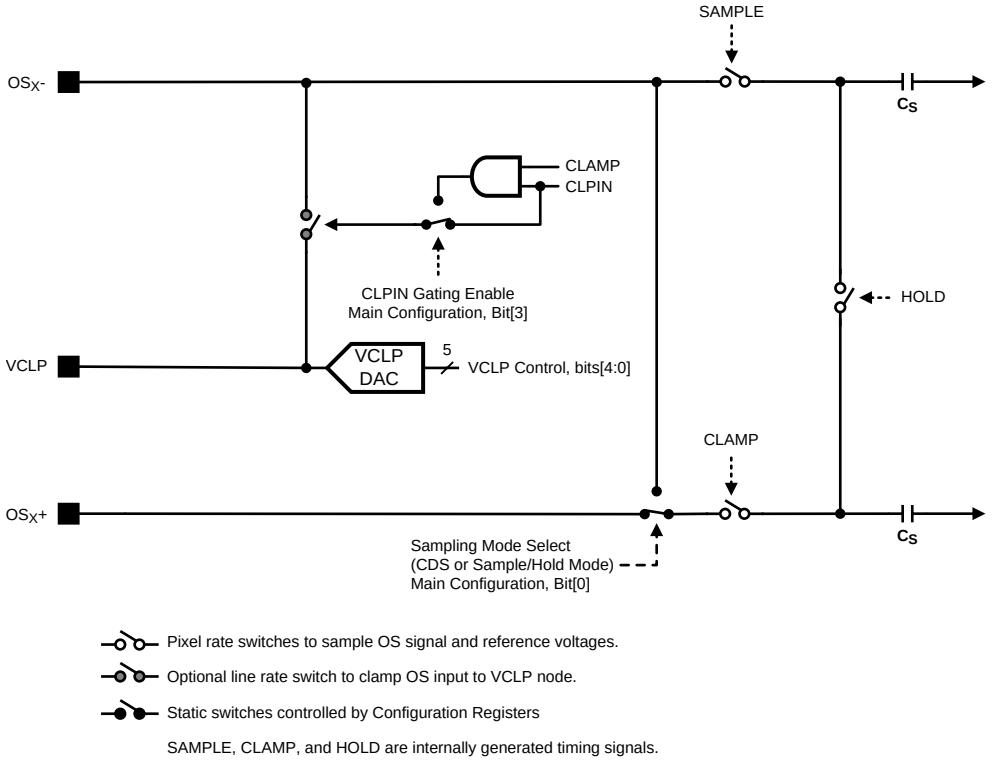


Figure 17. Input Structure Diagram

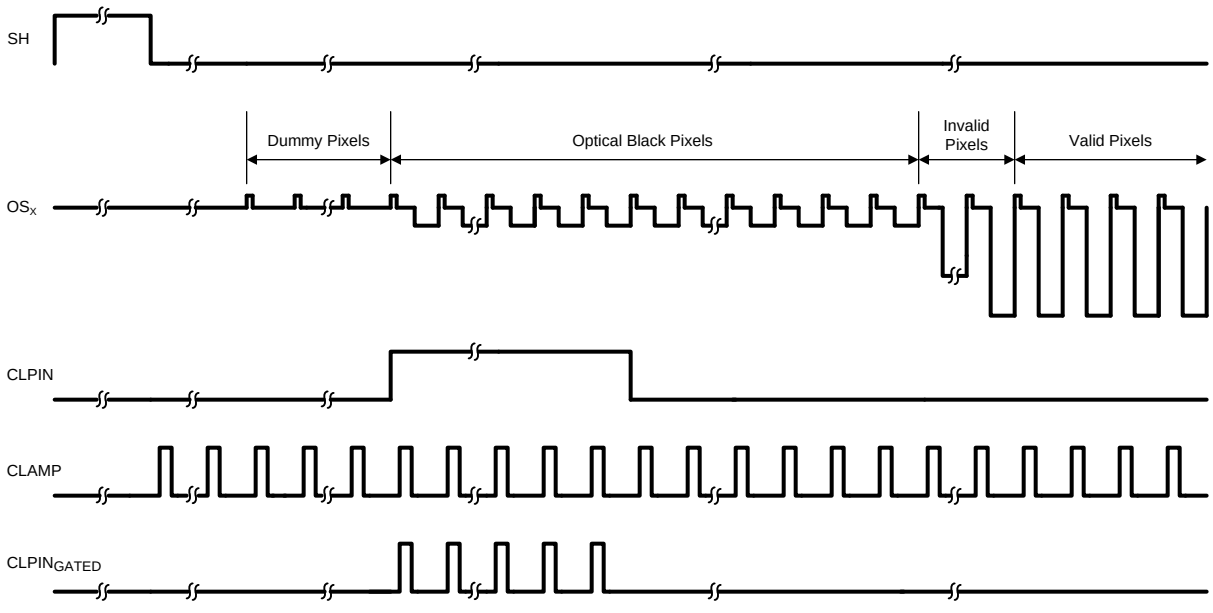


Figure 18. Typical CCD Waveform and LM98640QML-SP Input Clamp Signal (CLPIN)

Feature Description (continued)

7.3.2.1 Sample and Hold Mode Biasing

Proper DC biasing of the CCD waveform in Sample and Hold mode is critical for realizing optimal operating conditions. In Sample/Hold Mode, the DC bias point of the input pin is typically set by actuating the input clamp switch (see Figure 17) during optical black pixels which connects the input pins to the VCLP pin DC voltage. The signal controlling this switch is CLPIN. CLPIN is an external signal connected on the CLPIN pin.

Actuating the input clamp will force the average value of the CCD waveform to be centered around the VCLP DC voltage. During Optical Black Pixels, the CCD output has roughly three components. The first component of the pixel is a “Reset Noise” peak followed by the Reset (or Pedestal) Level voltage, then finally the Black Level voltage signal. Taking the average of these signal components will result in a final “clamped” DC bias point that is close to the Black Level signal voltage.

To provide a more precise DC bias point (i.e. a voltage closer to the Black Level voltage), the CLPIN pulse can be “gated” by the internally generated CLAMP clock. This resulting $CLPIN_{GATED}$ signal is the logical “AND” of the CLAMP and CLPIN signals as shown in Figure 18. By using the $CLPIN_{GATED}$ signal, the higher Reset Noise peak will not be included in the clamping period and only the Pedestal Level components of the CCD waveform will be centered around VCLP.

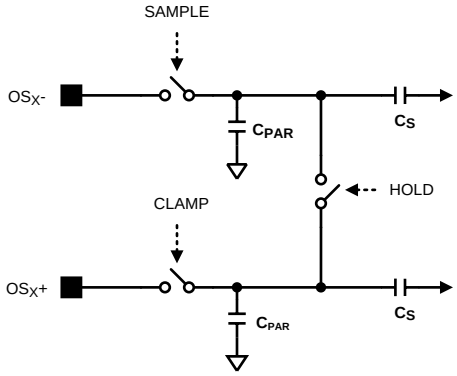


Figure 19. Sample and Hold Mode Simplified Input Diagram

In Sample and Hold Mode, the impedance of the analog input pins is dominated by the switched capacitance of the CDS/Sample and Hold amplifier. The amplifier switched capacitance, shown as C_S in Figure 19, and internal parasitic capacitances can be estimated by a single capacitor switched between the analog input and the VCLP reference pin for Sample and Hold mode. During each pixel cycle, the modeled capacitor, C_{SH}, is charged to the OS_X+ minus OS_X– voltage then discharged. The average input current at the OS_X– pin can be calculated knowing the input signal amplitude and the frequency of the pixel.

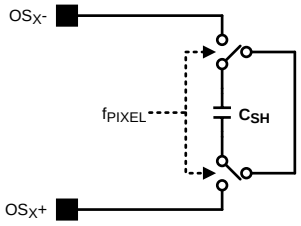


Figure 20. Equivalent Input Switched Capacitance S/H Mode

Feature Description (continued)

7.3.2.2 CDS Mode Biasing

Correlated Double Sampling mode does not require as precise a DC bias point as does Sample and Hold mode. This is due mainly to the nature of CDS itself, that is, the Video Signal voltage is referenced to the Reset Level voltage instead of the static DC VCLP voltage. The common mode voltage of these two points on the CCD waveform have little bearing on the resulting differential result. However, the DC bias point does need to be established to ensure the CCD waveform's common mode voltage is within rated operating ranges.

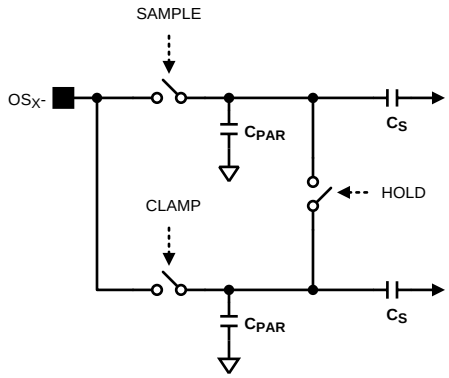


Figure 21. CDS Mode Simplified Input Diagram

The CDS mode biasing can be performed in the same way as described in the *Sample and Hold Mode Biasing* section, or, an external resistor divider can be placed across the OS_X– input to provide the DC bias voltage. In CDS Mode the OS_X+ pins should each be decoupled with 0.1-µF capacitors to ground.

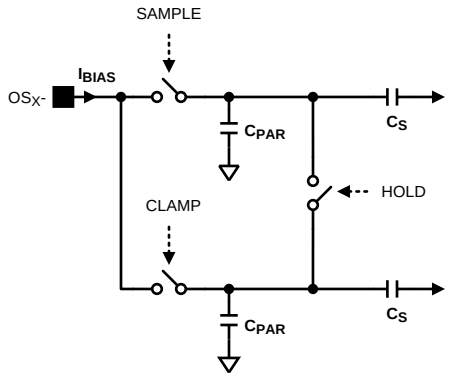


Figure 22. CDS Mode Input Bias Current

Unlike in Sample and Hold Mode, the input bias current in CDS Mode is relatively small. Due to the architecture of CDS switching, the average charge loss or gain on the input node is ideally zero over the duration of a pixel. This results in a much lower input bias current, whose main source is parasitic impedances and leakage currents. As a result of the lower input bias current in CDS Mode, maintaining the DC Bias point the input node over the length of a line will require a much smaller AC input coupling capacitor.

Feature Description (continued)

7.3.2.3 VCLP DAC

The VCLP pin can be used to provide the reference level for incoming signals in Sample and Hold Mode. The pin is driven by the VCLP DAC, the VCLP DAC has five bits and has an approximate range of 2.9 V. The VCLP DAC is controlled by the VCLP Control Register (0×04), and programmable through the serial interface.

7.3.3 Programmable Gain

The LM98640QML-SP provides two independent gain stages. The first stage is in the input CDS/SH circuit. The second is in the form of a Programmable Gain Amplifier (PGA).

7.3.3.1 CDS/SH Stage Gain

The CDS/SH gain is programmable to either 0-dB or 6-dB gain. The load presented to the user in 6-dB mode is roughly twice the switched load of 0-dB mode. The CDS/SH gain settings affect both channels. The CDS/SH gain bit is located in bit 2 of the Main Configuration register, and programmable through the serial interface.

7.3.3.2 PGA Gain Plots

The PGA has an 8-bit resolution with a gain range of –3 dB to 18 dB. Figure 23 below shows a plot for the gain. Each channel has a independent PGA controlled by registers CH1 PGA and CH2 PGA, and programmable through the serial interface.

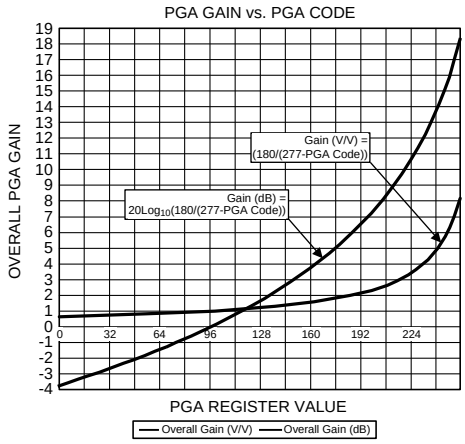


Figure 23. PGA Gain vs PGA Gain Code

Feature Description (continued)

7.3.4 Programmable Analog Offset Correction

The LM98640QML-SP provides two analog DACs per channel to provide flexibility in offset control. Each channel has a Coarse DAC and Fine DAC which have ±8-bit resolutions (8 bit + Sign). The two DACs can be used independently or as Coarse/Fine configuration. The Coarse DAC provides a sufficient range with moderate step sizes, while the Fine DAC is for designs which need a finely tuned offset. The correction voltage is applied to the "Video" level for both Sample & Hold and CDS input modes. Because of the DACs location in the signal path, the correction range lowers as CDS gain increases, and the output referred correction steps and ranges increase with PGA gain. Table 1 provides the range and step size of each DAC.

Table 1. Analog Offset DAC Specifications

	CDS/SH GAIN	RANGE(1)	STEP SIZE(1)	OUTPUT ADC CODES
Coarse DAC	1x	±250 mV	1 mV	±2048
	2x	±125 mV	500 µV	±2048
Fine DAC	1x	±5 mV	20 µV	±41
	2x	±2.5 mV	10 µV	±41

(1) Referred to Input

To use the Offset Correction DACs, the Coarse DAC and Fine DAC must be enabled using bits[6:5] of the Main Configuration Register (0x00). Then the desired correction value should be entered into the CDAC or FDAC register of the appropriate channel. The Offset Correction DACs use a signed binary format which is summarized in Table 2.

Table 2. Analog Offset Correction DAC Format

CDAC / FDAC INPUT VALUE	CDAC CORRECTION (CODES)	FDAC CORRECTION (CODES)
1 1111 1111	+2048	+41
1 0111 1111	+1024	+20
0 1111 1111	0	0
0 0111 1111	–1024	–20
0 0000 0000	–2048	–41

7.3.5 Analog to Digital Converter

The LM98640QML-SP has a 14-bit Analog to Digital Converts (ADC) for each channel. Each ADC has maximum and minimum conversion rate of 40 MSPS and 5 MSPS per channel respectively. The DNL performance is ±0.5 LSB and ±2 LSB for INL for a 14-bit out. The noise floor is –79 dB at 2 V with a programmable gain of 0 dB. If an out of range pixel is presented to the ADC, the ADC will return to full compliance within two cycles of the pixel clock.

7.3.6 LVDS Output

7.3.6.1 LVDS Output Voltage

The LM98640QML-SP output data is presented in LVDS format. Table 3 shows the available LVDS differential output voltage (VOD) settings and its associated offset voltage (VOS).

Table 3. LVDS Differential Output Voltage Settings

VOD	VOS
250 mV	1.2 V
300 mV	1.2 V
350 mV	1.1 V
400 mV	1.1 V

7.3.6.2 LVDS Output Modes

The LM98640QML-SP has a unique serial LVDS output format to protect data transfer during DLL upsets. The format provides a buffer on either side of the data word, this is accomplished by clocking a 14-bit word using a 16-bit clock rate. In the event of an upset that affects the DLL the output clock period could fluctuate; with no buffer for the data word this fluctuation could cause the loss of one or more of the data word bits, but because the LM98640QML-SP provides the buffer the fluctuation does not cause any data loss. The data can also be sent out in two modes: Dual or Quad Lane. The following sections describe these two modes.

7.3.6.3 TXFRM Output

The LM98640QML-SP output includes a frame signal (TXFRM) that should be used to locate the beginning and end of a particular pixel's serial data word. The rising edge of TXFRM is coincident with the pixel's leading bit transition (TXOUT MSB). This TXFRM rising edge can be detected by the capturing FPGA or ASIC to mark the start of the serial data word.

In CDS mode, the input sampling amplifier has two physical paths through which a particular pixel will be sampled. These two sampling paths are a requirement in the Correlated Double Sampling architecture. The sampling of the one pixel will travel the first path (arbitrarily called an even pixel), and the sampling of the next pixel will travel the second path (called an odd pixel). The sampling will continue in an even/odd/even/odd fashion for all pixels processed in a particular channel. Due to slight variances in the sampling paths (most commonly a difference in switched capacitor matching), the processing of identical pixels through the two different paths may result in a small offset in ADC output data between the two paths. To correct this, a simple digital offset can be applied in post processing to either the even pixel data or the odd pixel data. To simplify this action, the LM98640QML-SP will indicate (with the TXFRM signal) whether the pixel traveled the even path or the odd path. For all "Odd" pixels, the TXFRM signal is high for three TXCLK periods. For "Even" pixels, the TXFRM signal is high for two TXCLK periods. In Sample and Hold Mode there is only one sampling path, therefore there is no need to indicate an even or odd pixel. As a result, the TXFRM signal is the same for every pixel in Sample and Hold mode (i.e. high for three TXCLK periods).

7.3.6.3.1 Output Mode 1 - Dual Lane

In Dual Lane mode each input channel has its own data output presented at 16x the pixel clock rate. A frame signal (TXFRM) is output at the pixel clock rate with the rising edge occurring coincident with the transition of the MSB of the data. In Sample/Hold Modes of operation, the falling edge is coincident with the transition of bit 7 of the data. In CDS Mode, the falling edge of TXFRM toggles between the transition of bit 9 and bit 7 of the data. A differential clock is also output with transitions aligned with the center of the data eye. Data rates for Dual Lane mode range from 80 Mbps, with a 5-MHz clock, up to 640 Mbps, with a 40-MHz clock.

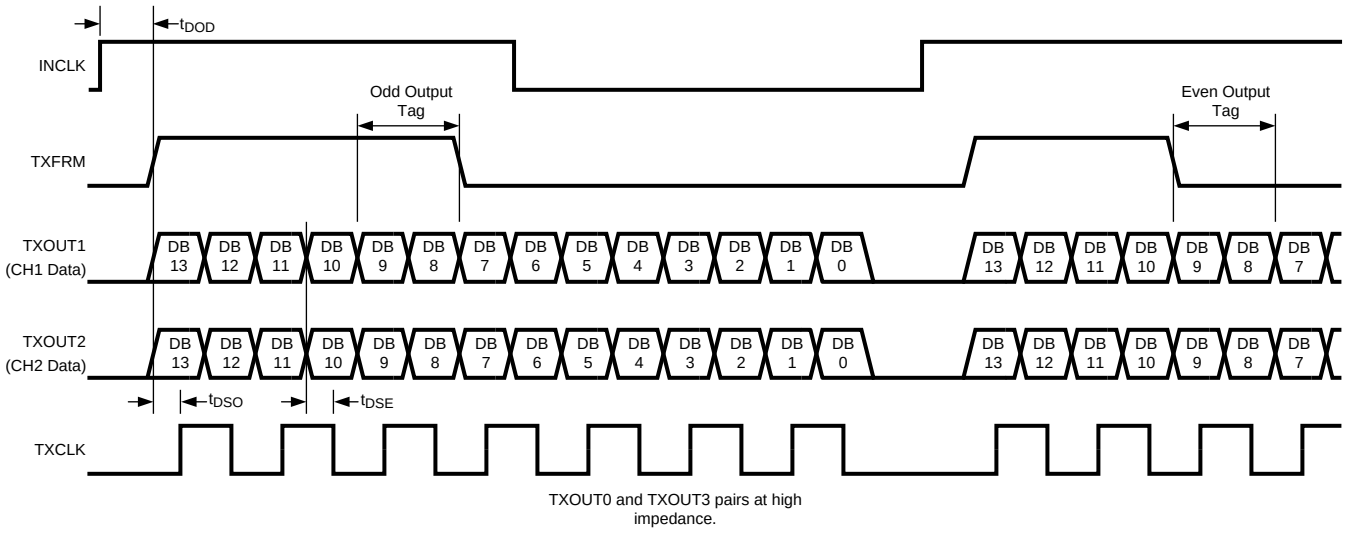


Figure 24. Dual Lane LVDS Output Timing Diagram

7.3.6.3.2 Output Mode 2 - Quad Lane

In Quad Lane mode each input channel is split into two data lanes which are presented at 8x the pixel rate. The MSBs (bits 13 through 7) will be presented to one channel while the LSBs (bits 6 through 0) will be presented to the other. A frame signal is run at the pixel clock rate with the rising edge coincident with the transition of the MSB of the data and the falling edge coincident with the transition of bits 10 and 3 of the data lanes for an odd output value, and coincident with the transition of bits 11 and 4 for a even output value. A differential clock is also output with rising edge transitions aligned within each data eye. Data rates for Quad Lane mode range from 40 Mbps, with a 5-MHz clock, up to 320 Mbps, with a 40-MHz clock.

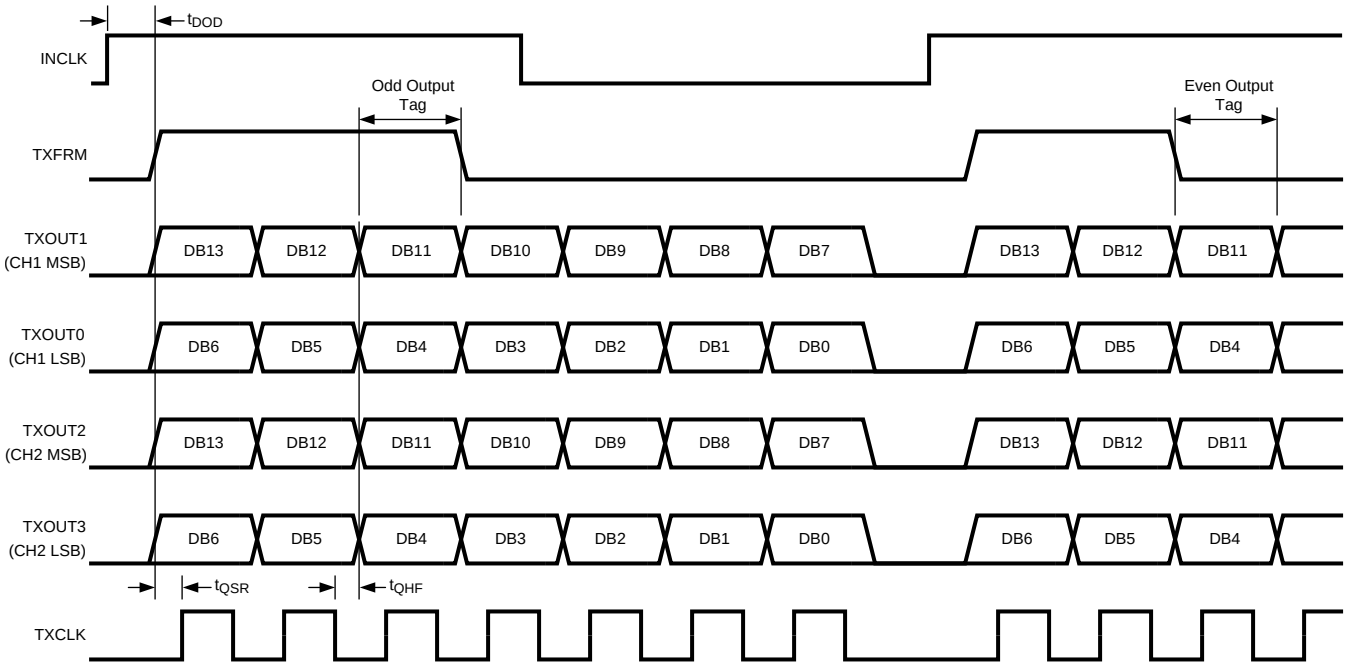


Figure 25. Quad Lane LVDS Data Output Timing Diagram

7.3.7 Clock Receiver

A differential clock receiver is used to generate all clock signals on the LM98640QML-SP. The clock input should be externally terminated with 100 Ω between the input clock pins. The clock may be DC or AC coupled to the AFE.

7.3.8 Power Trimming

The LM98640QML-SP provides an adaptive power scaling feature that allows the user to optimize power consumption based on the maximum operating frequency and the maximum amount of gain required. The power scaling mode is selectable through the PGA Power Trimming and ADC Power Trimming registers (0x02,0x03). The settings in these registers are common for both channels PGA and ADC. Using these registers the user can control the current of the two stages of the PGA, and the current for the two levels of the ADC. The following table provides a set of baseline configurations for various operating frequencies and gain ranges.

These configurations should be treated as baseline values and can be tuned to your specific application.

OPERATING FREQUENCY	1-4x MAX PGA GAIN	1-8x MAX PGA GAIN
5 - 15 MSPS	PGA Power Trimming = 0x00 ADC Power Trimming = 0x00	PGA Power Trimming = 0x01 ADC Power Trimming = 0x00
15 - 25 MSPS	PGA Power Trimming = 0x01 ADC Power Trimming = 0x00	PGA Power Trimming = 0x09 ADC Power Trimming = 0x00
25 - 40 MSPS	PGA Power Trimming = 0x01 ADC Power Trimming = 0x08	PGA Power Trimming = 0x09 ADC Power Trimming = 0x08

7.4 Device Functional Mode

7.4.1 Powerdown Modes

The LM98640QML-SP provides several ways to save power when the device is not in normal usage mode. Using the Powerdown Control Register (0x01) the part can be placed into Powerdown Mode, or Single Channel Mode. In Powerdown Mode (Powerdown Control, bit[7]) the following blocks are placed in a Powerdown mode: VCLP, Channel 1 and 2 Reference Buffers, Channel 1 and 2 PGA OpAmps, and Channel 1 and 2 Amplifiers. Powerdown Mode will override all other Powerdown Control Register bits. To place the part in Single Channel Mode each block of the unused channel can be powered down using their respective control bits (Powerdown Control, bits[5:0]). If an external reference clamp is used the VCLP block can be powered down during any Power mode. For applications operating at a low enough frequency additional power can be saved by powering down one channel reference buffer, then externally tie both channel's reference pins together.

7.4.2 LVDS Test Modes

The LVDS test modes present programmable data patterns to the input of the LVDS serializer block. The type of pattern is selectable through the Test Pattern Control register. Once the LVDS test mode is enabled the patterns are output indefinitely. Table 4 below shows the available test pattern modes.

Table 4. Test Pattern Modes

TEST PATTERN CONTROL[6:4]	TEST MODE
000	Fixed Code
001	Horizontal Gradient
010	Vertical Gradient
011	Lattice Pattern
100	Strip Pattern
101	LVDS Test Pattern (Synchronous)
110	LVDS Test Pattern (Asynchronous)
111	Reserved

Each pattern consists of a Start Period and Valid Pixel region. During the Start Period the output is the minimum code (0x0000). The Valid Pixel region contains the selected Test Pattern Mode output. The length (in pixels) of the Start period is set using the Test Pattern Start register, and the width of the Valid Pixel region is set using the Test Pattern Width register.

To start the test pattern generation, enable Test Mode using bit[1] of the Test and Scan Register (0x3D). Then load all parameters for the desired test pattern into the registers, and set Pattern Enable bit of the Test Pattern Control Register (0x34). Changing pattern parameters after the Pattern Enable bit is set may result in undesired output. The pattern will start at the next leading edge of CLPIN.

7.4.2.1 Test Mode 0 - Fixed Pattern

This test mode provides an LVDS output with a fixed value output during the valid pixel region. The fixed value is set via the Test Pattern Value registers. The Test Pattern Value register is split into two registers the upper 6 bits of the test code in first register, and the lower 8 bits of the test code in the second.

7.4.2.2 Test Mode 1 - Horizontal Gradient

This mode provides LVDS data that progresses horizontally from dark to light output values. This mode is highly variable, allowing control over the starting value of the gradient, the width of the gradient, and the increment rate of the gradient. The starting value can be set in the Test Pattern Value register, the width (in number of pixels) of each gradient step is set via Test Pattern Pitch register, and increment rate (in LSBs) is set via the Test Pattern Step register. When the LVDS Horizontal Gradient test pattern is selected, the ramp begins immediately and counts to the maximum value, and then repeats throughout the entire Valid Pixel region.

7.4.2.3 Test Mode 2 - Vertical Gradient

This mode is similar to the Horizontal Gradient, only the gradient is in the vertical direction. See the Horizontal Gradient mode description for details.

7.4.2.4 Test Mode 3 - Lattice Pattern

This mode provides LVDS data that creates a lattice grid. The lattice is made of dark lines on a light background. The line output value is set by Test Pattern Step register, and background value is set by Test Pattern Value register. The number of pixels & lines in the lattice is set via Test Pattern Pitch register.

7.4.2.5 Test Mode 4 - Stripe Pattern

This mode provides LVDS data that creates a vertical stripe pattern. The stripe pattern is made of dark and light lines. The output value of the dark portion is set via Test Pattern Step register, and the light portion is set via Test Pattern Value register. The stripe width in pixels is set via Test Pattern Pitch register.

7.4.2.6 Test Mode 5 - LVDS Test Pattern (Synchronous)

This mode provides an LVDS output with a fixed value repeated continuously. The pattern starts at the leading edge of CLPIN. The fixed value is set via the Test Pattern Value registers. The Test Pattern Value register is split into two registers the upper 8 bits of the test code in first register, and the lower 8 bits of the test code in the second. This is useful for system debugging of the LVDS link and receiver circuitry.

7.4.2.7 Test Mode 6 - LVDS Test Pattern (Asynchronous)

This mode provides an LVDS output with a fixed value repeated continuously. The pattern starts asynchronously without CLPIN. The fixed value is set via the Test Pattern Value registers. The Test Pattern Value register is split into two registers the upper 8 bits of the test code in first register, and the lower 8 bits of the test code in the second. This is useful for system debugging of the LVDS link and receiver circuitry.

7.4.2.8 Pseudo Random Number Mode

This mode provides LVDS data produced from the following polynomial:

$P(x) = X^{14} + X^{13} + X^{11} + X^{9} + 1$

To start the Pseudo Random Number mode, set the Test Mode bit of the Test and Scan Register. Then load the seed value in the Test Pattern Value register, and set the Pseudo Random Enable bit of the Test Pattern Control register. The pattern will start outputting after the next leading edge of CLPIN.

7.5 Programming

7.5.1 Serial Interface

A serial interface is used to write and read the configuration registers. The interface is a four wire interface using SCLK, $\overline{\text{SEN}}$, SDI, and SDO connections. The serial interface clock (SCLK) must be less than the main input clock (INCLK) for INCLK speeds of less than 20 MHz, for INCLK speeds greater than 20-MHz SCLK must remain below 20 MHz. The main input clock (INCLK) to the LM98640QML-SP must be active during all Serial Interface commands. The Serial Interface pins are high impedance while $\overline{\text{SEN}}$ is high, this allows multiple slave devices to be used with a single master device.

After power-up, all configuration registers must be written, using the serial interface, to place the part in a valid state.

Default registers must be written to the baseline values.

Be sure to set the INCLK Range (2x05) and Sample & Hold (0x06) registers for the sample rate being used.

Write the Clock Monitor (0x09) register after the Test & Scan Control (3x0D) register.

7.5.2 Writing to the Serial Registers

To write to the serial registers using the four wire interface, the timing diagram shown in Figure 26 must be met. First, SEN is toggled low. At the rising edge of the first clock, the master should assume control of the SDI pin and begin issuing the write command. The write command is built of a "write" bit (0), device address bit (0), six bit register address, and eight bit register value to be written. SDI is clocked into the LM98640QML-SP at the rising edge of SCLK. The LM98640QML-SP assumes control of the SDO pin during the first eight clocks of the cycle. During this period, data is clocked out of the device at the rising edge of SCLK. The eight bit value clocked out is the contents of the previously addressed register, regardless if the previous command was a read or a write. When SEN toggles high, the register is written to, and the LM98640QML-SP now functions with this new data.

7.5.3 Reading the Serial Registers

To read to the serial registers using the four wire interface, the timing diagram shown in Figure 27 must be met. Reading the registers takes two cycles. To start the first cycle, $\overline{\text{SEN}}$ is toggled low. At the rising edge of the first clock, the master should assume control of the SDI pin and begin issuing the read command. The read command is built of a "read" bit (1), device address bit (0), six bit register address, and eight "don't care" bits. SDI is clocked into the LM98640QML-SP at the rising edge of SCLK. $\overline{\text{SEN}}$ is toggled high for a delay of at least t_{SENW} (see Figure 28). The second cycle begins when $\overline{\text{SEN}}$ is toggled low. The LM98640QML-SP assumes control of the SDO pin during the first eight clocks of the cycle. During this period, data is clocked out of the device at the rising edge of SCLK. The eight bit value clocked out is the contents of the previously addressed register. The next command can be sent on the SDI pin simultaneously during this second cycle. When $\overline{\text{SEN}}$ toggles high, the register is not written to, but its contents are staged to be outputted at the beginning of the next command.

Programming (continued)

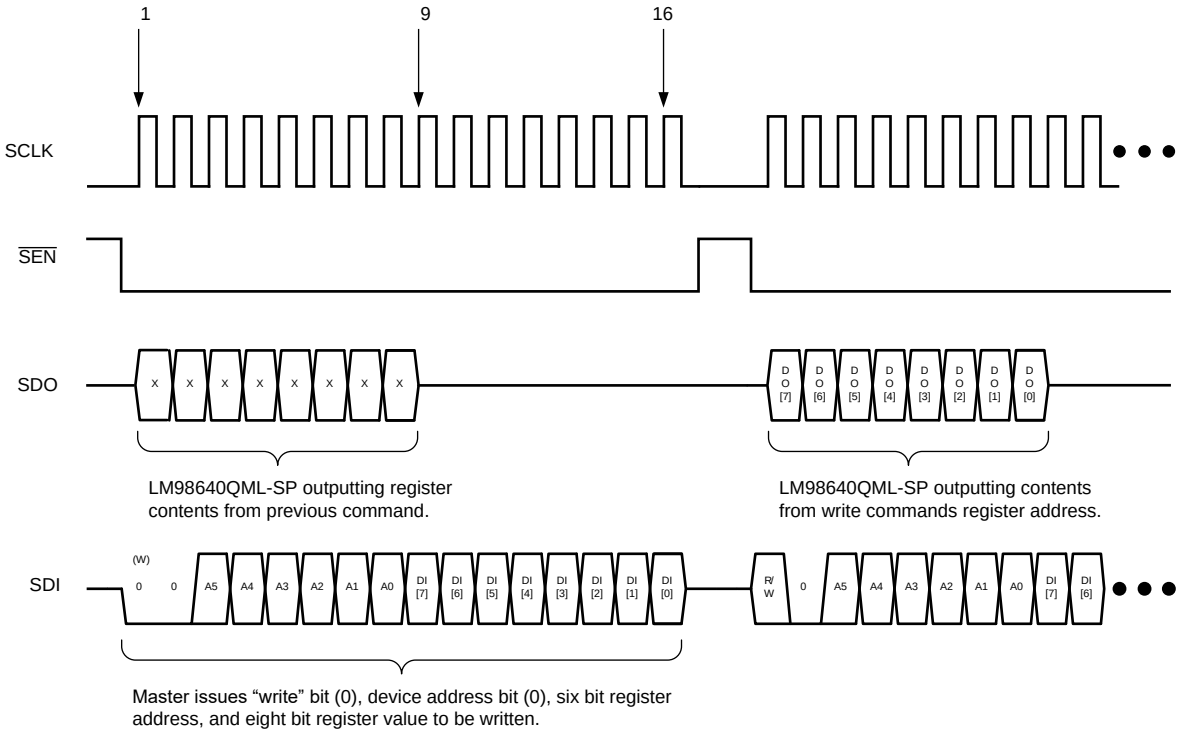


Figure 26. Four Wire Serial Write

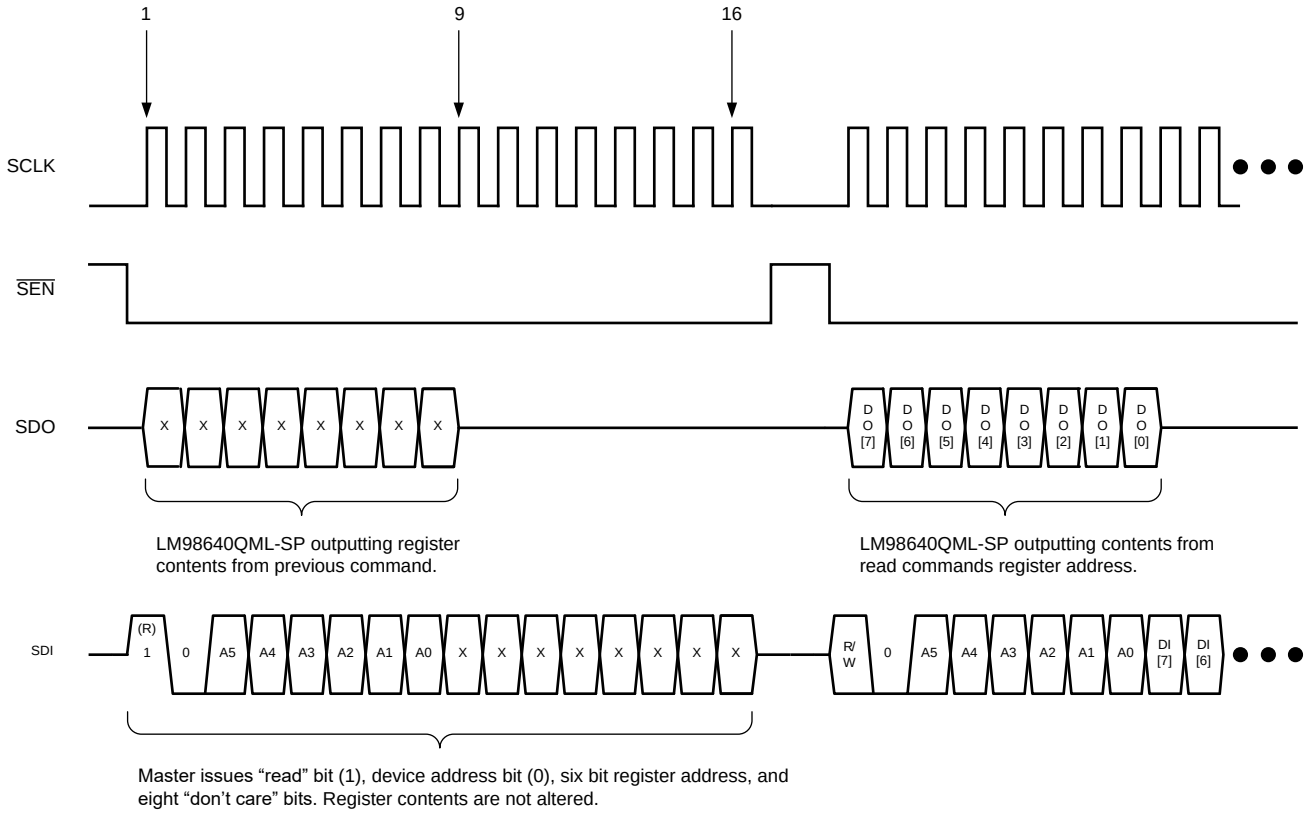


Figure 27. Four Wire Serial Read

Programming (continued)

7.5.4 Serial Interface Timing Details

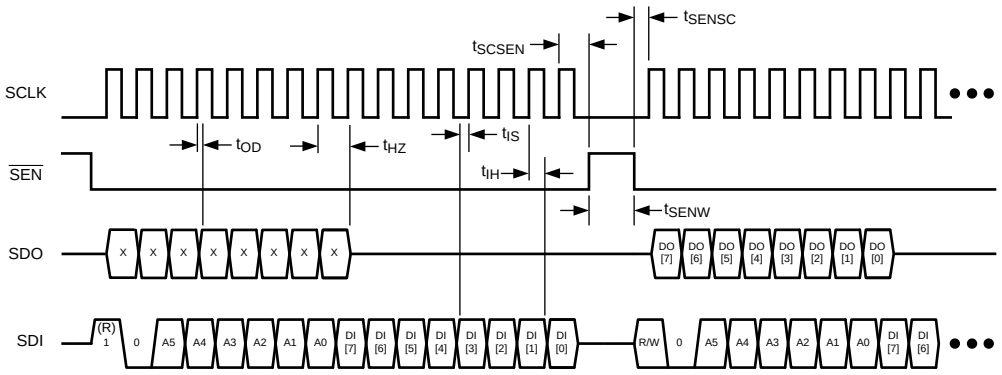


Figure 28. Serial Interface Specification Diagram

7.6 Register Maps

Registers need to be written with baseline values after power-up to place part in a valid state.

Table 5. Configuration Registers

ADDRESS (BINARY)	REGISTER TITLE (MNEMONIC)	BASELINE (BINARY)	REGISTER and BIT DESCRIPTION							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANALOG CONFIGURATION										
00 0000	Main Configuration	0000 0100	Not Used	Coarse DAC Enable	Fine DAC Enable	Reserved	CLPIN Gating Enable	CDS Gain Enable	Reserved	CDS Enable
00 0001	Powerdown Control	0000 0000	Master Powerdown	VCLP Powerdown	Ch2 Ref Buf Powerdown	Ch1 Ref Buf Powerdown	Ch2 PGA Powerdown	Ch1 PGA Powerdown	Ch2 ADC Powerdown	Ch1 ADC Powerdown
00 0010	PGA Power Trimming	0010 0100	Reserved		PGA Stage 2 Bias Current Trimming			PGA Stage 1 Bias Current Trimming		
00 0011	ADC Power Trimming	0101 1011	Reserved		ADC Current Trimming 2			ADC Current Trimming 1		
00 0100	VCLP Control	0111 0100	Not Used	Buffer Enable	VCLP Enable	VCLP Voltage Level				
00 0101	LVDS Output Modes	0000 1110	Clear	Reserved	Reserved	Reserved	Quad Lane Enable	LVDS Enable	LVDS Control	
00 0110	Sample & Hold	1000 0001	S/H Enable	Not Used				Ref Buf Power Level		Reserved
00 0111	Status	0000 0000	Not Used							False Lock
00 1000	Reserved	0000 0000	Reserved							
00 1001	Clock Monitor	0000 0000	Not Used			Enable/Select		Not Used		
00 1010	Reserved	0000 0000	Not Used							
00 1011	Reserved	0000 0000	Not Used							
00 1100	Reserved	0000 0000	Not Used							
00 1101	Reserved	0000 0000	Not Used							
00 1110	Reserved	0000 0000	Not Used							
00 1111	Reserved	0000 0000	Not Used							
GAIN & OFFSET DAC CONFIGURATION										
01 0000	CDAC1	0000 0000	Not Used							Offset bit 8
01 0001	CDAC1	1111 1111	Offset Value bits 7:0							
01 0010	FDAC1	0000 0000	Not Used							Offset bit 8
01 0011	FDAC1	1111 1111	Offset Value bits 7:0							
01 0100	Reserved	0000 0000	Not Used							
01 0101	PGA1	0110 0001	PGA Gain Value							
01 0110	Reserved	0000 0000	Not Used							
01 0111	Reserved	0000 0000	Not Used							
01 1000	CDAC2	0000 0000	Not Used							Offset Bit 8
01 1001	CDAC2	1111 1111	Offset Value bits 7:0							
01 1010	FDAC2	0000 0000	Not Used							Offset Bit 8
01 1011	FDAC2	1111 1111	Offset Value bits 7:0							

Register Maps (continued)

Table 5. Configuration Registers (continued)

ADDRESS (BINARY)	REGISTER TITLE (MNEMONIC)	BASELINE (BINARY)	REGISTER and BIT DESCRIPTION							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01 1100	PGA2	0110 0001	PGA Gain Value							
01 1101	Reserved	0000 0000	Not Used							
01 1110	Reserved	0000 0000	Not Used							
01 1111	Reserved	0000 0000	Not Used							
TIMING CONFIGURATION										
10 0000	Clamp Start	0000 1000	Not Used		Clamp Start Index					
10 0001	Clamp End	0001 1100	Not Used		Clamp End Index					
10 0010	Sample Start	0010 1000	Not Used		Sample Start Index					
10 0011	Sample End	0011 1100	Not Used		Sample End Index					
10 0100	Reserved	0011 0100	Reserved							
10 0101	INCLK Range	0000 0010	Not Used	INCLK Range			Not Used		Reserved	
10 0110	Reserved	0000 0000	Not Used							
10 0111	Reserved	0000 0000	Not Used							
10 1000	DLL Configuration	0000 1111	Reserved							DLL Reset
10 1001	Reserved	0000 0000	Not Used							
10 1010	Reserved	0000 0000	Not Used							
10 1011	Reserved	0000 0000	Not Used							
10 1100	Reserved	0000 0000	Not Used							
10 1101	Reserved	0000 0000	Not Used							
10 1110	Reserved	0000 0000	Not Used							
10 1111	Reserved	0000 0000	Not Used							
DIGITAL CONFIGURATION REGISTERS										
11 0000	Test Pattern Start	0000 0000	Start Upper Bits							
11 0001	Test Pattern Start	0000 0000	Start Lower Bits							
11 0010	Test Pattern Width	0000 0000	Width Upper Bits							
11 0011	Test Pattern Width	0000 0000	Width Lower Bits							
11 0100	Test Pattern Control	0000 0000	Pattern Enable	Pattern Mode			Pseudo Random Enable	Seed Enable	Pattern Output Channel	
11 0101	Test Pattern Pitch	0000 0000	Test Pattern Pitch							
11 0110	Test Pattern Step	0000 0000	Test Pattern Step Code							
11 0111	Test Pattern Channel Offset	0000 0000	Not Used				Test Pattern Channel Offset			
11 1000	Test Pattern Value	0000 0000	Pattern Upper Bits							
11 1001	Test Pattern Value	0000 0000	Pattern Lower Bits							
11 1010	Reserved	0000 0000	Not Used							
11 1011	Reserved	0000 0000	Not Used							
11 1100	Digital Configuration	0000 0000	Not Used							Auto Read
11 1101	Test & Scan Control	0000 0000	Not Used		Pattern Voting Enable	U-Wire Voting Enable	Not Used	Test Reset	Test Mode	Not Used
11 1110	Device ID	0100 1000	Device Revision ID. Engineering samples might be x01 or x47.							
11 1111	Reserved	0000 0000	Not Used							

7.6.1 Register Definitions

NOTE: Registers need to be written with baseline values after power-up to place part in a valid state.

Table 6. Register Definitions - Analog Configuration

ADDRESS (BINARY)	REGISTER TITLE	BASELINE (BINARY)	BIT(s)	DESCRIPTION
00 0000	Main Configuration	0000 0100	[7:0]	Main Configuration
			[7]	Not Used
			[6]	Coarse DAC Enable **0** Disable **1** Enable
			[5]	Fine DAC Enable **0** Disable **1** Enable
			[4]	Reserved
			[3]	CLPIN Gating Enable **0** CLPIN not gated by CLAMP **1** CLPIN gated by CLAMP (=logical "and" of CLPIN and CLAMP)
			[2]	Gain Mode Select. Selects either a 1x or 2x gain mode in the CDS/Sample/Hold Block **0** 1x Gain in the CDS/Sample/Hold Block **1** 2x Gain in the CDS/Sample/Hold Block
			[1]	Reserved. Set to 0.
			[0]	CDS / Sample/Hold Mode select. **0** Disabled. Correlated Double Sample Mode disabled. **1** Enabled. Correlated Double Sample Mode enabled.

Table 6. Register Definitions - Analog Configuration (continued)

ADDRESS (BINARY)	REGISTER TITLE	BASELINE (BINARY)	BIT(s)	DESCRIPTION
00 0001	Powerdown Control	0000 0000	[7:0]	Powerdown Control Register
			[7]	Master Powerdown **0** Fully Powered. **1** Powerdown Mode. Over rides bits [6:0].
			[6]	VCLP Powerdown **0** VCLP Fully Powered. **1** VCLP Powerdown Mode.
			[5]	Channel 2 Reference Buffer Powerdown **0** Reference Buffer Fully Powered. **1** Reference Buffer Powerdown Mode.
			[4]	Channel 1 Reference Buffer Powerdown **0** Reference Buffer Fully Powered. **1** Reference Buffer Powerdown Mode.
			[3]	Channel 2 PGA Powerdown **0** OpAmp Fully Powered. **1** OpAmp Powerdown Mode.
			[2]	Channel 1 PGA Powerdown **0** OpAmp Fully Powered. **1** OpAmp Powerdown Mode.
			[1]	Channel 2 ADC Powerdown **0** Amplifier Fully Powered. **1** Amplifier Powerdown Mode.
			[0]	Channel 1 ADC Powerdown **0** ADC Fully Powered. **1** ADC Powerdown Mode.
00 0010	PGA Power Trimming	0010 0100	[7:0]	PGA Power Trimming Register.
			[7:6]	Not Used
			[5:3]	PGA Stage 1 Current Trimming Tunable between **000**-Weak to **111**-Strong (Default **100**)
			[2:0]	PGA Stage 2 Current Trimming Tunable between **000**-Weak to **111**-Strong (Default **100**)

Table 6. Register Definitions - Analog Configuration (continued)

ADDRESS (BINARY)	REGISTER TITLE	BASELINE (BINARY)	BIT(s)	DESCRIPTION
00 0011	ADC Power Trimming	0101 1011	[7:0]	ADC Power Trimming Register.
			[7:6]	Reserved. Set to 2'b01.
			[5:3]	ADC Current Trimming 2(Not Binary Weighted) **000** 25% Power **001** 50% Power **011** 75% Power (Default) **111** 100% Power
			[2:0]	ADC Current Trimming 1 (Not Binary Weighted) **000** 25% Power **001** 50% Power **011** 75% Power (Default) **111** 100% Power
00 0100	VCLP Control	0111 0100	[7:0]	Voltage Clamp Buffer Control Register.
			[7]	Not Used
			[6]	Buffer Enable **0** Disabled. Resistor Ladder is driving VCLP pin. **1** Enabled. Resistor Ladder is buffered to VCLP pin.
			[5]	VCLP Enable **0** Disabled. VCLP pin can be externally driven. **1** Enabled. VCLP pin is in output mode.
			[4:0]	Voltage Level of VCLP pin. VCLP range is 200mV to 3.1V in 100mV steps for (binary) settings 00000 to 11101. Settings 11110 and 11111 are not used.
00 0101	LVDS Output Modes	0000 1110	[7:0]	LVDS Output Configuration Register.
			[7]	Serializer Data Reset. (Not self-clearing)
			[6:4]	Not Used.
			[3]	LVDS Output Mode **0** Dual Lane Mode (see Output Mode 1 - Dual Lane) **1** Quad Lane Mode (see Output Mode 2 - Quad Lane)
			[2]	LVDS Driver Enable. **0** LVDS Drivers Disabled **1** LVDS Drivers Enabled (Note: In Dual Lane Mode TX0 and TX3 are disabled regardless of driver enable)
			[1:0]	LVDS Amplitude and Common Mode Voltage. **00** 250mV (1.2V DC Offset) **01** 300mV (1.2V DC Offset) **10** 350mV (1.1V DC Offset) **11** 400mV (1.1V DC Offset)

Table 6. Register Definitions - Analog Configuration (continued)

ADDRESS (BINARY)	REGISTER TITLE	BASELINE (BINARY)	BIT(s)	DESCRIPTION
00 0110	Sample & Hold	1000 0001	[7:0]	Sample & Hold Mode Register
			[7]	Sample & Hold Mode Enable **0** Disabled. **1** Enabled.
			[6:3]	Not Used.
			[2:1]	Reference Buffer Power Level **11** 100% Power. Used for F_{INCLK} = 20-40MHz. **10** 60% Power. Used for F_{INCLK} = 10-20MHz. **01** 60% Power. Used for F_{INCLK} = 10-20MHz. **00** 30% Power. Used for F_{INCLK} = 5-10MHz.
			[0]	Reserved.
00 0111	Status	0000 0000	[7:0]	Status Register. (Read Only)
			[7:1]	Not Used.
			[0]	False Lock Detect. Indicates if DLL is locked into a half frequency state.
00 1001	Clock Monitor	0000 0000	[7:0]	Internal Clock Signal Monitor Register
			[7:5]	Not Used.
			[4:3]	Enable and select clocks to be monitored on the Digital Timing Monitor. (DTM) **00** Disable Digital Timing Monitor Pins (DTM0, DTM1) **01** Send $CLAMP_{EVEN}$ to DTM0 pin, and $SAMPLE_{EVEN}$ to DTM1 **10** Send $CLAMP_{ODD}$ to DTM0 pin, and $SAMPLE_{ODD}$ to DTM1 **11** Send ODD tag and ADC Clock to the DTM.
			[2:0]	Reserved. Set to 000.

Table 7. Register Definitions - GAIN & Offset DAC Configuration

ADDRESS (BINARY)	REGISTER TITLE	BASELINE (BINARY)	BIT(s)	DESCRIPTION
01 0000	CDAC1	0000 0000	[7:0]	Channel 1 Coarse DAC Register.
			[7:1]	Not Used.
			[0]	Bit 8 of Channel 1 Coarse DAC Offset Value.
01 0001	CDAC1	1111 1111	[7:0]	Channel 1 Coarse DAC Offset Value bits 7:0.
01 0010	FDAC1	0000 0000	[7:0]	Channel 1 Fine DAC Register.
			[7:1]	Not Used.
			[0]	Bit 8 of Channel 1 Fine DAC Offset Value.
01 0011	FDAC1	1111 1111	[7:0]	Channel 1 Fine DAC Offset Value bits 7:0.
01 0101	PGA1	0110 0001	[7:0]	Channel 1 Programmable Gain Amplifier Value.
01 1000	CDAC2	0000 0000	[7:0]	Channel 2 Coarse DAC Register.
			[7:1]	Not Used.
			[0]	Bit 8 of Channel 2 Coarse DAC Offset Value.
01 1001	CDAC2	1111 1111	[7:0]	Channel 2 Coarse DAC Offset Value bits 7:0.
01 1010	FDAC2	0000 0000	[7:0]	Channel 2 Fine DAC Register.
			[7:1]	Not Used.
			[0]	Bit 8 of Channel 2 Fine DAC Offset Value.
01 1011	FDAC2	1111 1111	[7:0]	Channel 2 Fine DAC Offset Value bits 7:0.
01 1100	PGA2	0110 0001	[7:0]	Channel 2 Programmable Gain Amplifier Value.

Table 8. Register Definitions - Timing Configuration

ADDRESS (BINARY)	REGISTER TITLE	BASELINE (BINARY)	BIT(s)	DESCRIPTION
10 0000	Clamp Start	0000 1000	[7:0]	Clamp Start Register.
			[7:6]	Not Used.
			[5:0]	CLAMP Starting Index. 0-63d position for rising edge of CLAMP signal. Valid only in CDS Mode.
10 0001	Clamp End	0001 1100	[7:0]	Clamp End Register.
			[7:6]	Not Used.
			[5:0]	CLAMP End Index. 0-63d position for falling edge of CLAMP signal. Valid only in CDS Mode.
10 0010	Sample Start	0010 1000	[7:0]	Sample Start Register.
			[7:6]	Not Used.
			[5:0]	SAMPLE starting Index. 0-63d position for rising edge of SAMPLE signal.
10 0011	Sample End	0011 1100	[7:0]	Sample End Register.
			[7:6]	Not Used.
			[5:0]	SAMPLE End Index. 0-63d position for falling edge of SAMPLE signal.
10 0101	INCLK Range	0000 0010	[7:0]	INCLK Range Register.
			[7]	Not Used.
			[6:4]	INCLK Range. **000** 25 to 40 MHz Operation **001** 14 to 25 MHz Operation **010** 10 to 14 MHz Operation **011** 7.5 to 10 MHz Operation **100** 6 to 7.5 MHz Operation **101** 5 to 6 MHz Operation **110** Not Used **111** Not Used
			[3:2]	Not Used.
			[1:0]	DLL Range **11** Reserved **10** 14 to 40 MHz Operation **01** 7.5 to 14 MHz Operation **00** 5 to 7.5 MHz Operation
10 1000	DLL Configuration	0000 1111	[7:0]	DLL Configuration Register
			[7:1]	Reserved
			[0]	DLL Reset. (Self Clearing)

Table 9. Register Definitions - Digital Configuration

ADDRESS (BINARY)	REGISTER TITLE	BASELINE (BINARY)	BIT(s)	DESCRIPTION
11 0000	Test Pattern Start	0000 0000	[15:8]	Upper 8 bits of the Test Pattern start value. Specifies the number of pixels after the leading edge of CLPIN to the Valid Pixel region.
11 0001	Test Pattern Start	0000 0000	[7:0]	Lower 8 bits of the Test Pattern start value. Specifies the number of pixels after the leading edge of CLPIN to the Valid Pixel region.
11 0010	Test Pattern Width	0000 0000	[15:8]	Upper 8 bits of the Test Pattern Width value. Specifies, in number of pixels, the width of the Valid Pixel region.
11 0011	Test Pattern Width	0000 0000	[7:0]	Lower 8 bits of the Test Pattern Width value. Specifies, in number of pixels, the width of the Valid Pixel region.
11 0100	Test Pattern Control	0000 0000	[7:0]	Test Pattern Control Register.
			[7]	Programmable Pattern Switch
				0 Disabled. Normal LVDS output operation.
				1 Enabled. AFE outputs LVDS test patterns.
			[6:4]	Test Pattern Mode
				000 Fixed Code
				001 Horizontal Gradient Scan (Main Scan)
				010 Vertical Gradient Scan (Sub Scan)
				011 Grid Scan (Lattice Pattern)
				100 Strip Pattern
				101 LVDS Test Pattern. (Synchronous to CLPIN)
				110 LVDS Test Pattern. (Asynchronous)
				111 Not Used.
			[3]	Pseudo Random Pattern Enable.
				Overrides Programmable Patter Switch setting (bit 7). Normally only one should be on.
			[2]	Load Seed Enable.
				When set, the seed value in the Test Pattern Value Register is loaded in the LFSR at the leading edge of CLPIN.
			[1:0]	Test Pattern Output Channel Select.
				00 Both Channels
				01 Channel 1
				10 Channel 2
				11 Not Used
11 0101	Test Pattern Pitch	0000 0000	[7:0]	Test Pattern pitch, specifies number of pixels for H Gradient pattern and Stripe pattern, or number of lines in the V Gradient pattern, or specifies pixels & lines in the Lattice pattern.
11 0110	Test Pattern Step	0000 0000	[7:0]	Test Pattern Step Code. Specifies step size in LSB codes the pattern is incremented in H Gradient and V Gradient pattern. In Lattice and Stripe pattern it specifies the code during the lower step.
11 0111	Test Pattern Channel Offset	0000 0000	[7:0]	Test Pattern Channel Offset Register.
			[7:4]	Not Used.
			[3:0]	Test Pattern Channel Offset. This specifies the number of lines the pattern on Channel 2 is delayed from Channel 1. This offset is maintained throughout the pattern.
11 1000	Test Pattern Value	0000 0000	[15:8]	Upper 8 bits of Test Pattern Value Register. Specifies the upper 8 bits of the test value code during Fixed Pattern and LVDS test, initial value during H Gradient & V Gradient pattern, and higher value in the Lattice and Stripe Pattern.

Table 9. Register Definitions - Digital Configuration (continued)

ADDRESS (BINARY)	REGISTER TITLE	BASELINE (BINARY)	BIT(s)	DESCRIPTION
11 1001	Test Pattern Value	0000 0000	[7:0]	Lower 6 bits of Test Pattern Value Register. Specifies the lower 6 bits of the test code value during Fixed Pattern and LVDS test, initial value during H Gradient & V Gradient pattern, and higher value in the Lattice and Stripe Pattern.
11 1100	Digital Configuration	0000 0000	[7:0]	Serial Communication Configuration Register.
			[7:1]	Not Used.
			[0]	Micro-Wire Automatic Read Disable. **0** Read data is always sent out on SDO during the first 8 SCLK cycles. The register is selected by the register address in the previous cycle. (read or write) **1** Automatic read is disabled. To read from a register two cycles need to be initiated by the master, first cycle should be a read with the correct register address and second can be a dummy read or read from another address or a write cycle, and the data is sent first 8 SCLK of the second cycle. After a write command SDO remains in Tri-State during first 8 SCLK.
11 1101	Test & Scan Control	0000 0000	[7:0]	Test & Scan Control Register
			[7:6]	Not Used.
			[5]	Test Pattern Voting Switch. **0** Enable. Circuit Redundancy Voting is active. **1** Disable. First redundancy block output is used.
			[4]	Micro-wire Voting Switch. **0** Enable. Circuit Redundancy Voting is active. **1** Disable. First Micro-wire block output is used.
			[3]	Not Used.
			[2]	Test Reset. Resets the test block when High, normal test block function when Low. This bit is not self-clearing.
			[1]	Test Mode Enable. **0** Disable. **1** Enable. Needed to run Test Pattern functions.
			[0]	Not Used.
11 1110	Device ID	0100 1000	[7:0]	Device Revision ID. Engineering samples might be x01 or x47.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

8.1.1 Total Ionizing Dose

Testing and qualification of this product is done according to MIL-STD-883, Test Method 1019.

This product is on Texas Instruments' CMOS9X process, a CMOS process shown to be ELDRS-Free. ELDRS report for the process is available upon request.

Radiation lot acceptance testing (RLAT) is performed at high dose rate. On some lots the room temperature anneal test is used, with anneal times up to 6 weeks. An RLAT report to the wafer level is available for each lot.

8.1.2 Single Event Latch-Up and Functional Interrupt

One time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. SEL testing was conducted with the junction temperature at 125°C. The linear energy transfer threshold (LETth) shown in the features list on the front page is the maximum LET tested. A test report is available upon request.

8.1.3 Single Event Effects

A report on single event upset (SEU) is available upon request.

8.2 Typical Application

8.2.1 Sample/Hold Mode

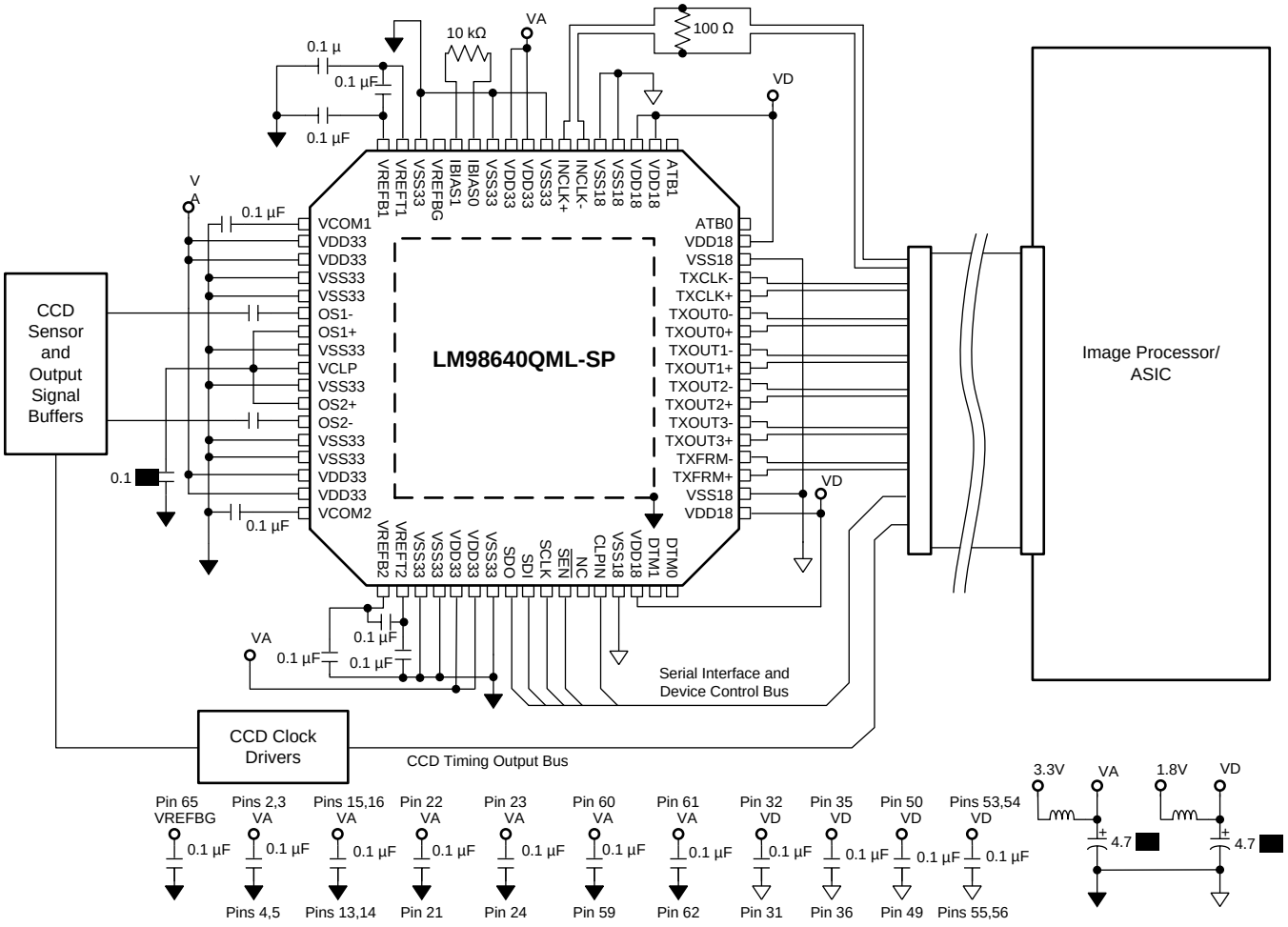


Figure 29. Typical CDS Mode Application Diagram

8.3 Initialization Set Up

1. Power up supply voltages VDD33 and VDD18.
2. Apply signal to INCLK.
3. Write all configuration registers. Be sure to set the INCLK Range (2x05) and Sample & Hold (0x06) for the INCLK frequency used.
4. Write the Test & Scan register (3x0D) before the Clock Monitor register (0x09).

9 Layout

9.1 Layout Guidelines

9.1.1 Power Planes

Power for the LM98640QML-SP should be provided through a broad plane which is located on one layer adjacent to the ground plane(s). Placing the power and ground planes on adjacent layers will provide low impedance decoupling of the AFE supplies, especially at higher frequencies. The output of a linear regulator should feed into the power plane through a low impedance multi-via connection. The power plane should be split into individual power peninsulas near the AFE. Each peninsula should feed a particular power bus on the AFE, with decoupling for that power bus connecting the peninsula to the ground plane near each power/ground pin pair. Using this technique can be difficult on many printed circuit CAD tools. To work around this, 0-Ω resistors can be used to connect the power source net to the individual nets for the different AFE power buses. As a final step, the 0-Ω resistors can be removed and the plane and peninsulas can be connected manually after all other error checking is completed.

9.1.2 Bypass Capacitors

The general recommendation is to have one 100-nF capacitor for each power/ground pin pair. The capacitors should be surface mount multi-layer ceramic chip capacitors.

9.1.3 Ground Plane

Grounding should be done using continuous full ground planes to minimize the impedance for all ground return paths, and provide the shortest possible image/return path for all signal traces.

9.1.4 Thermal Management

The exposed pad on bottom of the package is attached to the back of the die to act as a heat sink. Connecting this pad to the PCB ground planes with a low thermal resistance path is the best way to remove heat from the AFE. This pad should also be connected to the ground planes through low impedance path for electrical purposes.

10 器件和文档支持

10.1 器件支持

10.1.1 开发支持

10.1.1.1 评估板

LM98640CVAL 是一种灵活的评估板，可配置用于 LM98640 的多种不同工作模式。LM98640CVAL 可由 WaveVison 5 数据捕获板进行驱动。驱动评估板的软件仅适用于 Windows XP。

10.1.1.2 寄存器编程软件

可从 LM98640CVAL 工具文件夹下载图形用户界面 (GUI)。它可用于验证不同配置模式的寄存器设置。该软件仅适用于 Windows XP。

10.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 社区资源

通过以下链接可访问 TI 社区资源。链接的内容由各个分销商“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 TI 的高可用性产品工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

10.4 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

10.5 商标

All trademarks are the property of their respective owners.

10.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

10.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

11.1 工程样片

工程样片可用订购，在可订购器件名称中以“MPR”进行标识（请参阅“附录”中的“封装信息”）。工程 (MPR) 样片仅在室温下符合数据表性能规格，尚未经历全面的生产流程或测试。工程样片的 QCI 可能不符合规定，无法通过测试，但不会影响其在室温下的性能，如辐射或可靠性测试。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R1820301VXC	Active	Production	CFP (NBB) | 68	12 | JEDEC TRAY (5+1)	-	Call TI	Level-1-NA-UNLIM	-55 to 125	5962 R1820301VXC LM98640-RHA
5962R1820301VXC.A	Active	Production	CFP (NBB) | 68	12 | JEDEC TRAY (5+1)	-	Call TI	Level-1-NA-UNLIM	-55 to 125	5962 R1820301VXC LM98640-RHA
LM98640W-MLS	Active	Production	CFP (NBB) | 68	12 | JEDEC TRAY (5+1)	-	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM98640W, LM98640 W-MLS) -MLS
LM98640W-MLS.A	Active	Production	CFP (NBB) | 68	12 | JEDEC TRAY (5+1)	-	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM98640W, LM98640 W-MLS) -MLS
LM98640W-MPR	Active	Production	CFP (NBB) | 68	12 | JEDEC TRAY (5+1)	-	Call TI	Level-1-NA-UNLIM	25 to 25	LM98640W-MPR ES
LM98640W-MPR.A	Active	Production	CFP (NBB) | 68	12 | JEDEC TRAY (5+1)	-	Call TI	Level-1-NA-UNLIM	25 to 25	LM98640W-MPR ES

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

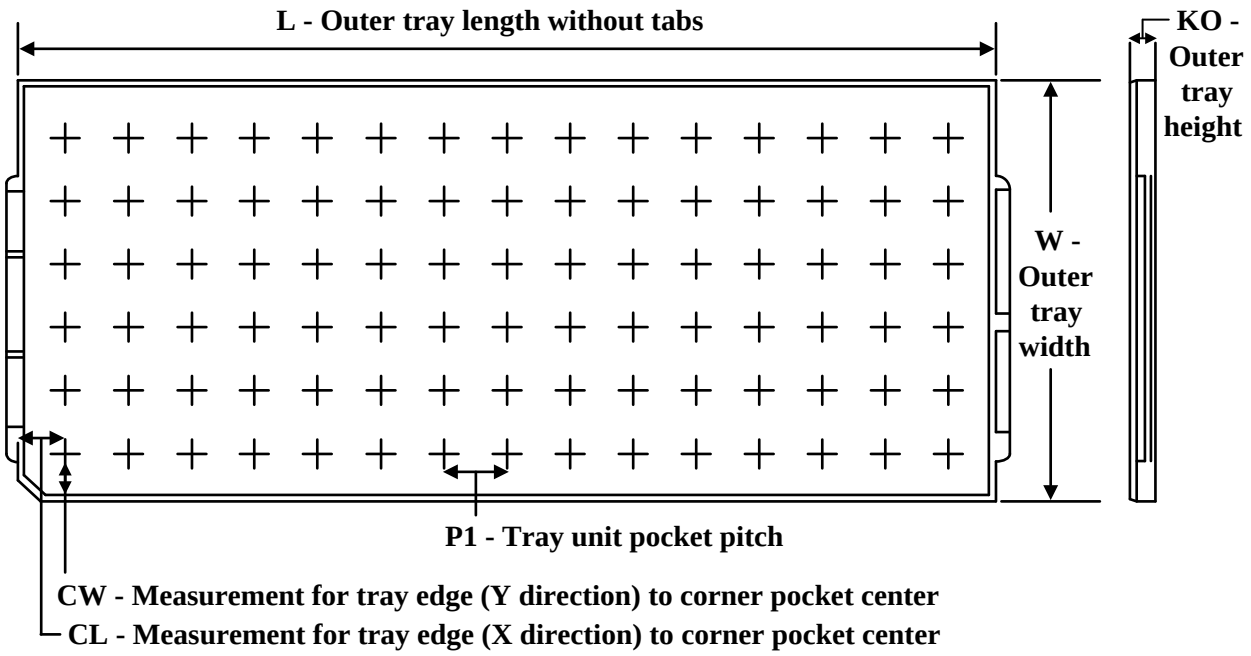
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY

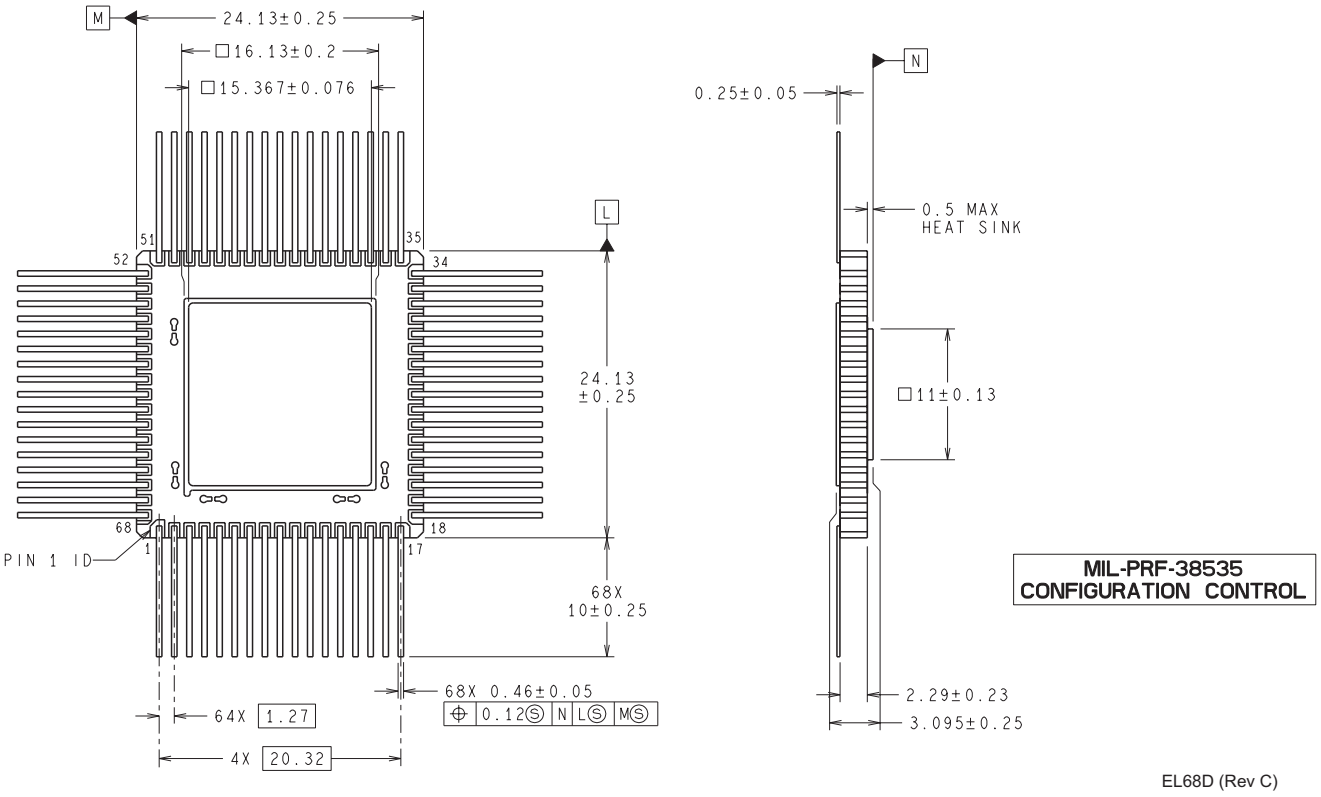


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962R1820301VXC	NBB	CFP	68	12	3 X 4	NA	280	230	19000	60.6	79.4	54.5
5962R1820301VXC.A	NBB	CFP	68	12	3 X 4	NA	280	230	19000	60.6	79.4	54.5
LM98640W-MLS	NBB	CFP	68	12	3 X 4	NA	280	230	19000	60.6	79.4	54.5
LM98640W-MLS.A	NBB	CFP	68	12	3 X 4	NA	280	230	19000	60.6	79.4	54.5
LM98640W-MPR	NBB	CFP	68	12	3 X 4	NA	280	230	19000	60.6	79.4	54.5
LM98640W-MPR.A	NBB	CFP	68	12	3 X 4	NA	280	230	19000	60.6	79.4	54.5

NBB0068D


M
24.13±0.25
□16.13±0.2
□15.367±0.076
L
51
35
52
34
24.13
±0.25
68
18
1
17
PIN 1 ID
68X
10±0.25
68X 0.46±0.05
0.12Ⓢ N LⓈ MⓈ
64X 1.27
4X 20.32
N
0.25±0.05
0.5 MAX
HEAT SINK
□11±0.13
2.29±0.23
3.095±0.25
MIL-PRF-38535
CONFIGURATION CONTROL
EL68D (Rev C)

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