TEXAS INSTRUMENTS

LM7705

ZHCSI84D – NOVEMBER 2008 – REVISED MAY 2018

《LM7705 低噪声负偏置发生器》

1 特性

- 经过稳压的输出电压 - 0.232V
- 输出电压容差为 5%
- 输出纹波电压为 $4mV_{PP}$
- 电源电压为 3V 至 5.25V
- 转换效率高达 98%
- 静态电流为 78µA
- 关断电流为 20nA
- 开通时间为 500µs
- 运行温度范围为 –40°C 至 125°C
- 8 引脚 VSSOP 封装

2 应用

- 真正的零放大器输出
- 便携式仪表
- 低压分离电源

3 说明

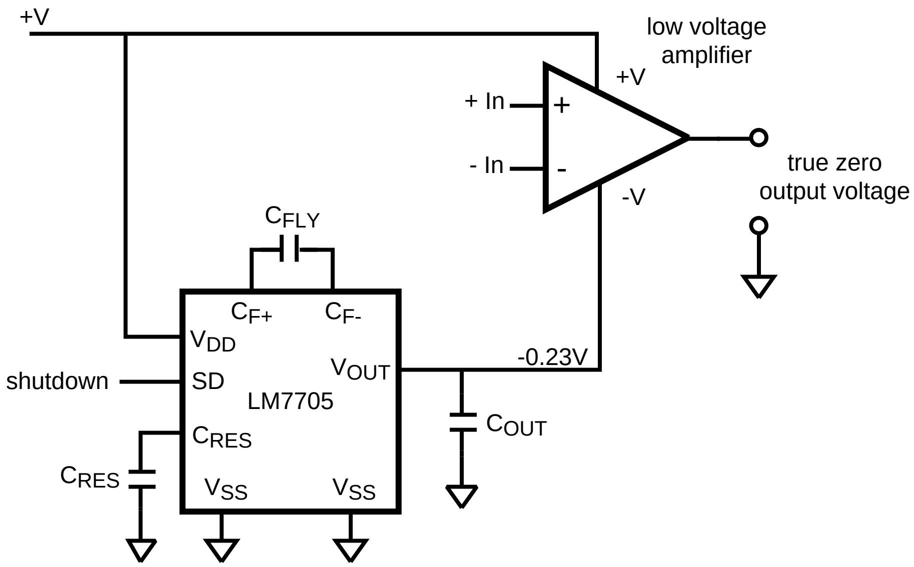
LM7705 器件是一款带有一个 −0.23V 低噪声固定式负电压稳压器的开关电容器电压逆变器。此器件专门用于低电压放大器，使放大器输出接近零电压。−0.23V 用于为放大器的负电源引脚供电，同时将整个放大器的电压维持在 5.5V 以下。在单电源电压下工作时，轨至轨输出放大器无法输出零电压，并且由于放大器输出饱和电压被以下增益级放大，因而会导致累积误差。较小的负电源电压会阻止放大器输出在零电压时达到饱和状态，并有助于通过信号处理链维持准确的零电压。而且，当使用放大器驱动 ADC 输入时，该放大器可以输出一个零电压信号，并可以使用完整的 ADC 输入范围。LM7705 器件具有一个关断引脚，可将待机功耗降至最低。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
LM7705	VSSOP (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见产品说明书末尾的可订购产品附录。

典型应用



English Data Sheet: SNVS420

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (September 2015) to Revision D **Page**

- 已删除 在 特性 列表中删除了“最大输出电流 26mA” 1
- Deleted I_O_MAX spec from 3.3-V Electrical Characteristics and 5-V Electrical Characteristics tables 4

Changes from Revision B (March 2013) to Revision C **Page**

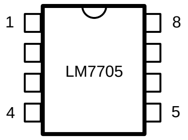
- 添加了 *引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 1

Changes from Revision A (November 2008) to Revision B **Page**

- Changed layout of National Semiconductor Data Sheet to TI format 19

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C_{F+}	1	Analog	C_{FLY} Positive Capacitor Connection
V_{SS}	2	Ground	Power Ground
SD	3	Input	Shutdown Pin If SD pin is LOW, device is ON If SD pin is HIGH, device is OFF
V_{DD}	4	Power	Positive Supply Voltage
V_{SS}	5	Ground	Power Ground
V_{OUT}	6	Output	Output Voltage
C_{RES}	7	Analog	Reserve Capacitor Connection
C_{F-}	8	Analog	C_{FLY} Negative Capacitor Connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage V_{DD} - V_{SS}			5.75	V
SD		V_{DD} + 0.3	V_{SS} – 0.3	V
Junction temperature(2)			150	°C
Mounting temperature	Infrared or Convection (20 sec)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	
		Machine model(3)	±200	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7.
(2) Field induced Charge-Device Model, applicable std. JESD22–C101–C. (ESD FICDM std of JEDEC).
(3) Machine model, applicable std JESD22–A115–A (ESSD MM srd of JEDEC).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage (V_{DD} to GND)	3	5.25	V
Supply voltage (V_{DD} wrt V_{OUT})	3.23	5.48	V
Temperature range	−40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM77005	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	253	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 3.3-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_{DD} = 3.3 V, V_{SS} = 0 V, SD = 0 V, C_{FLY}= 5 µF, C_{RES} = 22 µF, C_{OUT} = 22 µF.

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OUT}	Output Voltage	I_{OUT} = 0 mA	T_A = 25°C	−0.242	−0.232	−0.219	V
			−40°C to 125°C	−0.251		−0.209	
		I_{OUT} = −20 mA	T_A = 25°C	−0.242	−0.226	−0.219	
			−40°C to 125°C	−0.251		−0.209	
V_R	Output Voltage Ripple	I_{OUT} = −20 mA			4		mV_{PP}
I_S	Supply Current	No Load	T_A = 25°C	50	78	100	µA
			−40°C to 125°C			150	
I_{SD}	Shutdown Supply Current	SD = V_{DD}			20		nA
η_{POWER}	Current Conversion Efficiency	−5 mA ≤ I_{OUT} ≤ −20 mA			98%		
η_{POWER}	Current Conversion Efficiency	I_{OUT} = −5 mA			98%		
t_{ON}	Turnon Time	I_{OUT} = −5 mA			500		µs
t_{OFF}	Turnoff Time	I_{OUT} = −5 mA			700		µs
$t_{OFF\ CP}$	Turnoff Time Charge Pump	I_{OUT} = −5 mA			11		µs
Z_{OUT}	Output Impedance	−1 mA ≤ I_{OUT} ≤ −20 mA	T_A = 25°C		0.23	0.8	Ω
			−40°C to 125°C			1.3	
f_{OSC}	Oscillator Frequency				92		kHz
V_{IL}	Shutdown Input Low	T_A = 25°C				1.6	V
		−40°C to 125°C				1.25	
V_{IH}	Shutdown Input High	T_A = 25°C		1.85			V
		−40°C to 125°C		2.15			
I_C	Shutdown Pin Input Current	SD = V_{DD}			50		pA
	Load Regulation	0 mA ≤ I_{OUT} ≤ −20 mA	T_A = 25°C		0.12	0.6	%/mA
			−40°C to 125°C			0.85	

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

3.3-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_{DD} = 3.3 V, V_{SS} = 0 V, SD = 0 V, C_{FLY}= 5 µF, C_{RES} = 22 µF, C_{OUT} = 22 µF.

PARAMETER	TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
Line Regulation	3 V ≤ V_{DD} ≤ 5.25 V (No Load)	T_A = 25°C	–0.2	0.29	0.7	%/V
		−40°C to 125°C			1.1	

6.6 5-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_{DD} = 5.0V, V_{SS} = 0V, SD = 0V, C_{FLY} = 5 µF, C_{RES} = 22 µF, C_{OUT} = 22 µF.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OUT}	Output Voltage	I_{OUT} = 0 mA	T_A = 25°C	−0.242	−0.233	−0.219	V
			−40°C to 125°C	−0.251		−0.209	
		I_{OUT} = −20 mA	T_A = 25°C	−0.242	−0.226	−0.219	
			−40°C to 125°C	−0.251		−0.209	
V_R	Output Voltage Ripple	I_{OUT} = −20 mA			4		mV_{PP}
I_S	Supply Current	No Load	T_A = 25°C	60	103	135	µA
			−40°C to 125°C			240	
I_{SD}	Shutdown Supply Current	SD = V_{DD}			20		nA
η_{POWER}	Current Conversion Efficiency	−5 mA ≤ I_{OUT} ≤ −20 mA			98%		
η_{POWER}	Current Conversion Efficiency	I_{OUT} = −5 mA			98%		
t_{ON}	Turnon Time	I_{OUT} = −5 mA			200		µs
t_{OFF}	Turnoff Time	I_{OUT} = −5 mA			700		µs
$t_{OFF\ CP}$	Turnoff Time Charge Pump	I_{OUT} = −5 mA			11		µs
Z_{OUT}	Output Impedance	−1 mA ≤ I_{OUT} ≤ −20 mA	T_A = 25°C		0.26	0.8	Ω
			−40°C to 125°C			1.3	
f_{OSC}	Oscillator Frequency				91		kHz
V_{IL}	Shutdown Input Low	T_A = 25°C				2.55	V
		−40°C to 125°C				1.95	
V_{IH}	Shutdown Input High	T_A = 25°C		2.8			V
		−40°C to 125°C		3.25			
I_C	Shutdown Pin Input Current	SD = V_{DD}			50		pA
	Load Regulation	0 mA ≤ I_{OUT} ≤ −20 mA	T_A = 25°C		0.14	0.6	%/mA
			−40°C to 125°C			0.85	
	Line Regulation	3 V ≤ V_{DD} ≤ 5.25 V (No Load)	T_A = 25°C	−0.2	0.29	0.7	%/V
			−40°C to 125°C			1.1	

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

6.7 Typical Characteristics

V_{DD} = 3.3 V and T_A = 25°C unless otherwise noted.

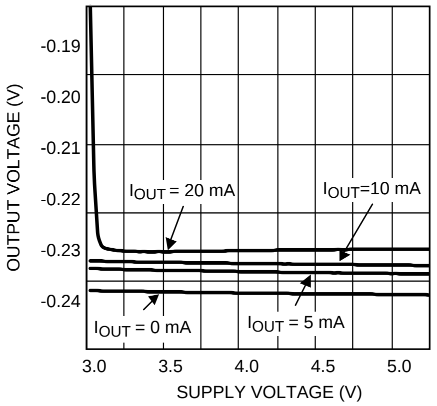


Figure 1. Output Voltage vs. Supply Voltage

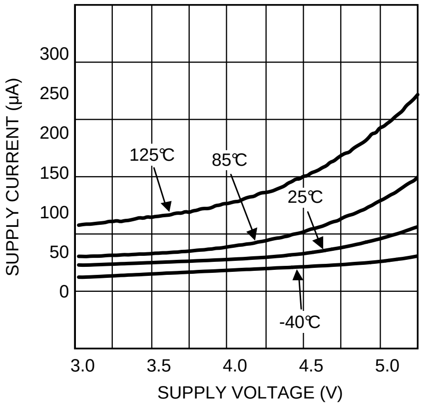


Figure 2. Supply Current vs. Supply Voltage

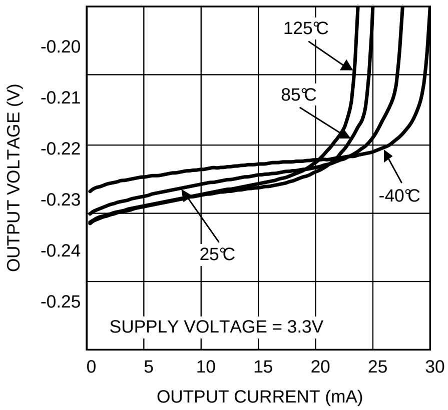


Figure 3. Output Voltage vs. Output Current

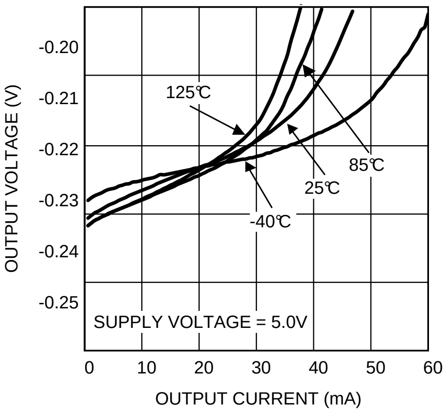


Figure 4. Output Voltage vs. Output Current

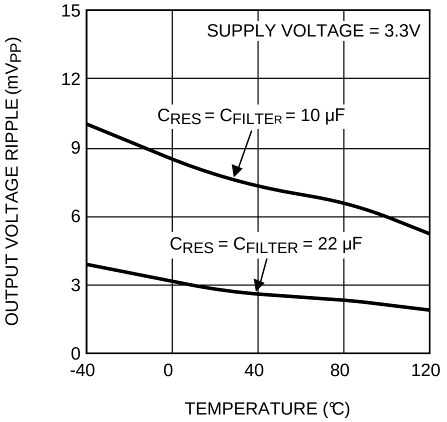


Figure 5. Output Voltage Ripple vs. Temperature

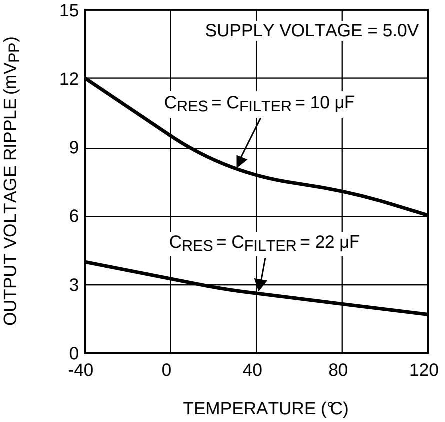


Figure 6. Output Voltage Ripple vs. Temperature

Typical Characteristics (continued)

V_{DD} = 3.3 V and T_A = 25°C unless otherwise noted.

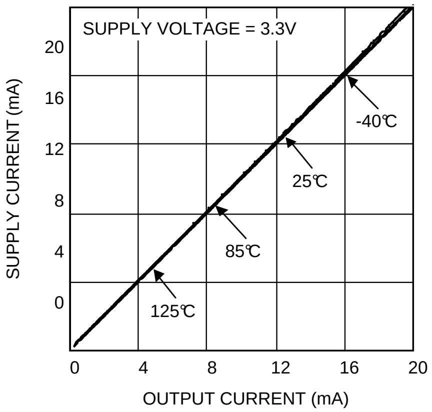


Figure 7. Supply Current vs. Output Current

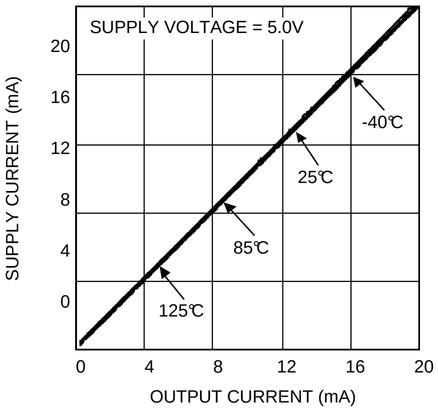


Figure 8. Supply Current vs. Output Current

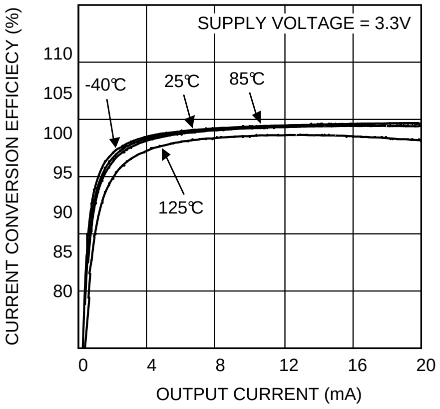


Figure 9. Current Conversion Efficiency vs. Output Current

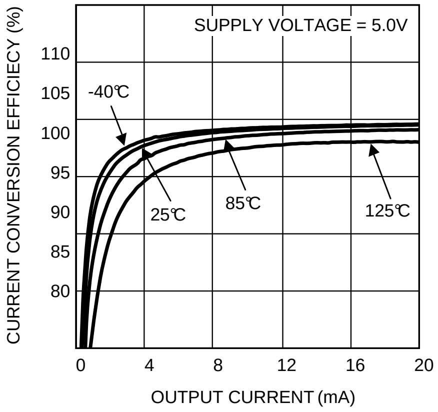


Figure 10. Current Conversion Efficiency vs. Output Current

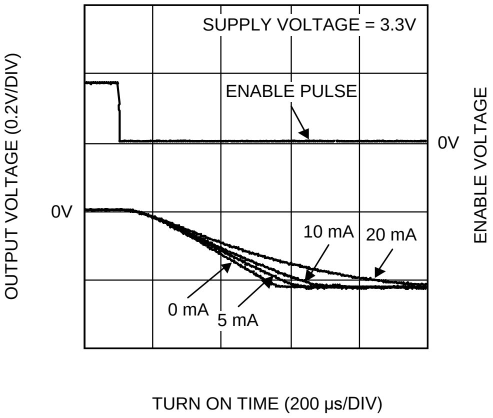


Figure 11. Turnon Time

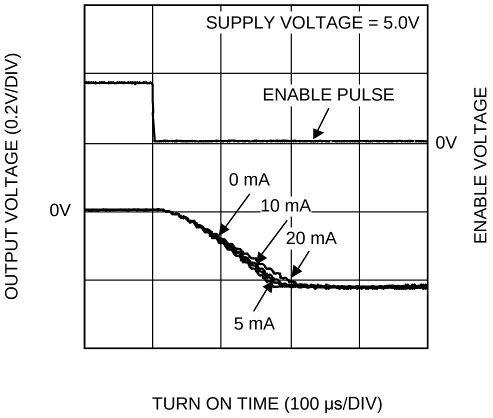


Figure 12. Turnon Time

Typical Characteristics (continued)

V_{DD} = 3.3 V and T_A = 25°C unless otherwise noted.

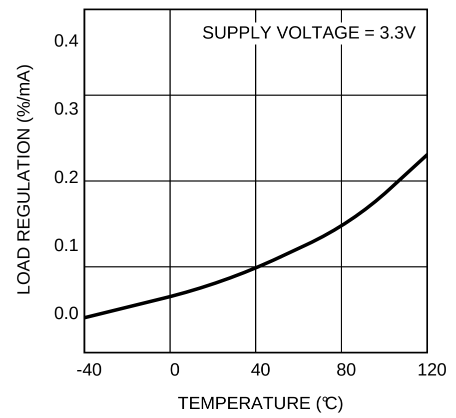


Figure 13. Load Regulation vs. Temperature

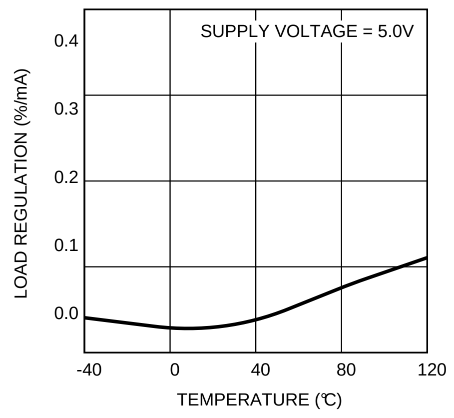


Figure 14. Load Regulation vs. Temperature

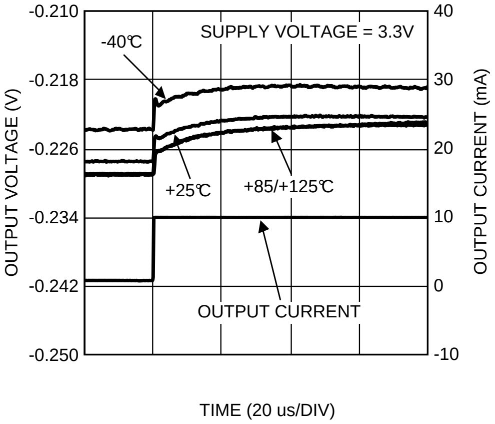


Figure 15. Transient Response

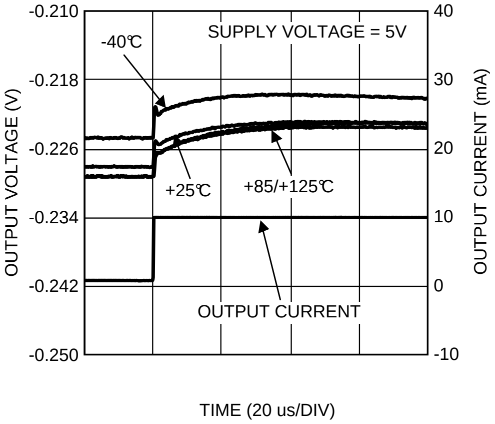


Figure 16. Transient Response

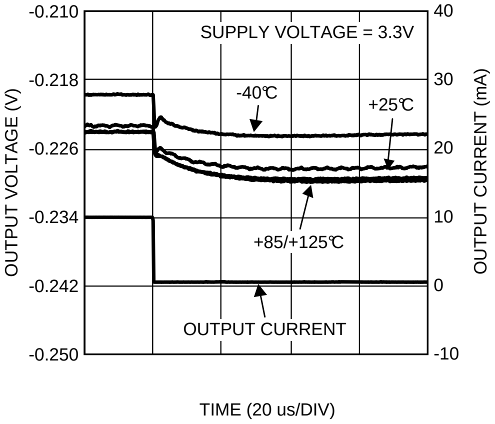


Figure 17. Transient Response

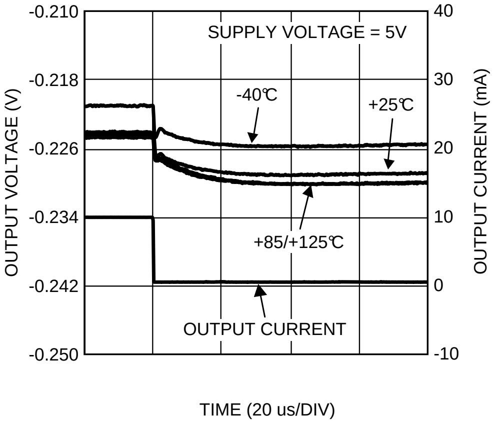


Figure 18. Transient Response

Typical Characteristics (continued)

V_{DD} = 3.3 V and T_A = 25°C unless otherwise noted.

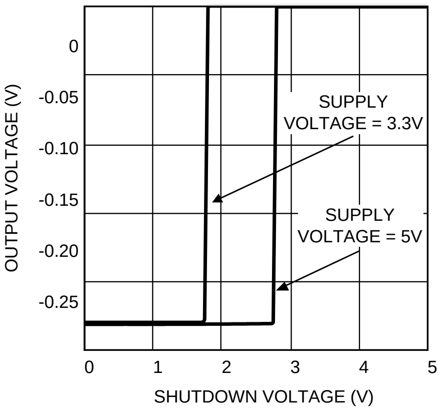


Figure 19. Output voltage vs. Shutdown Voltage

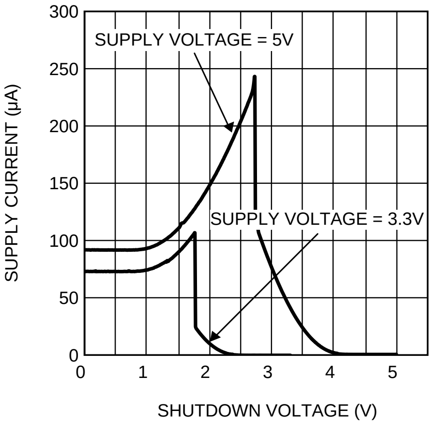


Figure 20. Supply Current vs. Shutdown Voltage

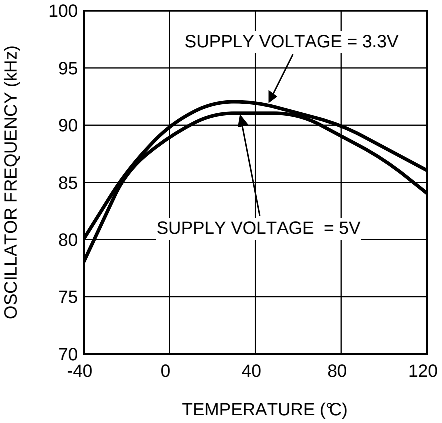


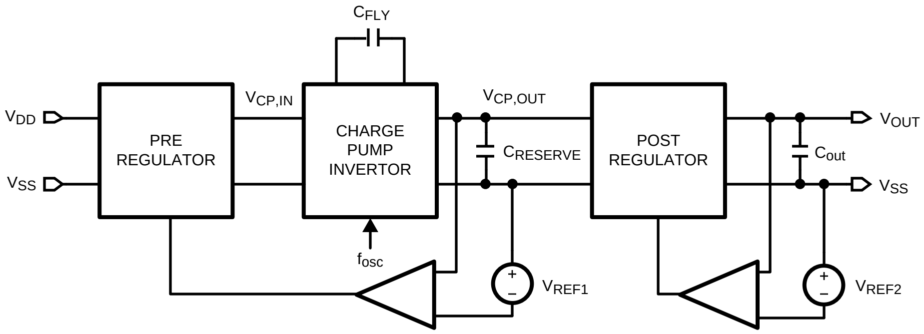
Figure 21. Oscillator Frequency vs. Temperature

7 Detailed Description

7.1 Overview

The LM7705 is a switched capacitor voltage inverter with a low-noise, −0.23-V fixed negative bias output. The part will operate over a supply voltage range of 3 V to 5.25 V. Applying a logical low level to the SD input will activate the part, and generate a fixed −0.23-V output voltage. The part can be disabled; the output is switched to ground level, by applying a logical high level to the SD input of the part.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supply Voltage

The LM7705 will operate over a supply voltage range of 3 V to 5.25 V, and meet the specifications given in the *3.3-V Electrical Characteristics* Table. Supply voltage lower than 3.3 V will decrease performance (The output voltage will shift towards zero, and the current sink capabilities will decrease) A voltage higher than 5.25 V will exceed the *Absolute Maximum Ratings* ratings and therefore damage the part.

7.3.2 Output Voltage and Line Regulation

The fixed and regulated output voltage of −0.23 V has tight limits, as indicated in the *3.3-V Electrical Characteristics* table, to ensure a stable voltage level. The usage of the pre- and post regulator in combination with the charge pump inverter ensures good line regulation of 0.29%/V

7.3.3 Output Current and Load Regulation

The LM7705 can sink currents more than 26 mA, causing an output voltage shift to −200 mV. A specified load-regulation of 0.14% mA/V ensures a minor voltage deviation for load current up to 20 mA.

7.3.4 Quiescent Current

The LM7705 consumes a quiescent current less than 100 µA. Sinking a load current, will result in a current conversion efficiency better than 90%, even for load currents of 1 mA, increasing to 98% for a current of 5mA.

7.4 Device Functional Modes

7.4.1 General Amplifier Application

This section will discuss a general DC coupled amplifier application. First, one of the limitations of a DC coupled amplifier is discussed. This is illustrated with two application examples. A solution is a given for solving this limitation by using the LM7705.

Due to the architecture of the output stage of general amplifiers, the output transistors will saturate. As a result, the output of a general purpose op amp can only swing to a few 100 mV of the supply rails. Amplifiers using CMOS technology do have a lower output saturation voltage. This is illustrated in Figure 22. For example, Texas Instruments' LM7332 can swing to 200 mV to the negative rail, for a 10-kΩ load, over all temperatures.

Device Functional Modes (continued)

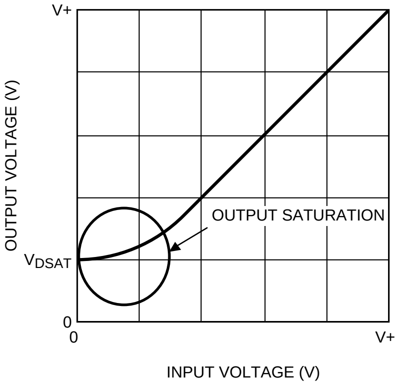


Figure 22. Limitation of the Output of an Amplifier

The introduction of operational amplifiers with output rail-to-rail drive capabilities is a strong improvement and the (output) performance of op amps is for many applications no longer a limiting factor. For example, Texas Instruments' LMP7701 (a typical rail-to-rail op amp), has an output drive capability of only 50 mV over all temperatures for a 10-kΩ load resistance. This is close to the lower supply voltage rail.

However, for true zero output applications with a single supply, the saturation voltage of the output stage is still a limiting factor. This limitation has a negative impact on the functionality of true zero output applications. This is illustrated in Figure 23.

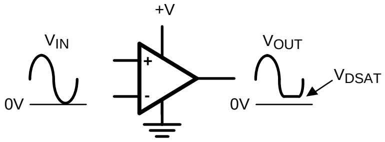


Figure 23. Output Limitation for Single-Supply True Zero Output Application

In the *One-Stage, Single-Supply True Zero Amplifier* section, two applications will be discussed, showing the limitations of the output stage of an op amp in a single supply configuration:

- A single stage true zero amplifier, with a 12-bit ADC back end.
- A dual stage true zero amplifier, with a 12-bit ADC back end.

7.4.1.1 One-Stage, Single-Supply True Zero Amplifier

This application shows a sensor with a DC output signal, amplified by a single supply op amp. The output voltage of the op amp is converted to the digital domain using an Analog to Digital Converter (ADC). Figure 24 shows the basic set-up of this application.

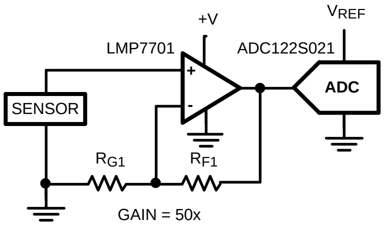


Figure 24. Sensor With DC Output and a Single-Supply Op Amp

Device Functional Modes (continued)

The sensor has a DC output signal that is amplified by the op amp. For an optimal signal-to-noise ratio, the output voltage swing of the op amp must be matched to the input voltage range of the Analog to Digital Converter (ADC). For the high side of the range this can be done by adjusting the gain of the op amp. However, the low side of the range cannot be adjusted and is affected by the output swing of the op amp.

Example:

Assume the output voltage range of the sensor is 0 to 90 mV. The available op amp is a LMP7701, using a 0/+5-V supply voltage, having an output drive of 50 mV from both rails. This results in an output range of 50 mV to 4.95V.

Select two resistors values for R_{G1} and R_{F1} that result in a gain of 50x. The output of the LMP7701 must swing from 0 mV to 4.5 V. The higher value is no problem, however the lower swing is limited by the output of the LM7701 and won't go below 50 mV instead of the desired 0 V, causing a non-linearity in the sensor reading. When using a 12-bit ADC, and a reference voltage of 5 V (having an ADC step size of approximate 1.2 mV), the output saturation results in a loss of the lower 40 quantization levels of the ADCs dynamic range.

7.4.1.2 Two-Stage, Single-Supply True Zero Amplifier

This sensor application produces a DC signal, amplified by a two cascaded op amps, having a single supply. The output voltage of the second op amp is converted to the digital domain. Figure 25 shows the basic setup of this application.

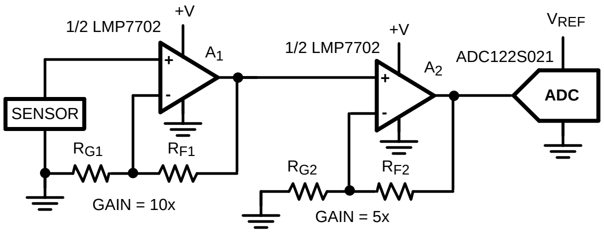


Figure 25. Sensor With DC Output and a 2-Stage, Single-Supply Op Amp

The sensor generates a DC output signal. In this case, a DC coupled, 2-stage amplifier is used. The output voltage swing of the second op amp must me matched to the input voltage range of the Analog to Digital Converter (ADC). For the high side of the range this can be done by adjusting the gain of the op amp. However, the low side of the range can't be adjusted and is affected by the output drive of the op amp.

Example:

Assume; the output voltage range of the sensor is 0 to 90 mV. The available op amp is a LMP7702 (Dual LMP7701 op amp) that can be used for A_1 and A_2. The op amp is using a 0/+5-V supply voltage, having an output drive of 50 mV from both rails. This results in an output range of 50 mV to 4.95 V for each individual amplifier.

Select two resistors values for R_{G1} and R_{F1} that result in a gain of 10x for the first stage (A_1) and a gain of 5x for the second stage (A_2) The output of the A_2 in the LMP7702 must swing from 0V to 4.5 V. This swing is limited by the 2 different factors:

1. The high voltage swing is no problem; however the low voltage swing is limited by the output saturation voltage of A_2 from the LM7702 and will not go below 50 mV instead of the desired 0 V.
2. Another effect has more impact. The output saturation voltage of the first stage will cause an offset for the input of the second stage. This offset of A_1 is amplified by the gain of the second stage (10x in this example), resulting in an output offset voltage of 500mV. This is significantly more that the 50 mV (V_{DSAT}) of A_2.

When using a 12-bit ADC, and a reference voltage of 5 Volt (having an ADC step size of approximate 1.2 mV), the output saturation results in a loss of the lower 400 quantization levels of the ADCs dynamic range. This will cause a major non-linearity in the sensor reading.

Device Functional Modes (continued)

7.4.1.3 Dual-Supply, True Zero Amplifiers

The limitations of the output stage of the op amp, as indicated in both examples, can be omitted by using a dual supply op amp. The output stage of the used op amp can then still swing from 50 mV of the supply rails. However, the functional output range of the op amp is now from ground level to a value near the positive supply rail. Figure 26 shows the output drive of an amplifier in a true zero output voltage application.

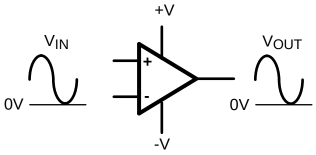


Figure 26. Amplifier Output Drive With a Dual-Supply

Disadvantages of this solution are:
- The usage of a dual-supply instead of a simple single supply is more expensive.
- A dual supply voltage for the op amps requires parts that can handle a larger operating range for the supply voltage. If the op amps used in the current solution cannot handle this, a redesign can be required.

A better solution is to use the LM7705. This low-noise negative bias generator has some major advantages with respect to a dual-supply solution:
- Operates with only a single positive supply, and is therefore a much cheaper solution.
- The LM7705 generates a negative supply voltage of only −0.23 V. This is more than enough to create a True-zero output for most op amps.
- In many applications, this *small* extension of the supply voltage range can be within the abs max rating for many op amps, so an expensive redesign is not necessary.

In the *Typical Application* section, a typical amplifier application will be evaluated. The performance of an amplifier will be measured in a single supply configuration. The results will be compared with an amplifier using a LM7705 supplying a negative voltage to the bias pin.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Functional Description

The LM7705, low-noise negative bias generator, can be used for many applications requiring a fixed negative voltage. A key application for the LM7705 is an amplifier with a true zero output voltage using the original parts, while not exceeding the maximum supply voltage ratings of the amplifier.

The voltage inversion in the LM7705 is achieved using a switched capacitor technique with two external capacitors (C_{FLY} and C_{RES}). An internal oscillator and a switching network transfers charge between the two storage capacitors. This switched capacitor technique is given in Figure 27.

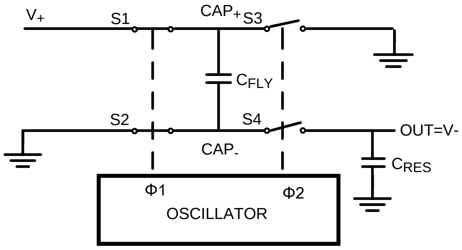


Figure 27. Voltage Inverter

The internal oscillator generates two anti-phase clock signals. Clock 1 controls switches S1 and S2. Clock 2 controls switches S3 and S4. When Switches S1 and S2 are closed, capacitor C_{FLY} is charged to V^+. When switches S3 and S4 are closed (S1 and S2 are open) charge from C_{FLY} is transferred to C_{RES} and the output voltage OUT is equal to $-V^+$.

Due to the switched capacitor technique, a small ripple will be present at the output voltage with a frequency of the oscillator. The magnitude of this ripple will increase for increasing output currents. The magnitude of the ripple can be influenced by changing the values of the used capacitors.

8.1.2 Technical Description

As indicated in *Functional Description*, the main function of the LM7705 is to supply a stabilized negative bias voltage to a load, using only a positive supply voltage. A general block diagram for this charge pump inverter is given in Figure 28. The external power supply and load are added in this diagram as well.

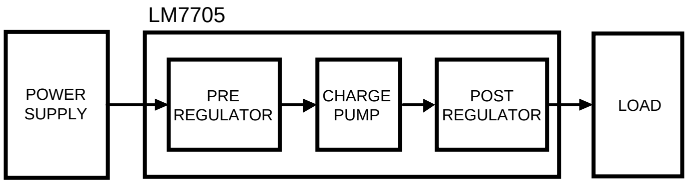


Figure 28. LM7705 Architecture

The architecture given in Figure 28 shows that the LM7705 contains 3 functional blocks:

- Pre-regulator
- Charge pump inverter
- Post-regulator

Application Information (continued)

The output voltage is stabilized by:

- Controlling the power supplied from the power supply to the charge pump input by the pre-regulator
- The power supplied from the charge pump output to the load by the post-regulator.

A more detailed block diagram of the negative bias generator is given in Figure 29. The control of the pre-regulator is based on measuring the output voltage of the charge pump. The goal of the post-regulator is to provide an accurate controlled negative voltage at the output, and acts as a lowpass filter to attenuate the output voltage ripple. The voltage ripple is a result of the switching behavior of the charge pump and is dependent of the output current and the values of the used capacitors.

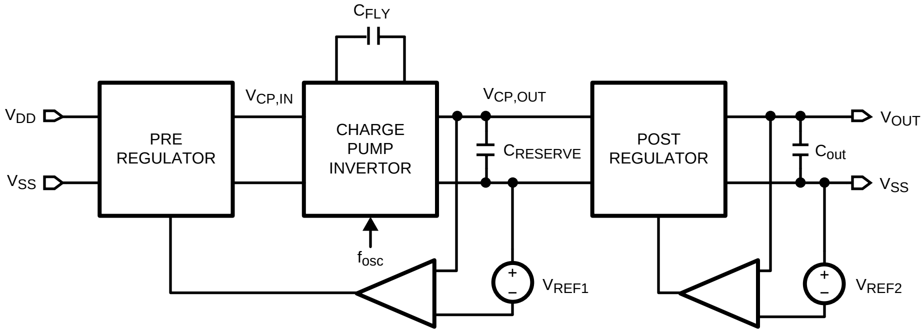


Figure 29. Charge Pump Inverter With Input and Output Control

In *Charge Pump Theory*, a simple equation will be derived that shows the relation between the ripple of the output current, the frequency of the internal clock generator and the value of the capacitor placed at the output of the LM7705.

8.1.3 Charge Pump Theory

This section uses a simplified but realistic equivalent circuit that represents the basic function of the charge pump. The schematic is given in Figure 30.

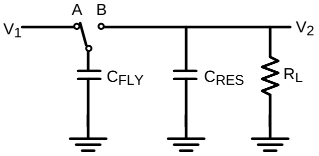


Figure 30. Charge Pump

When the switch is in position A, capacitor C_{FLY} will charge to voltage V_1. The total charge on capacitor C_{FLY} is $Q_1 = C_{FLY} \times V_1$. The switch then moves to position B, discharging C_{FLY} to voltage V_2. After this discharge, the charge on C_{FLY} will be $Q_2 = C_{FLY} \times V_2$. The charge has been transferred from the source V_1 to the output V_2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C_{FLY}(V1 - V2) \tag{1}$$

When the switch changes between A and B at a frequency f, the charge transfer per unit time, or current is:

$$I = f\,\Delta q = f\,C_{FLY}(V1 - V2) \tag{2}$$

The switched capacitor network can be replaced by an equivalent resistor, as indicated in Figure 31.

Application Information (continued)

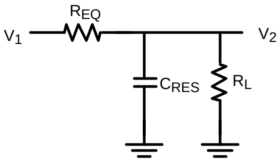


Figure 31. Switched Capacitor Equivalent Circuit

The value of this resistor is dependent on both the capacitor value and the switching frequency as given in Equation 3

$$I = \frac{V1 - V2}{\left(\frac{1}{f\,C_{FLY}}\right)} = \frac{V1 - V2}{R_{EQ}} \tag{3}$$

The value for R_{EQ} can be calculated from Equation 3 and is given in Equation 4

$$R_{EQ} = \left(\frac{1}{f\,C_{FLY}}\right) \tag{4}$$

Equation 4 show that the value for the resistance at an increased internal switching frequency, allows a lower value for the used capacitor.

8.2 Typical Application

This section shows the measurement results of a true zero output amplifier application with an analog to digital converter (ADC) used as back-end. The biasing of the op amp can be done in two ways:

- A single supply configuration
- A single supply in combination with the LM7705, extending the negative supply from ground level to a fixed –0.23 Voltage.

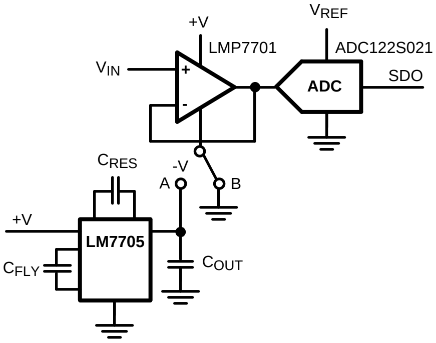


Figure 32. Typical True Zero Output Voltage Application With or Without LM7705

Typical Application (continued)

8.2.1 Design Requirements

The key specifications of the used components are shown in Table 1.

Table 1. Design Parameters

PARAMETERS	EXAMPLE VALUE
SUPPLY VOLTAGE/REFERENCE VOLTAGE	
Supply voltage	5 V
ADC Voltage Reference	5 V
LMP7701	
V_{DSAT} (typical)	18 mV
V_{DSAT} (over temperature)	50 mV
LM7705	
Output voltage ripple	4 mV_{PP}
Output voltage noise	10 mV_{PP}
ADC	
Type	ADC122S021
Resolution	12-bit
Quantization level	5V/4096 = 1.2 mV

8.2.2 Detailed Design Procedure

8.2.2.1 Basic Setup

The basic setup of this true zero output amplifier is given in Figure 32. The LMP7701 op amp is configured as a voltage follower to demonstrate the output limitation, due to the saturation of the output stage. The negative power supply pin of the op amp can be connected to ground level or to the output of the negative bias generator, to demonstrate the V_{DSAT} effect at the output voltage range.

The output voltage of the LMP7701 is converted to the digital domain using an ADC122S021. This is an 12-bit analog to digital converter with a serial data output. Data processing and graphical displaying is done with a computer. The negative power supply pin of the op amp can be connected to ground level or to the output of the negative bias generator, to demonstrate the effect at the output voltage range of the op amp.

8.2.3 Application Curves

The output voltage range of the LMP7701 has been measured, especially the range to ground level. A small DC signal, with a voltage swing of 50 mV_{PP} is applied to the input. The digitized output voltage of the op amp is measured over a given time period, when its negative supply pin is connected to ground level or connected to the output of the LM7705.

Figure 33 shows the digitized output voltage of the op amp when its negative supply pin is connected to ground level. The output of the amplifier saturates at a level of 14 mv (this is in line with the typical value of 18 mV given in the datasheet) The graph shows some fluctuations (1-bit quantization error). Figure 34 show the digitized output voltage of the op amp when its negative supply pin is connected to the output of the LM7705. Again, the graph shows some 1-bit quantization errors caused by the voltage ripple and output noise. In this case the op amps output level can reach the true zero output level.

Figure 33 and Figure 34 show that:

- With a single supply, the output of the amplifier is limited by the V_{DSAT} of the output stage.
- The amplifier can be used as a true zero output using a LM7705.
- The quantization error of the digitized output voltage is caused by the noise and the voltage ripple.
- Using the LM7705 does not increase the quantization error in this set up.

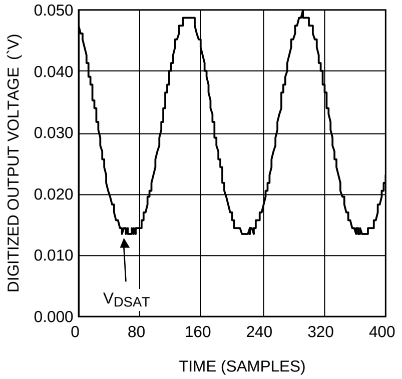


Figure 33. Digitized Output Voltage Without LM7705

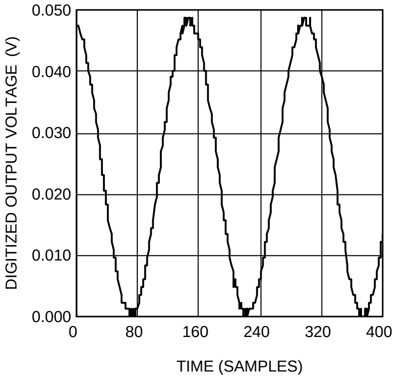


Figure 34. Digitized Output Voltage With LM7705

9 Power Supply Recommendations

To prevent large variations at the V_{DD} pin of the package it is recommended to add a decouple capacitor as close to the pin as possible.

10 Layout

10.1 Layout Guidelines

The LM7705 is a switched capacitor voltage inverter. This means that charge is transferred from different external capacitors, to generate a negative voltage. For this reason the part is very sensitive for contact resistance between the package and external capacitors. TI also recommends to use low ESR capacitors for C_{FLY}, C_{RES} and C_{OUT} in combination with short traces.

The output voltage noise can be suppressed using a small RF capacitor, will a value of, for example, 100 nF.

10.2 Layout Examples

Figure 35 contains a layout example for the LM7705.

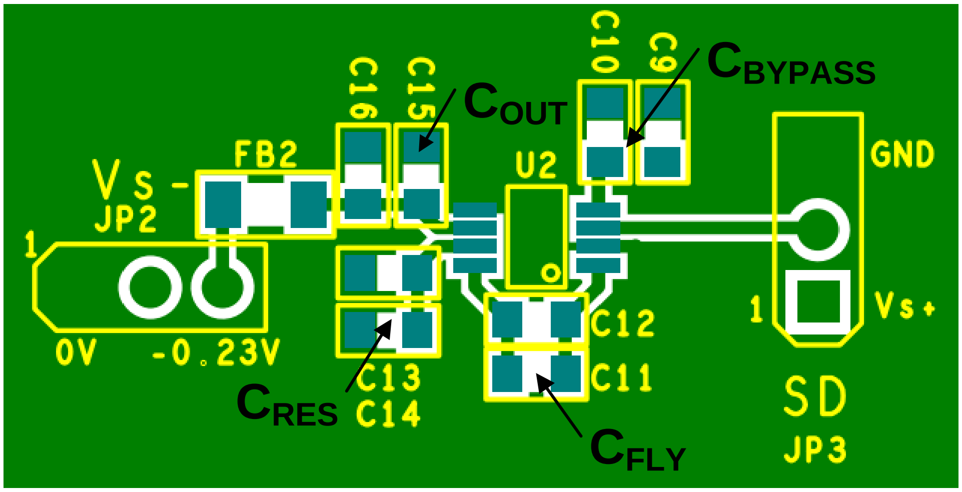


Figure 35. Example PCB Layout: Top layer

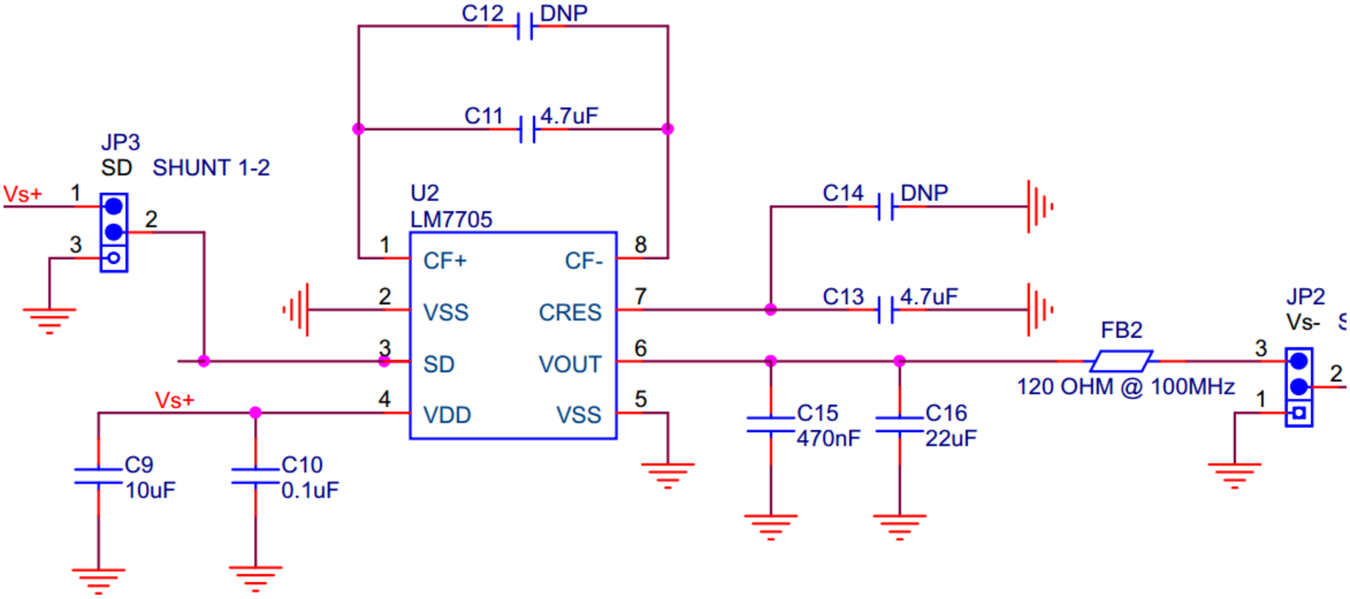


Figure 36. Schematics for Example PCB Layout

11 器件和文档支持

11.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.2 商标

E2E is a trademark of Texas Instruments.
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11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM7705MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	F26A
LM7705MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	F26A
LM7705MME/NOPB	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	F26A
LM7705MME/NOPB.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	F26A
LM7705MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	F26A
LM7705MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	F26A
LM7705MMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	F26A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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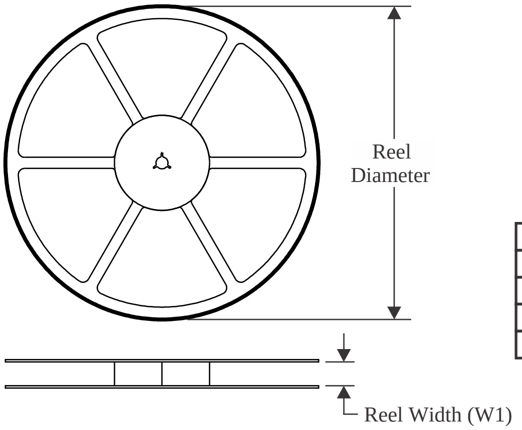
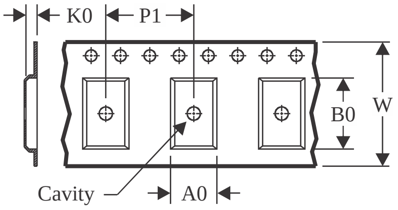
TAPE AND REEL INFORMATION

REEL DIMENSIONS

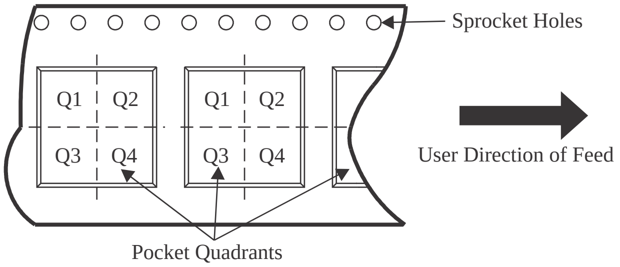


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

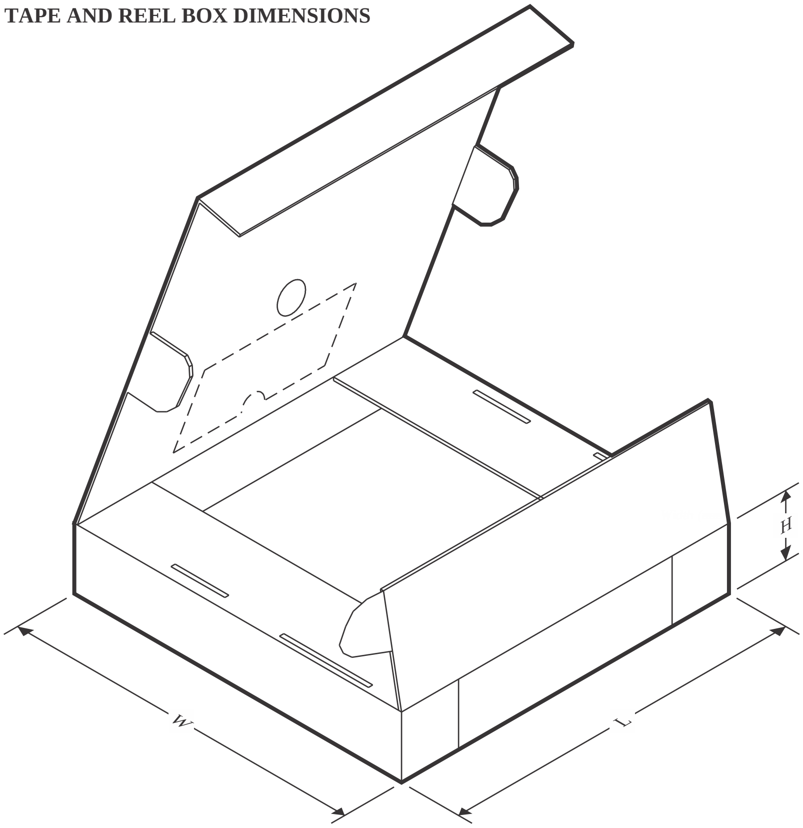
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7705MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7705MME/NOPB	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7705MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

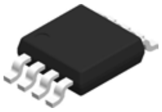
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7705MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM7705MME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0
LM7705MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

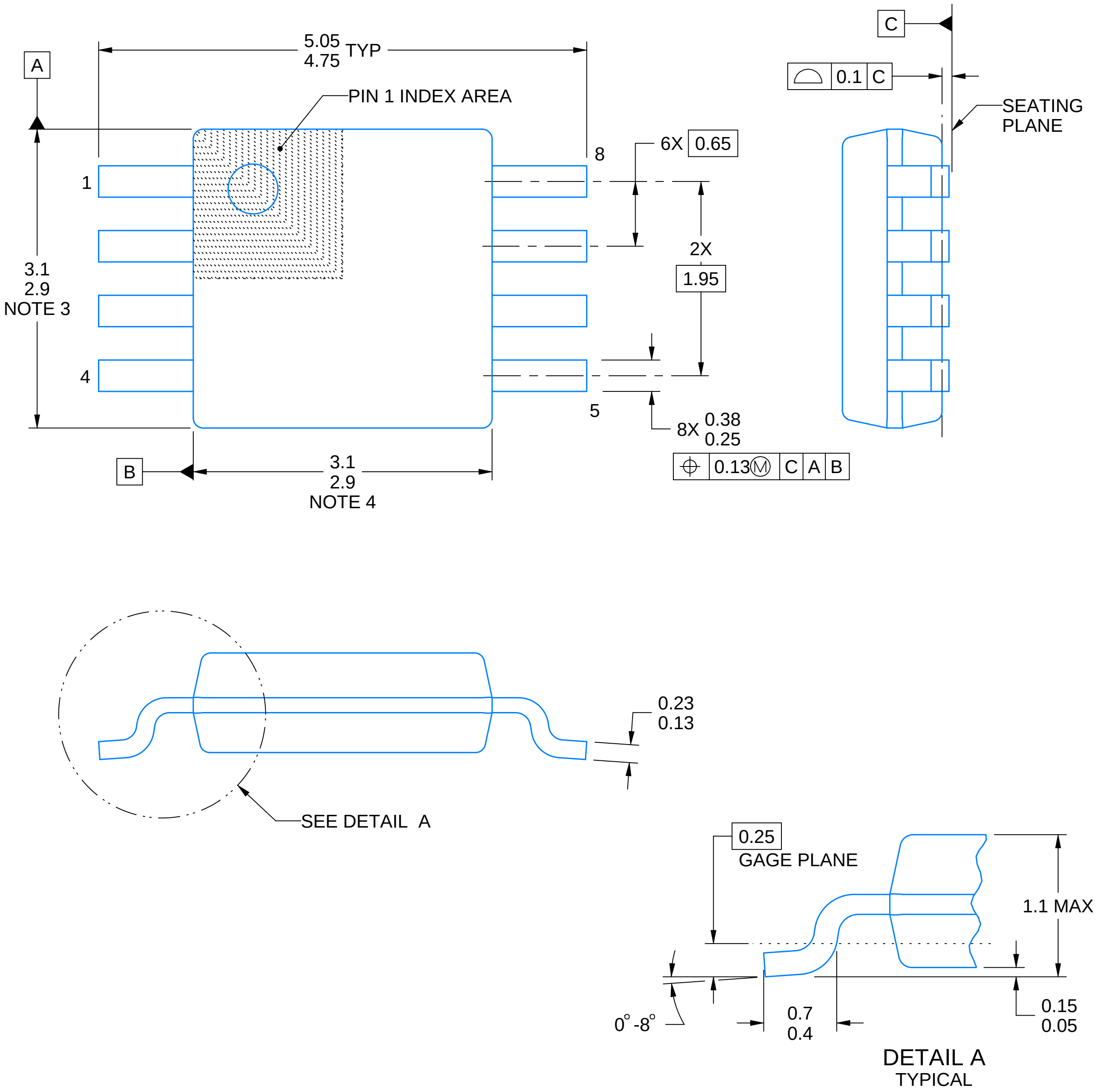
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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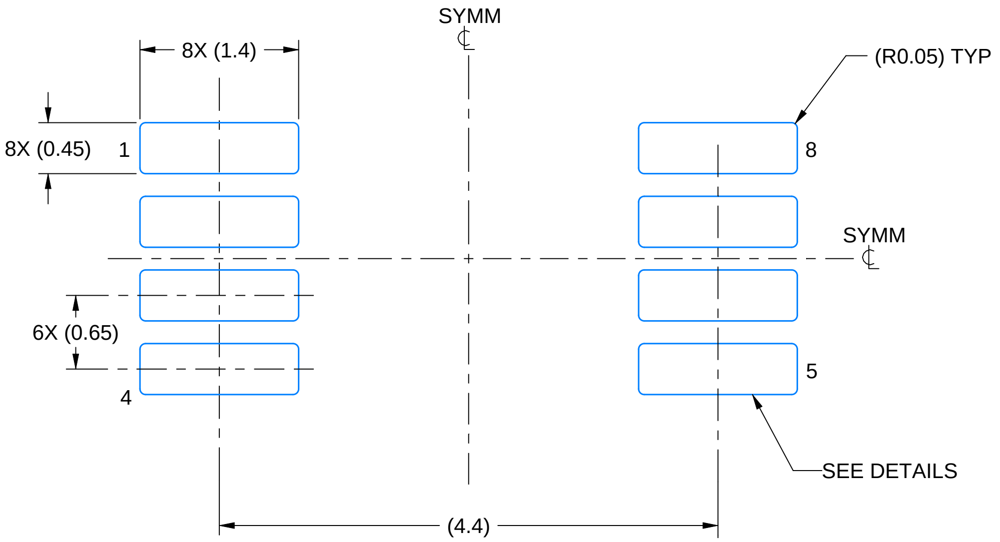
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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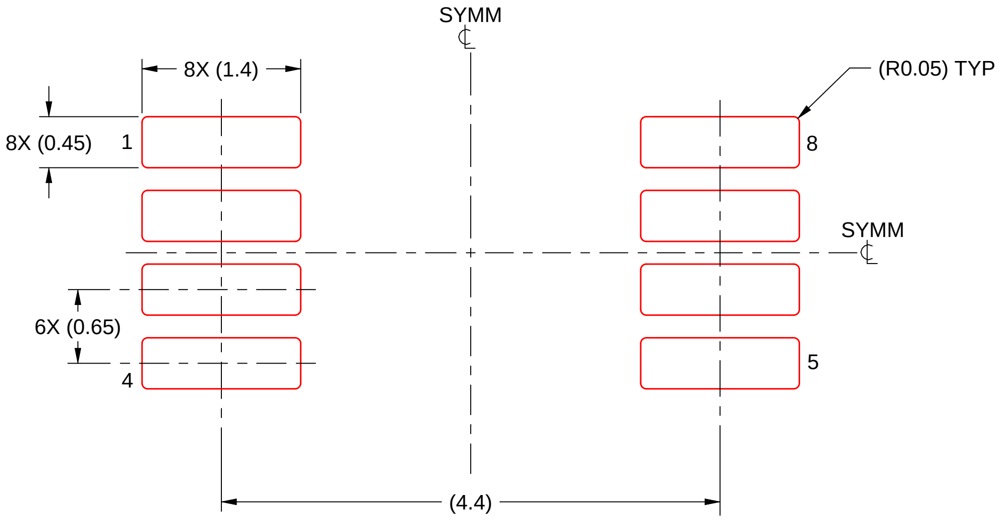
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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