

LM74700D-Q1 汽车类低 I_Q 电池反向保护理想二极管控制器

1 特性

- 具有符合 AEC-Q100 标准的下列特性
 - 器件温度等级 1 :
 - 40°C 至 +125°C 环境工作温度范围
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C4B
- 3.2V 至 65V 输入范围 (3.9V 启动)
- 65V 反向电压额定值
- 适用于外部 N 沟道 MOSFET 的电荷泵
- 20mV 阳极至阴极正向压降调节
- 使能引脚特性
- 1 μ A 关断电流 (EN = 低电平)
- 80 μ A 工作静态电流 (EN = 高电平)
- 2.3A 峰值栅极关断电流
- < 0.75 μ s 响应反向电流阻断
- 采用合适的 TVS 二极管, 符合汽车 ISO7637 瞬态要求
- 采用 8 引脚 SOIC 封装

2 应用

- 汽车 ADAS 系统 - 摄像头
- 汽车信息娱乐系统 - 音响主机
- 工业工厂自动化 - PLC
- 企业电源
- 用于冗余电源的有源 OR-ing

3 说明

LM74700D-Q1 是一款符合汽车 AEC Q100 标准的理想二极管控制器, 可与外部 N 沟道 MOSFET 配合工作, 作为理想二极管整流器利用 20mV 正向压降实现低损耗反极性保护。3.2V 至 65V 的宽电源输入范围可实现对众多常用直流总线电压 (例如 12V、24V 和 48V 汽车电池系统) 的控制。3.2V 输入电压支持可满足汽车系统中严苛的冷启动要求。该器件可耐受低至 -65V 的负电源电压, 并提供负载保护。

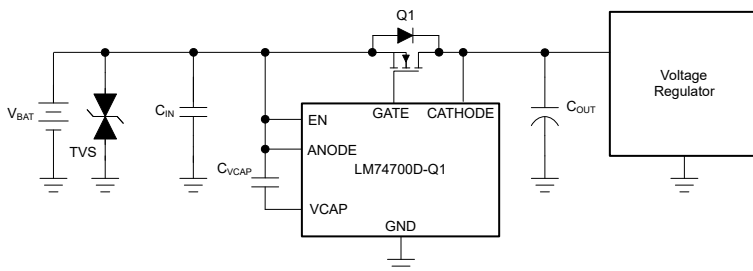
该器件通过控制 MOSFET 的栅极将正向压降调节至 20mV。该调节方案可在反向电流事件中支持 MOSFET 平稳关断, 并确保零直流反向电流。该器件能够快速 (< 0.75 μ s) 响应反向电流阻断, 专为在 ISO7637 脉冲测试以及电源故障和输入微短路条件下要求保持输出电压的系统而设计。

LM74700D-Q1 控制器可提供适用于外部 N 沟道 MOSFET 的电荷泵栅极驱动器。LM74700D-Q1 的高电压额定值有助于简化满足 ISO7637 汽车保护测试标准的系统设计。当使能引脚处于低电平时, 控制器关闭, 消耗大约 1 μ A 的电流。

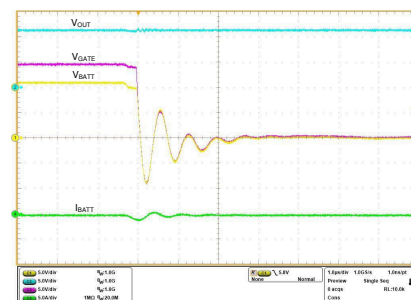
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
LM74700D-Q1	D (SOIC, 8)	5 mm x 3.9 mm

- 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。
- 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



典型应用原理图



输入短路期间的反向电流阻断



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
September 2023	*	Initial release

5 Pin Configuration and Functions

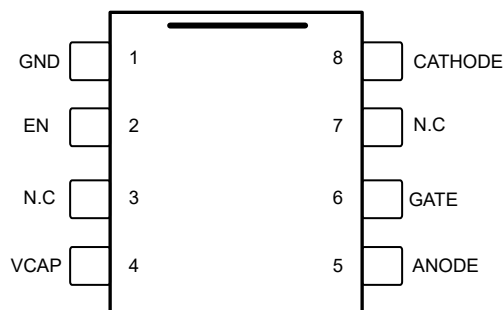


图 5-1. D Package, 8-Pin SOIC Top View

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	GND	G	Ground pin.
2	EN	I	Enable pin. Can be connected to ANODE for always ON operation.
3	N.C	—	No connection
4	VCAP	O	Charge pump output. Connect to external charge pump capacitor.
5	ANODE	I	Anode of the diode and input power. Connect to the source of the external N-channel MOSFET.
6	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
7	N.C	—	No connection
8	CATHODE	I	Cathode of the diode. Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input Pins	ANODE to GND	– 65	70	V
	EN to GND, $V_{(ANODE)} > 0$ V	– 0.3	70	V
	EN to GND, $V_{(ANODE)} \leq 0$ V	$V_{(ANODE)}$	$(70 + V_{(ANODE)})$	V
Output Pins	GATE to ANODE	– 0.3	15	V
	VCAP to ANODE	– 0.3	15	V
Output to Input Pins	CATHODE to ANODE	– 5	75	V
Operating junction temperature ⁽²⁾		– 40	150	°C
Storage temperature, T_{stg}		– 40	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	±750	
		Other pins	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
Input Pins	ANODE to GND	– 60		65	V
	CATHODE to GND			65	
	EN to GND	– 60		65	
Input to Output pins	ANODE to CATHODE	– 70			V
External capacitance	ANODE	22			nF
	CATHODE, VCAP to ANODE	0.1			μF
External MOSFET max V_{GS} rating	GATE to ANODE	15			V
T_J	Operating junction temperature range ⁽²⁾	– 40		150	°C

- (1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM74700D-Q1	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $V_{(ANODE)} = 12\text{ V}$, $C_{(VCAP)} = 0.1\text{ }\mu\text{F}$, $V_{(EN)} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ANODE} SUPPLY VOLTAGE						
$V_{(ANODE)}$	Operating input voltage		4		65	V
$V_{(ANODE\ POR)}$	VANODE POR Rising threshold				3.9	V
	VANODE POR Falling threshold		2.2	2.8	3.1	V
$V_{(ANODE\ POR(Hys))}$	VANODE POR Hysteresis		0.44		0.67	V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)} = 0\text{ V}$		0.9	1.5	μA
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)} = 0\text{ V}$, $V_{(ANODE)} = 48\text{ V}$		4.2		μA
$I_{(Q)}$	Operating Quiescent Current			80	130	μA
$I_{(Q)}$	Operating Quiescent Current	$V_{(ANODE)} = 48\text{ V}$		110		μA
ENABLE INPUT						
$V_{(EN_IL)}$	Enable input low threshold		0.5	0.9	1.22	V
$V_{(EN_IH)}$	Enable input high threshold		1.06	2	2.6	
$V_{(EN_Hys)}$	Enable Hysteresis		0.52		1.35	V
$I_{(EN)}$	Enable sink current	$V_{(EN)} = 12\text{ V}$		3	5	μA
V_{ANODE} to V_{CATHODE}						
$V_{(AK\ REG)}$	Regulated Forward $V_{(AK)}$ Threshold		13	20	29	mV
$V_{(AK)}$	$V_{(AK)}$ threshold for full conduction mode		34	50	57	mV
$V_{(AK\ REV)}$	$V_{(AK)}$ threshold for reverse current blocking		-17	-11	-2	mV
Gm	Regulation Error AMP Transconductance ⁽¹⁾		1200	1800	3100	$\mu\text{A/V}$
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(ANODE)} - V_{(CATHODE)} = 100\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$	3	11		mA
	Peak sink current	$V_{(ANODE)} - V_{(CATHODE)} = -20\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$		2370		mA
	Regulation max sink current	$V_{(ANODE)} - V_{(CATHODE)} = 0\text{ V}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$	6	26		μA
RDS_{ON}	discharge switch RDS_{ON}	$V_{(ANODE)} - V_{(CATHODE)} = -20\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 100\text{ mV}$	0.4		2	Ω
CHARGE PUMP						

6.5 Electrical Characteristics (续)

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $V_{(\text{ANODE})} = 12\text{ V}$, $C_{(\text{VCAP})} = 0.1\text{ }\mu\text{F}$, $V_{(\text{EN})} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(\text{VCAP})}$	Charge Pump source current (Charge pump on)	$V_{(\text{VCAP})} - V_{(\text{ANODE})} = 7\text{ V}$	162	300	600	μA
	Charge Pump sink current (Charge pump off)	$V_{(\text{VCAP})} - V_{(\text{ANODE})} = 14\text{ V}$		5	10	μA
$V_{(\text{VCAP})} - V_{(\text{ANODE})}$	Charge pump voltage at $V_{(\text{ANODE})} = 3.2\text{ V}$	$I_{(\text{VCAP})} \leq 30\text{ }\mu\text{A}$	8			V
	Charge pump turn on voltage		10.8	12.1	12.9	V
	Charge pump turn off voltage		11.6	13	13.9	V
	Charge Pump Enable comparator Hysteresis		0.54	0.9	1.36	V
$V_{(\text{VCAP UVLO})}$	$V_{(\text{VCAP})} - V_{(\text{ANODE})}$ UV release at rising edge	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$	5.8	6.6	7.7	V
	$V_{(\text{VCAP})} - V_{(\text{ANODE})}$ UV threshold at falling edge	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$	5.11	5.68	6	V
CATHODE						
$I_{(\text{CATHODE})}$	CATHODE sink current	$V_{(\text{ANODE})} = 12\text{ V}$, $V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$		1.7	2	μA
		$V_{(\text{ANODE})} = 48\text{ V}$, $V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$		1.7		μA
		$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$		1.2	2.2	μA
		$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$, $V_{(\text{ANODE})} = 48\text{ V}$		3.5		μA
		$V_{(\text{ANODE})} = -12\text{ V}$, $V_{(\text{CATHODE})} = 12\text{ V}$		1.25	2.06	μA

(1) Parameter specified by design and characterization

6.6 Switching Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $V_{(\text{ANODE})} = 12\text{ V}$, $C_{(\text{VCAP})} = 0.1\text{ }\mu\text{F}$, $V_{(\text{EN})} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to Gate Turn On delay	$V_{(\text{VCAP})} > V_{(\text{VCAP UVLOR})}$		75	110	μs
$t_{\text{Reverse delay}}$	Reverse voltage detection to Gate Turn Off delay	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$ to -100 mV		0.45	0.75	μs
$t_{\text{Reverse delay}}$	Reverse voltage detection to Gate Turn Off delay	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$ to -100 mV $V_{(\text{ANODE})} = 48\text{ V}$		0.45		μs
$t_{\text{Forward recovery}}$	Forward voltage detection to Gate Turn On delay	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$ to 700 mV		1.4	2.6	μs
$t_{\text{Forward recovery}}$	Forward voltage detection to Gate Turn On delay	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$ to 700 mV $V_{(\text{ANODE})} = 48\text{ V}$		1.4		μs

7 Typical Characteristics

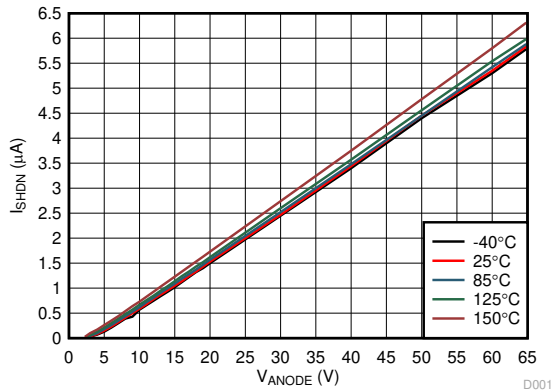


图 7-1. Shutdown Supply Current vs Supply Voltage

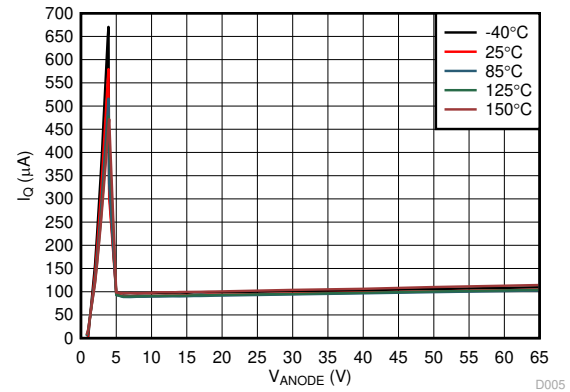


图 7-2. Operating Quiescent Current vs Supply Voltage

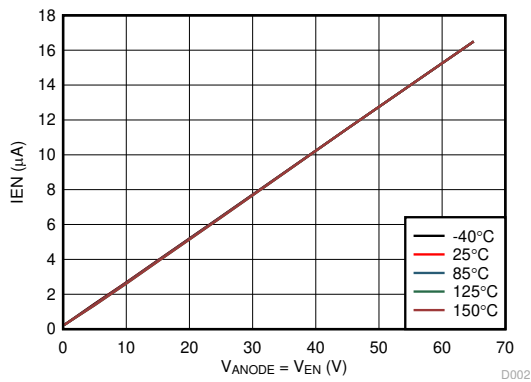


图 7-3. Enable Sink Current vs Supply Voltage

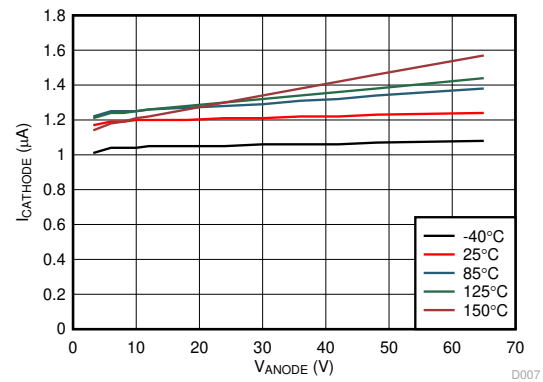


图 7-4. CATHODE Sink Current vs Supply Voltage

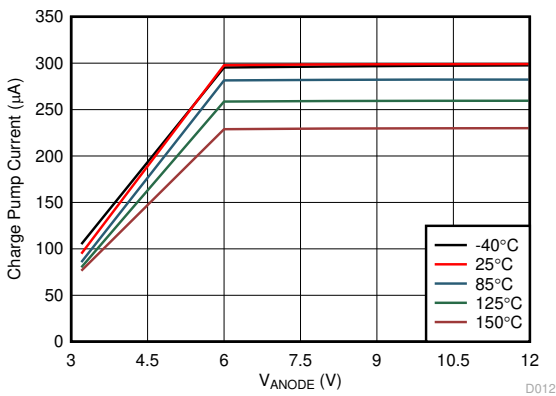


图 7-5. Charge Pump Current vs Supply Voltage at VCAP = 6 V

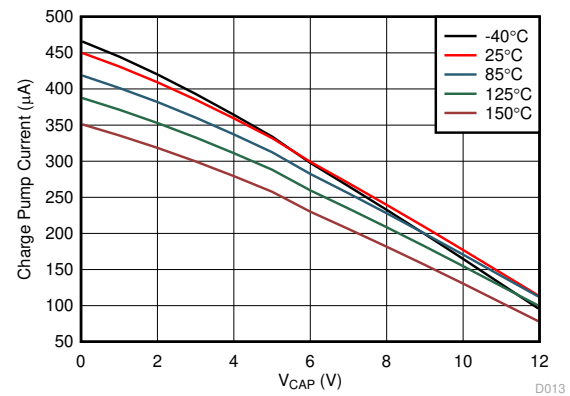


图 7-6. Charge Pump V-I Characteristics at ANODE >= 12 V

7 Typical Characteristics (continued)

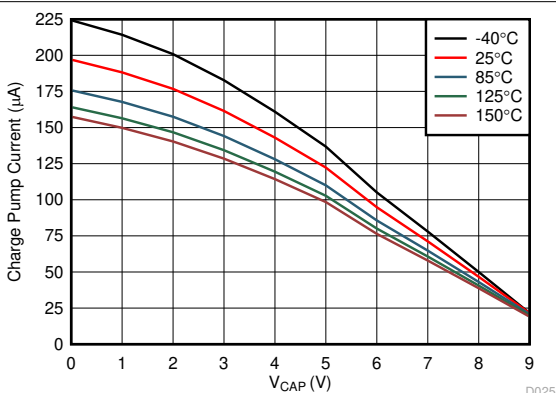


图 7-7. Charge Pump V-I Characteristics at ANODE = 3.2 V

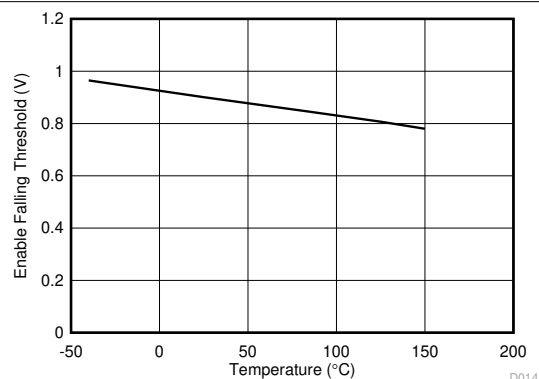


图 7-8. Enable Falling Threshold vs Temperature

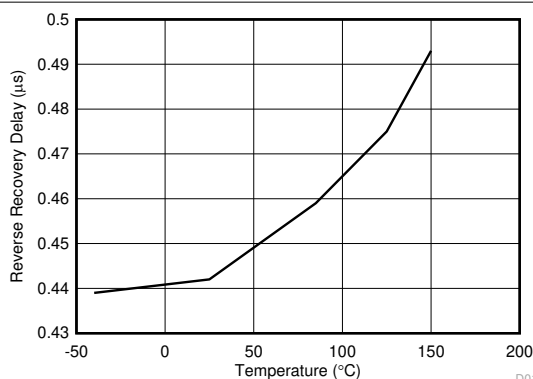


图 7-9. Reverse Current Blocking Delay vs Temperature

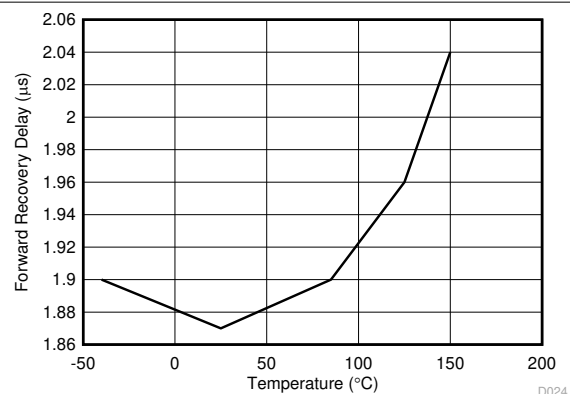


图 7-10. Forward Recovery Delay vs Temperature

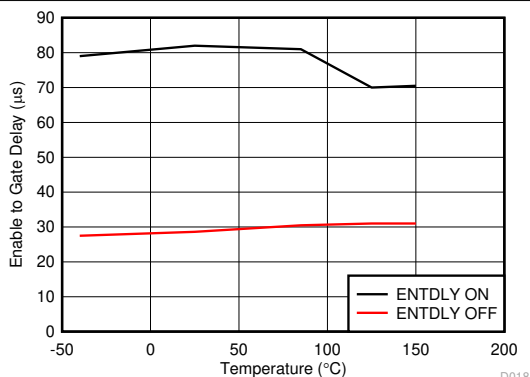


图 7-11. Enable to Gate Delay vs Temperature

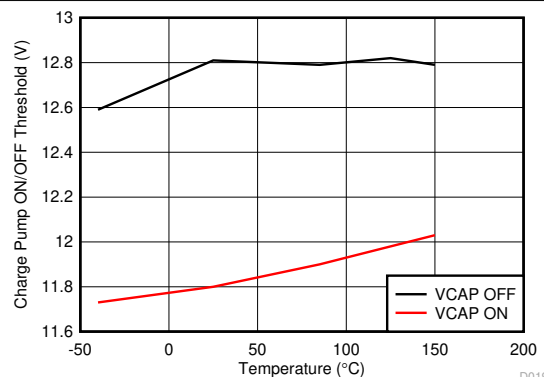


图 7-12. Charge Pump ON/OFF Threshold vs Temperature

7 Typical Characteristics (continued)

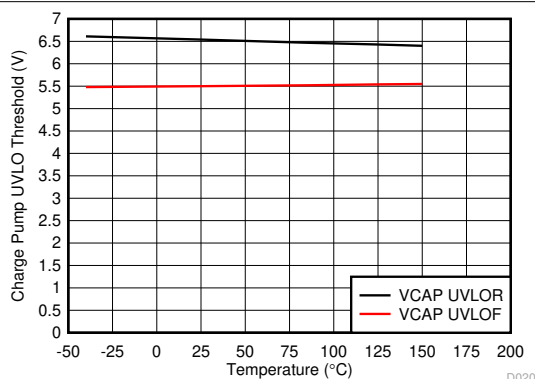


图 7-13. Charge Pump UVLO Threshold vs Temperature

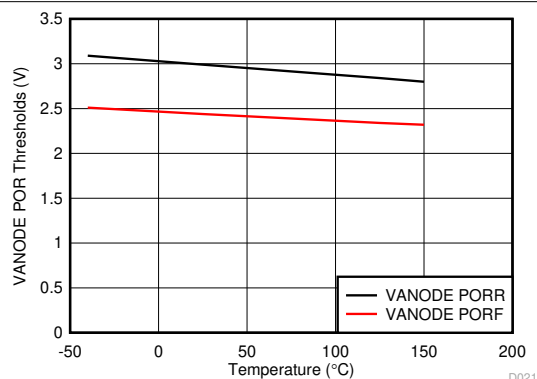


图 7-14. ANODE POR Threshold vs Temperature

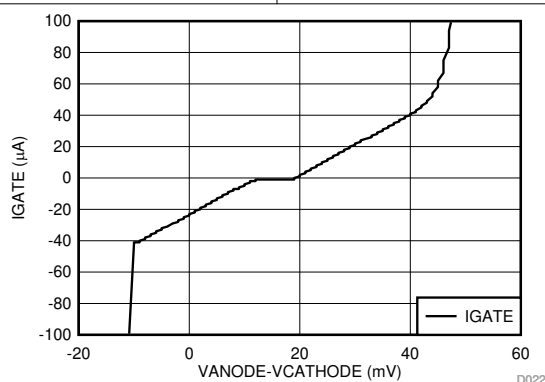


图 7-15. Gate Current vs Forward Voltage Drop

8 Parameter Measurement Information

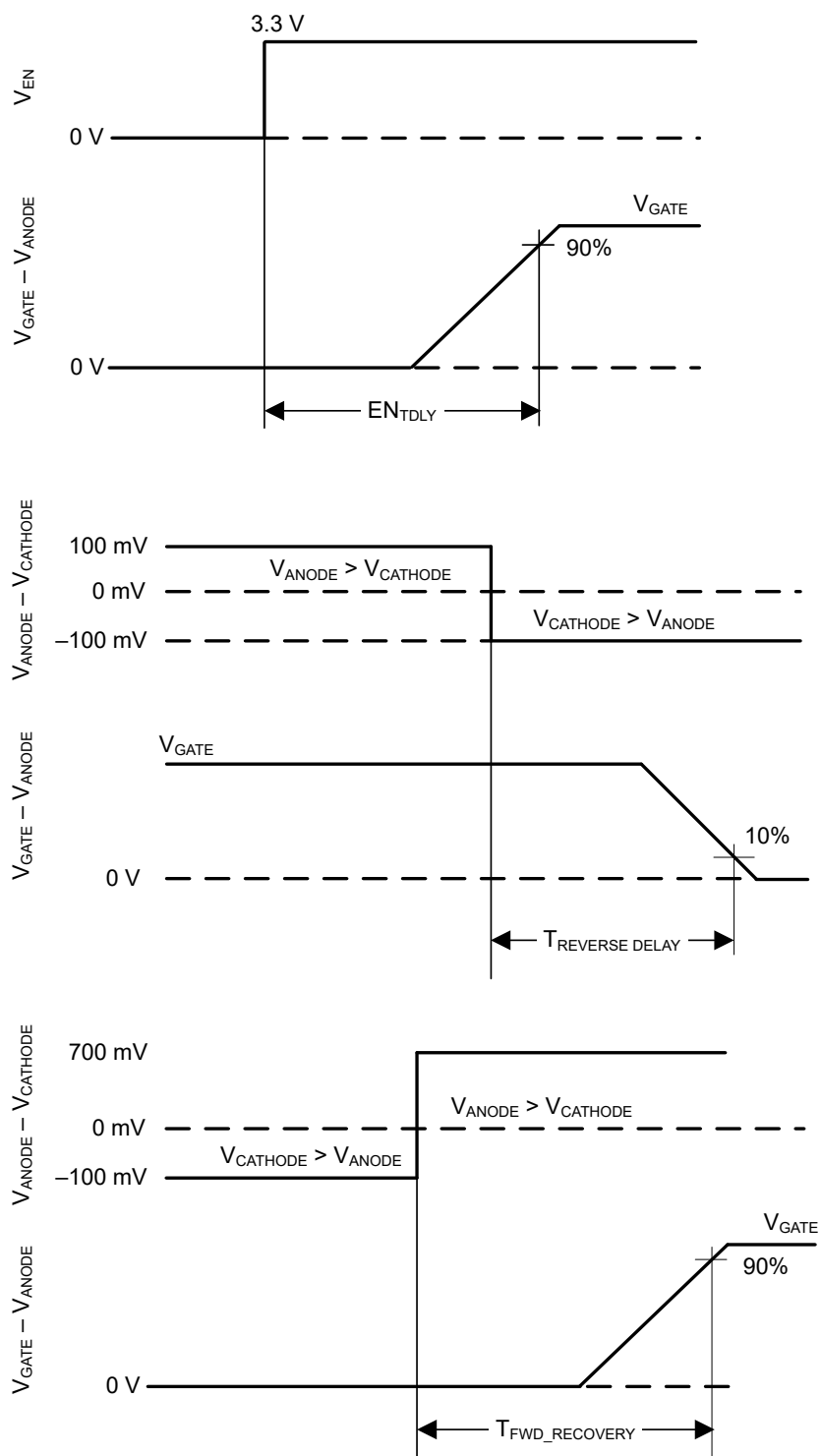


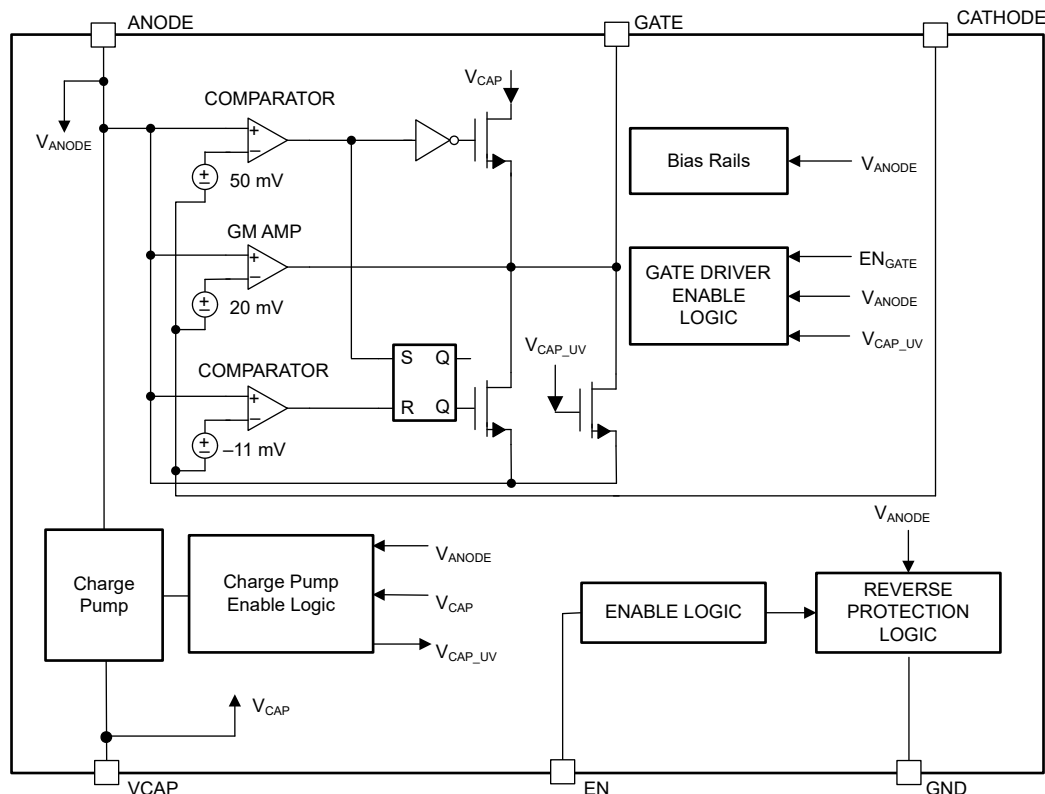
图 8-1. Timing Waveforms

9 Detailed Description

9.1 Overview

The LM74700D-Q1 [ideal diode controller](#) has all the features necessary to implement an efficient and fast reverse polarity protection circuit or be used in an OR-ing configuration while minimizing the number of external components. This easy to use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes such as a P-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate drive voltage of approximately 15 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20 mV. This closed loop regulation scheme enables graceful turn-off of the MOSFET during a reverse current event and make sure of zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below -11 mV , resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN, is available to place the LM74700D-Q1 in shutdown mode disabling the N-Channel MOSFET and minimizing the quiescent current.

9.2 功能方框图



9.3 Feature Description

9.3.1 Input Voltage

The ANODE pin is used to power the LM74700D-Q1 internal circuitry, typically drawing 80 μA when enabled and 1 μA when disabled. If the ANODE pin voltage is greater than the POR Rising threshold, then LM74700D-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65 V to -65 V, allowing the LM74700D-Q1 to withstand negative voltage transients.

9.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and ANODE pins to provide energy to turn on the external MOSFET. For the charge pump to supply current to the external capacitor the EN pin, voltage must be above the specified input high threshold, $V_{(EN_IH)}$. When enabled the charge pump sources a charging current of 300- μA typical. If EN pins is pulled low, then the charge pump remains disabled. To make sure that the external MOSFET can be driven above the specified threshold voltage, the VCAP to ANODE voltage must be above the under voltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled.

$$T_{DRV_EN} = 75\mu\text{s} + C_{VCAP} \times \frac{V_{VCAP_UVLOR}}{300\mu\text{A}} \quad (1)$$

where

- C_{VCAP} is the charge pump capacitance connected across ANODE and VCAP pins
- $V_{VCAP_UVLOR} = 6.6\text{ V}$ (typical)

To remove any chatter on the gate drive, approximately 900 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to ANODE voltage reaches 13 V, typically, at which point the charge pump is disabled decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCAP to ANODE voltage is below 12.1 V typically at which point the charge pump is enabled. The voltage between VCAP and ANODE continue to charge and discharge between 12.1 V and 13 V as shown in 图 9-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74700D-Q1 is reduced. When the charge pump is disabled, it sinks 5- μA typical.

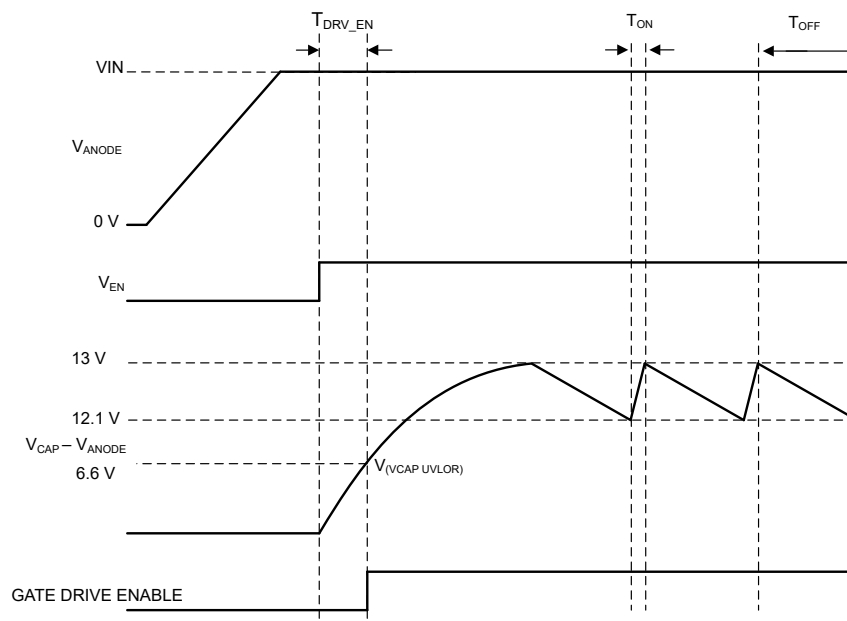


图 9-1. Charge Pump Operation

9.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are three defined modes of operation that the gate driver operates under forward regulation, full conduction mode and reverse current protection, according to the ANODE to CATHODE voltage. Forward regulation mode, full conduction mode and reverse current protection mode are described in more detail in the [Regulated conduction Mode](#), [Full Conduction Mode](#) and [Reverse Current Production Mode](#) sections. 图 9-2 depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74700D-Q1. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is -11 mV.

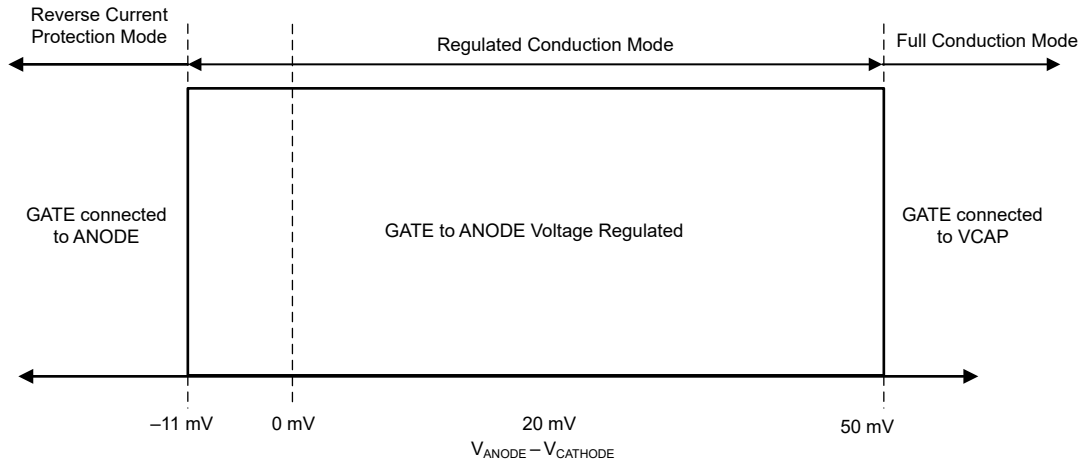


图 9-2. Gate Driver Mode Transitions

Before the gate driver is enabled, the following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to ANODE voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than ANODE POR Rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. After these conditions are achieved, the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

9.3.4 Enable

The LM74700D-Q1 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in [Gate Driver](#) and [Charge Pump](#) sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74700D-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as -65 V. This ability allows for the EN pin to be connected directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 3 μ A pulls the EN pin low and disables the device.

9.4 Device Functional Modes

9.4.1 Shutdown Mode

The LM74700D-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74700D-Q1 enters low I_Q operation with the ANODE pin only sinking 1 μ A. When the LM74700D-Q1 is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET body diode.

9.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE voltage of the LM74700D-Q1. Each of the three modes is described in the [Regulated Conduction Mode](#), [Full Conduction Mode](#), and [Reverse Current Protection Mode](#) sections.

9.4.2.1 Regulated Conduction Mode

For the LM74700D-Q1 to operate in regulated conduction mode, the gate driver must be enabled as described in the [Gate Driver](#) section, and the current from source to drain of the external MOSFET must be within the range to result in an ANODE to CATHODE voltage drop of -11 mV to 50 mV . During forward regulation mode, the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. This closed loop regulation scheme enables graceful turn-off of the MOSFET at very light loads and makes sure of zero DC reverse current flow.

9.4.2.2 Full Conduction Mode

For the LM74700D-Q1 to operate in full conduction mode, the gate driver must be enabled as described in the [Gate Driver](#) section, and the current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50-mV typical. If these conditions are achieved the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFET's $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

9.4.2.3 Reverse Current Protection Mode

For the LM74700D-Q1 to operate in reverse current protection mode, the gate driver must be enabled as described in the [Gate Driver](#) section, and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is typically less than -11 mV , reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

10 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LM74700D-Q1 is used with an N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in 图 10-1 where the LM74700D-Q1 is used in series with a battery to drive the MOSFET Q1. The TVS is not required for the LM74700D-Q1 to operate, but is used to clamp the positive and negative voltage surges. The output capacitor C_{OUT} is recommended to protect the immediate output voltage collapse as a result of line disturbance.

10.2 Typical Application

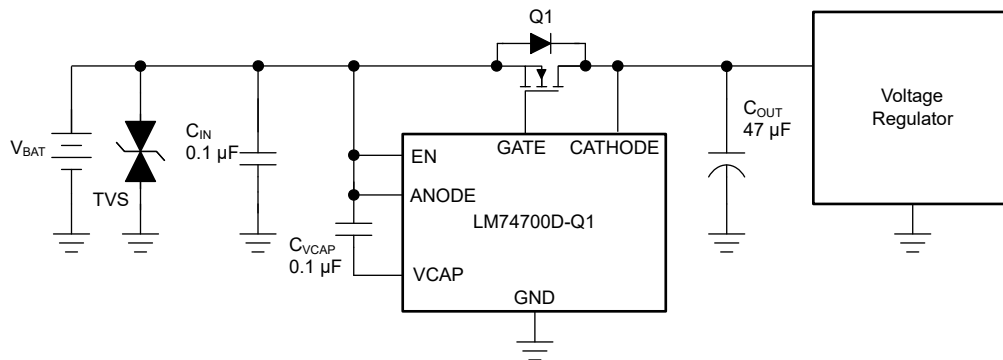


图 10-1. Typical Application Circuit

10.2.1 Design Requirements

A design example, with system design parameters listed in 表 10-1 is presented.

表 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V Battery, 12-V Nominal with 3.2-V Cold Crank and 35-V Load Dump
Output voltage	3.2 V during Cold Crank to 35-V Load Dump
Output current range	3-A Nominal, 5-A Maximum
Output capacitance	1-μF Minimum, 47-μF Typical Holdup Capacitance
Automotive EMC Compliance	ISO 7637-2 and ISO 16750-2

10.2.2 Detailed Design Procedure

10.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current

10.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current I_D , the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum source current through body diode and the drain-to-source On resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D , rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This includes any anticipated fault conditions. TI recommends to use MOSFETs with voltage rating up to 60-V maximum with the LM74700D-Q1 because anode-cathode maximum voltage is 65 V. The maximum V_{GS} LM74700D-Q1 can drive is 13 V, so select a MOSFET with 15-V minimum V_{GS} . If a MOSFET with < 15-V V_{GS} rating is selected, a Zener diode can be used to clamp V_{GS} to safe level. During start-up, inrush current flows through the body diode to charge the bulk hold-up capacitors at the output. The maximum source current through the body diode must be higher than the inrush current that can be seen in the application.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ can not be beneficial always. Higher $R_{DS(ON)}$ provides increased voltage information to the LM74700D-Q1 reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. TI recommends to operate the MOSFET in regulated conduction mode during nominal load conditions and select $R_{DS(ON)}$ such that at nominal operating current, forward voltage drop V_{DS} is close to 20-mV regulation point and not more than 50 mV.

As a guideline, TI suggests to choose $(20 \text{ mV} / I_{Load(Nominal)}) \leq R_{DS(ON)} \leq (50 \text{ mV} / I_{Load(Nominal)})$.

MOSFET manufacturers usually specify $R_{DS(ON)}$ at 4.5-V V_{GS} and 10-V V_{GS} . $R_{DS(ON)}$ increases drastically below 4.5-V V_{GS} and $R_{DS(ON)}$ is highest when V_{GS} is close to MOSFET V_{th} . For stable regulation at light load conditions, TI recommends to operate the MOSFET close to 4.5-V V_{GS} , that is, much higher than MOSFET gate threshold voltage. TI recommends to choose MOSFET gate threshold voltage V_{th} of 2-V to 2.5-V maximum. Choosing a lower V_{th} MOSFET also reduces the turn-ON time.

Based on the design requirements, preferred MOSFET ratings are:

- 60-V $V_{DS(MAX)}$ and ± 20 -V $V_{GS(MAX)}$
- $R_{DS(ON)}$ at 3-A nominal current: $(20 \text{ mV} / 3 \text{ A}) \leq R_{DS(ON)} \leq (50 \text{ mV} / 3 \text{ A}) = 6.67 \text{ m}\Omega \leq R_{DS(ON)} \leq 16.67 \text{ m}\Omega$
- MOSFET gate threshold voltage V_{th} : 2-V maximum

DMT6007LFG MOSFET from Diodes Inc. is selected to meet this 12-V reverse battery protection design requirements and is rated at:

- 60-V $V_{DS(MAX)}$ and ± 20 -V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 6.5-m Ω typical and 8.5-m Ω maximum rated at 4.5-V V_{GS}
- MOSFET V_{th} : 2-V maximum

Consider thermal resistance of the MOSFET against the expected maximum power dissipation in the MOSFET to make sure that the junction temperature (T_J) is well controlled.

10.2.2.3 Charge Pump VCAP, Input and Output Capacitance

Minimum required capacitance for charge pump VCAP and input and output capacitance are:

- VCAP: Minimum 0.1 μF is required; recommended value of VCAP (μF) $\geq 10 \times C_{ISS(MOSFET)}(\mu\text{F})$
- C_{IN} : minimum 22 nF of input capacitance
- C_{OUT} : minimum 100 nF of output capacitance

10.2.3 Selection of TVS Diodes for 12-V Battery Protection Applications

TVS diodes are used in automotive systems for protection against transients. In the 12-V battery protection application circuit shown in 图 10-2, a bi-directional TVS diode is used to protect from positive and negative

transient voltages that occur during normal operation of the car and these transient voltage levels and pulses are specified in ISO 7637-2 and ISO 16750-2 standards.

There are two important specifications are breakdown voltage and clamping voltage of the TVS. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a Zener diode and is specified at a low current value typical 1 mA and the breakdown voltage must be higher than worst case steady state voltages seen in the system. The breakdown voltage of the TVS+ must be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74700D-Q1 (65 V). The breakdown voltage of TVS – must be beyond than maximum reverse battery voltage – 16 V, so that the TVS – is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. TVS diodes are meant to clamp transient pulses and must not interfere with steady state operation. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to – 150 V with a generator impedance of 10 Ω . This translates to 15 A flowing through the TVS – and the voltage across the TVS is close to the clamping voltage.

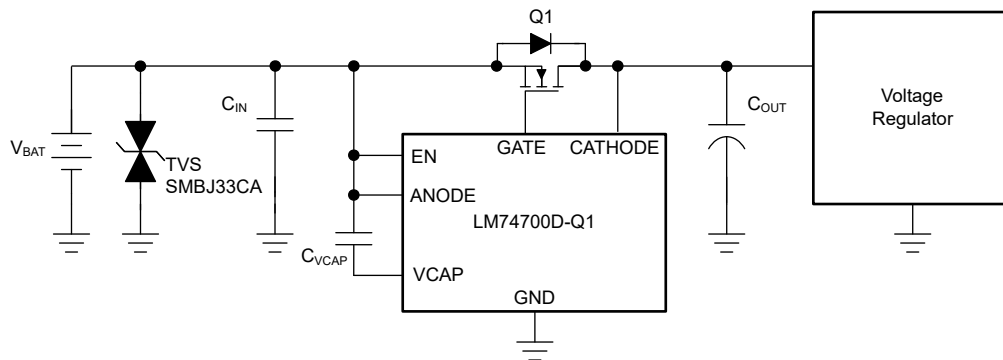


图 10-2. Typical 12-V Battery Protection With Single Bi-Directional TVS

The next criterion is that the absolute maximum rating of Anode to Cathode reverse voltage of the LM74700D-Q1 (– 75 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, a 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

In case of ISO 7637-2 pulse 1, the anode of LM74700D-Q1 is pulled down by the ISO pulse and clamped by TVS –. The MOSFET is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS – must not exceed $(60 \text{ V} - 16) \text{ V} = -44 \text{ V}$.

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at – 44 V with 15 A of peak surge current as shown in 图 10-5 and it meets the clamping voltage $\leq 44 \text{ V}$.

SMBJ series of TVS are rated up to 600-W peak pulse power levels. This rating is sufficient for ISO 7637-2 pulses and suppressed load dump (ISO-16750-2 pulse B).

10.2.4 Selection of TVS Diodes and MOSFET for 24-V Battery Protection Applications

The typical 24-V battery protection application circuit shown in 图 10-3 uses two uni-directional TVS diodes to protect from positive and negative transient voltages.

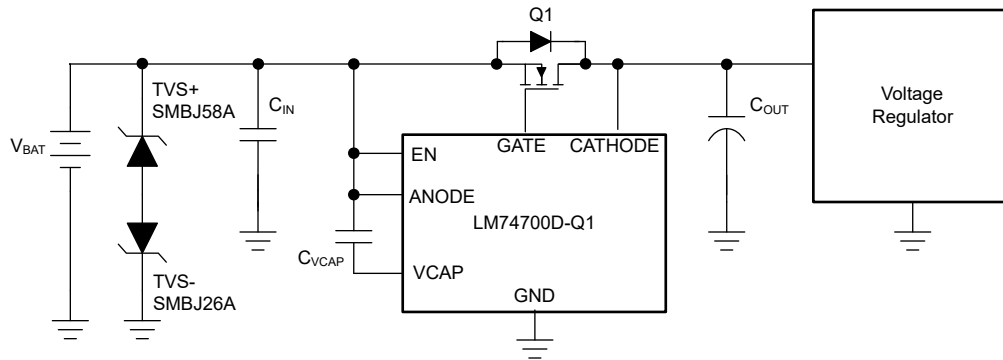


图 10-3. Typical 24-V Battery Protection with Two Uni-Directional TVS

The breakdown voltage of the TVS+ must be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM74700D-Q1 (65 V), and must withstand 65-V suppressed load dump. The breakdown voltage of TVS - must be lower than maximum reverse battery voltage - 32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to - 600 V with a generator impedance of 50 Ω . This action translates to 12 A flowing through the TVS -. The clamping voltage of the TVS - cannot be same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal to (- TVS Clamping voltage + Output capacitor voltage). For a 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS - must not exceed, $75 \text{ V} - 32 \text{ V} = 43 \text{ V}$.

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ $\geq 65 \text{ V}$, maximum clamping voltage is $\leq 43 \text{ V}$ and the clamping voltage cannot be less than the breakdown voltage. Two uni-directional TVS connected back-back must be used at the input. For positive side TVS+, TI recommends SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical). For the negative side TVS -, TI recommends SMBJ26A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage - 32 V) and maximum clamping voltage of 42.1 V.

For 24-V battery protection, TI recommends a 75-V rated MOSFET to be used along with SMBJ26A and SMBJ58A connected back-to-back at the input.

10.2.5 Application Curves

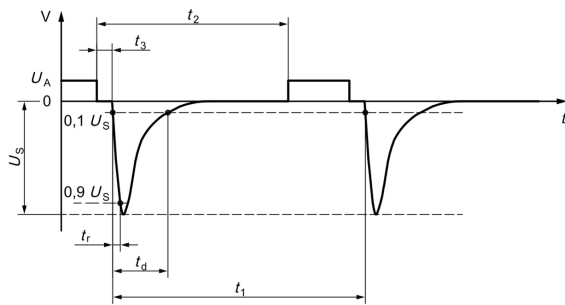
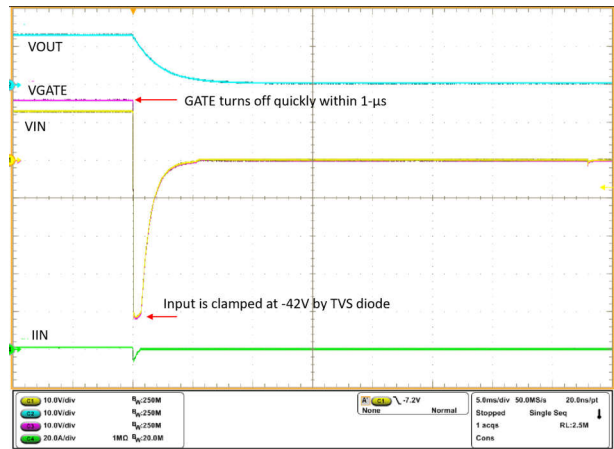
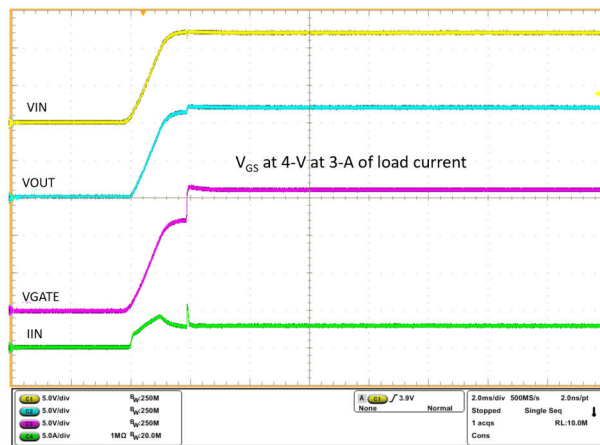


图 10-4. ISO 7637-2 Pulse 1



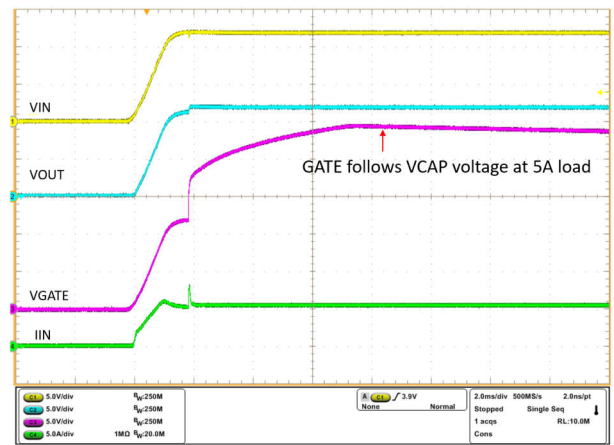
Time (5 ms/DIV)

图 10-5. Response to ISO 7637-2 Pulse 1



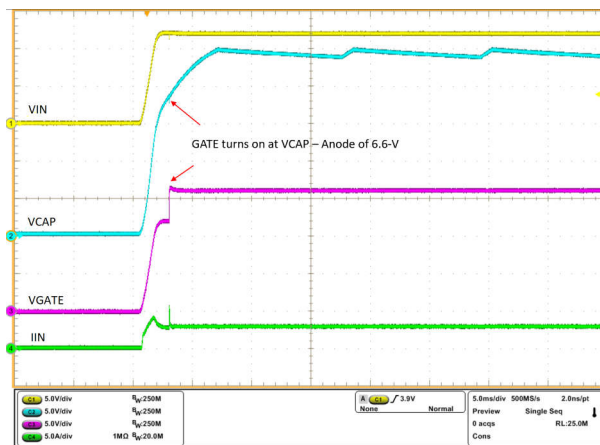
Time (2 ms/DIV)

图 10-6. Start-Up With 3-A Load



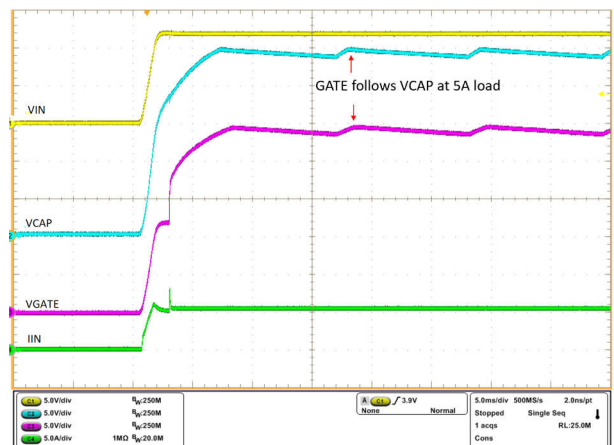
Time (2 ms/DIV)

图 10-7. Start-Up With 5-A Load



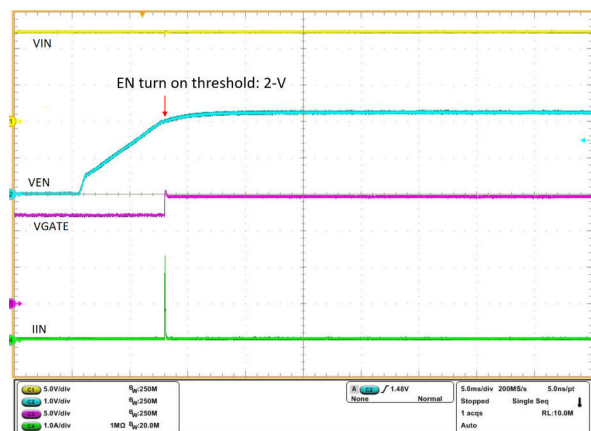
Time (5 ms/DIV)

图 10-8. VCAP During Start-Up at 3-A Load



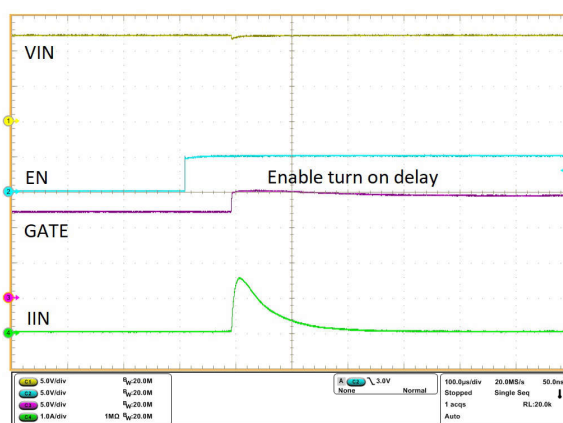
Time (5 ms/DIV)

图 10-9. VCAP During Start-Up at 5.8-A Load



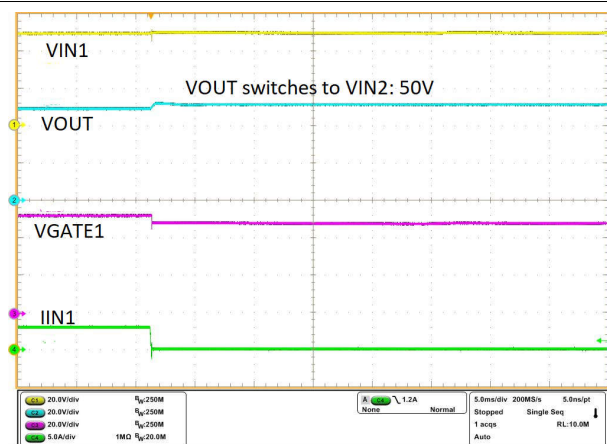
Time (5 ms/DIV)

图 10-10. Enable Threshold

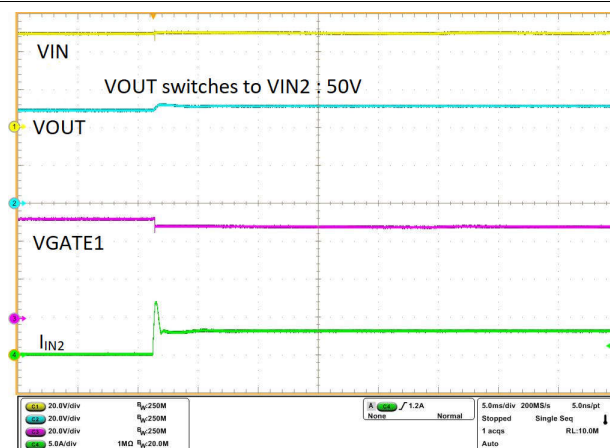


Time (100 μs/DIV)

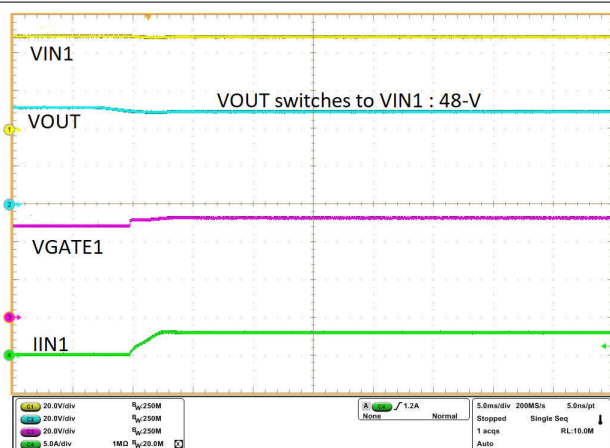
图 10-11. Enable Turn-ON Delay



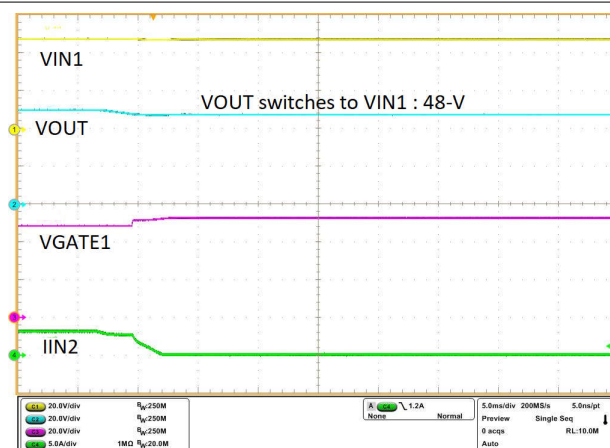
Time (5 ms/DIV)

图 10-12. OR-ing V_{IN1} to V_{IN2} Switch Over

Time (5 ms/DIV)

图 10-13. OR-ing V_{IN1} to V_{IN2} Switch Over

Time (5 ms/DIV)

图 10-14. OR-ing V_{IN2} to V_{IN1} Switch Over

Time (5 ms/DIV)

图 10-15. OR-ing V_{IN2} to V_{IN1} Switch Over

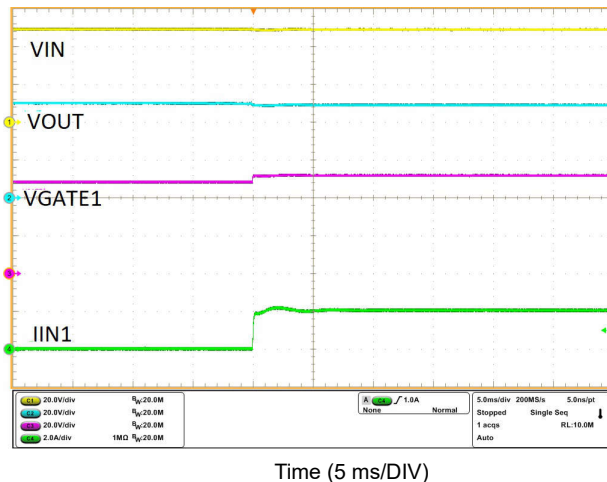


图 10-16. OR-ing - V_{IN2} Failure and Switch Over to V_{IN1}

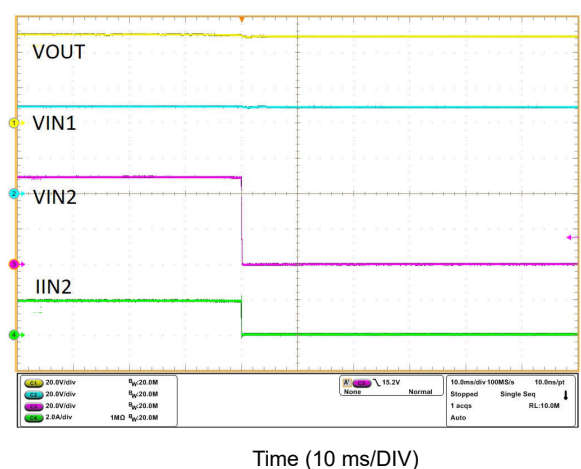


图 10-17. OR-ing - V_{IN2} Failure and Switch Over to V_{IN1}

10.2.6 OR-ing Application Configuration

Basic redundant power architecture comprises of two or more voltage or power supply sources driving a single load. In simplest form, the OR-ing solution for redundant power supplies consists of Schottky OR-ing diodes that protect the system against an input power supply fault condition. A diode OR-ing device provides effective and low cost solution with few components. However, the diodes forward voltage drops affects the efficiency of the system permanently, because each diode in an OR-ing application spends most of the time in forward conduction mode. These power losses increase the requirements for thermal management and allocated board space.

The LM74700D-Q1 ICs combined with external N-Channel MOSFETs can be used in OR-ing Solution as shown in 图 10-18. The forward diode drop is reduced as the external N-Channel MOSFET is turned ON during normal operation. LM74700D-Q1 quickly detects the reverse current, pulls down the MOSFET gate fast, leaving the body diode of the MOSFET to block the reverse current flow. An effective OR-ing solution must be extremely fast to limit the reverse current amount and duration. The LM74700D-Q1 devices in OR-ing configuration constantly sense the voltage difference between Anode and Cathode pins, which are the voltage levels at the power sources (V_{IN1} , V_{IN2}) and the common load point respectively. The source to drain voltage V_{DS} for each MOSFET is monitored by the Anode and Cathode pins of the LM74700D-Q1. A fast comparator shuts down the Gate Drive through a fast Pull-Down within 0.45 μ s (typical) as soon as $V_{(IN)} - V_{(OUT)}$ falls below -11 mV. A fast comparator turns on the Gate with 11-mA gate charge current once the differential forward voltage $V_{(IN)} - V_{(OUT)}$ exceeds 50 mV.

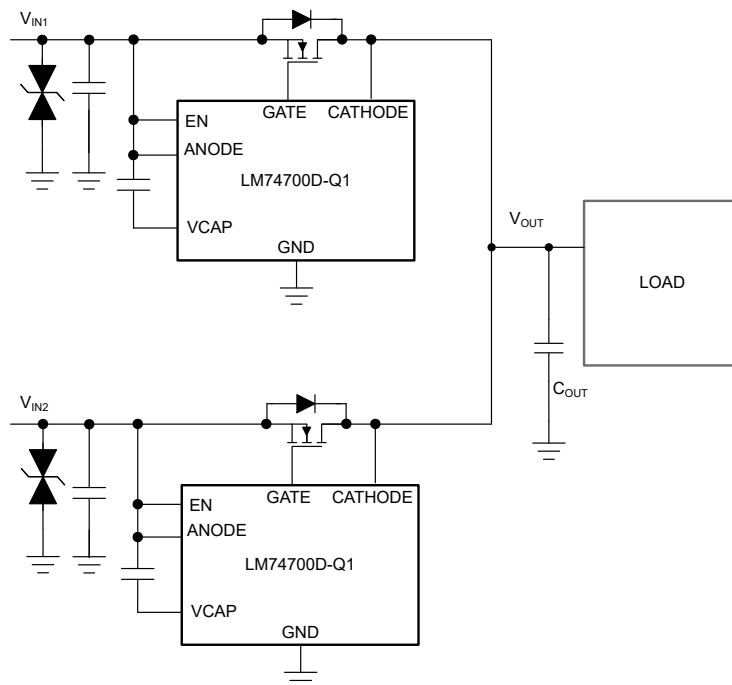


图 10-18. Typical OR-ing Application

图 10-12 到 图 10-15 show the smooth switch over between two power supply rails V_{IN1} at 48 V and V_{IN2} at 50 V. 图 10-16 and 图 10-17 illustrate the performance when V_{IN2} fails. LM74700D-Q1 controlling V_{IN2} power rail turns off quickly, so that the output remains uninterrupted and V_{IN1} is protected from V_{IN2} failure.

10.3 Power Supply Recommendations

The LM74700D-Q1 ideal diode controller is designed for the supply voltage range of $3.2\text{ V} \leq V_{ANODE} \leq 65\text{ V}$. If the input supply is located more than a few inches from the device, TI recommends an input ceramic bypass capacitor higher than 22 nF. To prevent LM74700D-Q1 and surrounding components from damage under the conditions of a direct output short circuit, make sure to use a power supply having over load and short-circuit protection.

10.4 Layout

10.4.1 Layout Guidelines

- Connect ANODE, GATE, and CATHODE pins of LM74700D-Q1 close to the MOSFET SOURCE, GATE, and DRAIN pins.
- Use thick traces for source and drain of the MOSFET to minimize resistive losses because the high current path of for this design is through the MOSFET
- Keep the charge pump capacitor across VCAP and ANODE pins away from the MOSFET to lower the thermal effects on the capacitance value.
- Place input capacitor close to the device ANODE and GND pins.
- Connect the Gate pin of the LM74700D-Q1 to the MOSFET gate with short trace. Avoid excessively thin and long trace to the Gate Drive.
- Keep the GATE pin close to the MOSFET to avoid increase in MOSFET turn-off delay due to trace resistance.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the [Layout Example](#) is intended as a guideline and to produce good results.

10.4.2 Layout Example

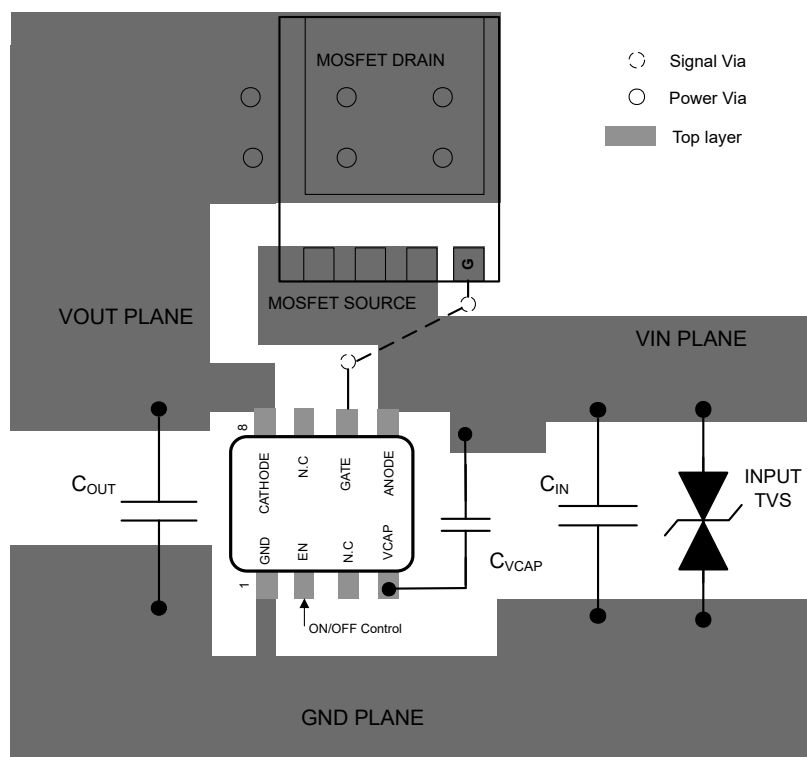


图 10-19. LM74700D-Q1 Example Layout

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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11.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

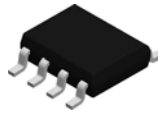
ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

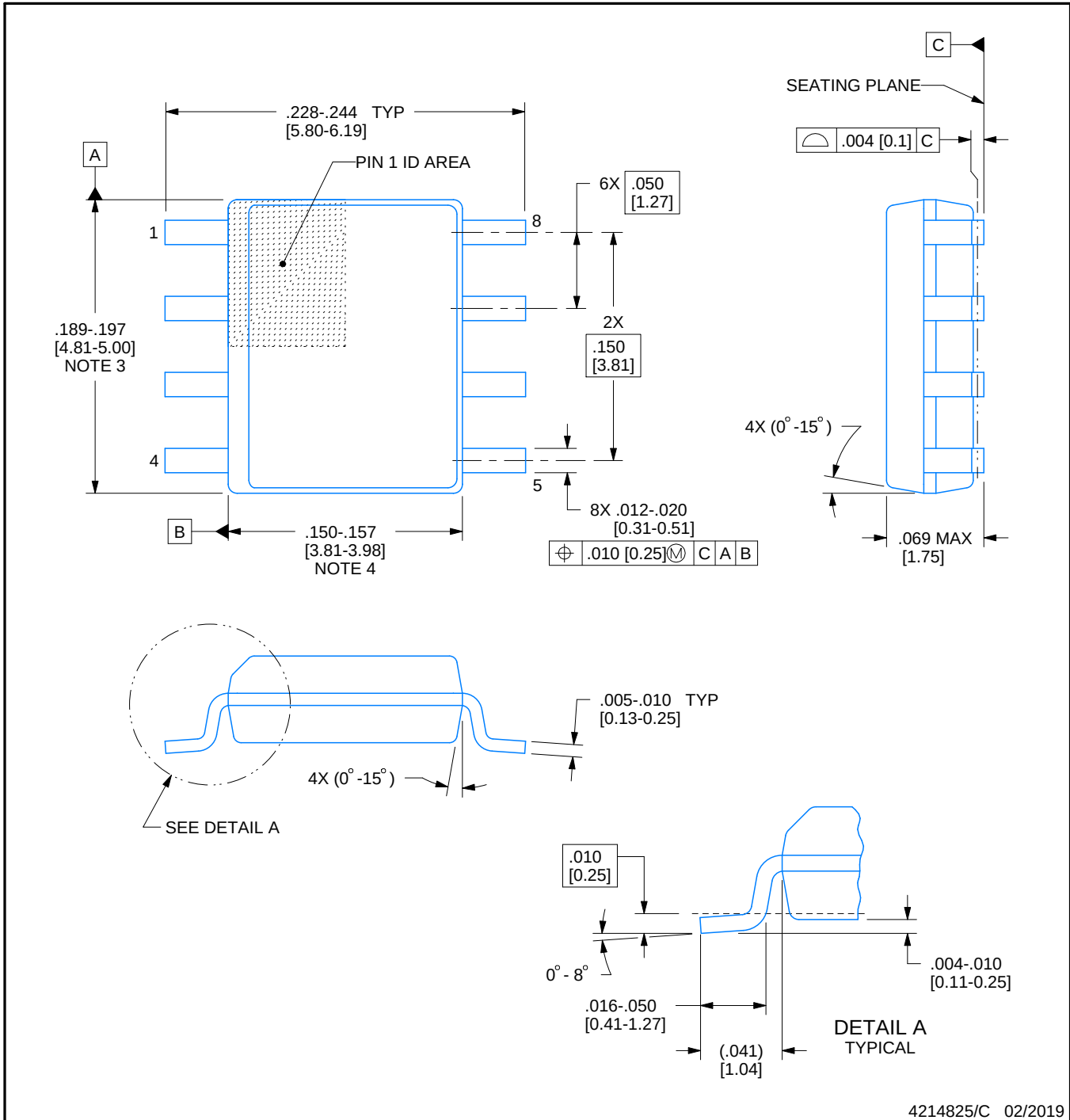


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

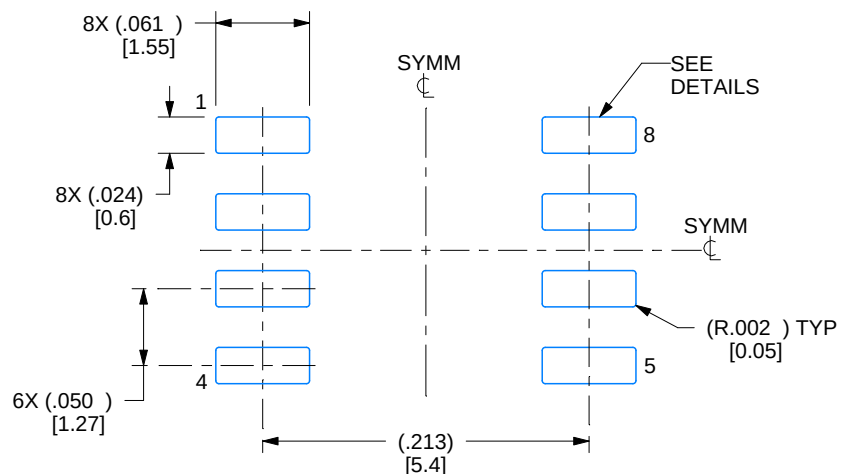
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

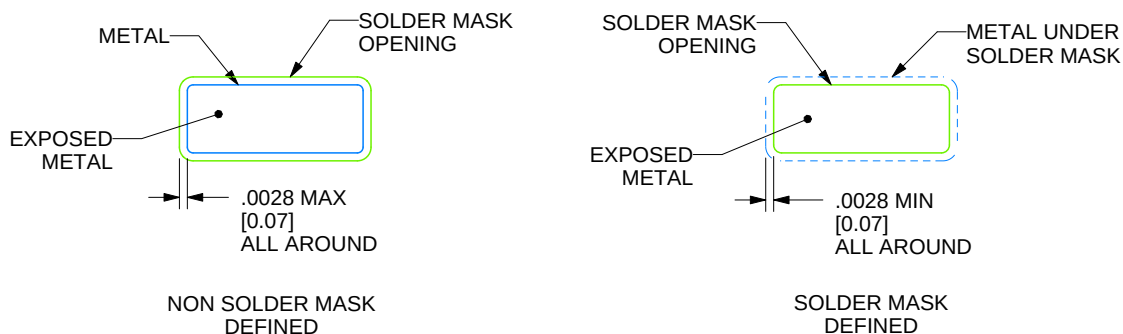
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

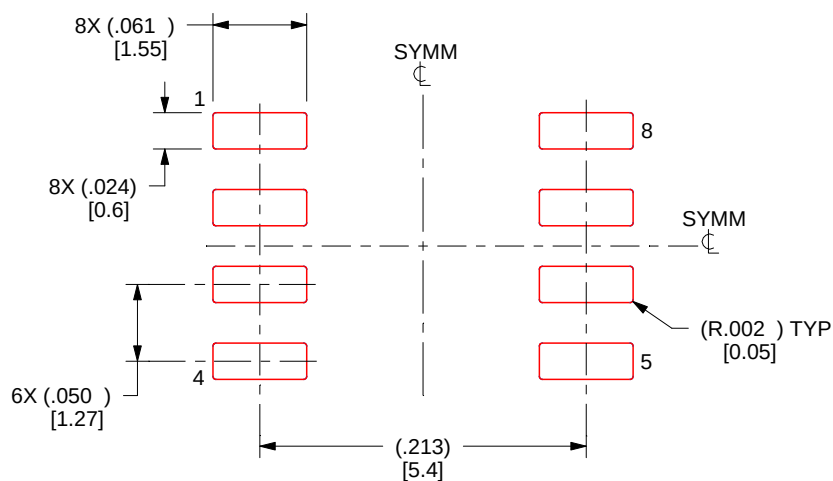
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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