LM5574-Q1 —— 75V/0.5A 汽车级降压开关稳压器

1 特性

- LM5574-Q1 是一款通过 AEC-Q100 Grade 认证的汽车级产品
- –40°C 至 150°C 的工作结温范围
- 集成 75V、750mΩ N 沟道 MOSFET
- 6V 至 75V 的超宽输入电压范围
- 可调节的输出电压低至 1.225V
- 1.5% 反馈基准电压精度
- 工作频率可在 50kHz 至 500kHz 范围内调节，采用单个电阻器。
- 控制器或外设频率同步
- 可调软启动
- 仿真电流模式控制架构
- 宽带宽误差放大器
- 内置保护
- 封装：
  - TSSOP-16
- 使用 LM5574-Q1 和 WEBENCH® Power Designer 工具创建定制设计方案

2 应用

- 汽车

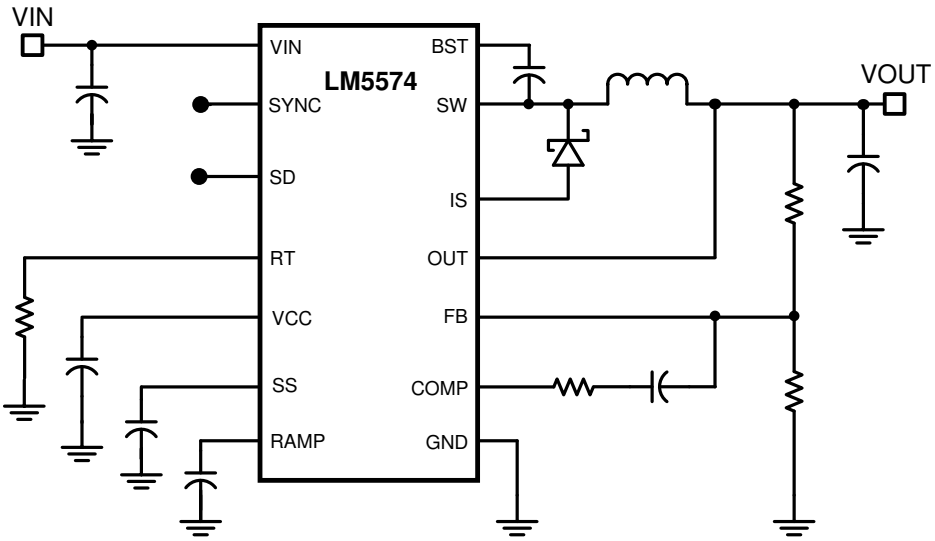
3 说明

LM5574-Q1 是一款方便易用的降压稳压器，使设计工程师能够利用最少的组件来设计和优化可靠的电源。LM5574-Q1 在 6V 至 75V 的输入电压范围内工作，通过集成的 750mΩ N 沟道 MOSFET 提供 0.5A 的连续输出电流。该稳压器采用仿真电流模式架构，不仅具备固有的线路调节能力、出色的负载瞬态响应特性以及简化的环路补偿设计，更突破了传统电流模式稳压器在低占空比工况下的应用限制。工作频率可在 50kHz 至 500kHz 范围内调节，以便对尺寸和效率进行优化。为降低 EMI，频率同步引脚使 LM(2)557x 系列的多款 IC 可以自同步或同步到外部时钟。LM5574-Q1 具有逐周期电流限制、短路保护、热关断和远程关断功能，为可靠性提供了保证。该器件采用 16 引脚 TSSOP 封装。LM5574-Q1 由全套 WEBENCH 在线设计工具提供支持。

封装信息

器件型号	封装(1)	封装尺寸(2)
LM5574-Q1	PW（TSSOP，16）	5mm × 6.4mm

(1) 有关更多信息，请参阅 节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化版应用原理图

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4 Pin Configuration and Functions

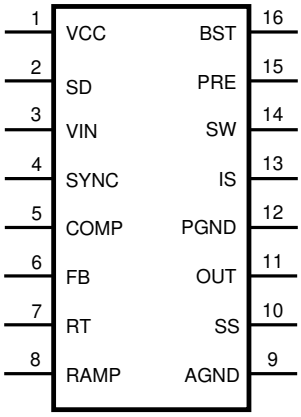


图 4-1. PW Package 16-Pin TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VCC	O	Output of the bias regulator	V_{CC} monitors V_{IN} up to 9V. Beyond 9V, V_{CC} is regulated to 7V. A 0.1µF to 1µF ceramic decoupling capacitor is required. An external voltage (7.5V – 14V) can be applied to this pin to reduce internal power dissipation.
2	SD	I	Shutdown or UVLO input	If the SD pin voltage is less than 0.7V, the regulator is in a low power state. If the SD pin voltage is between 0.7V and 1.225V, the regulator is in standby mode. If the SD pin voltage is more than 1.225V, the regulator is operational. An external voltage divider can be used to set a line undervoltage shutdown threshold. If the SD pin is left open circuit, a 5µA pullup current source configures the regulator fully operational.
3	Vin	I	Input supply voltage	Nominal operating range: 6V to 75V
4	SYNC	I	Oscillator synchronization input or output	The internal oscillator can be synchronized to an external clock with an external pulldown device. Multiple LM5574-Q1 devices can be synchronized together by connection of the SYNC pins.
5	COMP	O	Output of the internal error amplifier	The loop compensation network must be connected between this pin and the FB pin.
6	FB	I	Feedback signal from the regulated output	This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.225V.
7	RT	I	Internal oscillator frequency set input	The internal oscillator is set with a single resistor connected between this pin and the AGND pin.
8	RAMP	O	Ramp control signal	An external capacitor connected between this pin and the AGND pin sets the ramp slope used for current mode control. Recommended capacitor range 50pF to 2000pF.
9	AGND	Ground	Analog ground	Internal reference for the regulator control functions
10	SS	O	Soft-start	An external capacitor and an internal 10µA current source set the time constant for the rise of the error amp reference. The SS pin is held low during standby, V_{CC} UVLO, and thermal shutdown.
11	OUT	O	Output voltage connection	Connect directly to the regulated output voltage.
12	PGND	Ground	Power ground	Low-side reference for the PRE switch and the IS sense resistor.

表 4-1. Pin Functions（续）

PIN		TYPE(1)	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
13	IS	I	Current sense	Current measurement connection for the re-circulating diode. An internal sense resistor and a sample and hold circuit sense the diode current near the conclusion of the off-time. This current measurement provides the DC level of the emulated current ramp.
14	SW	O	Switching node	The source terminal of the internal buck switch. The SW pin must be connected to the external Schottky diode and to the buck inductor.
15	PRE	O	Pre-charge assist for the bootstrap capacitor	This open-drain output can be connected to SW pin to help charging the bootstrap capacitor during very light load conditions or in applications where the output can be pre-charged before the LM5574-Q1 is enabled. An internal pre-charge MOSFET is turned on for 250ns each cycle just prior to the on-time interval of the buck switch.
16	BST	I	Boost input for bootstrap capacitor	An external capacitor is required between the BST and the SW pins. A 0.022µF ceramic capacitor is recommended. The capacitor is charged from V_{CC} through an internal diode during the off-time of the buck switch.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

See (1) (2)

	MIN	MAX	UNIT
V_{IN} to GND		76	V
BST to GND		90	V
PRE to GND		76	V
SW to GND (steady-state)		–1.5	V
BST to V_{CC}		76	V
SD, V_{CC} to GND		14	V
BST to SW		14	V
OUT to GND	Limited to V_{IN}		
SYNC, SS, FB, RAMP to GND		7	V
Storage temperature, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If Military, aerospace specified devices are required, please contact the Texas Instruments Sales Office, Distributors for availability and specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) (2)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The human-body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

5.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{IN}	6	75	V
Operation junction temperature	–40	150	°C

5.4 Thermal Information

THERMAL METRIC(1)		LM5574 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, V_{IN} = 48V, R_T = 32.4kΩ unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
V_{CC} Reg	V_{CC} Regulator Output		6.85	7.15	7.45	V
	V_{CC} LDO Mode turn-off			9		V
	V_{CC} Current Limit	V_{CC} = 0 V,		25		mA
VCC SUPPLY						
	V_{CC} UVLO Threshold	(V_{CC} increasing).	5.03	5.35	5.67	V
	V_{CC} Undervoltage Hysteresis			0.35		V
	Bias Current (Iin)	FB = 1.3 V.		2	4.5	mA
	Shutdown Current (Iin)	SD = 0 V.		48	85	µA
SHUTDOWN THRESHOLDS						
	Shutdown Threshold	(SD Increasing)	0.47	0.7	0.9	V
	Shutdown Hysteresis			0.1		V
	Standby Threshold	(Standby Increasing)	1.17	1.225	1.28	V
	Standby Hysteresis			0.1		V
	SD Pull-up Current Source			5		µA
SWITCH CHARACTERISTICS						
	Buck Switch Rds(on)			750	1500	mΩ
	BOOST UVLO			4		V
	BOOST UVLO Hysteresis			0.93		V
	Pre-charge Switch Rds(on)			70		Ω
	Pre-charge Switch on-time			250		ns
CURRENT LIMIT						
	Cycle by Cycle Current Limit	RAMP = 0 V	0.6	0.7	0.8	A
	Cycle by Cycle Current Limit Delay	RAMP = 2.5 V		75		ns
SOFT-START						
	SS Current Source		7	10	14	µA
OSCILLATOR						
	Frequency1		180	200	220	kHz
	Frequency2	R_T = 11 kΩ.	425	485	525	kHz
	SYNC Source Impedance			11		kΩ
	SYNC Sink Impedance			110		Ω
	SYNC Threshold (falling)			1.3		V
	SYNC Frequency	R_T = 11 kΩ.	550			kHz
	SYNC Pulse Width Minimum		15			ns
RAMP GENERATOR						
	Ramp Current 1	V_{IN} = 60 V, V_{OUT}=10 V.	467	550	633	µA
	Ramp Current 2	V_{IN} = 10 V, V_{OUT}=10 V.	36	50	64	µA
PWM COMPARATOR						
	Forced Off-time		416	500	575	ns
	Min On-time			80		ns
	COMP to PWM Comparator Offset			0.7		V
ERROR AMPLIFIER						
	Feedback Voltage	Vfb = COMP.	1.207	1.225	1.243	V
	FB Bias Current			10		nA
	DC Gain			70		dB
	COMP Sink / Source Current		3			mA
	Unity Gain Bandwidth			3		MHz

Specifications with standard typeface are for T_J = 25°C, V_{IN} = 48V, R_T = 32.4kΩ unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIODE SENSE RESISTANCE						
D_{SENSE}				250		mΩ
THERMAL SHUTDOWN						
Tsd	Thermal Shutdown Threshold			165		°C
	Thermal Shutdown hysteresis			25		°C

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).

5.6 Typical Characteristics

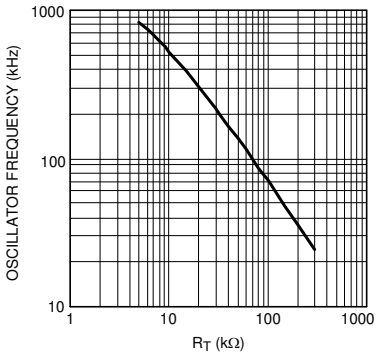


图 5-1. Oscillator Frequency vs R_T

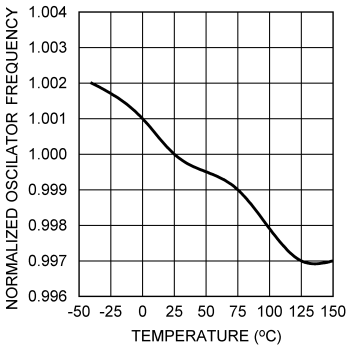


图 5-2. Oscillator Frequency vs Temperature F_{OSC} = 200kHz

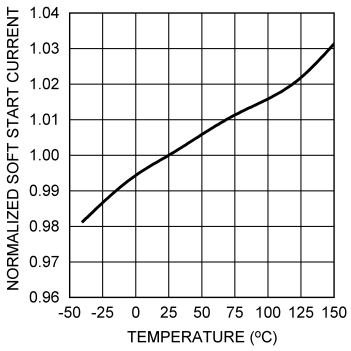


图 5-3. Soft-Start Current vs Temperature

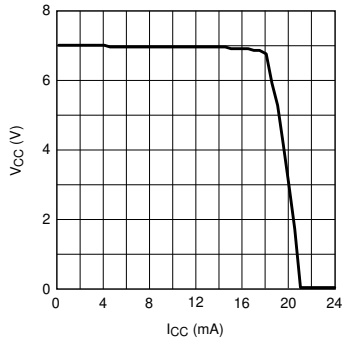


图 5-4. V_{CC} vs I_{CC} V_{IN} = 12V

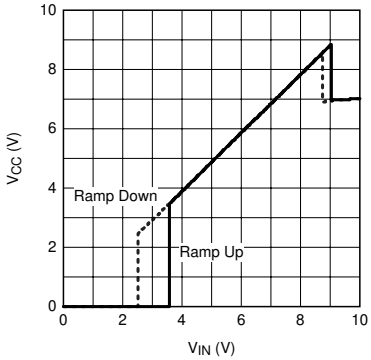


图 5-5. V_{CC} vs V_{IN} R_L = 7kΩ

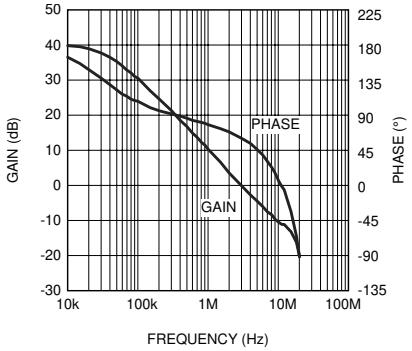


图 5-6. Error Amplifier Gain And Phase A_{VCL} = 101

5.6 Typical Characteristics (continued)

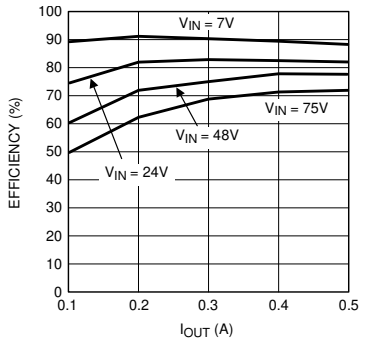


图 5-7. Demoboard Efficiency vs I_{OUT} and V_{IN}

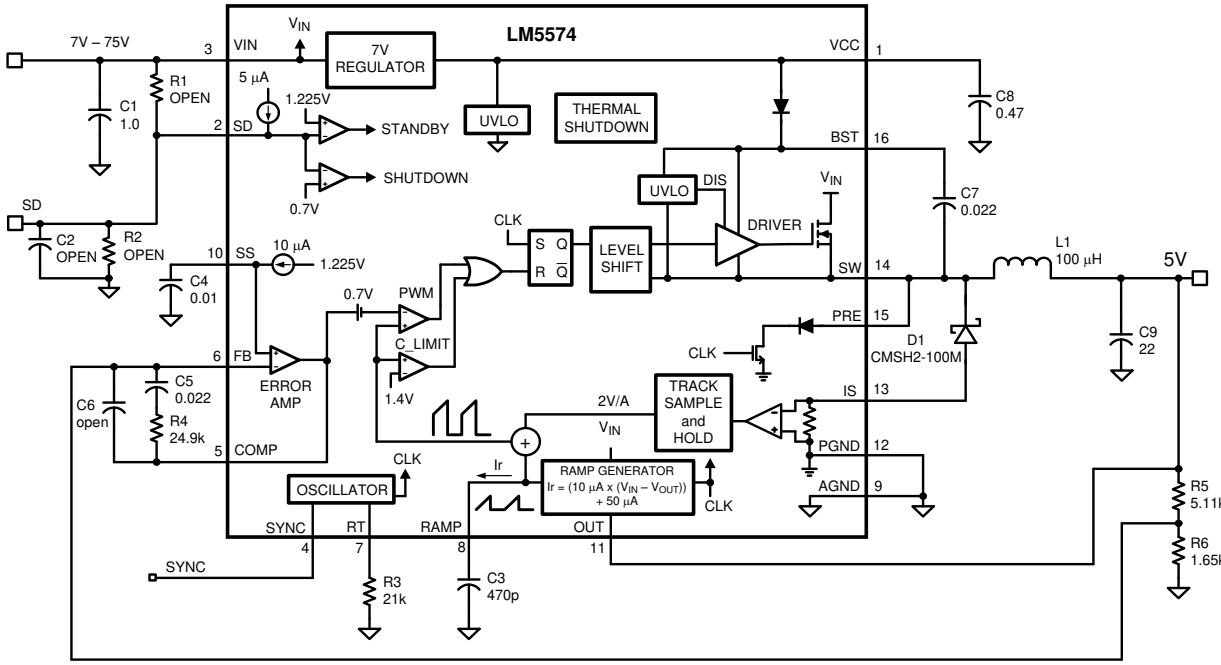
6 Detailed Description

6.1 Overview

The LM5574-Q1 switching regulator features the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy-to-use regulator integrates a 75V, N-Channel buck switch with an output current capability of 0.5 Amps. The regulator control method is based on current mode control using an emulated current ramp. Peak current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting, and ease-of-loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse width modulation circuit, which allows reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50kHz to 500kHz. An oscillator synchronization pin allows multiple LM5574-Q1 regulators to self-synchronize or be synchronized to an external clock. The output voltage can be set as low as 1.225V. Fault protection features include current limiting, thermal shutdown, and remote shutdown capability. The device is available in the 16-pin TSSOP package.

The functional block diagram and typical application of the LM5574-Q1 are shown in 图 7-3. The LM5574-Q1 can be applied in numerous applications to efficiently step-down a high, unregulated input voltage. The device is designed for telecom, industrial and automotive power bus voltage ranges.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Shutdown and Standby

The LM5574-Q1 contains a dual-level Shutdown (SD) circuit. When the SD pin voltage is less than 0.7V, the regulator is in a low current shutdown mode. When the SD pin voltage is greater than 0.7V but less than 1.225V, the regulator is in standby mode. In standby mode the V_{CC} regulator is active but the output switch is disabled. When the SD pin voltage exceeds 1.225V, the output switch is enabled and normal operation begins. An internal 5µA pullup current source configures the regulator to be fully operational if the SD pin is left open.

An external set-point voltage divider from VIN to GND can be used to set the operational input range of the regulator. The divider must be designed such that the voltage at the SD pin is greater than 1.225V when Vin is in the desired operating range. The internal 5µA pullup current source must be included in calculations of the external set-point divider. Hysteresis of 0.1V is included for both the shutdown and standby thresholds. The SD

pin is internally clamped with a 1kΩ resistor and an 8V Zener clamp. The voltage at the SD pin must never exceed 14V. If the voltage at the SD pin exceeds 8V, the bias current increases at a rate of 1mA/V.

The SD pin can also be used to implement various remote enable, disable functions. Pulling the SD pin below the 0.7V threshold totally disables the controller. If the SD pin voltage is above 1.225V, the regulator is operational.

6.3.2 Current Limit

The LM5574-Q1 contains a unique current monitoring scheme for control and overcurrent protection. When set correctly, the emulated current sense signal provides a signal which is proportional to the buck switch current with a scale factor of 2.0V/A. The emulated ramp signal is applied to the current limit comparator. If the emulated ramp signal exceeds 1.4V (0.7A), the present current cycle is terminated (cycle-by-cycle current limiting). In applications with small output inductance and high input voltage the switch current can overshoot due to the propagation delay of the current limit comparator. If an overshoot occurs, the diode current sampling circuit detects the excess inductor current during the off-time of the buck switch. If the sample and hold DC level exceeds the 1.4V current limit threshold, the buck switch is disabled and skips pulses until the diode current sampling circuit detects the inductor current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation because the inductor current is forced to decay following any current overshoot.

6.3.3 Soft Start

The soft-start feature allows the regulator to gradually reach the initial steady-state operating point, thus reducing start-up stresses and surges. The internal soft-start current source, set to 10µA, gradually increases the voltage of an external soft-start capacitor connected to the SS pin. The soft-start capacitor voltage is connected to the reference input of the error amplifier. Various sequencing and tracking schemes can be implemented using external circuits that limit or clamp the voltage level of the SS pin.

In the event a fault is detected (overtemperature, V_{CC} UVLO, SD) the soft-start capacitor is discharged. When the fault condition is no longer present a new soft-start sequence commences.

6.3.4 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 180°C, the controller is forced into a low power reset state, which disables the output driver and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

6.4 Device Functional Modes

6.4.1 High Voltage Start-Up Regulator

The LM5574-Q1 contains a dual-mode internal high voltage start-up regulator that provides the V_{CC} bias supply for the PWM controller and boot-strap MOSFET gate driver. The input pin (VIN) can be connected directly to the input voltage, as high as 75V. For input voltages below 9V, a low dropout switch connects V_{CC} directly to V_{IN}. In this supply range, V_{CC} is approximately equal to V_{IN}. For V_{IN} voltage greater than 9V, the low dropout switch is disabled and the V_{CC} regulator is enabled to maintain V_{CC} at approximately 7V. The wide operating range of 6V to 75V is achieved through the use of this dual-mode regulator.

The output of the V_{CC} regulator is current limited to 25mA. Upon power up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds the V_{CC} UVLO threshold of 5.35V and the SD pin is greater than 1.225V, the output switch is enabled and a soft-start sequence begins. The output switch remains enabled until V_{CC} falls below 5.0V or the SD pin falls below 1.125V.

An auxiliary supply voltage can be applied to the V_{CC} pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 7.3V, the internal regulator essentially shuts off, reducing the IC power dissipation. The V_{CC} regulator series pass transistor includes a diode between V_{CC} and V_{IN} that can not be forward biased in normal operation. Therefore, the auxiliary V_{CC} voltage must never exceed the V_{IN} voltage.

In high voltage applications, take extra care to make sure the VIN pin does not exceed the absolute maximum voltage rating of 76V. During line or load transients, voltage ringing on the V_{IN} line that exceeds the absolute maximum ratings can damage the IC. Both careful printed-circuit board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

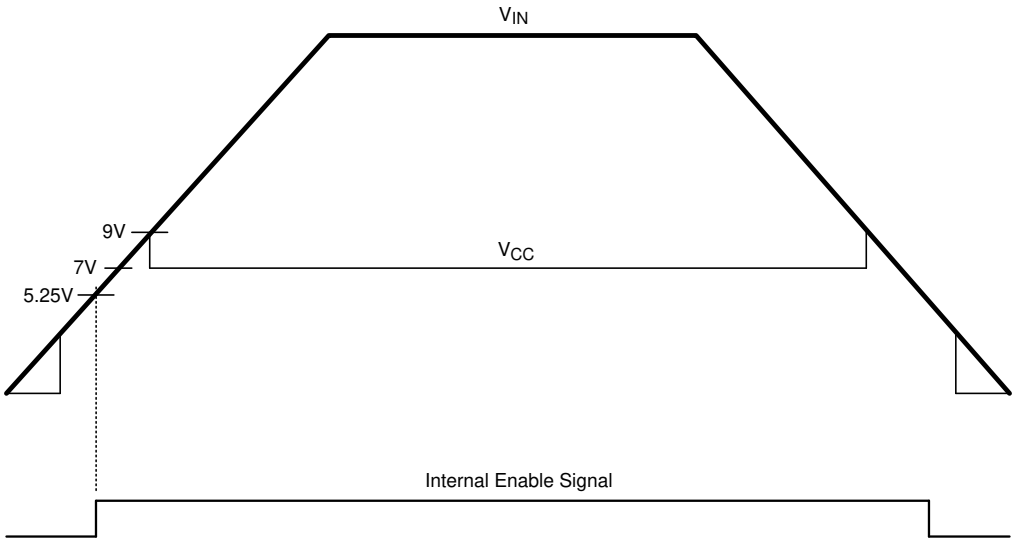


图 6-1. V_{IN} and V_{CC} Sequencing

6.4.2 Oscillator and Sync Capability

The LM5574-Q1 oscillator frequency is set by a single external resistor connected between the RT pin and the AGND pin. The R_T resistor must be placed very close to the device and connected directly to the pins of the IC (RT and AGND). To set a desired oscillator frequency (F), use the following equation to calculate the necessary value for the R_T resistor.

$$R_T = \frac{\frac{1}{F} - 580 \times 10^{-9}}{135 \times 10^{-12}} \quad (1)$$

The SYNC pin can be used to synchronize the internal oscillator to an external clock. The external clock must be of higher frequency than the free-running frequency set by the R_T resistor. A clock circuit with an open-drain output is the recommended interface from the external clock to the SYNC pin. The clock pulse duration must be greater than 15ns.

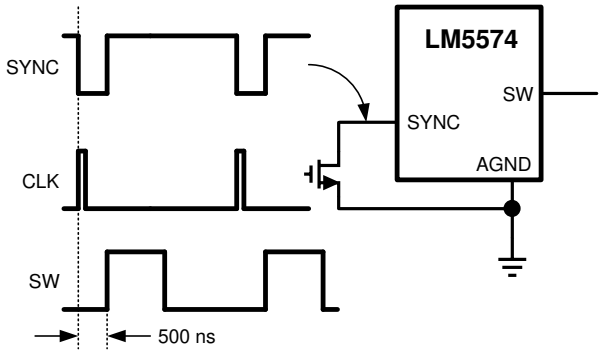


图 6-2. Sync From External Clock

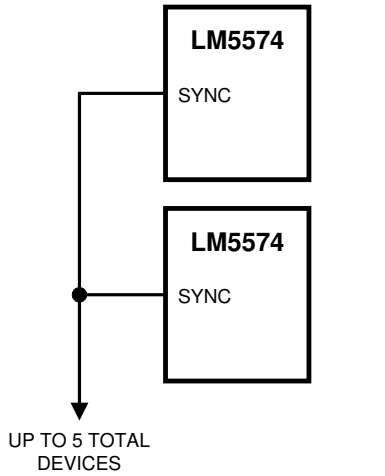


图 6-3. Sync From Multiple Devices

Multiple LM5574-Q1 devices can be synchronized together simply by connecting the SYNC pins together. In this configuration, all of the devices are synchronized to the highest frequency device. The diagram in 图 6-4 shows the SYNC input and output features of the LM5574-Q1. The internal oscillator circuit drives the SYNC pin with a strong pulldown and weak pullup inverter. When the SYNC pin is pulled low either by the internal oscillator or an external clock, the ramp cycle of the oscillator is terminated and a new oscillator cycle begins. Thus, if the SYNC pins of several LM5574-Q1 ICs are connected together, the IC with the highest internal clock frequency pulls the connected SYNC pins low first and terminate the oscillator ramp cycles of the other ICs. The LM5574-Q1 with the highest programmed clock frequency served as the controller and control the switching frequency of the all the devices with lower oscillator frequency.

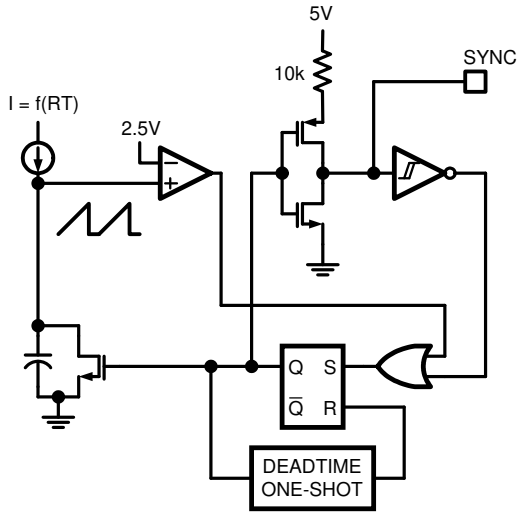


图 6-4. Simplified Oscillator Block Diagram and SYNC I/O Circuit

6.4.3 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.225V). The output of the error amplifier is connected to the COMP pin allowing the user to provide loop compensation components, generally a type II network, as shown in 图 7-3. This network creates a pole at DC, a zero and a noise-reducing, high-frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin.

6.4.4 Ramp Generator

The ramp signal used in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the output inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement can introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulse width. In applications where the input voltage can be relatively large in comparison to the output voltage, controlling small pulse widths and duty cycles is necessary for regulation. The LM5574-Q1 uses a unique ramp generator, which does not actually measure the buck switch current but rather reconstructs the signal. Reconstructing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements: a sample and hold DC level and an emulated current ramp.

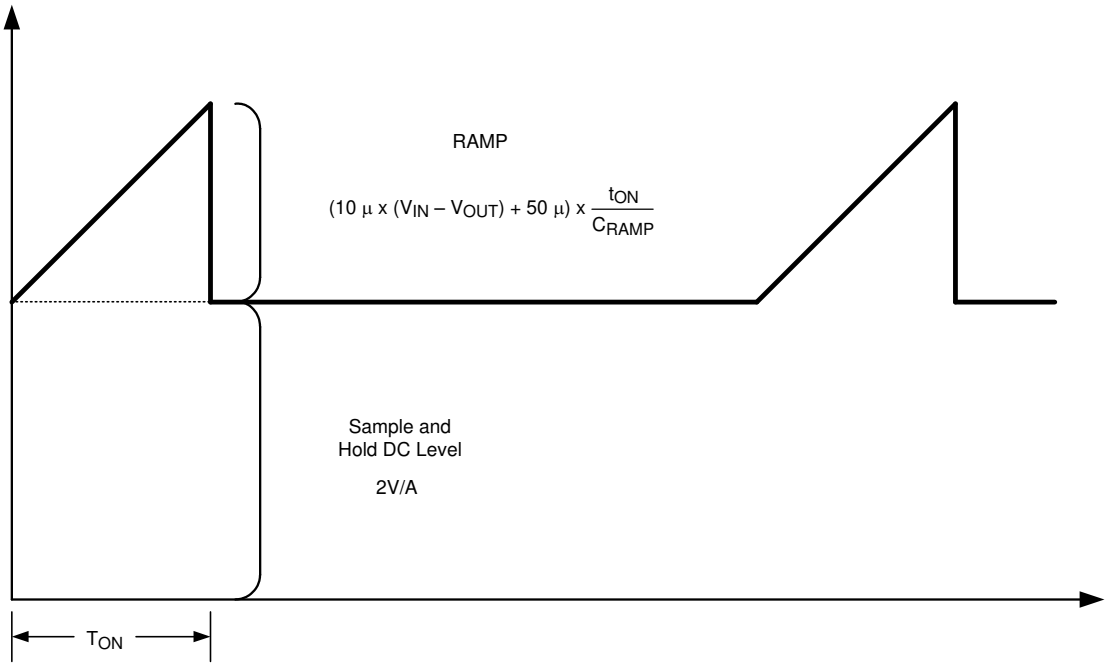


图 6-5. Composition of Current Sense Signal

The sample and hold DC level shown in 图 6-5 is derived from a measurement of the re-circulating Schottky diode anode current. The re-circulating diode anode must be connected to the IS pin. The diode current flows through an internal current sense resistor between the IS and PGND pins. The voltage level across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample and hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to AGND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the V_{IN} and V_{OUT} voltages per 方程式 2.

$$I_{RAMP} = (10\mu \times (VV_{IN} - V_{OUT})) + 50\mu A \quad (2)$$

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor. The value of C_{RAMP} can be selected from 方程式 3.

$$C_{RAMP} = L \times 5 \times 10^{-6} \quad (3)$$

where

- L is the value of the output inductor in Henrys.

With this value, the scale factor of the emulated current ramp is approximately equal to the scale factor of the DC level sample and hold (2.0V/A). The C_{RAMP} capacitor must be placed very close to the device and connected directly to the pins of the IC (RAMP and AGND).

For duty cycles greater than 50%, peak current mode control circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Add a fixed slope voltage ramp (slope compensation) to the current sense signal to prevent this oscillation. The 50µA of offset current provided from the emulated current source adds some fixed slope to the ramp signal. In some high output voltage, high duty cycle applications, additional slope can be required. In these applications, a pullup resistor can be added between the V_{CC} and RAMP pins to increase the ramp slope compensation.

For V_{OUT} > 7.5V:

Calculate the excellent choice slope current, $I_{OS} = V_{OUT} \times 10\mu A/V$.

For example, at V_{OUT} = 10V, I_{OS} = 100µA.

Use 方程式 4 to install a resistor from the RAMP pin to V_{CC}.

$$R_{RAMP} = V_{CC} / (I_{OS} - 50\mu A) \quad (4)$$

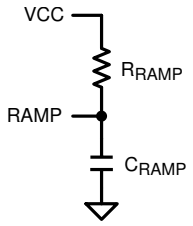


图 6-6. R_{RAMP} to V_{CC} for V_{OUT} > 7.5V

6.4.5 Maximum Duty Cycle and Input Dropout Voltage

There is a forced off-time of 500ns implemented each cycle to make sure of sufficient time for the diode current to be sampled. This forced off-time limits the maximum duty cycle of the buck switch. The maximum duty cycle varies with the operating frequency.

$$D_{MAX} = 1 - Fs \times 500ns \quad (5)$$

where

- Fs is the oscillator frequency.

Limiting the maximum duty cycle raises the input dropout voltage. The input dropout voltage is the lowest input voltage required to maintain regulation of the output voltage. Use 方程式 6 to calculate an approximation of the input dropout voltage.

$$Vin_{MIN} = \frac{Vout + V_D}{1 - Fs \times 500\ ns} \quad (6)$$

where

- V_D is the voltage drop across the re-circulatory diode.

Operating at high switching frequency raises the minimum input voltage necessary to maintain regulation.

6.4.6 Boost Pin

The LM5574-Q1 integrates an N-Channel buck switch and associated floating high voltage level shift, gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. TI recommends a 0.022µF ceramic capacitor connected with short traces between the BST pin and SW pin. During the off-time of the buck switch, the SW pin voltage is approximately –0.5V and the bootstrap capacitor is charged from V_{CC} through the internal bootstrap diode. When operating with a high PWM duty cycle, the buck switch is forced off each cycle for 500ns to make sure that the bootstrap capacitor is recharged.

Under very light load conditions or when the output voltage is pre-charged, the SW voltage does not remain low during the off-time of the buck switch. If the inductor current falls to zero and the SW pin rises, the bootstrap capacitor does not receive sufficient voltage to operate the buck switch gate driver. For these applications, the PRE pin can be connected to the SW pin to pre-charge the bootstrap capacitor. The internal pre-charge MOSFET and diode connected between the PRE pin and PGND turns on each cycle for 250ns just prior to the onset of a new switching cycle. If the SW pin is at a normal negative voltage level (continuous conduction mode), then no current flows through the pre-charge MOSFET/diode.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

7.1.1 Bias Power Dissipation Reduction

Buck regulators operating with high input voltage can dissipate an appreciable amount of power for the bias of the IC. The V_{CC} regulator must step-down the input voltage V_{IN} to a nominal V_{CC} level of 7V. The large voltage drop across the V_{CC} regulator translates into a large power dissipation within the V_{CC} regulator. There are several techniques that can significantly reduce this bias regulator power dissipation. 图 7-1 and 图 7-2 depict two methods to bias the IC from the output voltage. In each case the internal V_{CC} regulator is used to initially bias the VCC pin. After the output voltage is established, the VCC pin potential is raised above the nominal 7V regulation level, which effectively disables the internal V_{CC} regulator. The voltage applied to the VCC pin must never exceed 14V. The V_{CC} voltage must never be larger than the V_{IN} voltage.

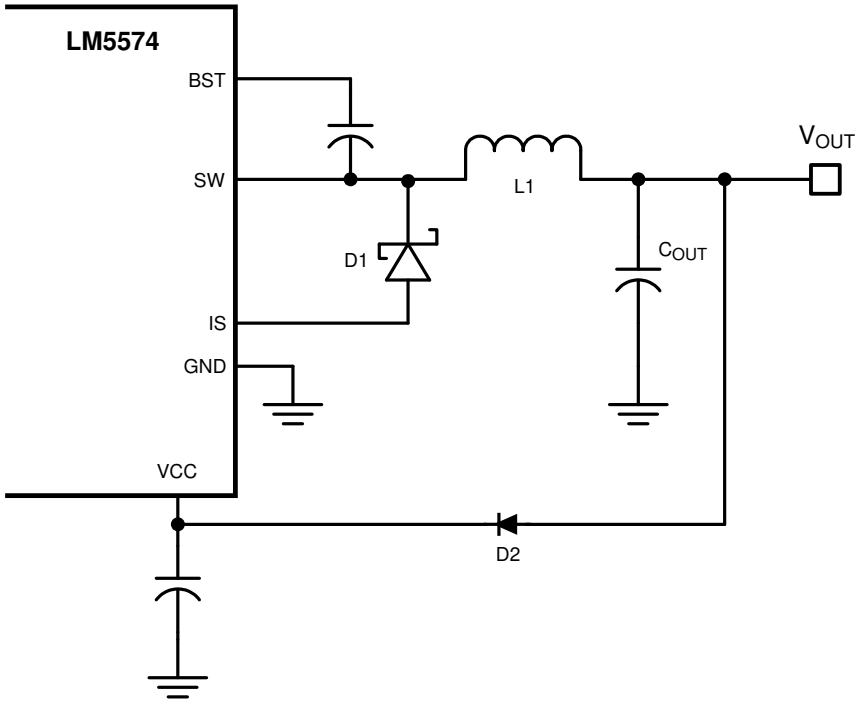


图 7-1. VCC Bias From VOUT for 8V < VOUT < 14V

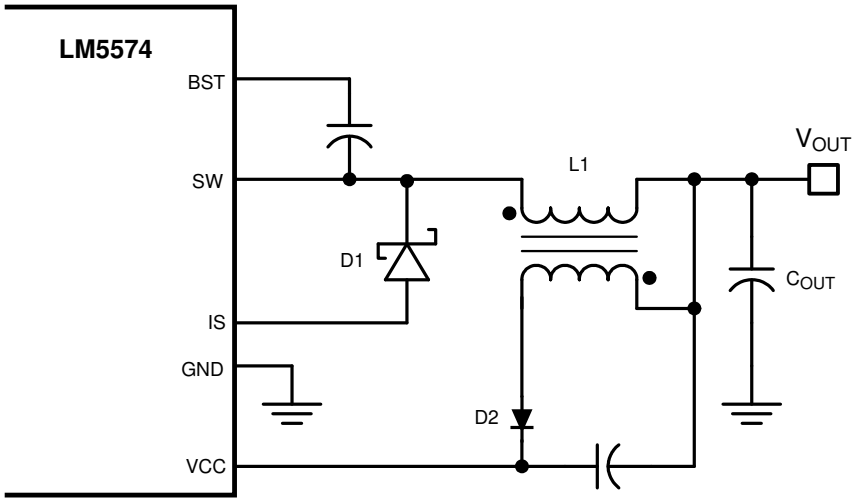


图 7-2. VCC Bias With Additional Winding on the Output Inductor

7.2 Typical Application

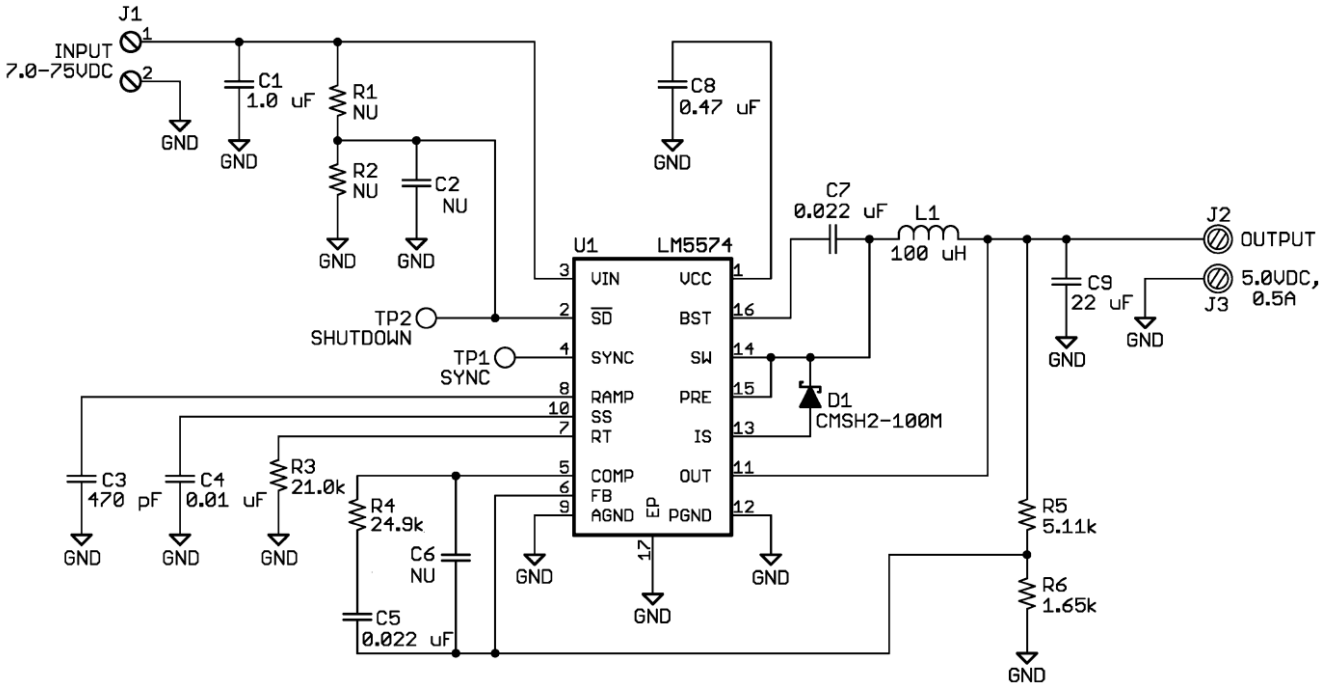


图 7-3. Typical Application Schematic

7.2.1 Design Requirements

The circuit shown in 图 7-3 is configured for the following specifications:

- V_{OUT} = 5V
- V_{IN} = 7V to 75V
- Fs = 300kHz
- Minimum load current (for CCM) = 100mA
- Maximum load current = 0.5A

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5574-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 External Components

The procedure for calculating the external components is shown with the following design example.

7.2.2.3 R3 (R_T)

R_T sets the oscillator switching frequency. Generally, higher frequency applications are smaller but have higher losses. Operation at 300kHz was selected for this example as a reasonable compromise for both small size and high efficiency. The value of R_T for 300kHz switching frequency can be calculated by 方程式 7.

$$R_T = \frac{[(1 / 300 \times 10^3) - 580 \times 10^{-9}]}{135 \times 10^{-12}} \quad (7)$$

The nearest standard value of 21kΩ was chosen for R_T.

7.2.2.4 L1- Inductor

The inductor value is determined based on the operating frequency, load current, ripple current, and the minimum and maximum input voltage ($V_{IN(min)}$, $V_{IN(max)}$).

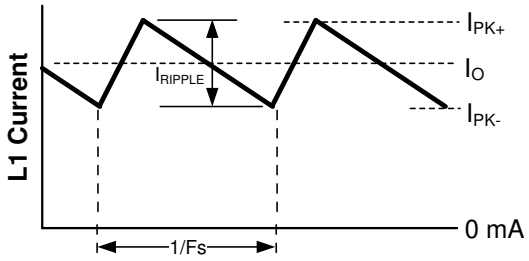


图 7-4. Inductor Current Waveform

To keep the circuit in continuous conduction mode (CCM), the maximum ripple current I_{RIPPLE} must be less than twice the minimum load current, or 0.2 Ap-p. With this value of ripple current, use 方程式 8 and 方程式 9 to calculate the value of inductor (L1).

$$L1 = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{I_{RIPPLE} \times F_S \times V_{IN(max)}} \quad (8)$$

$$L1 = \frac{5V \times (75V - 5V)}{0.2A \times 300\ kHz \times 75V} = 78\ \mu H \quad (9)$$

This procedure provides a guide to select the value of L1. The nearest standard value (100µH) is used. L1 must be rated for the peak current (I_{PK+}) to prevent saturation. During normal loading conditions, the peak current occurs at maximum load current plus maximum ripple. During an overload condition the peak current is limited to 0.7A nominal (0.85A maximum). The selected inductor has a conservative 1.0-Amp saturation current rating. For this manufacturer, the saturation rating is defined as the current necessary for the inductance to reduce by 30%, at 20°C.

7.2.2.5 C3- Ramp Capacitor

With the inductor value selected, 方程式 10 use to calculate the value of C3 (C_{RAMP}) necessary for the emulation ramp circuit.

$$C_{RAMP} = L \times 5 \times 10^{-6} \quad (10)$$

where

- L is in Henrys.

With L1 selected for 100µH, the recommended value for C3 is 470pF (nearest standard value).

7.2.2.6 C9 -Output Capacitor

The output capacitor, C9 smooths the inductor ripple current and provides a source of charge for transient loading conditions. For this design, a 22µF ceramic capacitor was selected. The ceramic capacitor provides ultra-low ESR to reduce the output ripple voltage and noise spikes. Use 方程式 11 to calculate an approximation for the output ripple voltage.

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times F_S \times C_{OUT}} \right) \quad (11)$$

7.2.2.7 D1 - Async Diode

A Schottky type re-circulating diode is required for all LM5574-Q1 applications. Ultra-fast diodes are not recommended and can result in damage to the IC due to reverse recovery current transients. The near excellent choice reverse recovery characteristics and low forward voltage drop are particularly important diode characteristics for high input voltage and low output voltage applications common to the LM5574-Q1. The reverse recovery characteristic determines how long the current surge lasts each cycle when the buck switch is turned on. The reverse recovery characteristics of Schottky diodes minimize the peak instantaneous power in the buck switch occurring during turn-on each cycle. The resulting switching losses of the buck switch are significantly reduced when using a Schottky diode. The reverse breakdown rating must be selected for the maximum V_{IN}, plus some safety margin.

The forward voltage drop has a significant impact on the conversion efficiency, especially for applications with a low output voltage. *Rated* current for diodes vary widely from various manufacturers. The worst case is to assume a short-circuit load condition. In this case the diode carries the output current almost continuously. For the LM5574-Q1, this current can be as high as 0.7A. Assuming a worst case, 1V drop across the diode, the maximum diode power dissipation can be as high as 0.7W. For the reference design, a 100V Schottky in a SMA package was selected.

7.2.2.8 C1- Input Capacitor

The regulator supply voltage has a large source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the VIN pin steps to the lower peak of the inductor current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into

VIN during the on-time is the load current. The input capacitance must be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$.

Quality ceramic capacitors with a low ESR must be selected for the input filter. To allow for capacitor tolerances and voltage effects, one 1.0µF, 100V ceramic capacitor are used. If step input voltage transients are expected near the maximum rating of the LM5574-Q1, a careful evaluation of ringing and possible spikes at the device VIN pin must be completed. An additional damping network or input voltage clamp can be required in these cases.

7.2.2.9 C8 - Vcc Capacitor

The capacitor at the VCC pin provides noise filtering and stability for the V_{CC} regulator. The recommended value of C8 must be no smaller than 0.1µF, and must be a good-quality, low-ESR, ceramic capacitor. A value of 0.47µF was selected for this design.

7.2.2.10 C7 - BST Capacitor

The bootstrap capacitor between the BST and the SW pins supplies the gate current to charge the buck switch gate at turn-on. The recommended value of C7 is 0.022µF, and must be a good-quality, low-ESR, ceramic capacitor.

7.2.2.11 C4 - SS Capacitor

The capacitor at the SS pin determines the soft-start time, that is the time for the reference voltage and the output voltage, to reach the final regulated value. 方程式 12 determines the time.

$$t_{ss} = \frac{C4 \times 1.225V}{10\ \mu A} \tag{12}$$

For this application, a C4 value of 0.01µF was chosen which corresponds to a soft-start time of 1ms.

7.2.2.12 R5, R6 - Feedback Resistor

R5 and R6 set the output voltage level. Use 方程式 13 to calculate the ratio of these resistors.

$$R5/R6 = (V_{OUT} / 1.225V) - 1 \tag{13}$$

For a 5V output, the R5/R6 ratio calculates to 3.082. The resistors must be chosen from standard value resistors. A good starting point is selection in the range of 1.0kΩ to 10kΩ. Values of 5.11kΩ for R5, and 1.65kΩ for R6 were selected.

7.2.2.13 R1, R2, C2 - SD Pin Components

A voltage divider can be connected to the SD pin to set a minimum operating voltage $V_{IN\ (min)}$ for the regulator. If this feature is required, the easiest approach to select the divider resistor values is to select a value for R1 (between 10kΩ and 100kΩ recommended) then calculate R2 from 方程式 14.

$$R2 = 1.225 \times \left(\frac{R1}{V_{IN(min)} + (5 \times 10^{-6} \times R1) - 1.225} \right) \tag{14}$$

Capacitor C2 provides filtering for the divider. The voltage at the SD pin must never exceed 8V, when using an external set-point divider, clamping the SD pin at high input voltage conditions can be necessary. The reference design uses the full range of the LM5574-Q1 (6V to 75V); therefore these components can be omitted. With the SD pin open circuit the LM5574-Q1 responds once the V_{CC} UVLO threshold is satisfied.

7.2.2.14 R4, C5, C6 - Compensation Components

These components configure the error amplifier gain characteristics to accomplish a stable overall loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components: R4

and C5. The overall loop gain is the product of the modulator gain and the error amplifier gain. The DC modulator gain of the LM5574-Q1 is 方程式 15.

$$\text{DC Gain}_{(MOD)} = G_{m(MOD)} \times R_{LOAD} = 0.5 \times R_{LOAD} \quad (15)$$

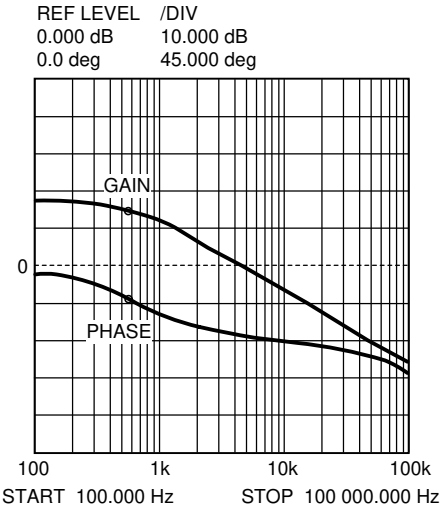
The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD},) and output capacitance (C_{OUT}). The corner frequency of this pole is 方程式 16.

$$f_{p(MOD)} = 1 / (2\pi\ R_{LOAD}\ C_{OUT}) \quad (16)$$

For R_{LOAD} = 20Ω and C_{OUT} = 22µF then $f_{p(MOD)}$ = 362Hz

$\text{DC Gain}_{(MOD)}$ = 0.5 × 20 = 20dB

For the design example of 图 7-3 the measured modulator gain vs. frequency characteristic is shown in 图 7-5.



R_{LOAD} = 20 Ω
C_{OUT} = 22µF

图 7-5. Gain and Phase of Modulator

Components R4 and C5 configure the error amplifier as a type II configuration which has a pole at DC and a zero at f_Z = 1 / (2 π R4C5). The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the loop gain. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

For the design example, a target loop bandwidth (crossover frequency) of 25kHz was selected. The compensation network zero (f_Z) must be selected at least an order of magnitude less than the target crossover frequency. This requirement constrains the product of R4 and C5 for a desired compensation network zero 1 / (2 π R4 C5) to be less than 2kHz. Increasing R4, while proportionally decreasing C5, increases the error amp gain. Conversely, decreasing R4 while proportionally increasing C5 decreases the error amp gain. For the design example, C5 was selected for 0.022µF and R4 was selected for 24.9kΩ. These values configure the compensation network zero at 290Hz. The error amp gain at frequencies greater than f_Z is: R4 / R5, which is approximately 5 (14dB).

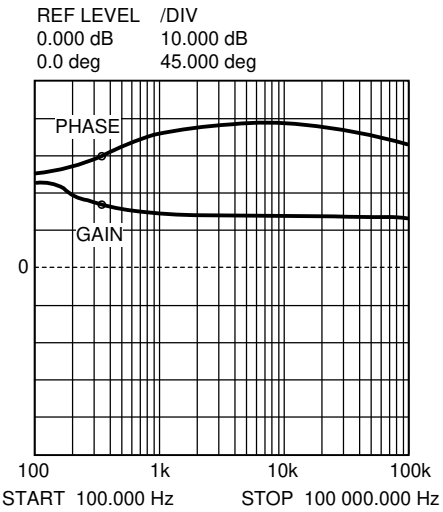


图 7-6. Error Amplifier Gain and Phase

The overall loop can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

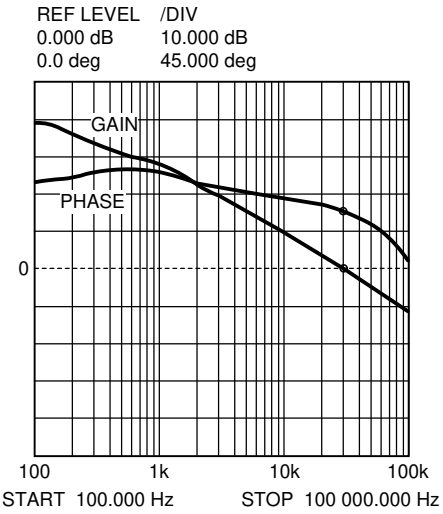


图 7-7. Overall Loop Gain and Phase

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot with a damped response. C6 can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C6 must be sufficiently small because the addition of this capacitor adds a pole in the error amplifier transfer function. This pole must be well beyond the loop crossover frequency. Use 方程式 17 to calculate a good approximation of the location of the pole added by C6.

$$f_{p2} = fz \times C5 / C6 \quad (17)$$

7.2.3 Application Curves

The following characteristics apply to the circuit shown in 图 7-3. These parameters are not tested and represent typical performance only. Unless otherwise stated, the following conditions apply: VIN = 24V, TA = 25°C.

图 7-8. DCM Steady State Ripple

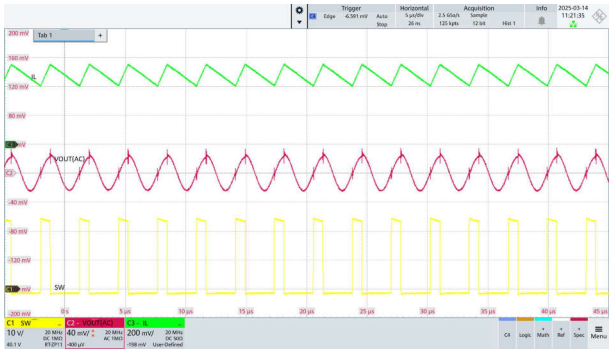


图 7-9. CCM Steady State Ripple

图 7-10. Load Regulation

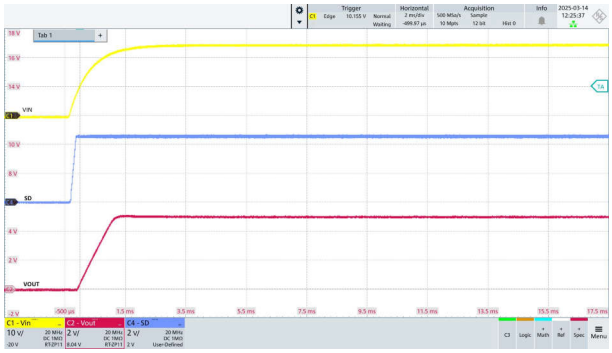


图 7-11. Start-Up Operation

7.3 Power Supply Recommendations

The characteristics of the input supply must be compatible with the specifications found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with the following equation

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (18)$$

Where

η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20µF to 100µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This action can lead to instability, as well as some of the effects mentioned above, unless designed carefully. *The AN-2162 Simple Success With Conducted EMI From DC/DC Converters* application note provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a snap-back characteristic (thyristor type). TI does not recommend the use of a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

7.4 Layout

7.4.1 Layout Guidelines

The circuit in 图 7-3 serves as both a block diagram of the LM5574-Q1 and a typical application board schematic for the LM5574-Q1. In a buck regulator there are two loops where currents are switched very fast. The first loop starts from the input capacitors, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the regulator IS pins, to the diode anode, to the inductor, and then out to the load. Minimize the loop area of these two loops to reduce the stray inductance and to minimize noise and possible erratic operation. A ground plane in the printed-circuit board (PCB) is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through the topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane.

The two highest power dissipating components are the re-circulating diode and the LM5574-Q1 regulator IC. The easiest method to determine the power dissipated within the LM5574-Q1 is to measure the total conversion losses (P_{IN} – P_{OUT}) then subtract the power losses in the Schottky diode, output inductor and snubber resistor. Use 方程式 19 to calculate an approximation for the Schottky diode.

$$P = (1 - D) \times Iout \times Vfwd. \quad (19)$$

Use 方程式 20 to calculate an approximation for the output inductor power.

$$P = I_{OUT}^{2} \times R \times 1.1 \quad (20)$$

where

- R is the DC resistance of the inductor
- and the 1.1 factor is an approximation for the AC losses.

If a snubber is used, use 方程式 21 to calculate an approximation for the damping resistor power dissipation.

$$P = V_{IN}^{2} \times Fsw \times Csnub \quad (21)$$

where

- where Fsw is the switching frequency
- and Csnub is the snubber capacitor.

The regulator has an exposed thermal pad to help power dissipation. Add several vias under the device to the ground plane to greatly reduce the regulator junction temperature. Select a diode with an exposed pad to help the power dissipation of the diode.

7.4.2 Layout Example

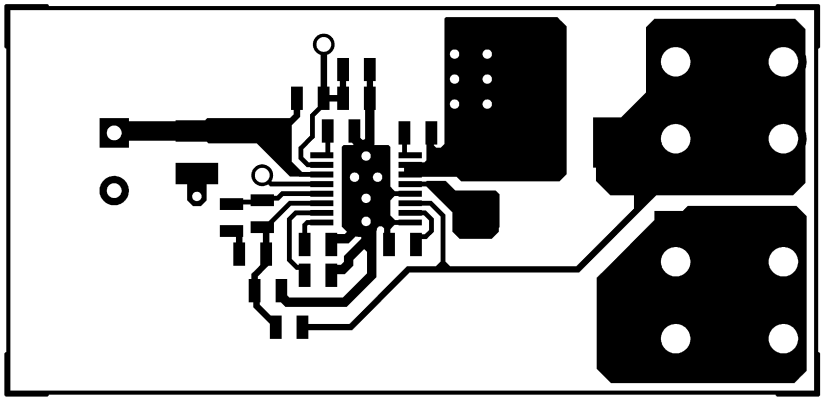


图 7-12. Component Side

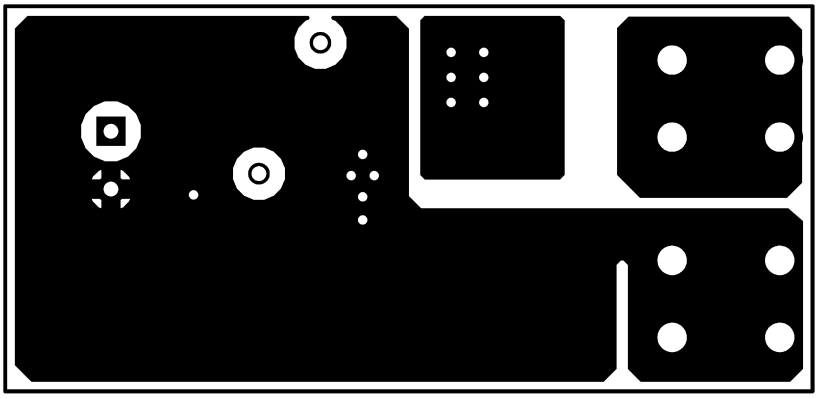


图 7-13. Solder Side

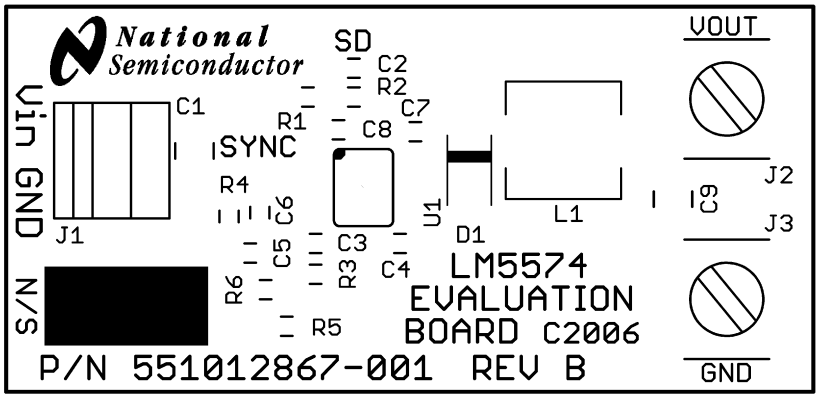


图 7-14. Silkscreen

7.4.3 Power Dissipation

The most significant variables that affect the power dissipated by the LM5574-Q1 are the output current, input voltage, and operating frequency. The power dissipated while operating near the maximum output current and maximum input voltage can be appreciable. The operating frequency of the LM5574 evaluation board has been designed for 300kHz.

7.4.4 Thermal Considerations

The junction-to-ambient thermal resistance of the LM5574-Q1 varies with the application. The most significant variables are the area of copper in the PCB and the amount of forced air cooling provided. The junction-to-ambient thermal resistance of the LM5574-Q1 mounted in the evaluation board varies from 90°C/W with no airflow to 60°C/W with 900 LFM (Linear Feet per Minute). With a 25°C ambient temperature and no airflow, the predicted junction temperature for the LM5574-Q1 is 25 + ((90 × 0.6) = 79°C. If the evaluation board is operated at 0.5A output current, 70V input voltage and high ambient temperature for a prolonged period of time the thermal shutdown protection within the IC can activate. The IC turns off to allow the junction to cool, followed by restart with the soft-start capacitor reset to zero.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5574-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2014) to Revision D (April 2025) **Page**

Changes from Revision B (April 2013) to Revision C (October 2014) **Page**

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5574Q0MT/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-	LM5574 Q0MT
LM5574Q0MT/NOPB.A	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 Q0MT
LM5574Q0MT/NOPB.B	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 Q0MT
LM5574Q0MTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	LM5574 Q0MT
LM5574Q0MTX/NOPB.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 Q0MT
LM5574Q0MTX/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 Q0MT
LM5574QMT/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 QMT
LM5574QMT/NOPB.A	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 QMT
LM5574QMT/NOPB.B	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 QMT
LM5574QMTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 QMT
LM5574QMTX/NOPB.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 QMT
LM5574QMTX/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5574 QMT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LM5574-Q1 :

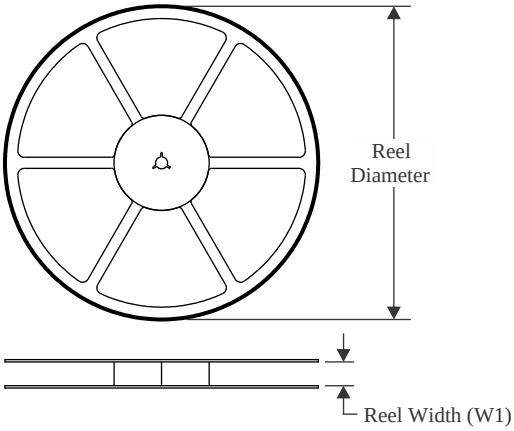
- Catalog : LM5574

NOTE: Qualified Version Definitions:

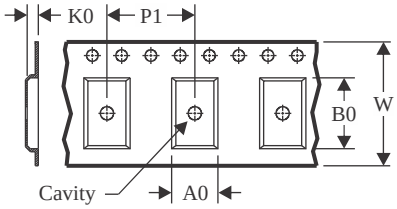
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

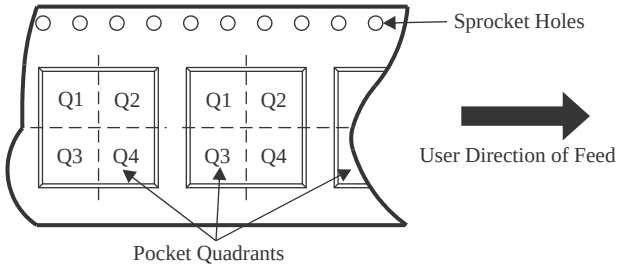


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

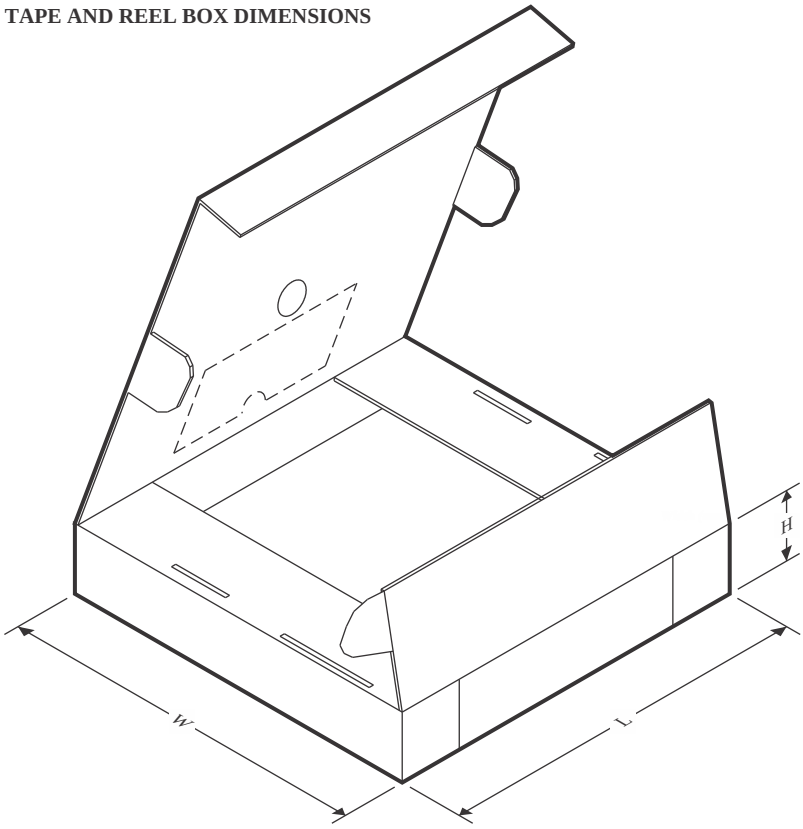
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5574Q0MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5574QMTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

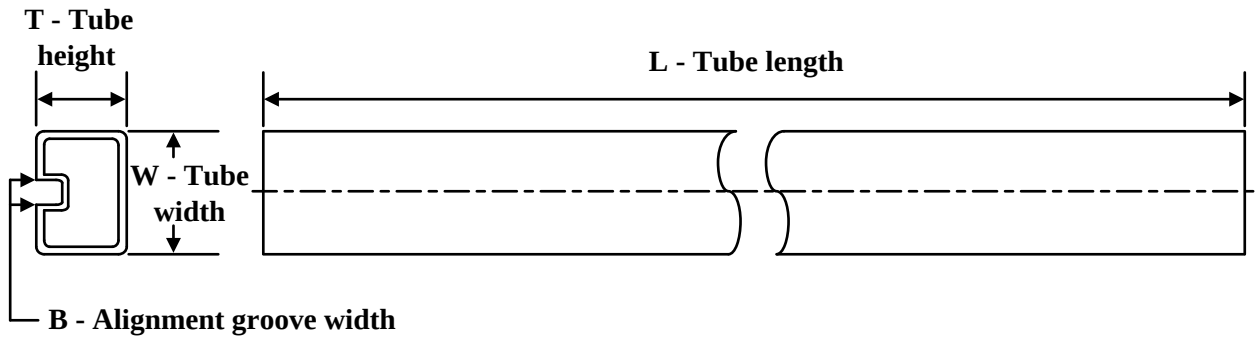
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5574Q0MTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5574QMTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

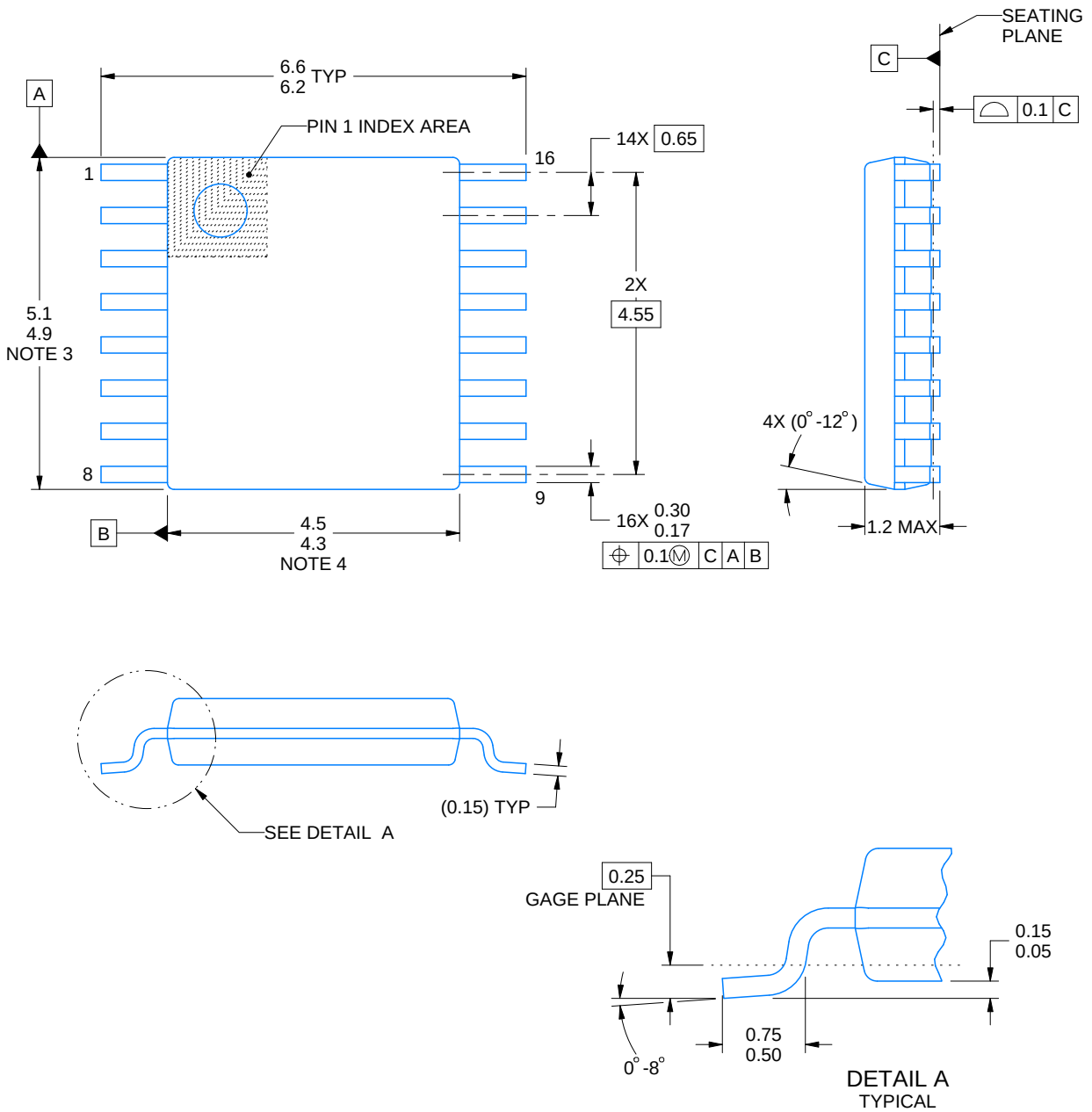
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5574Q0MT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5574Q0MT/NOPB.A	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5574Q0MT/NOPB.B	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5574QMT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5574QMT/NOPB.A	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5574QMT/NOPB.B	PW	TSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0016A

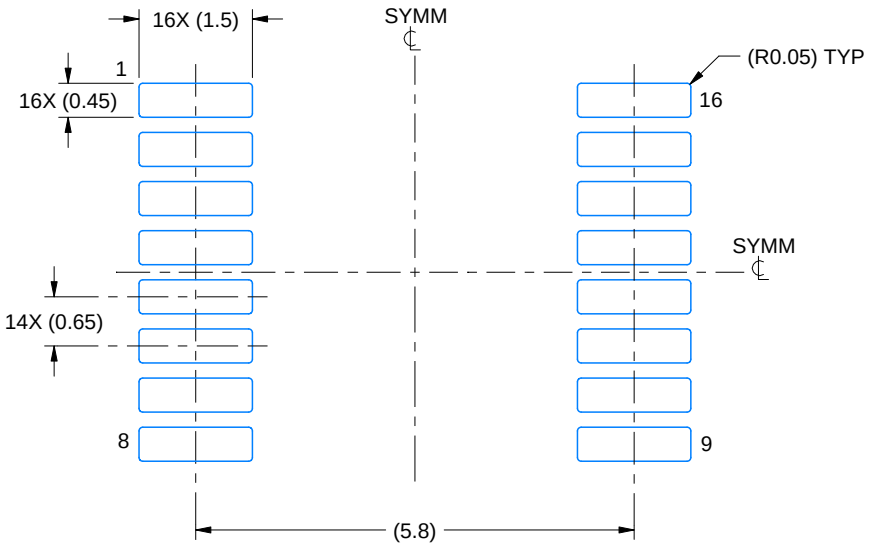
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



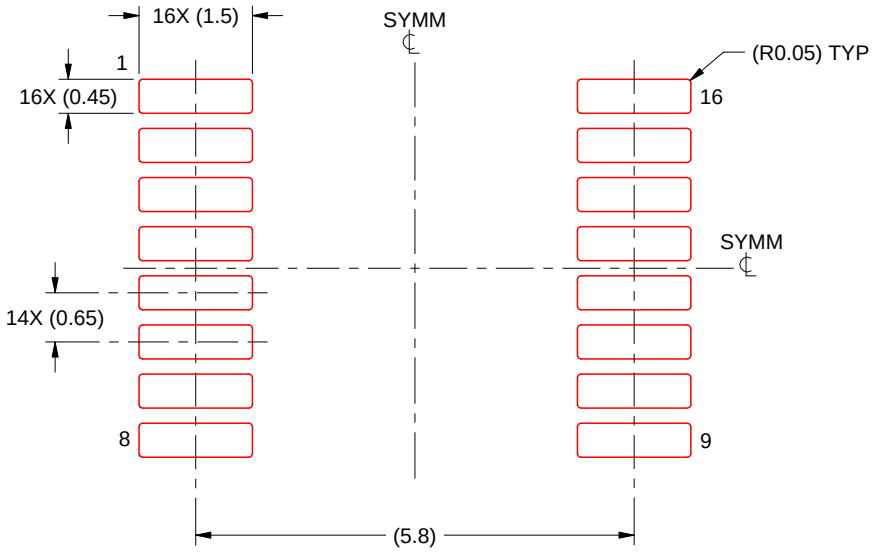
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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