采用双随机展频技术的 LM5158x 2.2MHz 宽输入电压 85V 输出升压/SEPIC/反激式转换器

1 特性

- 适用于电池应用中的宽工作电压范围
  - 3.2V 至 60V 输入电压工作范围（绝对最大值 65V）
  - 最大输出电压为 83V（最大绝对电压为 85V）
  - BIAS 电压大于等于 3.2 V 时最小升压电源电压为 1.5V
  - 高达 65V 的输入瞬态保护
  - 最小电池消耗
    - 低关断电流 (I_Q ≤ 2.6μA)
    - 低工作电流 (I_Q ≤ 670μA)
- 解决方案尺寸小、成本低
  - 开关频率高达 2.2MHz（最大值）
  - 16 引脚 QFN 封装 (3mm × 3mm)
  - 集成的误差放大器支持在没有光耦合器的情况下进行初级侧稳压（反激）
  - 精确的电流限制（请参阅*器件比较表*）
- 缓减 EMI
  - 可选双随机展频
  - 无引线封装
- 低功耗、高效率
  - 133mΩ R_{DSON} 开关
  - 快速开关，开关损耗低
- 避免 AM 频带干扰和串扰
  - 可选的时钟同步
  - 100kHz 至 2.2MHz 的动态可编程宽开关频率范围
- 集成型保护特性
  - 在输入电压范围内具有恒定电流限制
  - 可选间断模式过载保护
  - 可编程线路 UVLO
  - OVP 保护
  - 热关断保护
- 精确的 ±1% 精度反馈基准
- 可调软启动
- PGOOD 指示器
- 使用 LM5158x 并借助 WEBENCH® Power Designer 创建定制设计

2 应用

- 电池供电的宽输入升压、SEPIC 和反激式转换器
- LED 偏置电源
- 无光耦合器的多输出反激式应用
- 环路供电式火灾探测
- 保持电容器充电器
- 电源模块
- 工业 PLC
- 逆变器偏置电源
- 压电式驱动器/电机驱动器偏置电源

3 说明

LM5158x 器件是一款具有集成式 85V、3.26A (LM5158) 或 85V、1.63A (LM51581) 电源开关和宽输入范围的非同步升压转换器。

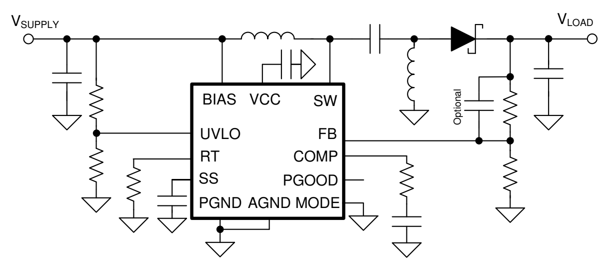
该器件可用于升压、SEPIC 和反激式拓扑。该器件可由电压至少为 3.2V 的单芯电池启动。如果 BIAS 引脚的电压高于 3.2V，该器件可在低至 1.5V 的输入电源电压下运行。

BIAS 引脚可在高达 60V（最大绝对值为 65V）的电压下运行。用户可通过外部电阻器对开关频率进行动态编程，编程范围为 100kHz 至 2.2MHz。2.2MHz 的开关频率可最大限度地降低 AM 频带干扰，并支持实现小解决方案尺寸和快速瞬态响应。该器件提供可选的双随机展频技术，可在宽频率范围内降低 EMI。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM5158	WQFN (16)	3.00mm × 3.00mm
LM51581		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型 SEPIC 应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
October 2021	*	Initial Release

5 说明（续）

该器件在输入电压范围内具有准确的峰值电流限制，可避免对功率电感器进行过度设计。运行低电流和脉冲跳跃模式可在轻负载时提高效率。

该器件具有内置保护特性，例如过压保护、线路 UVLO、热关断和可选的断续模式过载保护。其他特性包括低关断 I_Q、可编程软启动、精密补偿、电源正常指示器以及外部时钟同步。

6 Device Comparison Table

DEVICE OPTION	MINIMUM PEAK CURRENT LIMIT	MAXIMUM SW VOLTAGE
LM5158	3.26 A	83 V (85-V abs max)
LM51581	1.63 A	

7 Pin Configuration and Functions

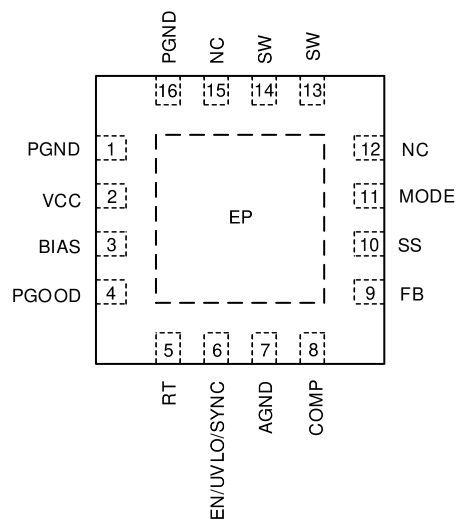


图 7-1. RTE Package 16-Pin WQFN Top View

表 7-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1, 16	PGND	P	Power ground pin. Source connection of the internal N-channel power MOSFET
2	VCC	P	Output of the internal VCC regulator and supply voltage input of the internal MOSFET driver. Connect a 1-µF ceramic bypass capacitor from this pin to PGND.
3	BIAS	P	Supply voltage input to the VCC regulator. Connect a bypass capacitor from this pin to PGND.
4	PGOOD	O	Power-good indicator. An open-drain output, which goes low if FB is below the undervoltage threshold (V_{UVTH}). Connect a pullup resistor to the system voltage rail.
5	RT	I	Switching frequency setting pin. The switching frequency is programmed by a single resistor between RT and AGND.
6	EN/UVLO/ SYNC	I	Enable pin. The converter shuts down when the pin is less than the enable threshold (V_{EN}).
			Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a voltage divider. If using a programmable UVLO, connect the low-side UVLO resistor to AGND. This pin must not be left floating. Connect to the BIAS pin if not used.
			External synchronization clock input pin. The internal clock can be synchronized to an external clock by applying a negative pulse signal into the pin.
7	AGND	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
8	COMP	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and AGND.
9	FB	I	Inverting input of the error amplifier. Connect a voltage divider to set the output voltage in boost, SEPIC, or primary-side regulated flyback topologies. Connect the low-side feedback resistor as close to AGND as possible.
10	SS	I	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. Connect the ground connection of the capacitor to AGND.
11	MODE	I	MODE = 0 V or connect to AGND during initial power up: Hiccup mode protection is disabled and spread spectrum is disabled.
			MODE = 370 mV or connect a 37.4-kΩ resistor between this pin and AGND during initial power up: Hiccup mode protection is enabled and spread spectrum is enabled.
			MODE = 620 mV or connect a 62.0-kΩ resistor between this pin and AGND during initial power up: Hiccup mode protection is enabled and spread spectrum is disabled.
			MODE > 1 V or connect a 100-kΩ resistor between this pin and AGND during initial power up: Hiccup mode protection is disabled and spread spectrum is enabled.

表 7-1. Pin Functions (continued)

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
13, 14	SW		Switch pin. Drain connection of the internal N-channel power MOSFET
12, 15	NC	—	No internal electrical contact
—	EP	—	Exposed pad of the package. The exposed pad must be connected to AGND and the large ground copper plane to decrease thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range[(1)]

		MIN	MAX	UNIT
Input	BIAS to AGND	–0.3	65	V
	UVLO to AGND	–0.3	V_{BIAS} + 0.3	
	SS, RT to AGND[(2)]	–0.3	3.8	
	FB to AGND	–0.3	4.0	
	MODE to AGND	–0.3	3.8	
	PGND to AGND	–0.3	0.3	
Output	VCC to AGND	–0.3	5.8[(3)]	V
	PGOOD to AGND[(4)]	–0.3	18	
	COMP to AGND[(5)]	–0.3		
	SW to AGND (DC)	–0.3	85	
	SW to AGND (5-ns transient)	–6		
Junction temperature, T_J [(6)]		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) These pins are not specified to have an external voltage applied.
(3) Operating lifetime is de-rated when the pin voltage is greater than 5.5 V.
(4) The maximum current sink is limited to 1 mA when V_{PGOOD} > V_{BIAS}.
(5) This pin has an internal max voltage clamp which can handle up to 1.6 mA.
(6) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range[(1)]

		MIN	NOM	MAX	UNIT
V_{SUPPLY}	Boost converter input (when BIAS ≥ 3.2 V)	1.5		60	V
V_{LOAD}	Boost converter output	V_{SUPPLY}		83[(2)]	V
V_{BIAS}	BIAS input[(3)]	3.2		60	V
V_{UVLO}	UVLO input	0		60	V
V_{FB}	FB input	0		4.0	V
I_{SW}	Switch current	0		See note[(4)]	A
f_{SW}	Typical switching frequency	100		2200	kHz
f_{SYNC}	Synchronization pulse frequency	100		2200	kHz
T_J	Operating junction temperature	–40		125	°C

(1) *Recommended Operating Conditions* are conditions under the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics*.
(2) The boost converter output can be up to 83 V, but the SW pin voltage should be less than or equal to 85 V during transient.
(3) The BIAS pin operating range is from 3.2 V to 60 V when VCC is supplied from the internal VCC regulator.

(4) The maximum switch current is limited by pre-programmed peak current limit (I_{LIM}) when $T_J < T_{TSD}$.

8.4 Thermal Information

THERMAL METRIC[(1)]		LM5158x RTE(QFN) 16 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance (LM5158EVM-BST)	32.7	°C/W
$R_{θJA}$	Junction-to-ambient thermal resistance	45.6	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	44.8	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	19.1	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter (LM5158EVM-BST)	0.6	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	0.8	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter (LM5158EVM-BST)	15.1	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	19.1	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{SHUTDOWN(BIAS)}$	BIAS shutdown current	V_{BIAS} = 12 V, V_{UVLO} = 0 V		2.6	5	µA
$I_{OPERATING(BIAS)}$	BIAS operating current	V_{BIAS} = 12 V, V_{UVLO} = 2.0 V, V_{FB} = V_{REF}, R_T = 220 kΩ		670	850	µA
VCC REGULATOR						
$V_{VCC-REG}$	VCC regulation	V_{BIAS} = 8 V, I_{VCC} = 18 mA	4.66	4.9	5.14	V
$V_{VCC-UVLO(RISING)}$	VCC UVLO threshold	VCC rising	3.05	3.10	3.15	V
	VCC UVLO hysteresis	VCC falling		0.1		V
ENABLE						
$V_{EN(RISING)}$	Enable threshold	EN rising	0.4	0.52	0.7	V
$V_{EN(FALLING)}$	Enable threshold	EN falling	0.33	0.49	0.63	V
$V_{EN(HYS)}$	Enable hysteresis	EN falling		0.03		V
UVLO/SYNC						
$V_{UVLO(RISING)}$	UVLO / SYNC threshold	UVLO rising	1.425	1.5	1.575	V
$V_{UVLO(FALLING)}$	UVLO / SYNC threshold	UVLO falling	1.370	1.45	1.520	V
$V_{UVLO(HYS)}$	UVLO / SYNC threshold hysteresis	UVLO falling		0.05		V
I_{UVLO}	UVLO hysteresis current	V_{UVLO} = 1.6 V	4	5	6	µA
MODE, SPREAD SPECTRUM						
	F_{SW} modulation (upper limit)			7.8%		
	F_{SW} modulation (lower limit)			–7.8%		
SOFT START						
I_{SS}	Soft-start current		9	10	11	µA
	SS pulldown switch R_{DSON}			50		Ω
PULSE WIDTH MODULATION						
fsw1	Switching frequency	R_T = 220 kΩ	85	100	115	kHz

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
fsw2	Switching frequency	R_T = 49.3 kΩ	388	440	492	kHz
fsw3	Switching frequency	R_T = 9.09 kΩ	1980	2200	2420	kHz
$t_{ON(MIN)}$	Minimum on time	R_T = 9.09 kΩ		80		ns
D_{MAX1}	Maximum duty cycle limit	R_T = 9.09 kΩ	80%	85%	90%	
D_{MAX2}	Maximum duty cycle limit	R_T = 220 kΩ	90%	93%	96%	
	RT regulation voltage			0.5		V
CURRENT LIMIT						
I_{LIM}	Internal MOSFET current limit	LM5158	3.26	3.75	4.24	A
	Internal MOSFET current limit	LM51581	1.63	1.875	2.12	A
HICCUP MODE PROTECTION						
	Hiccup enable cycles			64		Cycles
	Hiccup timer reset cycles			8		Cycles
ERROR AMPLIFIER						
V_{REF}	FB reference		0.99	1	1.01	V
Gm	Transconductance			2		mA/V
	COMP sourcing current	V_{COMP} = 1.2 V	180			µA
	COMP clamp voltage	COMP rising (V_{UVLO} = 2.0 V)	2.5	2.8		V
	COMP clamp voltage	COMP falling		1	1.1	V
A_{CS}	$\Delta V_{COMP} / \Delta I_{SW}$			0.19		
OVP						
V_{OVTH}	Overvoltage threshold	FB rising (reference to V_{REF})	107%	110%	113%	
	Overvoltage threshold	FB falling (reference to V_{REF})		105%		
PGOOD						
	PGOOD pulldown switch R_{DSON}	1-mA sinking		70		Ω
V_{UVTH}	Undervoltage threshold	FB falling (reference to V_{REF})	87%	90%	93%	
	Undervoltage threshold	FB rising (reference to V_{REF})		95%		
POWER SWITCH						
$r_{DS(ON)}$	Internal MOSFET on-resistance	V_{BIAS} = 12 V		133	290	mΩ
		V_{BIAS} = 3.5 V		138	300	mΩ
	Leakage current	V_{SW} = 12 V			1100	nA
THERMAL SHUTDOWN						
T_{TSD}	Thermal shutdown threshold	Temperature rising		175		°C
	Thermal shutdown hysteresis			15		°C

8.6 Typical Characteristics

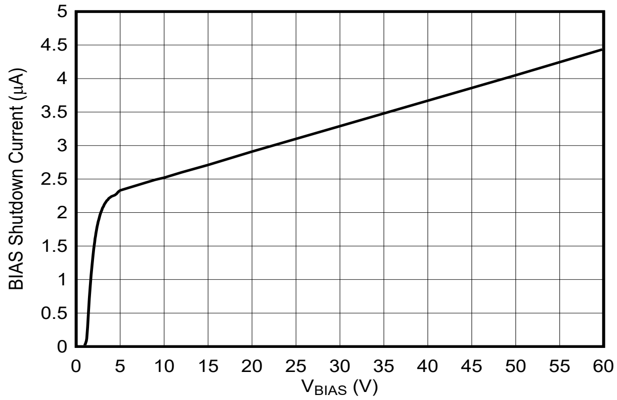


图 8-1. BIAS Shutdown Current vs V_{BIAS}

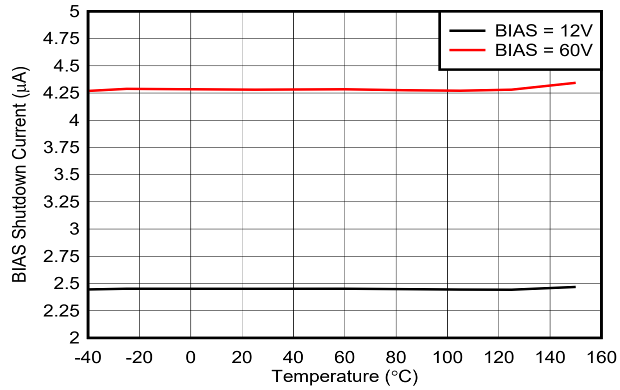


图 8-2. BIAS Shutdown Current vs Temperature

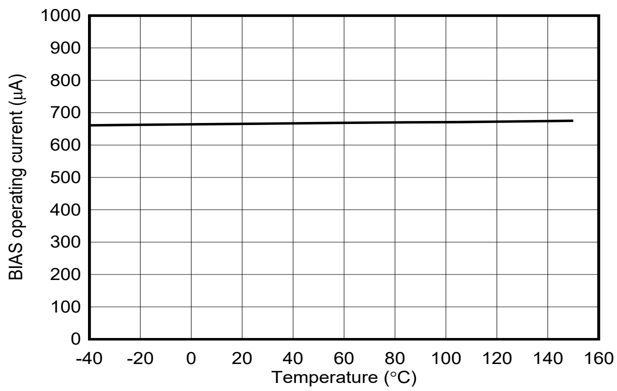


图 8-3. BIAS Operating Current vs Temperature

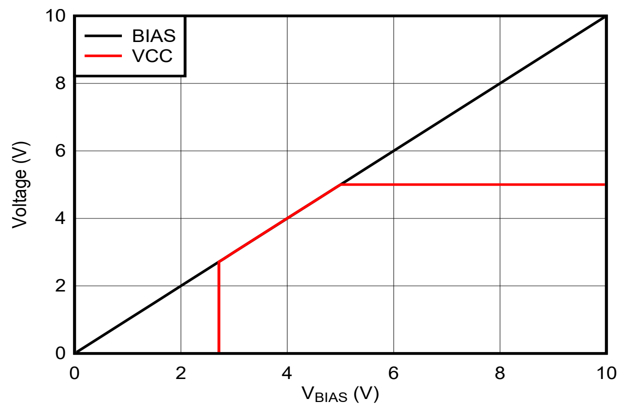


图 8-4. V_{VCC} vs V_{BIAS}

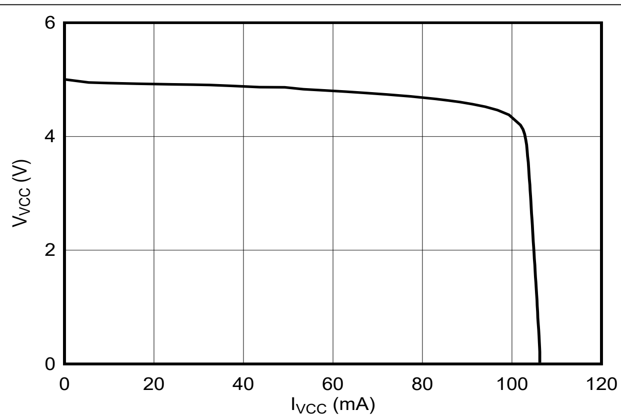


图 8-5. V_{VCC} vs I_{VCC}

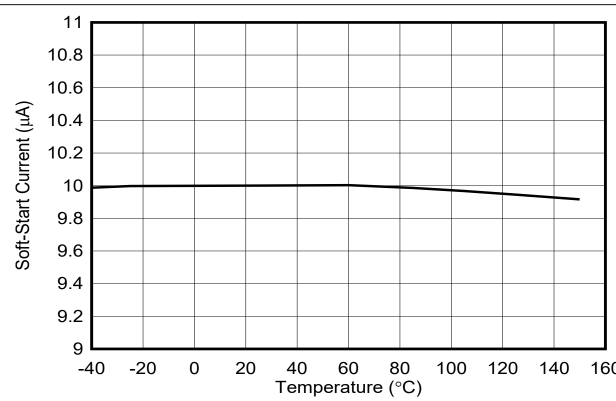


图 8-6. I_{SS} vs Temperature

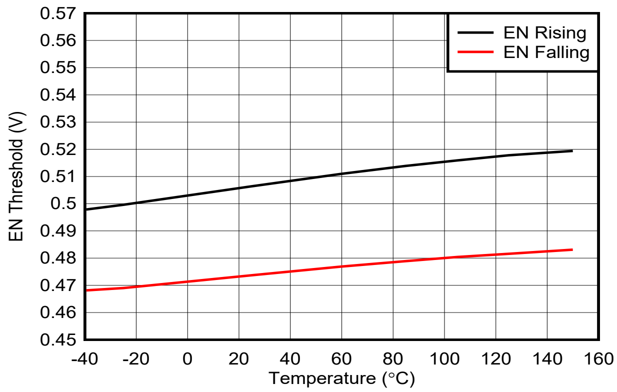


图 8-7. EN Threshold vs Temperature

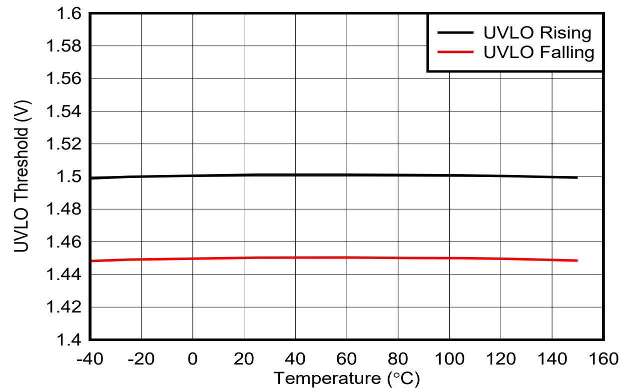


图 8-8. UVLO Threshold vs Temperature

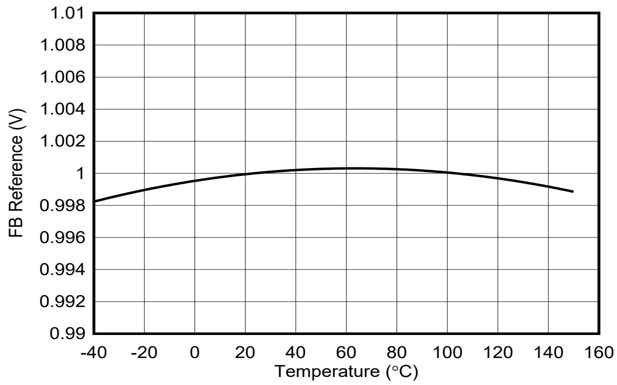


图 8-9. FB Reference vs Temperature

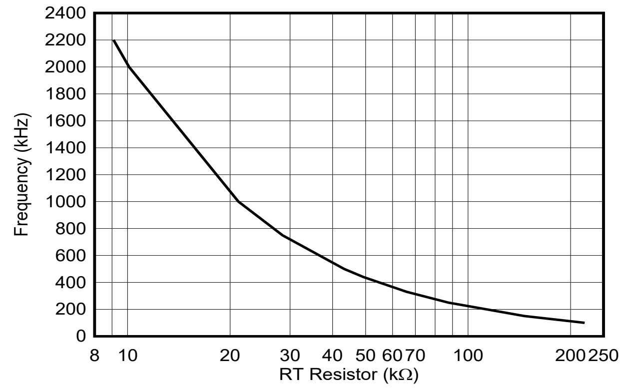


图 8-10. Frequency vs RT Resistance

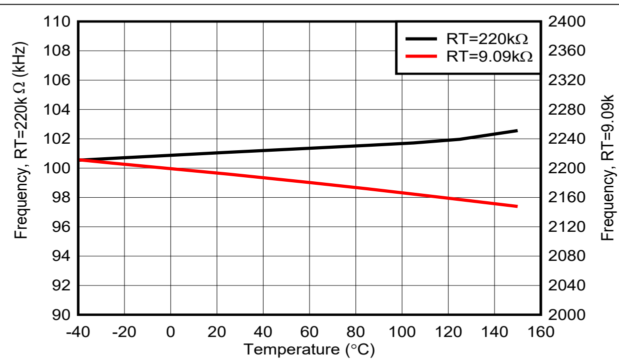


图 8-11. Frequency vs Temperature

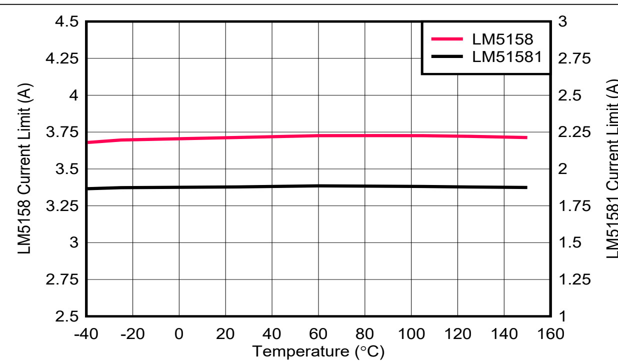


图 8-12. Current Limit Threshold vs Temperature

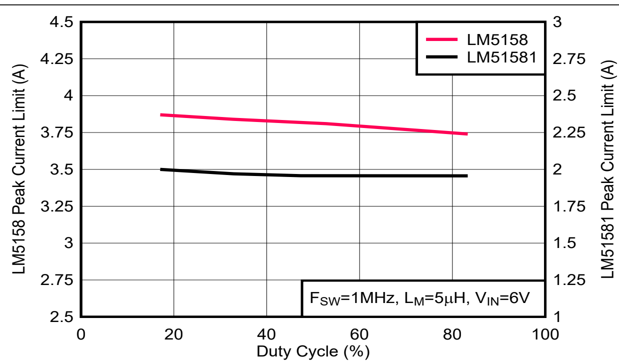


图 8-13. Peak Current Limit vs Duty Cycle

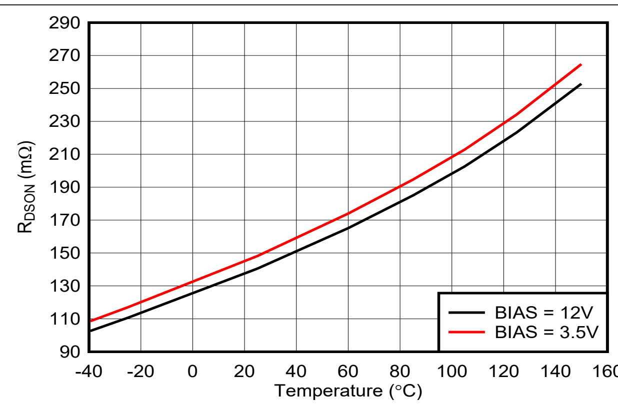


图 8-14. Internal MOSFET Drain Source On-state Resistance vs Temperature

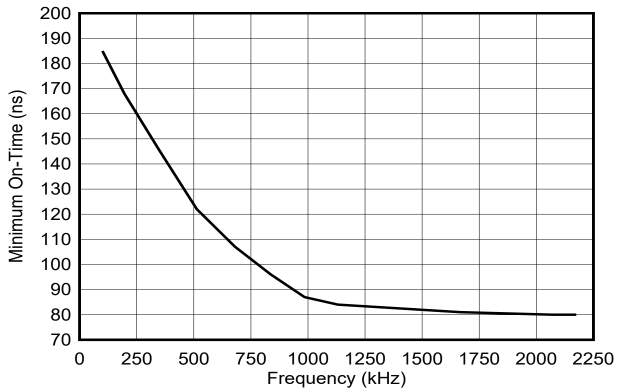


图 8-15. Minimum On Time vs Frequency

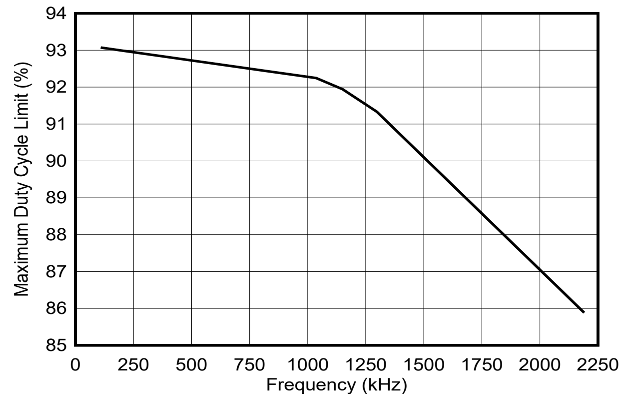


图 8-16. Maximum Duty Cycle Limit vs Frequency

9 Detailed Description

9.1 Overview

The LM5158x is a wide input range, non-synchronous boost converter that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

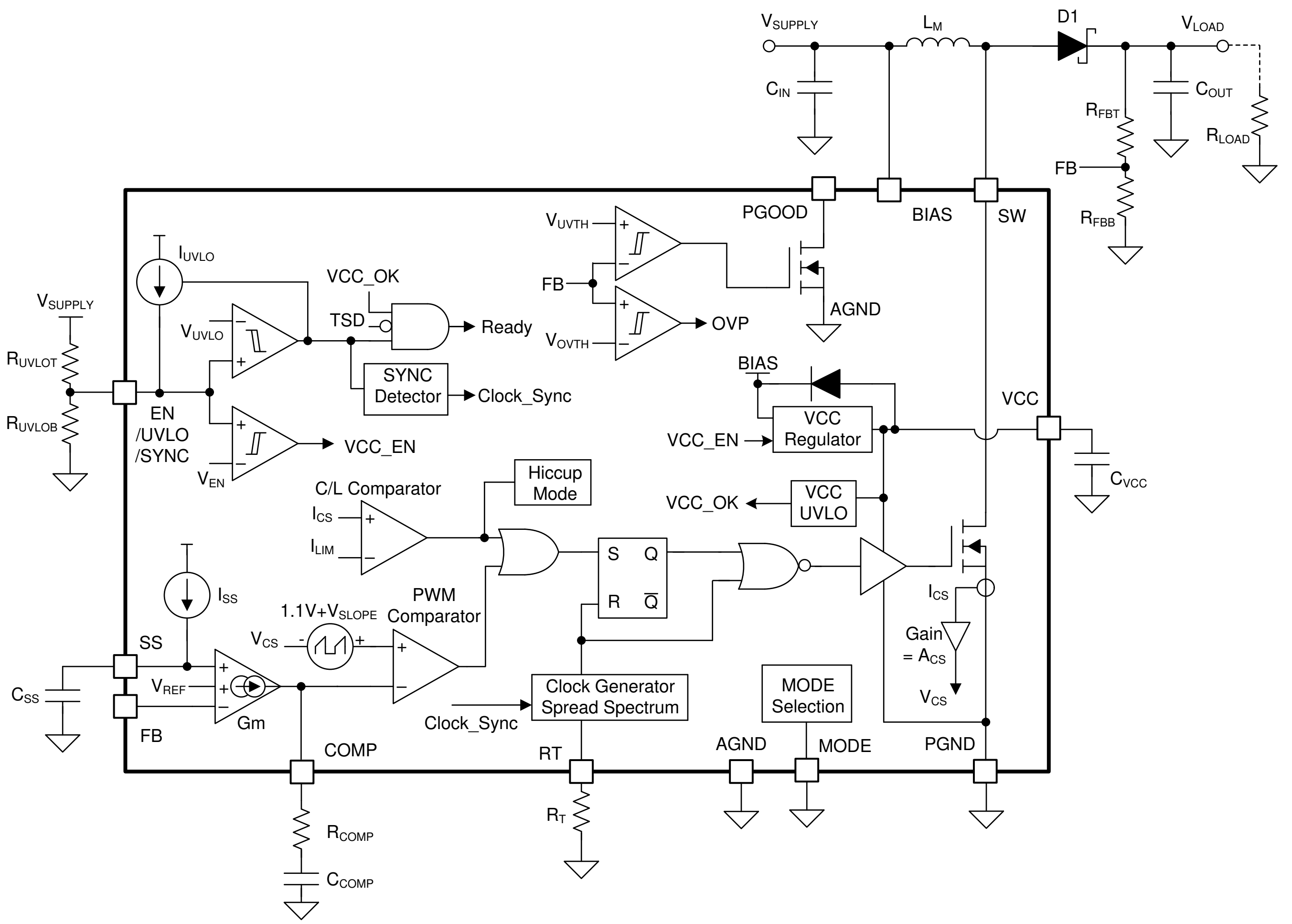
The device can start up with a minimum of 3.2 V. It can operate with input supply voltage as low as 1.5 V if the BIAS pin is greater than 3.2 V. The internal VCC regulator also supports BIAS pin operation up to 60 V (65-V absolute maximum). The switching frequency is dynamically programmable from 100 kHz to 2.2 MHz with an external resistor. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response. The device provides an optional dual random spread spectrum to help reduce the EMI over a wide frequency span.

The device features an accurate current limit over the input voltage range. Low operating current and pulse skipping operation improve efficiency at light loads.

The device also has built-in protection features such as overvoltage protection, line UVLO, and thermal shutdown. Selectable hiccup mode overload protection protects the converter during prolonged current limit conditions. Additional features include the following:

- Low shutdown I_Q
- Programmable soft start
- Precision reference
- Power-good indicator
- External clock synchronization

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Line Undervoltage Lockout (EN/UVLO/SYNC Pin)

The device has a dual-level EN/UVLO circuit. During power-on, if the BIAS pin voltage is greater than 2.7 V, the UVLO pin voltage is in between the enable threshold (V_{EN}), and the UVLO threshold (V_{UVLO}) for more than 1.5 µs (see 节 9.3.6 for more details), the device starts up and an internal configuration starts. The device typically requires a 90-µs internal start-up delay before entering standby mode. In standby mode, the VCC regulator and RT regulator are operational, the SS pin is grounded, and there is no switching at the SW pin.

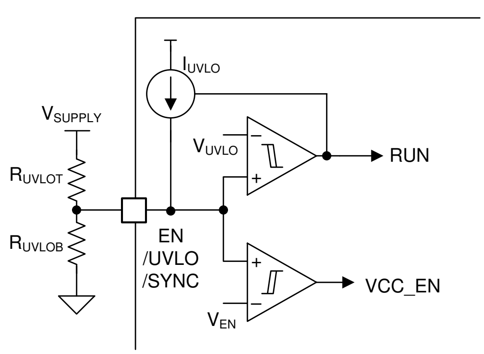


图 9-1. Line UVLO and Enable

When the UVLO pin voltage is above the UVLO threshold, the device enters run mode. In run mode, a soft-start sequence starts if the VCC voltage is greater than VCC UV threshold ($V_{VCC\text{-}UVLO}$). UVLO hysteresis is accomplished with an internal 50-mV voltage hysteresis and an additional 5-μA current source that is switched on or off. When the UVLO pin voltage exceeds the UVLO threshold, the UVLO hysteresis current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the UVLO threshold, the current source is disabled, causing the voltage at the UVLO pin to fall quickly. When the UVLO pin voltage is less than the enable threshold (V_{EN}), the device enters shutdown mode after a 40-μs (typical) delay with all functions disabled.

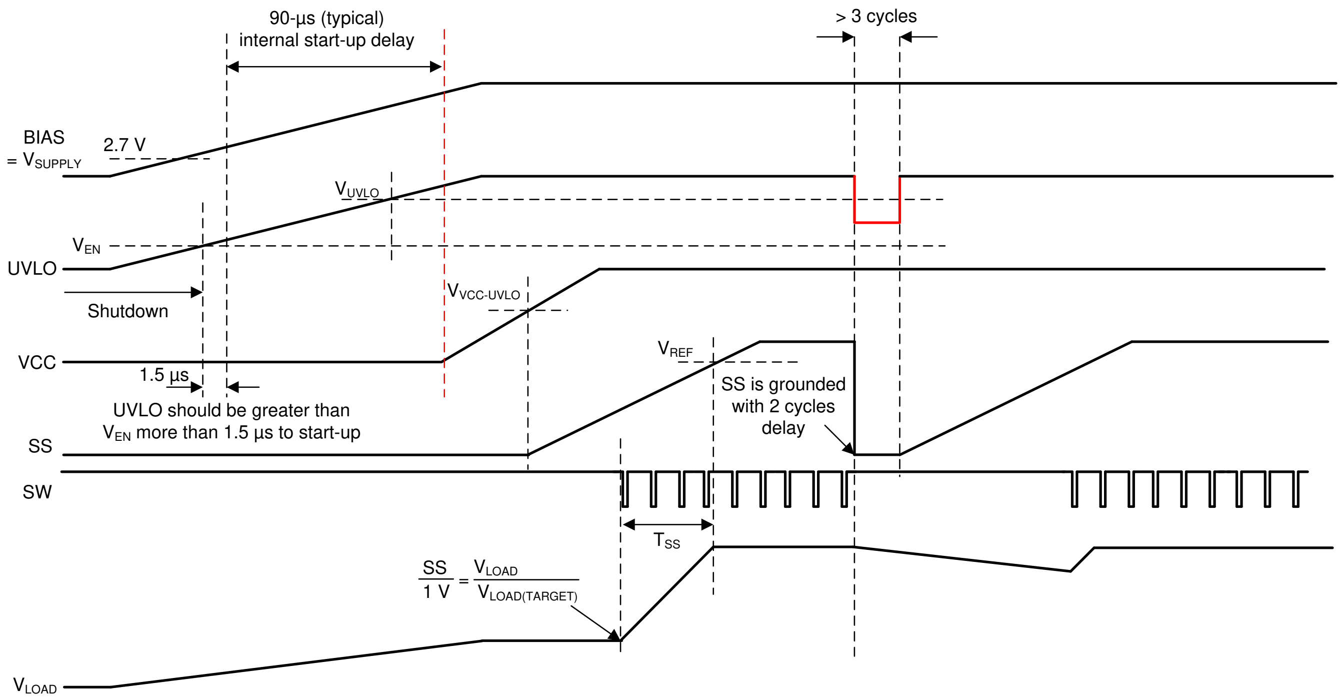


图 9-2. Boost Start-Up Waveforms Case 1: Start-Up by VCC UVLO, UVLO Toggle After Start-Up

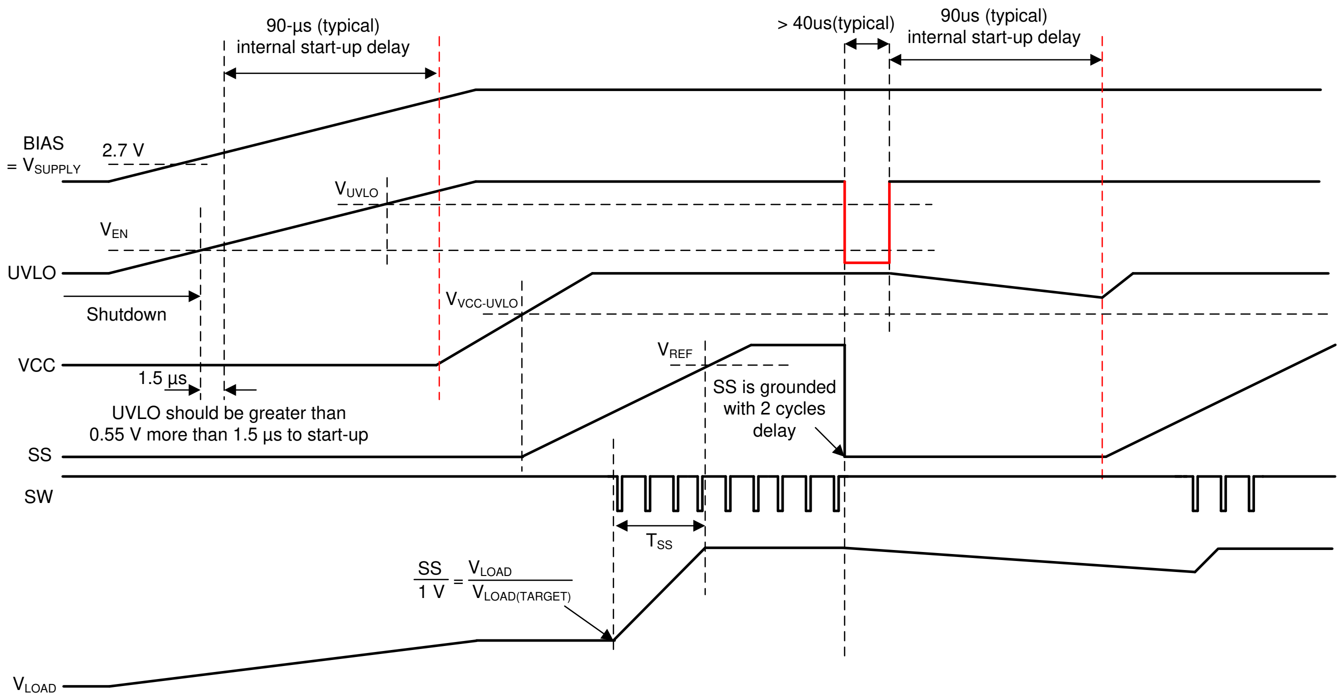


图 9-3. Boost Start-Up Waveforms Case 2: Start-Up by VCC UVLO, EN Toggle After Start-Up

The external UVLO resistor divider must be designed so that the voltage at the UVLO pin is greater than 1.5 V (typical) when the input voltage is in the desired operating range. The values of R_{UVLOT} and R_{UVLOB} can be calculated as shown in 方程式 1 and 方程式 2.

$$R_{UVLOT} = \frac{V_{SUPPLY(ON)} \times \frac{V_{UVLO(FALLING)}}{V_{UVLO(RISING)}} - V_{SUPPLY(OFF)}}{I_{UVLO}} \tag{1}$$

where

- $V_{SUPPLY(ON)}$ is the desired start-up voltage of the converter.
- $V_{SUPPLY(OFF)}$ is the desired turn-off voltage of the converter.

$$R_{UVLOB} = \frac{V_{UVLO(RISING)} \times R_{UVLOT}}{V_{SUPPLY(ON)} - V_{UVLO(RISING)}} \tag{2}$$

A UVLO capacitor (C_{UVLO}) is required in case the input voltage drops below the $V_{SUPPLY(OFF)}$ momentarily during the start-up or during a severe load transient at the low input voltage. If the required UVLO capacitor is large, an additional series UVLO resistor (R_{UVLOS}) can be used to quickly raise the voltage at the UVLO pin when the 5-µA hysteresis current turns on.

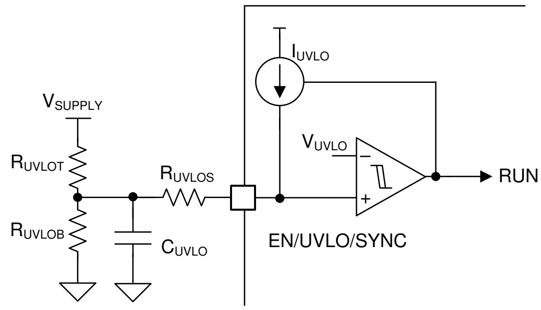


图 9-4. Line UVLO Using Three UVLO Resistors

Do not leave the UVLO pin floating. Connect to the BIAS pin if not used.

9.3.2 High Voltage VCC Regulator (BIAS, VCC Pin)

The device has an internal wide input VCC regulator that is sourced from the BIAS pin. The wide input VCC regulator allows the BIAS pin to be connected directly to supply voltages from 3.2 V to 60 V (transient protection up to 65 V).

The VCC regulator turns on when the device is in standby or run mode. When the BIAS pin voltage is below the VCC regulation target, the VCC output tracks the BIAS with a small dropout voltage. When the BIAS pin voltage is greater than the VCC regulation target, the VCC regulator provides a 5-V supply (typical) for the device and the internal N-channel MOSFET driver.

The VCC regulator sources current into the capacitor connected to the VCC pin. The recommended VCC capacitor value is 1 µF.

The minimum supply voltage after start-up can be further decreased by supplying the BIAS pin from the boost converter output or from an external power supply as shown in 图 9-5. Also, this configuration allows the device to handle more power when the V_{SUPPLY} is less than 5 V. Practical minimum supply voltage after start-up is decided by the maximum duty cycle limit (D_{MAX}).

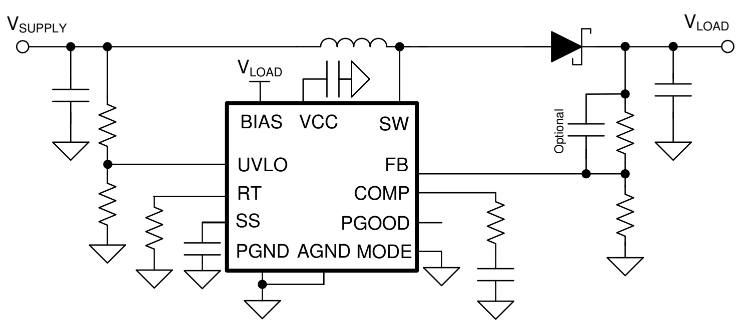


图 9-5. Decrease the Minimum Operating Voltage After Start-Up

In flyback topology, the internal power dissipation of the device can be decreased by supplying the BIAS using an additional transformer winding, especially in PSR flyback. In this configuration, the external BIAS supply voltage (V_{AUX}) must be greater than the regulation target of the external LDO, and the BIAS pin voltage must always be greater than 3.2 V.

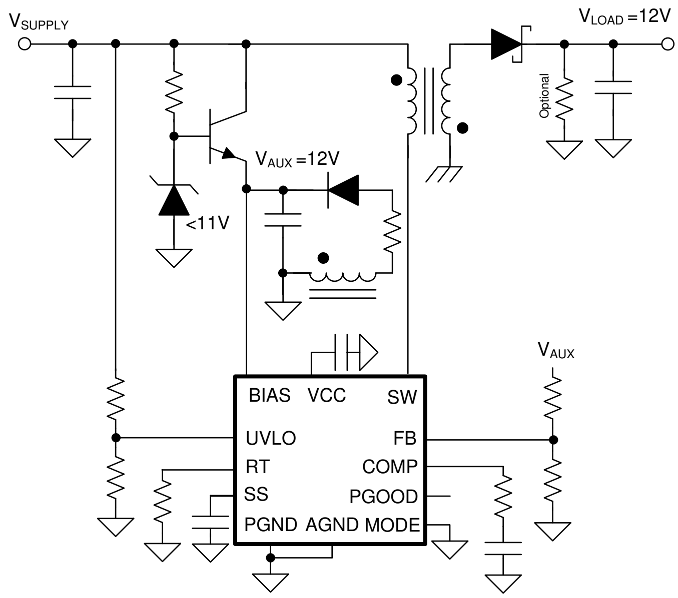


图 9-6. External BIAS Supply (PSR Flyback)

9.3.3 Soft Start (SS Pin)

The soft-start feature helps the converter gradually reach the steady state operating point, thus reducing start-up stresses and surges. The device regulates the FB pin to the SS pin voltage or the internal reference, whichever is lower.

At start-up, the internal 10-µA soft-start current source (I_{SS}) turns on after the VCC voltage exceeds the VCC UV threshold. The soft-start current gradually increases the voltage on an external soft-start capacitor connected to the SS pin. This results in a gradual rise of the output voltage. The SS pin is pulled down to ground by an internal switch when the VCC is less than the VCC UVLO threshold, the UVLO is less than the UVLO threshold, during hiccup mode off time or thermal shutdown.

In boost topology, soft-start time (t_{SS}) varies with the input supply voltage. The soft-start time in boost topology is calculated as shown in 方程式 3.

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \times \left(1 - \frac{V_{SUPPLY}}{V_{LOAD}}\right) \tag{3}$$

In SEPIC topology, the soft-start time (t_{SS}) is calculated as follows.

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \tag{4}$$

TI recommends choosing the soft-start time long enough so that the converter can start up without going into an overcurrent state. See 节 9.3.11 for more detailed information.

图 9-7 shows an implementation of primary-side soft start in flyback topology.

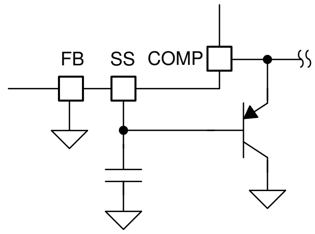


图 9-7. Primary-Side Soft Start in Flyback

图 9-8 shows an implementation of secondary-side soft start in flyback topology.

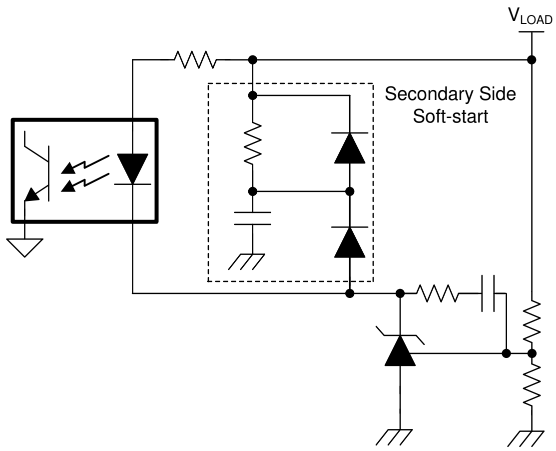


图 9-8. Secondary-Side Soft Start in Flyback

9.3.4 Switching Frequency (RT Pin)

The switching frequency of the device can be set by a single RT resistor connected between the RT and the AGND pins. The resistor value to set the RT switching frequency (f_{RT}) is calculated as shown in 方程式 5.

$$R_T = \frac{2.21 \times 10^{10}}{f_{RT(TYPICAL)}} - 955 \tag{5}$$

The RT pin is regulated to 0.5 V by the internal RT regulator when the device is enabled.

9.3.5 Dual Random Spread Spectrum – DRSS (MODE Pin)

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. This function is enabled by a single resistor (37.4 kΩ or 100 kΩ) between the MODE pin and the AGND pin or by programming the MODE pin voltage (370 mV or greater than 1.0 V) during initial power up. When spread spectrum is enabled, the internal modulator dithers the internal clock. When an external synchronization clock is applied to the SYNC pin, the internal spread spectrum is disabled. DRSS (a) combines a low frequency triangular modulation profile (b) with a high frequency cycle-by-cycle random modulation profile (c). The low frequency triangular modulation improves performance in lower radio frequency bands (for example, the AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example, the FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. In order to minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled (see 图 9-9).

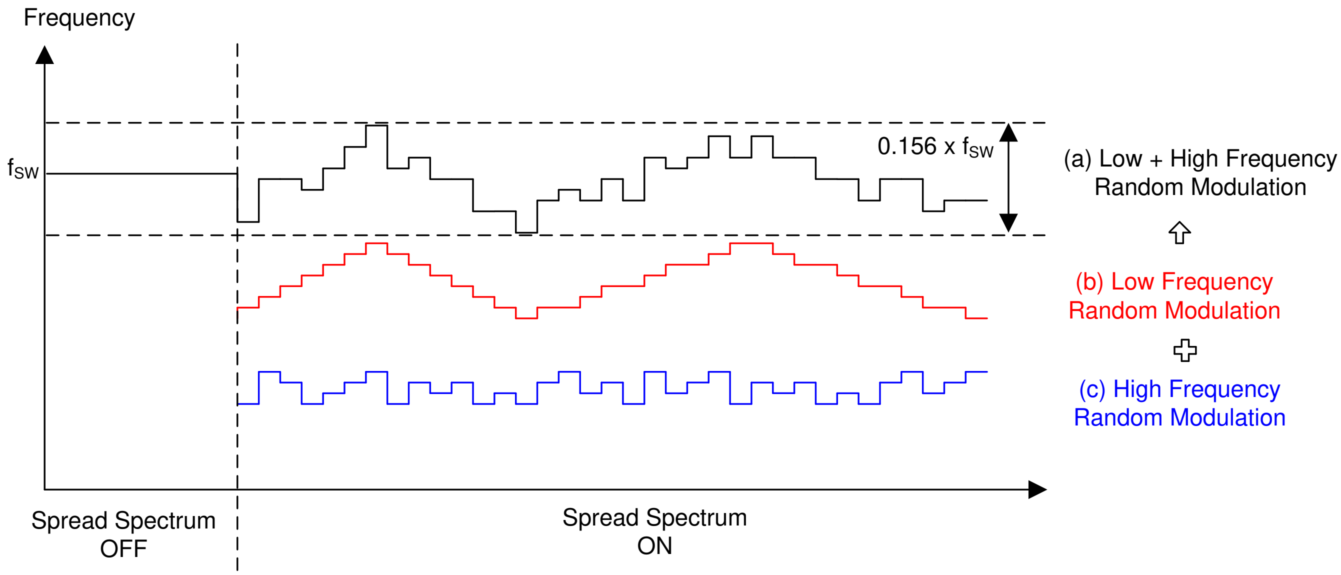


图 9-9. Dual Random Spread Spectrum

9.3.6 Clock Synchronization (EN/UVLO/SYNC Pin)

The switching frequency of the device can be synchronized to an external clock by pulling down the EN/UVLO/SYNC pin. The internal clock of the device is synchronized at the falling edge, but ignores the falling edge input during the forced off time, which is determined by the maximum duty cycle limit. The external synchronization clock must pull down the EN/UVLO/SYNC pin voltage below $V_{UVLO(FALLING)}$. The duty cycle of the pulldown pulse is not limited, but the minimum pulldown pulse width must be greater than 150 ns, and the minimum pullup pulse width must be greater than 250 ns. 图 9-10 shows an implementation of the remote shutdown function. The UVLO pin can be pulled down by a discrete MOSFET or an open-drain output of an MCU. In this configuration, the device stops switching immediately after the UVLO pin is grounded, and the device shuts down 40 µs (typical) after the UVLO pin is grounded.

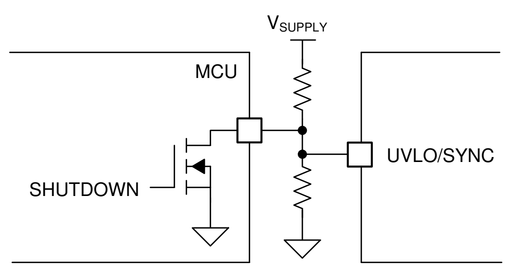


图 9-10. UVLO and Shutdown

图 9-11 shows an implementation of shutdown and clock synchronization functions together. In this configuration, the device stops switching immediately when the UVLO pin is grounded, and the device shuts down if the f_{SYNC} stays in high logic state for longer than 40 µs (typical) (UVLO is in low logic state for more than 40 µs (typical)). The device runs at f_{SYNC} if clock pulses are provided after the device is enabled.

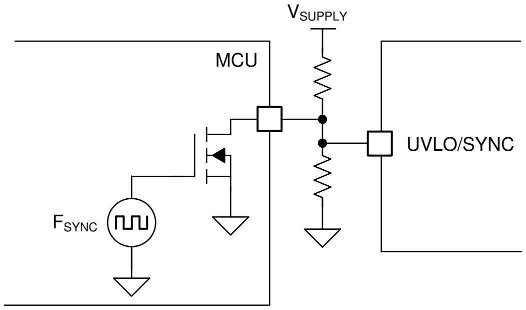


图 9-11. UVLO, Shutdown, and Clock Synchronization

图 9-13 and 图 9-14 show implementations of standby and clock synchronization functions together. In this configuration, The device stops switching immediately if f_{SYNC} stays in high logic state and enters Standby mode if f_{SYNC} stays in high logic state for longer than two switching cycles. The device runs at f_{SYNC} if clock pulses are provided. Because the device can be enabled when the UVLO pin voltage is greater than the enable threshold for more than 1.5 µs, the configurations in 图 9-13 and 图 9-14 are recommended if the external clock synchronization pulses are provided from the start before the device is enabled. This 1.5-µs requirement can be relaxed when the duty cycle of the synchronization pulse is greater than 50%. 图 9-12 shows the required minimum duty cycle to start up by synchronization pulses. When the switching frequency is greater than 1.1 MHz, the UVLO pin voltage must be greater than the enable threshold for more than 1.5 µs before applying the external synchronization pulse.

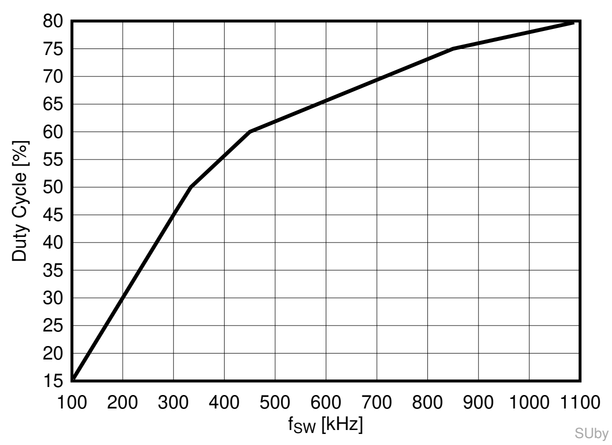


图 9-12. Required Duty Cycle to Start Up by External Synchronization Clock

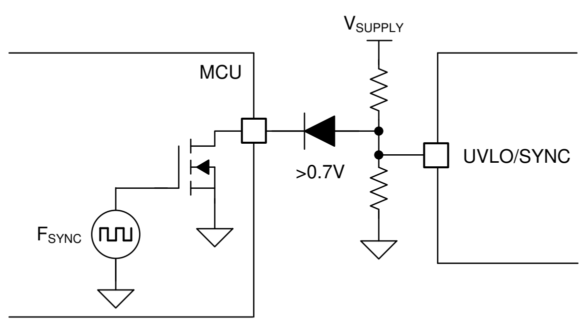


图 9-13. UVLO, Standby, and Clock Synchronization (a)

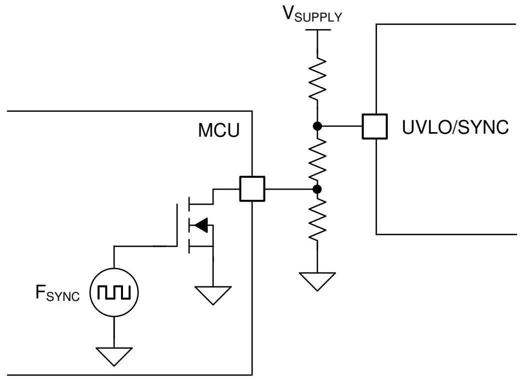


图 9-14. UVLO, Standby, and Clock Synchronization (b)

If the UVLO function is not required, the shutdown and clock synchronization functions can be implemented together by using one push-pull output of the MCU. In this configuration, the device shuts down if f_{SYNC} stays in low logic state for longer than 40 µs (typical). The device is enabled if f_{SYNC} stays in high logic state for longer than 1.5 µs. The device runs at f_{SYNC} if clock pulses are provided after the device is enabled. Also, in this configuration, it is recommended to apply the external clock pulses after the BIAS is supplied. By limiting the current flowing into the UVLO pin below 1 mA using a current limiting resistor, the external clock pulses can be supplied before the BIAS is supplied (see 图 9-15).

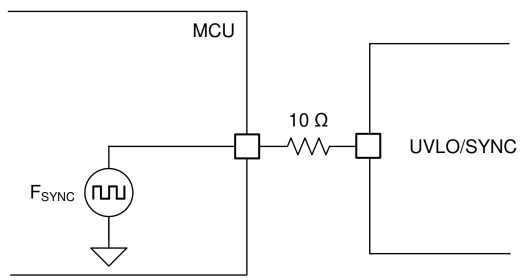


图 9-15. Shutdown and Clock Synchronization

图 9-16 shows an implementation of inverted enable using external circuit.

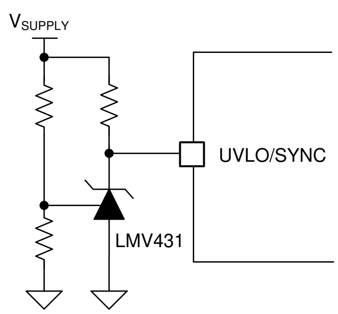


图 9-16. Inverted UVLO

The external clock frequency (f_{SYNC}) must be within +25% and –30% of $f_{RT(TYPICAL)}$. Because the maximum duty cycle limit and the peak current limit with slope resistor (R_{SL}) are affected by the clock synchronization, take extra care when using the clock synchronization function. See 节 9.3.7 and 节 9.3.12 for more information.

9.3.7 Current Sense and Slope Compensation

The device senses switch current, which flows into the SW pin and provides a fixed internal slope compensation ramp, which helps prevent subharmonic oscillation at high duty cycle. The internal slope compensation ramp is added to the sensed switch current for the PWM operation. But, no slope compensation ramp is added to the sensed inductor current for the current limit operation to provide an accurate peak current limit over the input supply voltage (see 图 9-17).

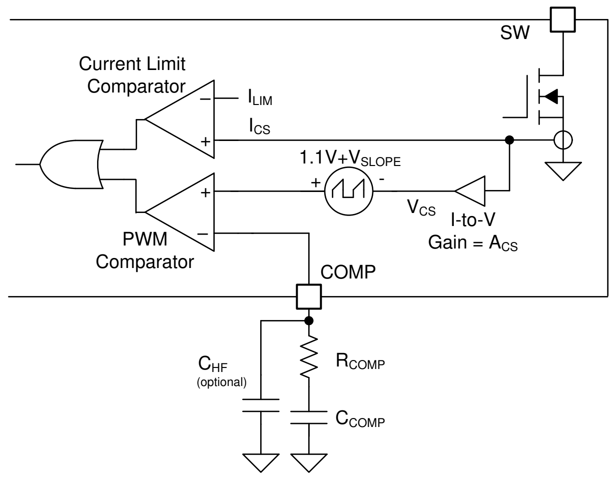


图 9-17. Current Sensing and Slope Compensation

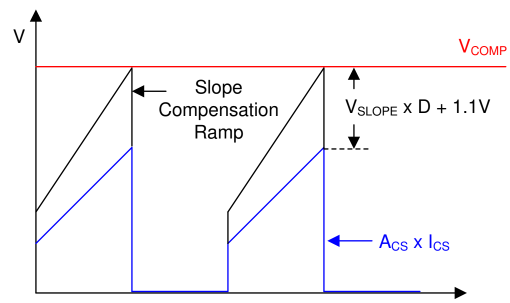


图 9-18. Current Sensing and Slope Compensation (a) at PWM Comparator Inputs

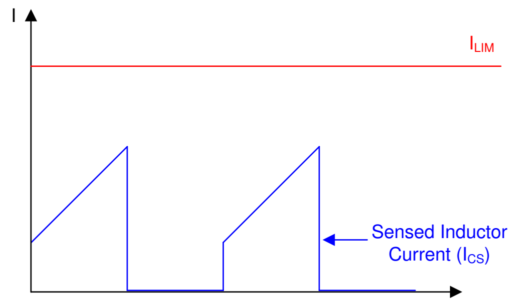


图 9-19. Current Sensing (b) at Current Limit Comparator Inputs

Use 方程式 6 to calculate the value of the peak slope voltage (V_{SLOPE}).

$$V_{SLOPE} = 500mV \times \frac{f_{RT}}{f_{SYNC}} \quad (6)$$

where

- f_{SYNC} is f_{RT} if clock synchronization is not used.

According to peak current mode control theory, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the minimum amount of slope compensation in boost topology must satisfy the following inequality:

$$0.5 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times A_{CS} \times \text{Margin} < 500mV \times f_{SW} \quad (7)$$

where

- V_F is a forward voltage drop of D1, the external diode.

Typically 82% of the sensed inductor current falling slope is known as an optimal amount of the slope compensation. By increasing the margin to 1.6, the amount of slope compensation becomes close to the optimal amount.

If clock synchronization is not used, the f_{SW} frequency equals the f_{RT} frequency. If clock synchronization is used, the f_{SW} frequency equals the f_{SYNC} frequency.

9.3.8 Current Limit and Minimum On Time

The device provides cycle-by-cycle peak current limit protection that turns off the internal MOSFET when the inductor current reaches the current limit threshold (I_{LIM}). To avoid an unexpected hiccup mode operation during a harsh load transient condition, it is recommended to have more margin when programming the peak-current limit.

Boost converters have a natural pass-through path from the supply to the load through the high-side power diode (D1). Because of this path and the minimum on-time limitation of the device, boost converters cannot provide current limit protection when the output voltage is close to or less than the input supply voltage. The minimum on time is shown in 图 8-15 and is calculated as 方程式 8.

$$t_{ON(MIN)} \approx \begin{cases} \dfrac{800 \times 10^{-15}}{\frac{1}{8 \times R_T} + 4 \times 10^{-6}} \, (R_T \geq 20.83\text{k}\Omega) \\ 80 \times 10^{-9} \, (R_T < 20.83\text{k}\Omega) \end{cases} \quad (8)$$

9.3.9 Feedback and Error Amplifier (FB, COMP Pin)

The feedback resistor divider is connected to an internal transconductance error amplifier, which features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 7 MHz). The internal transconductance error amplifier sources current, which is proportional to the difference between the FB pin and the SS pin voltage or the internal reference, whichever is lower. The internal transconductance error amplifier provides symmetrical sourcing and sinking capability during normal operation and reduces its sinking capability when the FB is greater than OVP threshold.

To set the output regulation target, select the feedback resistor values as shown in 方程式 9.

$$V_{LOAD} = V_{REF} \times \left(\frac{R_{FBT}}{R_{FBB}} + 1 \right) \tag{9}$$

The output of the error amplifier is connected to the COMP pin, allowing the use of a Type 2 loop compensation network. R_{COMP}, C_{COMP}, and optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. The absolute maximum voltage rating of the FB pin is 4.0 V. If necessary, the feedback resistor divider input can be clamped by using an external Zener diode.

The COMP pin features internal clamps. The maximum COMP clamp limits the maximum COMP pin voltage below its absolute maximum rating even in shutdown. The minimum COMP clamp limits the minimum COMP pin voltage in order to start switching as soon as possible during no load to heavy load transition. The minimum COMP clamp is disabled when FB is connected to ground in flyback topology.

9.3.10 Power-Good Indicator (PGOOD Pin)

The device has a power-good indicator (PGOOD) to simplify sequencing and supervision. The PGOOD switches to a high impedance open-drain state when the FB pin voltage is greater than the feedback undervoltage threshold (V_{UVTH}), the VCC is greater than the VCC UVLO threshold and the UVLO/EN is greater than the EN threshold. A 25-µs deglitch filter prevents any false pulldown of the PGOOD due to transients. The recommended minimum pullup resistor value is 10 kΩ.

Due to the internal diode path from the PGOOD pin to the BIAS pin, the PGOOD pin voltage cannot be greater than V_{BIAS} + 0.3 V.

9.3.11 Hiccup Mode Overload Protection (MODE Pin)

To further protect the converter during prolonged current limit conditions, the device provides a selectable hiccup mode overload protection. This function is enabled by a single resistor (37.4 kΩ or 62.0 kΩ) between the MODE pin and the AGND pin or by programming the MODE pin voltage (370 mV or 620 mV) during initial power up. The internal hiccup mode fault timer of the device counts the PWM clock cycles when the cycle-by-cycle current limiting occurs after soft start is finished. When the hiccup mode fault timer detects 64 cycles of current limiting, an internal hiccup mode off timer forces the device to stop switching and pulls down SS. Then, the device restarts after 32,768 cycles of hiccup mode off time. The 64 cycle hiccup mode fault timer is reset if eight consecutive switching cycles occur without exceeding the current limit threshold. The soft-start time must be long enough not to trigger the hiccup mode protection after the soft start is finished.

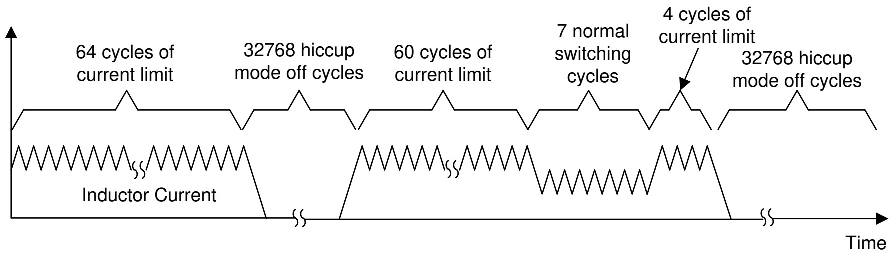


图 9-20. Hiccup Mode Overload Protection

9.3.12 Maximum Duty Cycle Limit and Minimum Input Supply Voltage

The practical duty cycle is greater than the estimated due to voltage drops across the MOSFET and sense resistor. The estimated duty cycle is calculated as shown in 方程式 10.

$$D = 1 - \frac{V_{SUPPLY}}{V_{LOAD} + V_F} \tag{10}$$

When designing boost converters, the maximum required duty cycle must be reviewed at the minimum supply voltage. The minimum input supply voltage that can achieve the target output voltage is limited by the maximum duty cycle limit, and it can be estimated as follows.

$$V_{SUPPLY(MIN)} \approx \left(V_{LOAD} + V_F\right) \times \left(1 - D_{MAX}\right) + I_{SUPPLY(MAX)} \times R_{DCR} + I_{SUPPLY(MAX)} \times 110m \times D_{MAX} \tag{11}$$

where

- $I_{SUPPLY(MAX)}$ is the maximum input current.
- R_{DCR} is the DC resistance of the inductor.

$$D_{MAX1} = 1 - 0.1 \times \frac{f_{SYNC}}{f_{RT}} \tag{12}$$

$$D_{MAX2} = 1 - 100ns \times f_{SW} \tag{13}$$

The minimum input supply voltage can be further decreased by supplying f_{SYNC}, which is less than f_{RT}. Practical D_{MAX} is D_{MAX1} or D_{MAX2}, whichever is lower.

9.3.13 Internal MOSFET (SW Pin)

The device provides an internal switch where $r_{DS(ON)}$ is typically 133 mΩ when the BIAS pin is greater than 5 V. The $r_{DS(ON)}$ of the internal switch is increased when the BIAS pin is less than 5 V. The device temperature must be checked at the minimum supply voltage especially when the BIAS pin is less than 5 V.

The dV/dT of the SW pin must be limited during the 90-µs internal start-up delay to avoid a false turn-on, which is caused by the coupling through C_{DG} parasitic capacitance of the internal MOSFET switch.

9.3.14 Overvoltage Protection (OVP)

The device has OVP for the output voltage. OVP is sensed at the FB pin. If the voltage at the FB pin rises above the overvoltage threshold (V_{OVTH}), OVP is triggered and switching stops. During OVP, the internal error amplifier is operational, but the maximum source and sink capability is decreased to 60 µA.

9.3.15 Thermal Shutdown (TSD)

An internal thermal shutdown turns off the VCC regulator, disables switching, and pulls down the SS when the junction temperature exceeds the thermal shutdown threshold (T_{TSD}). After the junction temperature is decreased by 15°C, the VCC regulator is enabled again and the device performs a soft start.

9.4 Device Functional Modes

9.4.1 Shutdown Mode

If the EN/UVLO/SYNC pin voltage is below V_{EN} for longer than 40 µs (typical), the device goes into shutdown mode with all functions disabled. In shutdown mode, the device decreases the BIAS pin current consumption to below 2.6 µA (typical).

9.4.2 Standby Mode

If the EN/UVLO/SYNC pin voltage is greater than V_{EN} and below V_{UVLO} for longer than 1.5 µs, the device enters standby mode with the VCC regulator operational, the RT regulator operational, the SS pin grounded, and no switching. The PGOOD is activated when the VCC voltage is greater than the VCC UV threshold.

9.4.3 Run Mode

If the UVLO pin voltage is above V_{UVLO} and the VCC voltage is sufficient, the device enters run mode.

9.4.3.1 Spread Spectrum Enabled

The spread spectrum function is enabled by a single resistor (37.4 kΩ ±5% or 100 kΩ ±5%) between the MODE pin and the AGND pin or by programming the MODE pin voltage (370mV ±10% or greater than 1.0 V) during initial power up. To switch the spread spectrum function, EN must be grounded for more than 60 µs or VCC must be fully discharged.

9.4.3.2 Hiccup Mode Protection Enabled

Hiccup mode protection is enabled by a single resistor (37.4 kΩ ±5% or 62.0 kΩ ±5%) between the MODE pin and the AGND pin or by programming the MODE pin voltage (370 mV ±10% or 620 mV ±10%) during initial power up. To switch the hiccup mode protection function, EN must be grounded for more than 60 µs or VCC must be fully discharged.

10 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

TI provides application notes explaining how to design boost and flyback converters using the device. These comprehensive application notes include component selections and loop response optimization.

See these application reports for more information on loop response and component selection:

- *How to Design a Boost Converter Using LM5157x / LM5158x*
- *How to Design an Isolated Flyback Converter Using LM5157x / LM5158x*

10.2 Typical Boost Application

图 10-1 shows all optional components to design a boost converter.

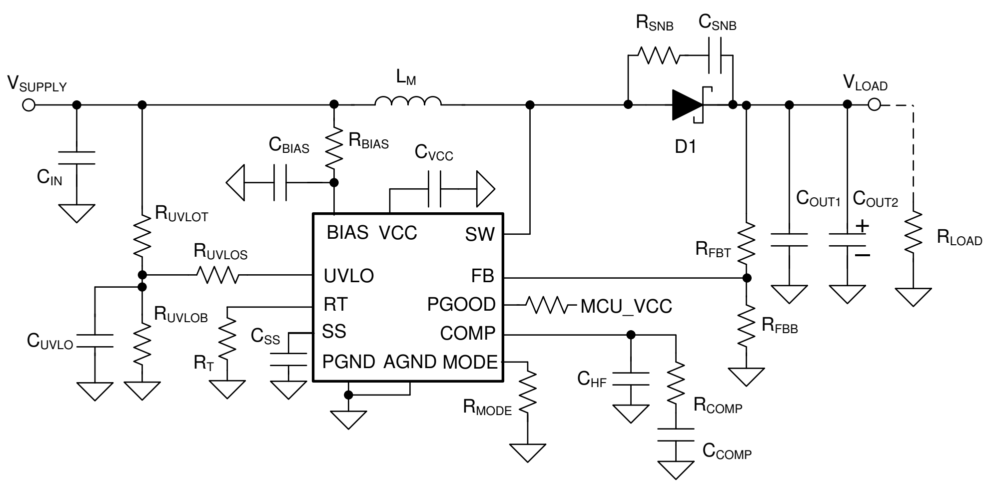


图 10-1. Typical Boost Converter Circuit with Optional Components

10.2.1 Design Requirements

表 10-1 shows the intended input, output, and performance parameters for this application example.

表 10-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Minimum input supply voltage ($V_{SUPPLY(MIN)}$)	6 V
Target output voltage (V_{LOAD})	12 V
Maximum load current (I_{LOAD})	1.2 A (≈ 14.4 Watt)
Typical switching frequency (f_{SW})	2100 kHz

10.2.2 Detailed Design Procedure

Use the Quick Start Calculator to expedite the process of designing of a regulator for a given application. Download these Quick Start Calculator for more information on loop response and component selection:

- *LM5158x-Q1 Excel Quickstart Calculator for Boost Converter Design*
- *LM5158x-Q1 Excel Quickstart Calculator for isolated Flyback Converter Design*
- *LM5158x-Q1 Excel Quickstart Calculator for SEPIC Converter Design*

The device is also WEBENCH® Designer enabled. The WEBENCH software uses an iterative design procedure and accesses comprehensive data bases of components when generating a design.

10.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5158x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.2.2 Recommended Components

表 10-2 shows a recommended list of materials for this typical application.

表 10-2. List of Materials

REFERENCE DESIGNATOR	QTY.	SPECIFICATION	MANUFACTURER(1)	PART NUMBER
R_T	1	RES, 9.53 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06039K53FKEA
R_{FBT}	1	RES, 49.9 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0749K9L
R_{FBB}	1	RES, 4.53 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06034K53FKEA
L_M	1	Inductor, Shielded, Composite, 1.5 µH, 14 A, 0.01052 Ω, AEC-Q200 Grade 1, SMD	Coilcraft	XEL6030-152MEB
C_{OUT1}	6	CAP, CERM, 4.7 µF, 50 V, ±10%, X7R, 1210	TDK	C3225X7R1H475K250AB
C_{OUT2} (Bulk)	2	CAP, Aluminum Polymer, 100 µF, 50 V, ±20%, 0.025 Ω, AEC-Q200 Grade 2, D10xL10mm SMD	Chemi-Con	HHXB500ARA101MJA0G
C_{IN1}	4	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	MuRata	GRM32ER71H106KA12L
C_{IN2} (Bulk)	1	CAP, AL, 22 µF, 100 V, ±20%, 1.3 Ω, AEC-Q200 Grade 2, SMD	Panasonic	EEE-FK2A220P
D1	1	Diode, Schottky, 45 V, 10 A, AEC-Q101, CFP15	Nexperia	PMEG045V100EPDAZ
R_{COMP}	1	RES, 2.61 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-072K61L
C_{COMP}	1	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603X103K5RACTU
C_{HF}	1	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 0, 0603	TDK	CGA3E2NP01H101J080AA
R_{UVLOT}	1	RES, 61.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060361K9FKEA
R_{UVLOB}	1	RES, 71.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060371K5FKEA
R_{UVLOS}	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
C_{SS}	1	CAP, CERM, 0.022 µF, 50 V, ±10%, X7R, 0603	Kemet	C0603X223K5RACTU
R_{BIAS}	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
C_{BIAS}	1	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCJ188R72A104KA01D
C_{VCC}	1	CAP, CERM, 1 µF, 16 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E1X7R1C105K080AC
R_{PG}	1	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA
R_{MODE}	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL

(1) See the *Third-Party Products Disclaimer*.

10.2.2.3 Inductor Selection (L_M)

When selecting the inductor, consider three key parameters: inductor current ripple ratio (RR), falling slope of the inductor current, and RHP zero frequency (f_{RHP}).

The inductor current ripple ratio is selected to have a balance between core loss and copper loss. The falling slope of the inductor current must be low enough to prevent subharmonic oscillation at high duty cycle (additional R_{SL} resistor is required if not). Higher f_{RHP} (equal to lower inductance) allows a higher crossover frequency and is always preferred when using a small value output capacitor.

The inductance value can be selected to set the inductor current ripple between 30% and 70% of the average inductor current as a good compromise between RR, F_{RHP}, and inductor falling slope.

10.2.2.4 Output Capacitor (C_{OUT})

There are a few ways to select the proper value of output capacitor (C_{OUT}). The output capacitor value can be selected based on output voltage ripple, output overshoot, or undershoot due to load transient.

The ripple current rating of the output capacitors must be enough to handle the output ripple current. By using multiple output capacitors, the ripple current can be split. In practice, ceramic capacitors are placed closer to the diode and the MOSFET than the bulk aluminum capacitors in order to absorb the majority of the ripple current.

10.2.2.5 Input Capacitor

The input capacitors decrease the input voltage ripple. The required input capacitor value is a function of the impedance of the source power supply. More input capacitors are required if the impedance of the source power supply is not low enough.

10.2.2.6 Diode Selection

A Schottky is the preferred type for D1 diode due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus any switching node ringing. Also, it must be able to handle the average output current. For the optimal performance, it is highly recommended to use a diode with a junction capacitance lower than 1 nF at 0 V.

10.2.3 Application Curve

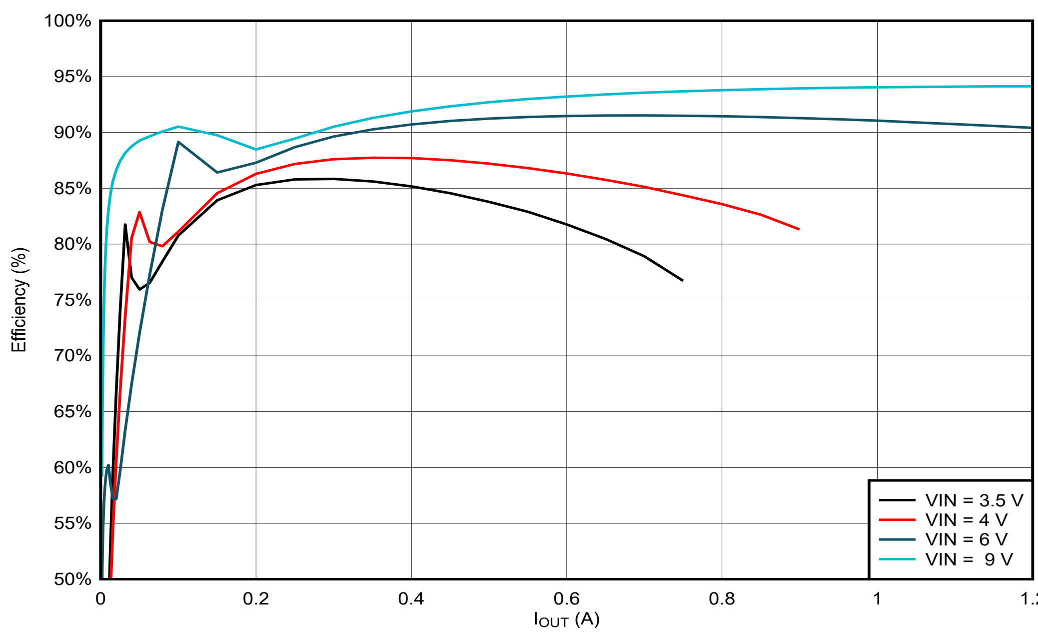


图 10-2. Efficiency Versus Output Current

10.3 System Examples

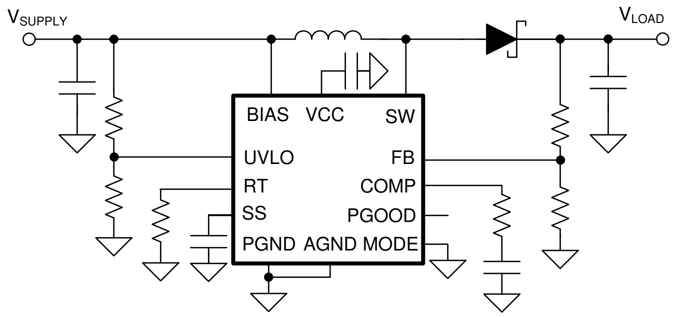


图 10-3. Typical Boost Application

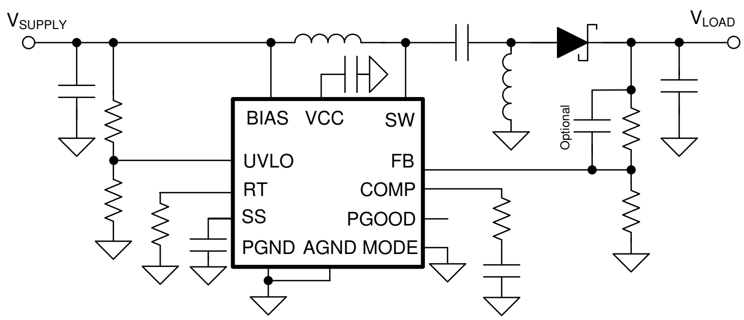


图 10-4. Typical SEPIC Application

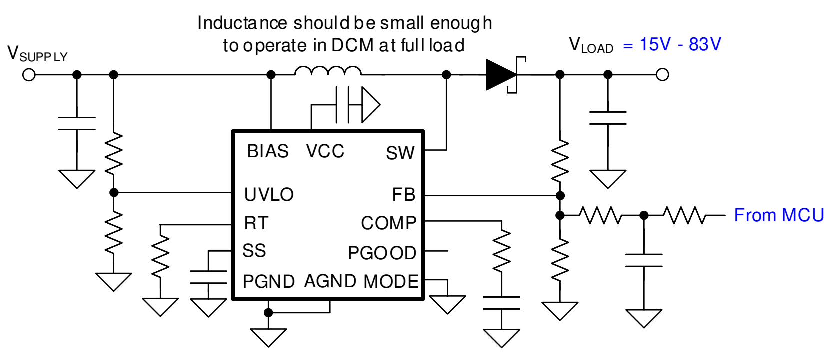


图 10-5. LIDAR Bias Supply 1 (DCM Operation)

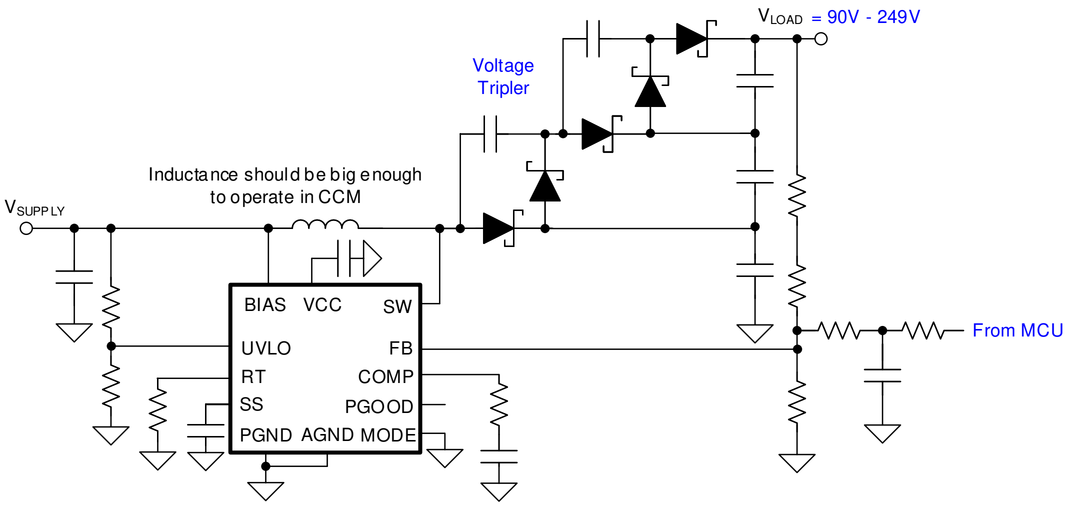


图 10-6. LIDAR Bias Supply 2 (CCM Operation)

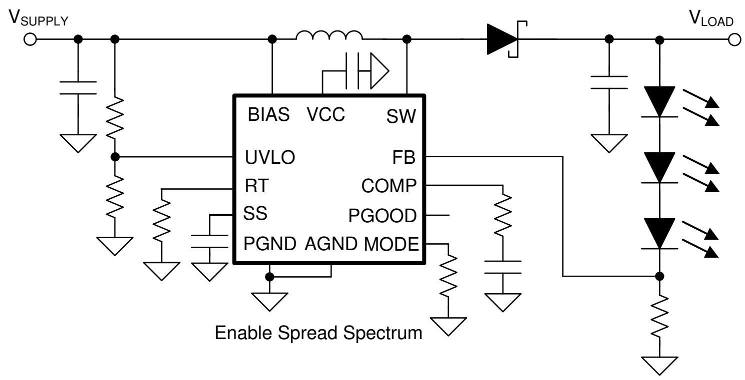


图 10-7. Low-Cost Single String LED Driver

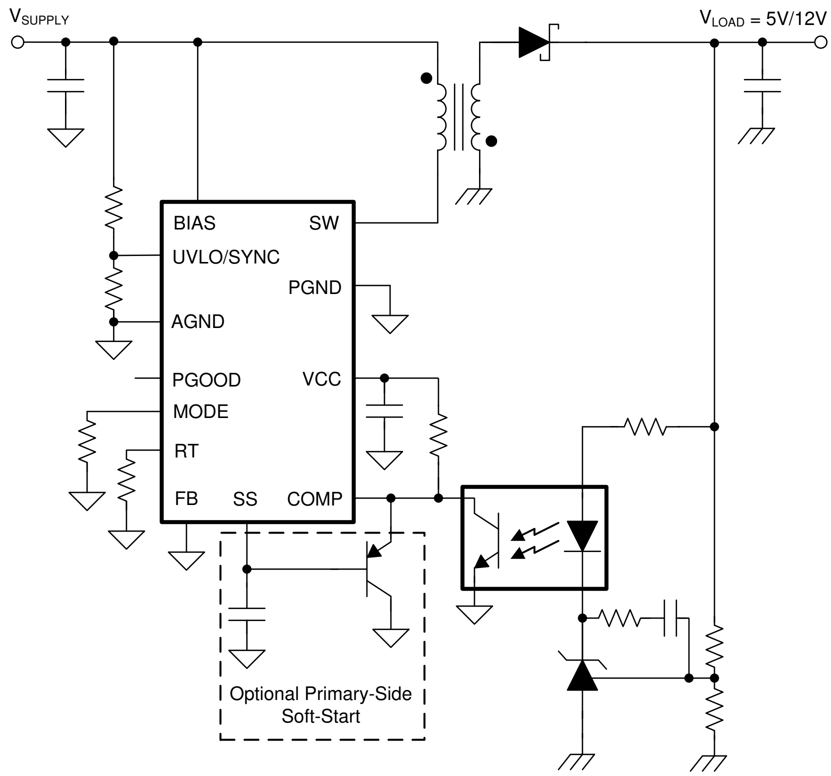


图 10-8. Secondary-Side Regulated Isolated Flyback

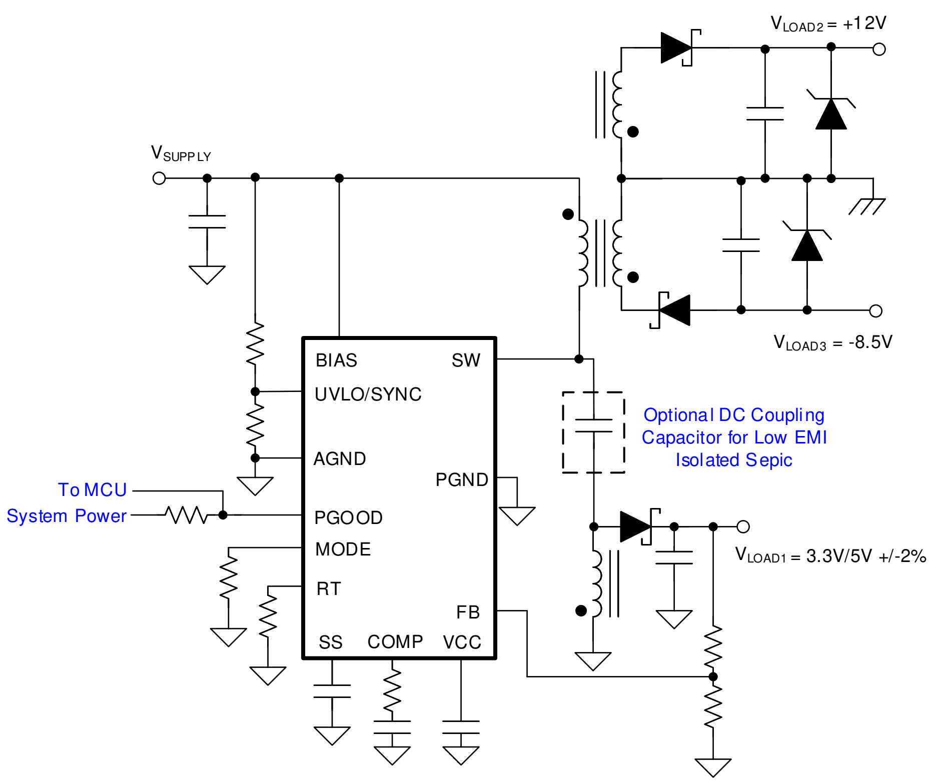


图 10-9. Primary-Side Regulated Multiple-Output Isolated Flyback/Isolated SEPIC

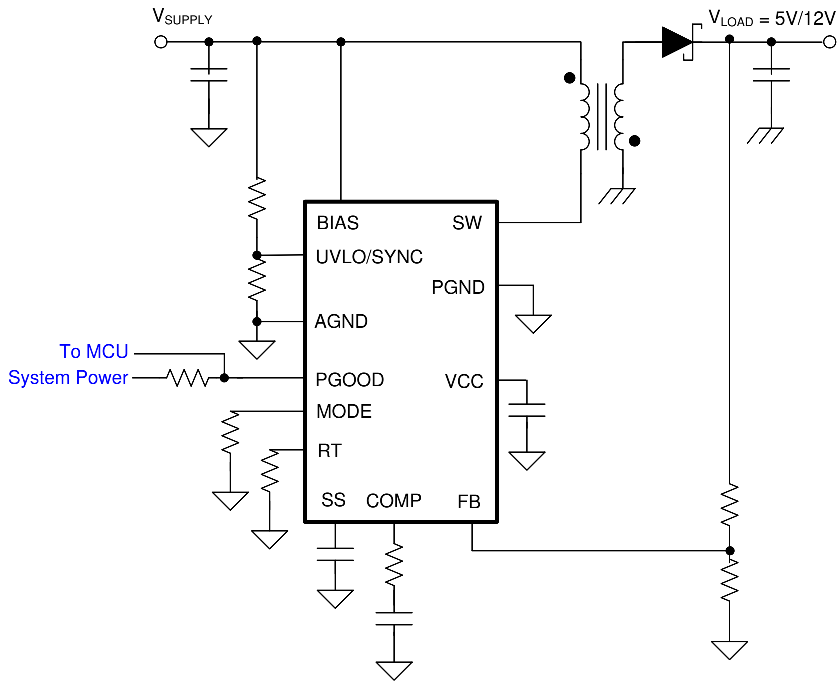


图 10-10. Typical Non-Isolated Flyback

11 Power Supply Recommendations

The device is designed to operate from a power supply or a battery with a voltage range from 1.5 V to 60 V. The input power supply must be able to supply the maximum boost supply voltage and handle the maximum input current at 1.5 V. The impedance of the power supply and battery including cables must be low enough that an input current transient does not cause an excessive drop. Additional input ceramic capacitors can be required at the supply input of the converter.

12 Layout

12.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines can help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Put the D1 component on the board first.
- Use a small size ceramic capacitor for C_{OUT}.
- Make the switching loop (C_{OUT} to D1 to SW to PGND to C_{OUT}) as small as possible.
- Leave a copper area near the D1 diode for thermal dissipation.
- Put the C_{VCC} capacitor as near the device as possible between the VCC and PGND pins.
- Connect the COMP pin to the compensation components (R_{COMP} and C_{COMP}).
- Connect the C_{COMP} capacitor to the analog ground trace.
- Connect the AGND pin directly to the analog ground plane. Connect the AGND pin to the R_{MODE}, R_{UVLOB}, R_T, C_{SS}, and R_{FBB} components.
- Add several vias under the exposed pad to help conduct heat away from the device. Connect the vias to a large ground plane on the bottom layer.

12.2 Layout Examples

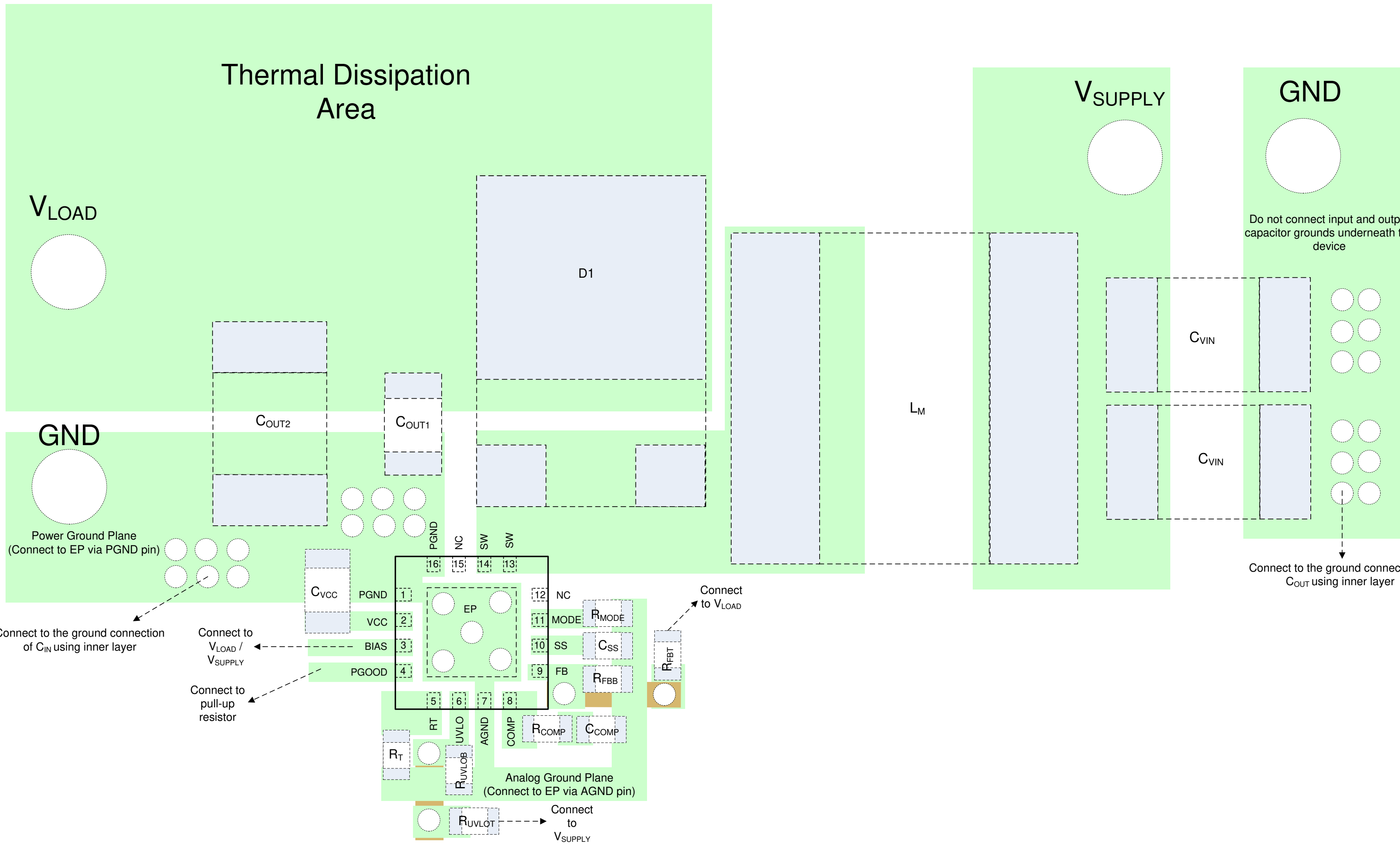


图 12-1. PCB Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 第三方产品免责声明

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13.1.2 Development Support

For development support see the following:

- *LM5157x / LM5158x Boost Quick Start Calculator*
- *LM5157x / LM5158x Flyback Quick Start Calculator*
- *LM5157x / LM5158x SEPIC Quick Start Calculator*
- *How to Design a Boost Converter Using LM5157x / LM5158x*
- *How to Design an Isolated Flyback Converter Using LM5157x / LM5158x*

13.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5158x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *LM5158Q1EVM-BST User's Guide*
- Texas Instruments, *LM5158Q1EVM-FLY User's Guide*
- Texas Instruments, *LM5158Q1EVM-SEPIC User's Guide*

13.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 术语表

TI 术语表　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM51581RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L51581
LM51581RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L51581
LM5158RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM5158
LM5158RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM5158

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

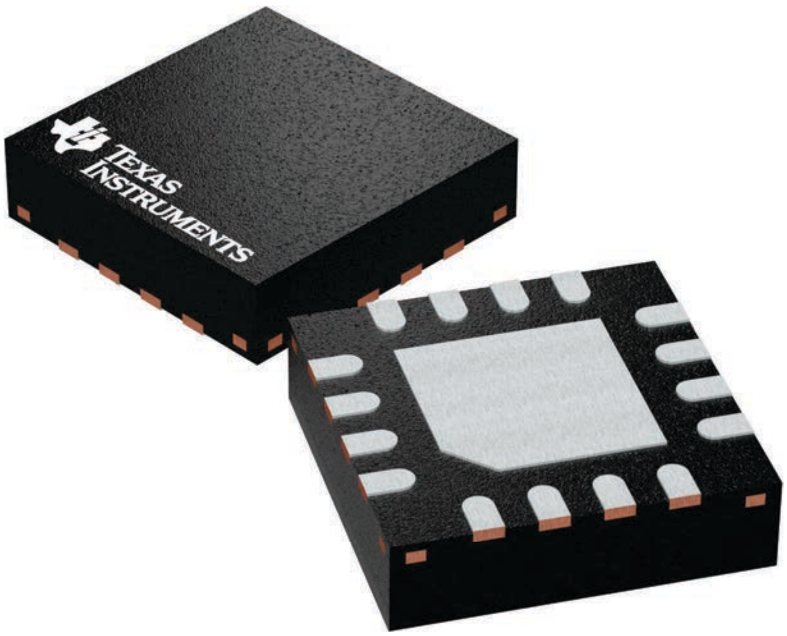
OTHER QUALIFIED VERSIONS OF LM5158, LM51581 :

- Automotive : LM5158-Q1, LM51581-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

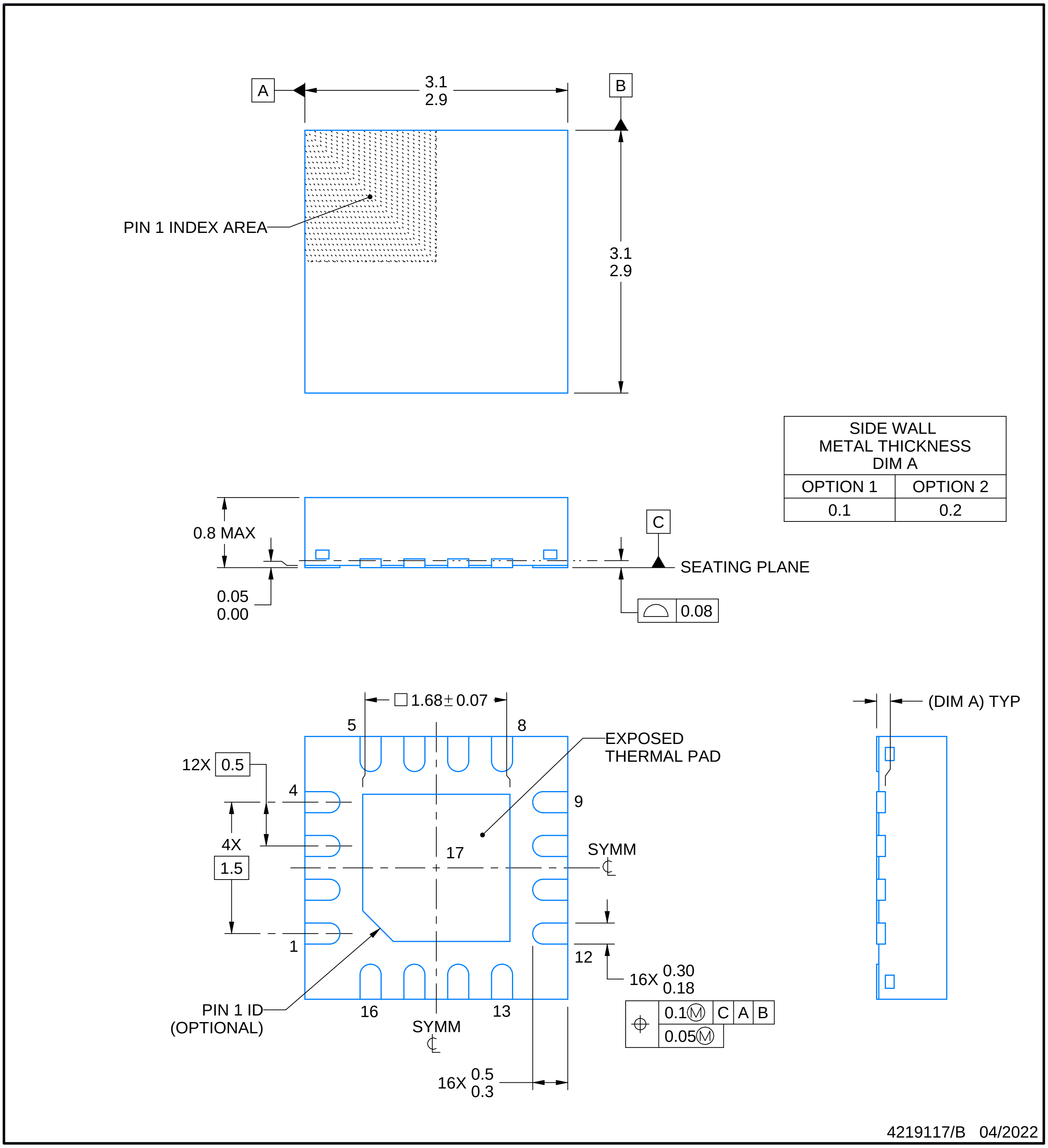


4225944/A

PACKAGE OUTLINE

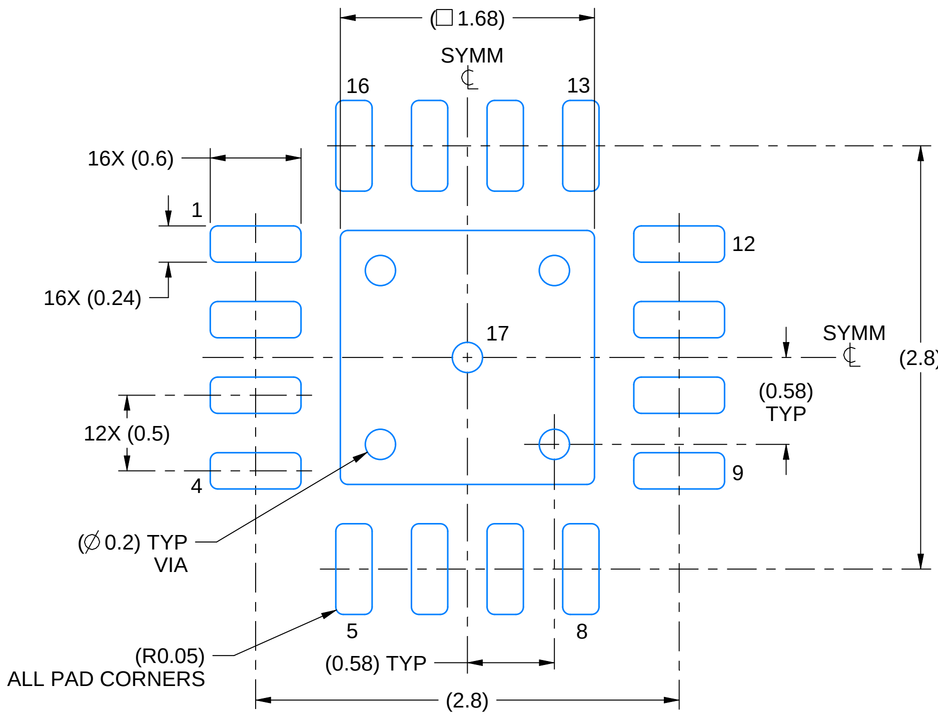
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

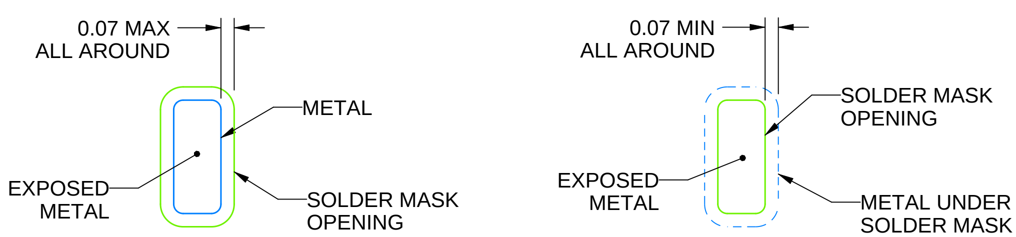


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

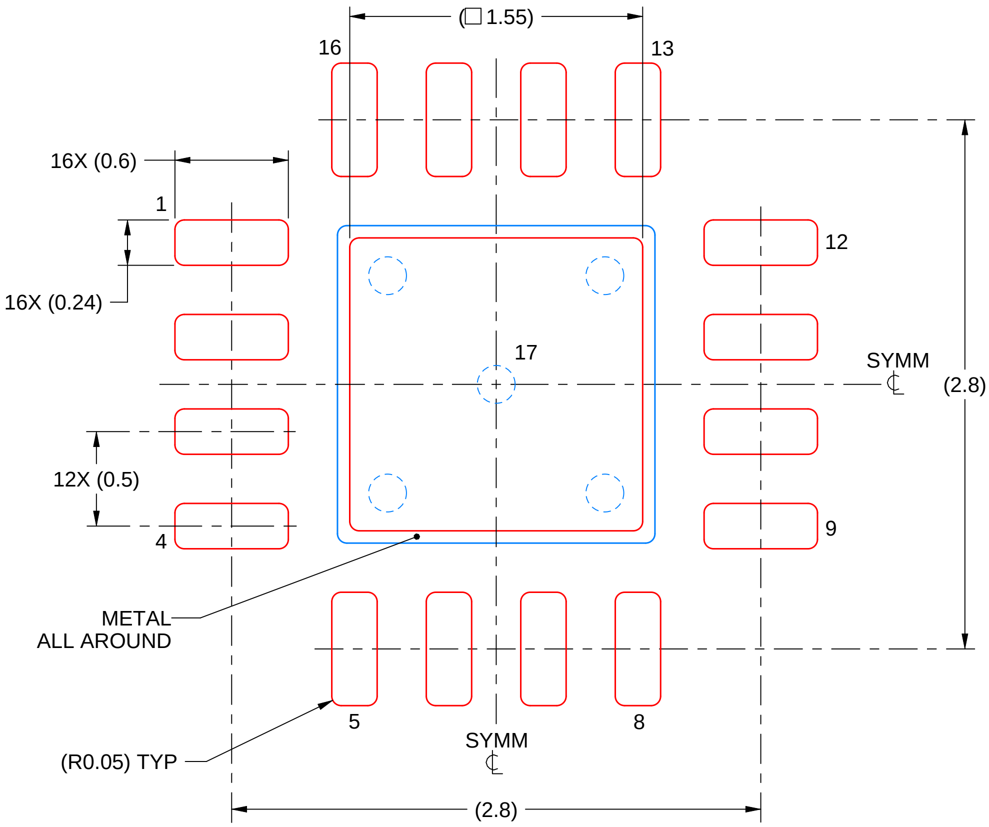
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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