



LM5140-Q1 具有宽输入范围的双路同步降压控制器

1 特性

- 符合 AEC-Q100 1 级标准
($T_A = -40^{\circ}\text{C}$ 至 125°C)
- 输入工作电压范围为 3.8V 至 65V (最高绝对电压为 70V)
- 两个具有以下电压特性的交错式降压控制器：
 - VOUT1**: 3.3V、5V 固定电压或 1.5V 至 15V 可调节电压，精度为 $\pm 1\%$
 - VOUT2**: 5V、8V 固定电压或 1.5V 至 15V 可调节电压，精度为 $\pm 1\%$
- 2.2MHz 或 440kHz 固定开关频率，精度为 $\pm 7\%$
- 可选择与外部时钟保持同步
- 用于附加转换器的 SYNC 输出时钟
- 关断模式电流: 9 μA (典型值)
- 无负载待机电流: 35 μA (典型值) (单通道运行)
- 电流限值阈值可编程为 50mV 或 75mV，精度为 $\pm 10\%$
- 用于 VOUT1 和 VOUT2 的独立使能输入
- 针对持续过载条件的断续模式保护
- 独立的电源正常输出
- 具有可调节转换率控制的高侧和低侧栅极驱动器
- 在轻负载条件下可选择二极管仿真或连续导通
- 具有可湿性侧面的超薄型四方扁平无引线 (VQFN)-40 封装

2 应用

- 汽车电子产品
- 信息娱乐系统
- 仪表板
- 高级驾驶员辅助系统 (ADAS)

3 说明

LM5140-Q1 是一款双路同步降压控制器，用于高电压、宽 V_{IN} 降压转换器应用。此控制方法基于电流模式控制。电流模式控制可提供固有线路前馈、逐周期电流限制和简化的环路补偿。

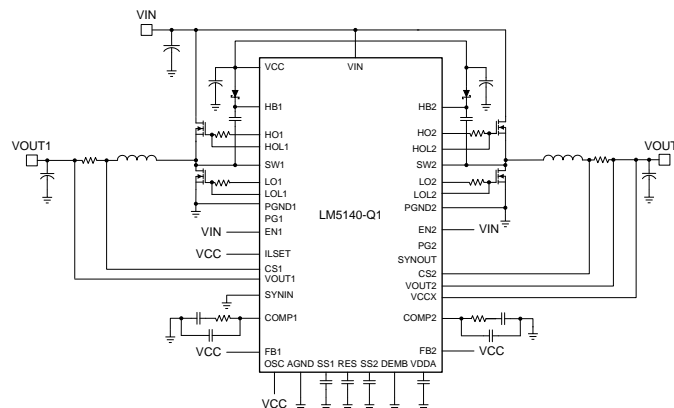
LM5140-Q1 具有可调节转换率控制功能，能够简化 CISPR 和汽车级电磁干扰 (EMI) 要求的合规性。LM5140-Q1 可在 2.2MHz 或 440kHz 的可选开关频率下运行，两条控制器通道发生 180° 出相。在轻负载或无负载条件下，LM5140-Q1 通过在跳周期模式下运行来提升低功耗效率。LM5140-Q1 具备一个自动切换至外部偏置电源的高电压偏置稳压器，能够提升效率并降低输入电流。其他功能包括频率同步、逐周期电流限制、针对持续过载条件的断续模式保护、独立的电源正常输出以及独立的使能输入。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
LM5140-Q1	VQFN (40)	6.00mm x 6.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



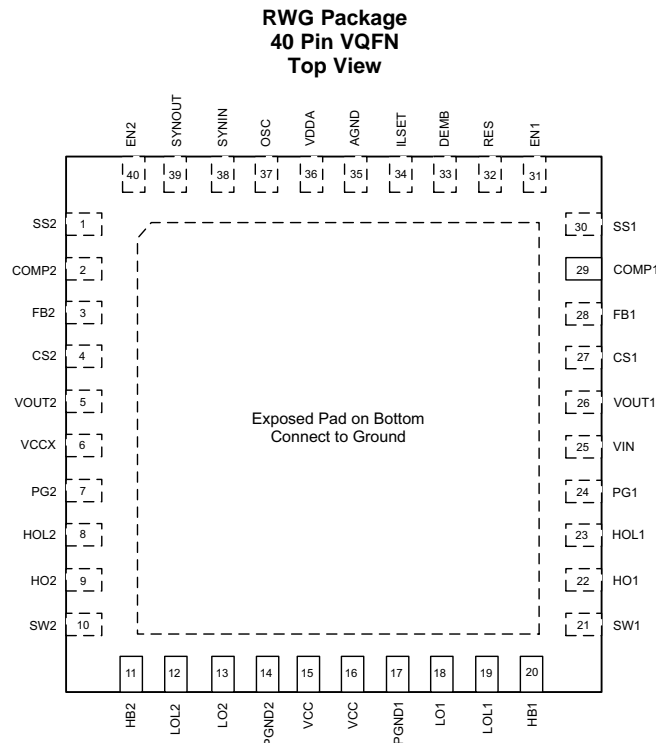
目录

1	特性	1	8.3	Feature Description	15
2	应用	1	8.4	Device Functional Modes	22
3	说明	1	9	Application and Implementation	25
4	简化电路原理图	1	9.1	Application Information	25
5	修订历史记录	2	9.2	Typical Application	25
6	Pin Configuration and Functions	3	10	Power Supply Recommendations	37
7	Specifications	5	11	Layout	38
7.1	Absolute Maximum Ratings	5	11.1	Layout Procedure	38
7.2	ESD Ratings	5	11.2	Layout Example	38
7.3	Recommended Operating Conditions	6	12	器件和文档支持	42
7.4	Thermal Information	6	12.1	器件支持	42
7.5	Electrical Characteristics	7	12.2	社区资源	42
7.6	Switching Characteristics	9	12.3	商标	42
7.7	Typical Characteristics	10	12.4	静电放电警告	42
8	Detailed Description	13	12.5	Glossary	42
8.1	Overview	13	13	机械、封装和可订购信息	42
8.2	Functional Block Diagram	14			

5 修订历史记录

日期	修订版本	注释
2016 年 1 月	*	最初发布版本。

6 Pin Configuration and Functions



Connect Exposed Pad on bottom to AGND and PGND on the PCB.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SS2	1	I	Channel 2 soft-start programming pin. An external capacitor and an internal 20-μA current source set the ramp rate of the internal error amplifier reference during soft-start. Pulling SS pin below 80mV turns-off the channel 2 gate driver outputs, but all the other functions remain active.
COMP2	2	O	Output of the channel 2 transconductance error amplifier.
FB2	3	I	Feedback input of channel 2. Connect the FB2 pin to VDD for a 5 V output or connect FB2 to ground for a fixed 8V output. A resistive divider from the VOUT2 to the FB2 pin sets the output voltage level between 1.5 V and 15 V. The regulation threshold at the FB2 pin is 1.2 V.
CS2	4	I	Channel 2 current sense amplifier input. Make a low current Kelvin connection between this pin and the inductor side of the external current sense resistor.
VOUT2	5	I	Output and the current sense amplifier input of channel 2 . Connect this pin to the output side of the channel 2 current sense resistor.
VCCX	6	I	Optional input for an external bias supply. If VCCX > 4.5 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. If VCCX is unused, it should be grounded.
PG2	7	O	An open collector output which goes low if VOUT2 is outside a specified regulation window.
HOL2	8	O	Channel 2 high-side gate driver turn-off output.
HO2	9	O	Channel 2 high-side gate driver turn-on output.
SW2	10	I	Switching node of the channel 2 buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET.
HB2	11	O	Channel 2 high-side driver supply for bootstrap gate drive.
LOL2	12	O	Channel 2 low-side gate driver turn-off output.
LO2	13	O	Channel 2 low-side gate driver turn-on output.
PGND2	14	G	Power ground connection pin for low-side NMOS gate driver.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VCC	15	P	VCC bias supply pin. Pin 15 and pin 16 must to be connected together on the PCB.
VCC	16	P	VCC bias supply pin. Pin 15 and pin 16 must to be connected together on the PCB.
PGND1	17	G	Power ground connection pin for low-side NMOS gate driver.
LO1	18	O	Channel 1 low-side gate driver turn-on output.
LOL1	19	O	Channel 1 low-side gate driver turn-off output.
HB1	20	O	Channel 1 high-side driver supply for bootstrap gate drive.
SW1	21	I	Switching node of the channel 1 buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET.
HO1	22	O	Channel 1 high-side gate driver turn-on output
HOL1	23	O	Channel 1 high-side gate driver turn-off output.
PG1	24	O	An open collector output which goes low if VOUT1 is outside a specified regulation window.
VIN	25	P	Supply voltage input source for the VCC regulators.
VOUT1	26	I	VOUT1 and current sense amplifier input of channel 1. Connect to the output side of the channel 1 current sense resistor.
CS1	27	I	Channel 1 current sense amplifier input. Make a low current Kelvin connection between this pin and the inductor side of the external current sense resistor.
FB1	28	I	Feedback input of channel 1. Connect the FB1 pin to VDDA for a 3.3-V output or connect FB1 to ground for a 5-V output. A resistive divider from the VOUT1 to the FB1 pin sets the output voltage level between 1.5 V and 15 V. The regulation threshold at the FB1 pin is 1.2 V.
COMP1	29	O	Output of the channel 1 transconductance error amplifier.
SS1	30	I	Channel 2 soft-start programming pin. An external capacitor and an internal 20μA current source set the ramp rate of the internal error amplifier reference during soft-start. Pulling SS pin below 80mV turns-off the channel 1 gate driver outputs, but the all the other function remain active.
EN1	31	I	An active high logic input enables channel 1.
RES	32	O	Restart timer pin. An external capacitor configures the hiccup mode current limiting. The capacitor at the RES pin determines the time the controller will remain off before automatically restarting in hiccup mode. The two regulator channels operate independently. One channel may operate in normal mode while the other is in hiccup mode overload protection. The hiccup mode commences when either channel experiences 512 consecutive PWM cycles with cycle-by-cycle current limiting. Connect the RES pin to VDD during power up to disable hiccup mode protection.
DEMB	33	I	Diode Emulation pin. If the DEMB pin is grounded, diode emulation is enabled. If it is connected to VDDA the LM5140-Q1 operates in FPWM mode with continuous conduction at light loads.
ILSET	34	I	Current Limit Threshold pin. Connecting the ILSET pin to VDDA sets the current limit threshold to 73 mV for channel 1 and channel 2. Connecting the ILSET pin to GND sets the current limit thresholds to 48 mV.
AGND	35	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits.
VDDA	36	P	Internal analog bias regulator output. Connect a capacitor from the VDDA pin the AGND.
OSC	37	I	Frequency selection pin. Connecting the OSC pin to VDDA selects the default oscillator frequency of 2.2 MHz. Connecting the OSC pin to ground sets frequency to 440 kHz.
SYNIN	38	I	Sync input pin. The internal oscillator can be synchronized to an external clock. If the synchronization feature is not used, the SYNIN pin should be connected to AGND.
SYNOUT	39	O	Sync output pin. The TTL level output signal is 180° out of phase with the HO1 gate drive of channel 1.
EN2	40	I	An active high logic input enables channel 2.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	70	V
	SW1, SW2 to PGND	-0.3	70	V
	SW1, SW2 to PGND (20ns transient)	-5		V
	HB1 to SW1, HB2 to SW2	-0.3	6.5	V
	HB1 to SW1, HB2 to SW2 (20ns transient)	-5		V
	HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2	-0.3	HB + 0.3	V
	HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2 (20ns transient)	-5		V
	LO1, LOL1, LO2, LOL2 to PGND	-0.3	VCC + 0.3	V
	LO1, LOL1, LO2, LOL2 to PGND (20ns transient)	-1.5	VCC + 0.3	V
	OSC, SS1, SS2, COMP1, COMP2, RES, DEMB, ILSET	-0.3	VDDA + 0.3	V
	EN1, EN2 to PGND	-0.3	70	V
	VCC, VCCX, VDDA, PG1, PG2, FB1, FB2, SYNIN	-0.3	6.5	V
	VOUT1, VOUT2, CS1, CS2	-0.3	15.5	V
	VOUT1 to CS1, VOUT2 to CS2	-0.3	0.3	V
PGND to AGND		-0.3	0.3	V
Operating Junction Temperature ⁽²⁾		-40	150	°C
Storage temperature, T _{stg}		-40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾⁽²⁾		±2000	V
	Charged-device model (CDM), per AEC Q100-011 ⁽³⁾	All pins	±500	
		Corner pins	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	VIN	3.8		65	V
		SW1, SW2 to PGND	–0.3		65	V
		HB1 to SW1, HB2 to SW2	–0.3	5	5.25	V
		HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2	–0.3		HB + 0.3	V
		LO1, LOL1, LO2, LOL2 to PGND	–0.3	5	5.25	V
		FB1, FB2, PG1, PG2, SYNIN, OSC, SS1, SS2, RES, DEMB, VCCX, ILSET	–0.3		5	V
		EN1, EN2 to PGND	–0.3		65	V
		VCC, VDDA	–0.3	5	5.25	V
		VOUT1, VOUT2, CS1, CS2	1.5	5	15	V
V_O	Output voltage range	SYNOUT	–0.3		5.25	V
		PGND to AGND	–0.3		0.3	V
T_J	Operating Junction Temperature ⁽²⁾		–40		150	°C

(1) *Recommended Operating Conditions* are conditions under which the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM5140-Q1	UNIT
		VQFN (RWG)	
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$, $V_{CCX} = 5\text{ V}$, $V_{OUT1} = 3.3\text{ V}$, $V_{OUT2} = 5\text{ V}$, $EN1 = EN2 = 5\text{ V}$, $OSC = V_{DDA}$, $SYNIN = 0\text{ V}$, $FSW = 2.2\text{ MHz}$, no-load on the Drive Outputs (HO1, HOL1, LO2, LOL1, HO2, HOL2, LO2, and LOL2 outputs) (unless otherwise noted). ⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN SUPPLY VOLTAGE						
I _(SHUTDOWN)	Shutdown mode current	V _{IN} 8 V- 18 V, EN1 = 0 V, EN2 = 0 V, VCCX = 0 V		9	12.5	μA
I _(STANDBY)	Standby Current	EN1 = 5 V, EN2 = 0 V, VOUT1, in regulation, no-load, not switching. VIN 8 V - 18 V. DEMB = GND		35		μA
		Or EN1 = 0 V, EN2 = 5 V, VOUT2 in regulation, no-load, not switching, VOUT2 connected to VCCX, DEMB = GND.		42		μA
VCC REGULATOR						
VCC _(REG)	VCC regulation voltage	V _{IN} = 6 V - 18 V, 0 - 150 mA, VCCX = 0 V	4.75	5.0	5.25	V
VCC _(UVLO)	VCC under voltage threshold	VCC rising, VCCX = 0 V	3.25	3.4	3.55	V
VCC _(HYST)	VCC hysteresis voltage	VCCX = 0 V		175		mV
I _{CC(LIM)}	VCC sourcing current limit	VCCX = 0 V	170	250		mA
VDDA						
VDDA _(REG)	Internal bias supply power	VCCX = 0 V	4.75	5.0	5.25	V
VDDA _(UVLO)		V _{CC} rising, VCCX = 0 V	3.1	3.2	3.3	V
VDDA _(HYST)		VCCX = 0 V		180		mV
R _(VDDA)		VCCX = 0 V		50		Ω
VCCX						
VCCX _(ON)		V _{CC} rising	4.1	4.3	4.4	V
R _(VCCX)		VCCX = 5 V		1		Ω
VCCX _(HYST)				200		mV
OSCILLATOR SELECT THRESHOLDS						
	2.2 MHz Oscillator select threshold	(OSC pin)	2.4			V
	440 kHz Oscillator select threshold	(OSC pin)			0.4	V
CURRENT LIMIT						
V _(CS1)	Current limit threshold1	ILSET = VDDA, Measure from CS to VOUT	66	73	80	mV
V _(CS2)	Current limit threshold2	ILSET = GND, Measure from CS to VOUT	44	48	53	mV
	Current sense delay to output			40		ns
	Current sense amplifier gain		11.4	12	12.6	V/V
ICS _(BIAS)	Amplifier input bias				10	nA
	75mV current limit select threshold (ILSET)		2.4			V
	75mV current limit select threshold (ILSET)				0.4	V
RES						
I _(RES)	RES current source			20		μA
V _(RES)	RES threshold			1.2		V
	Timer hlccup mode fault			512		cycles
R _{DS(ON)}	RES pull-down			5.0		Ω

- (1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
- (2) The junction temperature (T_J in $^{\circ}\text{C}$) is calculated from the ambient temperature (T_A in $^{\circ}\text{C}$) and power dissipation (P_D in Watts) as follows:
 $T_J = T_A + (P_D \cdot R_{\theta JA})$ where $R_{\theta JA}$ (in $^{\circ}\text{C/W}$) is the package thermal impedance provided in the [Thermal Information](#) section.

Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$, $V_{CCX} = 5\text{ V}$, $V_{OUT1} = 3.3\text{ V}$, $V_{OUT2} = 5\text{ V}$, $EN1 = EN2 = 5\text{ V}$, $OSC = V_{DDA}$, $SYNIN = 0\text{ V}$, $FSW = 2.2\text{ MHz}$, no-load on the Drive Outputs (HO1, HOL1, LO2, LOL1, HO2, HOL2, LO2, and LOL2 outputs) (unless otherwise noted). ⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE REGULATION						
3.3 V		$V_{IN} = 3.8\text{ V} - 42\text{ V}$	3.273	3.3	3.327	V
5 V		$V_{IN} = 5.5\text{ V} - 42\text{ V}$	4.95	5.0	5.05	V
8 V		$V_{IN} = 8.5\text{ V} - 42\text{ V}$	7.92	8.0	8.08	V
FEEDBACK						
VOUT1 select threshold 3.3V Output			VDDA-0.3			V
VOUT2 select threshold 5.0V			VDDA-0.3			V
Regulated Feedback Voltage			1.19	1.2	1.21	V
$FB_{(LOWRES)}$	Resistance to ground on FB for $FB=0$ detection				500	Ω
$FB_{(EXTRES)}$	Thevenin equivalent resistance at FB for external regulation detection	$FB < 2\text{ V}$	5			k Ω
TRANSCONDUCTANCE AMPLIFIER						
G_m	Gain	Feedback to COMP	1010	1200		μS
FB	Input Bias Current				15	nA
	Transconductance Amplifier source current	COMP = 1 V, FB = 1.0 V		100		μA
	Transconductance Amplifier sink current	COMP = 1 V, FB = 1.4 V		100		μA
POWER GOOD						
$PG_{(UV)}$	PG1 and PG2 Under Voltage trip levels	Falling with respect to the regulation voltage	90%	92%	94%	
$PG_{(OVP)}$	PG1 and PG2 Over Voltage trip levels	Rising with respect to the regulation voltage	108%	110%	112%	
$PG_{(HYST)}$				3.4%		
$PG_{(VOL)}$	PG1 and PG2	Open Collector, $I_{sink} = 2\text{ mA}$			0.4	V
$PG_{(rdly)}$	OV Filter Time	V_{OUT} rising		25		μs
$PG_{(fdly)}$	UV Filter Time	V_{OUT} falling		30		μs
HO GATE DRIVER						
V_{OLH}	HO Low-state output voltage	$I_{HO} = 100\text{ mA}$		0.05		V
V_{OHH}	HO High-state output voltage	$I_{HO} = -100\text{ mA}$, $V_{OHH} = V_{HB} - V_{HO}$		0.07		V
t_{rHO}	HO rise time (10% to 90%)	$C_{LOAD} = 2700\text{ pF}$		4		ns
t_{fHO}	HO fall time (90% to 10%)	$C_{LOAD} = 2700\text{ pF}$		3		ns
I_{OHH}	HO peak source current	$V_{HO} = 0\text{ V}$, $SW = 0\text{ V}$, $HB = 5\text{ V}$, $V_{CCX} = 5\text{ V}$		3.25		Apk
I_{OLH}	HO peak sink current	$V_{CCX} = 5\text{ V}$		4.25		Apk
$V_{(BOOT)}$	UVLO	HO falling		2.5		V
	Hysteresis			110		mV
$I_{(BOOT)}$	Quiescent current			3		μA

Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$, $V_{CCX} = 5\text{ V}$, $V_{OUT1} = 3.3\text{ V}$, $V_{OUT2} = 5\text{ V}$, $EN1 = EN2 = 5\text{ V}$, $OSC = V_{DDA}$, $SYNIN = 0\text{ V}$, $FSW = 2.2\text{ MHz}$, no-load on the Drive Outputs (HO1, HOL1, LO2, LOL1, HO2, HOL2, LO2, and LOL2 outputs) (unless otherwise noted). ⁽¹⁾⁽²⁾

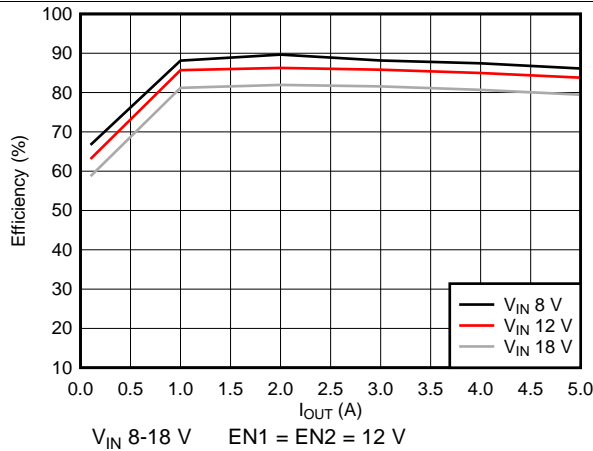
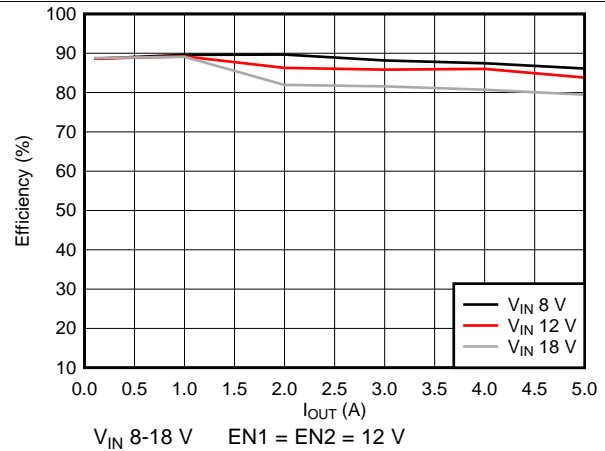
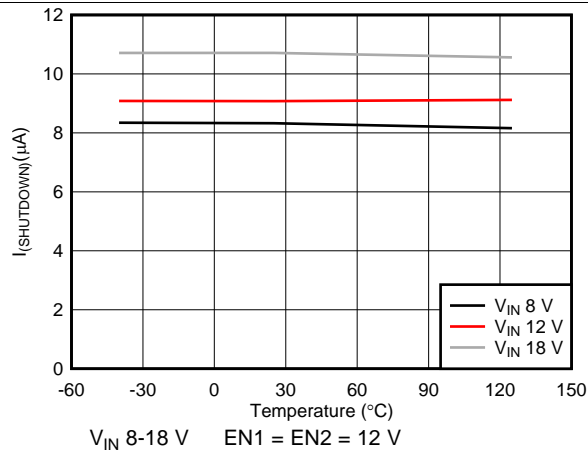
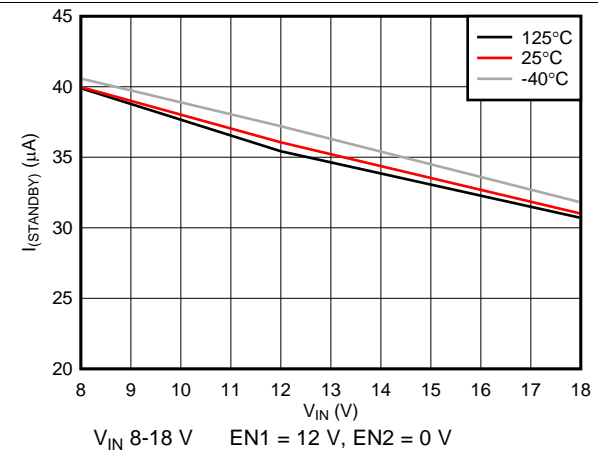
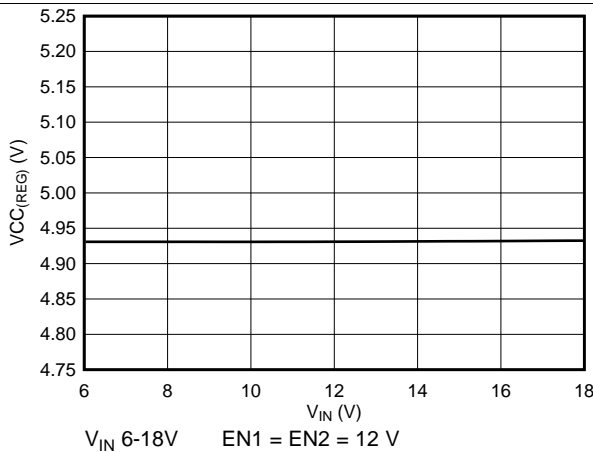
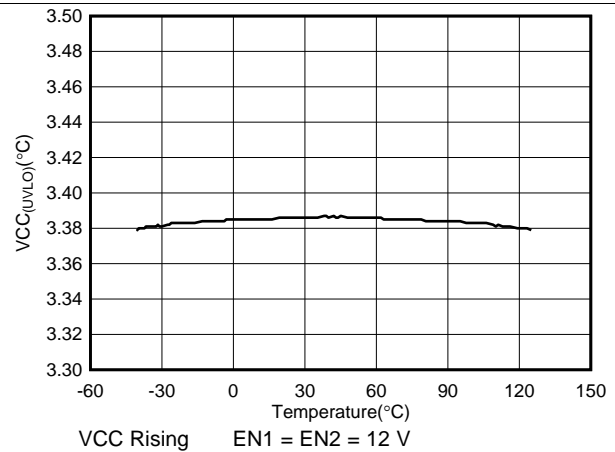
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LO GATE DRIVER						
V_{OLL}	LO Low-state Output Voltage	$I_{LO} = 100\text{ mA}$		0.05		V
V_{OHL}	LO High-state Output voltage	$I_{LO} = -100\text{ mA}$, $V_{OHL} = V_{CC} - V_{LO}$		0.07		V
t_{rLO}	LO rise time (10% to 90%)	$C_{LOAD} = 2700\text{ pf}$		4		ns
t_{fLO}	LO fall time (90% to 10%)	$C_{LOAD} = 2700\text{ pf}$		3		ns
I_{OHL}	LO peak source current	$V_{CCX} = 5\text{ V}$		3.25		Apk
I_{OLL}	LO peak sink current	$V_{CCX} = 5\text{ V}$		4.25		Apk
ADAPTIVE DEAD TIME CONTROL						
$V_{(GS-DET)}$	VGS detection threshold	VGS falling, no-load		2.5		V
$tdly1$	HO off to LO on dead time			20		ns
$tdly2$	LO off to HO on dead time			15		ns
DIODE EMULATION						
V_{IL}	DEM input low threshold				0.4	V
V_{IH}	FPWM input high threshold		2.4			V
SW	zero cross threshold			-5		mV
ENABLE INPUTS EN1 AND EN2						
V_{IL}	Enable input low threshold	$V_{CCX} = 0\text{ V}$			0.4	V
V_{IH}	Enable input high threshold	$V_{CCX} = 0\text{ V}$	2.4			V
I_{lkg}	Leakage	EN1, EN2 logic inputs only		1		μA
SYN INPUT						
V_{IL}	SYNIN input low threshold				0.4	V
V_{IH}	SYNIN input high threshold		2.4			V
	SYNIN input low frequency range 440kHz		350		550	kHz
	SYNIN input low frequency range 2.2MHz		1800		2600	kHz
SYN OUTPUT						
V_{OH}		Source -16 mA, $V_{DDA} = 5\text{ V}$	2.4			V
V_{OL}		Sink 16 mA			0.4	V
	Phase between HO1 and HO2			180		degrees
	Duty Cycle			50%		
SOFT-START						
I_{SS}	Soft-Start current		16	22	28	μA
$R_{DS(ON)}$	Soft-start pull-down resistance			3		Ω
THERMAL						
	TSD Thermal Shutdown			175		$^{\circ}\text{C}$
	Thermal shutdown hysteresis			15		$^{\circ}\text{C}$

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Oscillator Frequency, 2.2 MHz	$OSC = V_{DDA}$, $V_{IN} = 8\text{ V} - 18\text{ V}$	2060	2200	2340	kHz
	Oscillator Frequency, 440 kHz	$OSC = GND$, $V_{IN} = 8\text{ V} - 18\text{ V}$	410	440	470	kHz
t_{on}	Minimum on-time			45		ns
t_{off}	Minimum off-time				100	ns

7.7 Typical Characteristics


Figure 1. Efficiency vs VIN, FPWM

Figure 2. Efficiency vs VIN, DEMB

Figure 3. $I_{SHUTDOWN}$ vs Temperature

Figure 4. $I_{STANDBY}$ vs VIN

Figure 5. $V_{CC(REG)}$ vs V_{IN}

Figure 6. $V_{CC(UVLO)}$ vs Temperature

Typical Characteristics (continued)

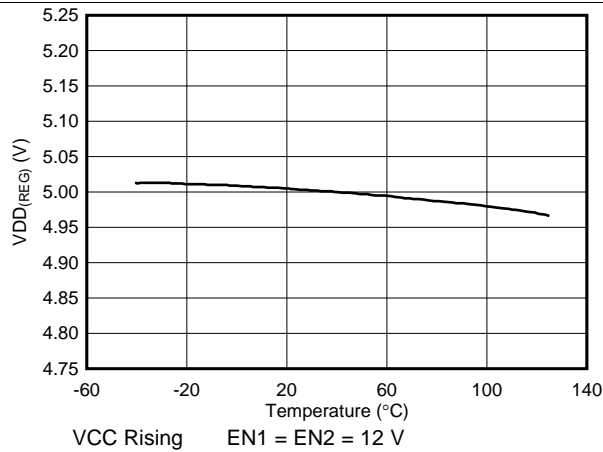


Figure 7. $V_{DDA(REG)}$ vs Temperature

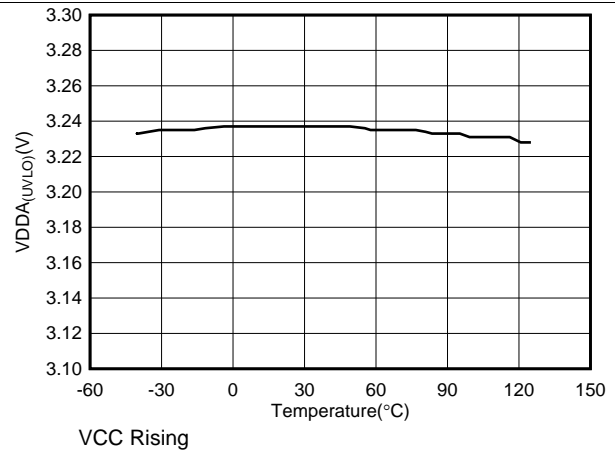


Figure 8. $V_{DDA(UVLO)}$ vs Temperature

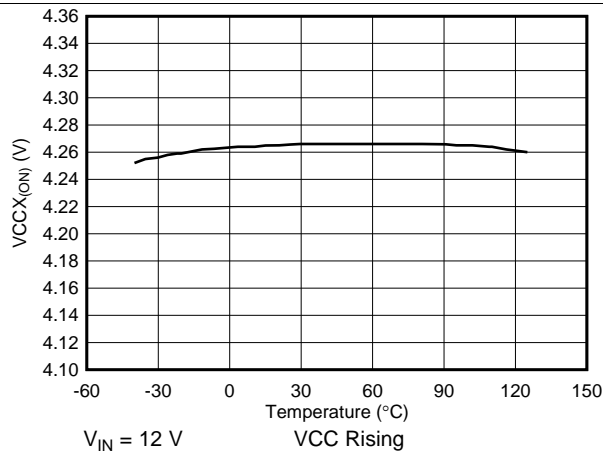


Figure 9. $V_{CCX(ON)}$ vs Temperature

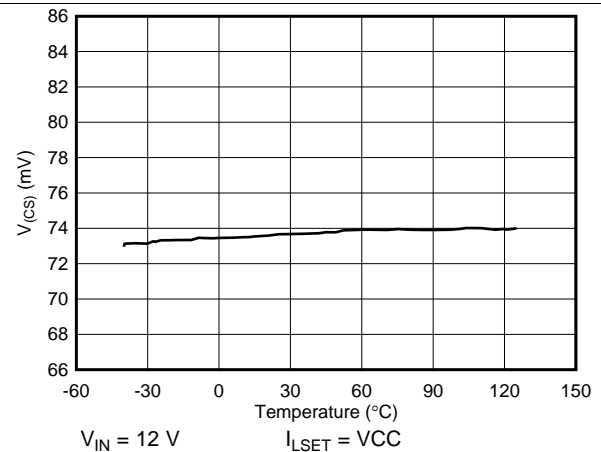


Figure 10. $V_{(CS1)}$ 73 mV Current Limit Threshold vs Temperature

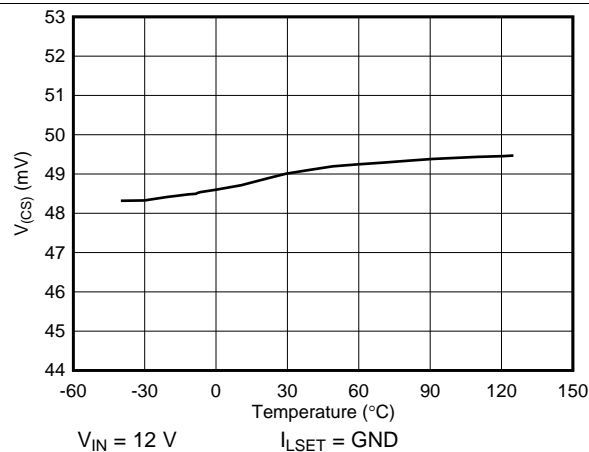


Figure 11. $V_{(CS2)}$ 48 mV Current Limit Threshold vs Temperature

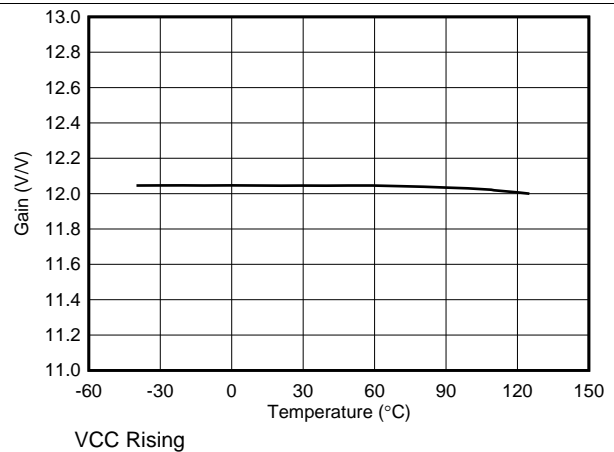


Figure 12. Current Sense Amplifier Gain vs Temperature

Typical Characteristics (continued)

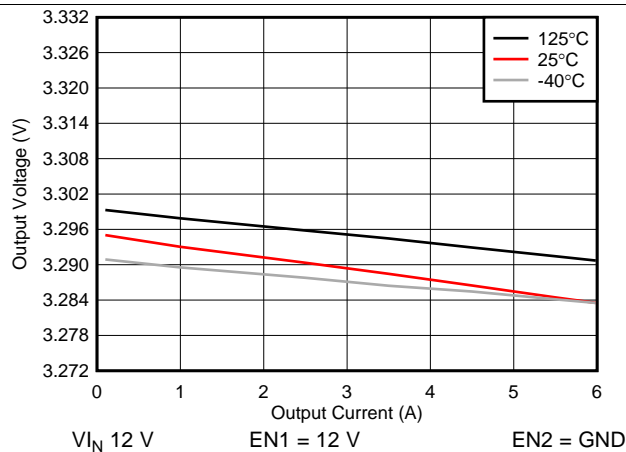


Figure 13. 3.3-V Output Voltage Regulation

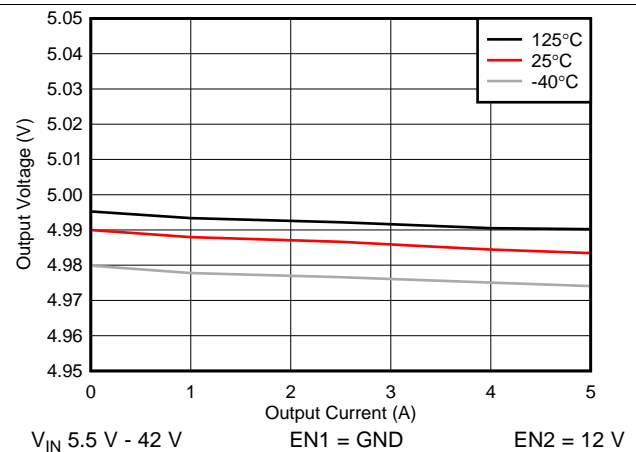


Figure 14. 5-V Output Voltage Regulation

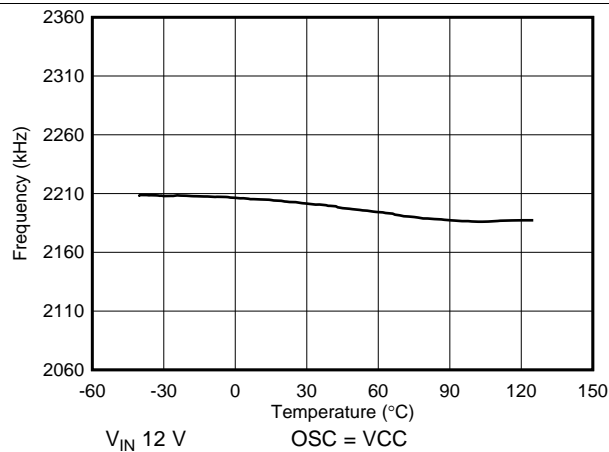


Figure 15. 2.2-MHz Oscillator Frequency vs Temperature

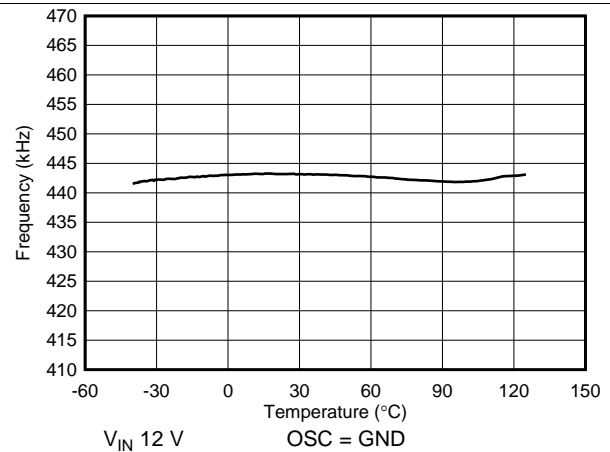


Figure 16. 440-kHz Oscillator Frequency vs Temperature

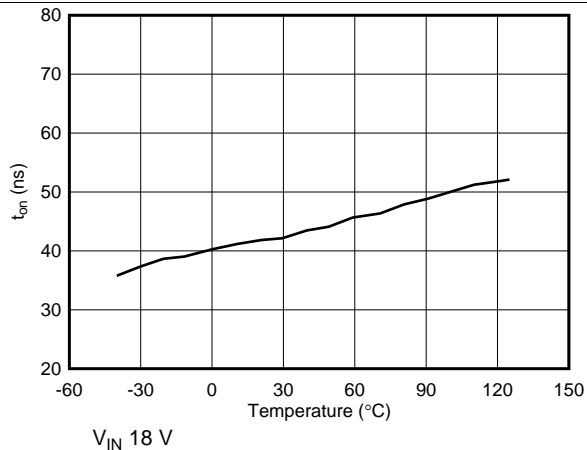


Figure 17. t_{on} Minimum vs Temperature

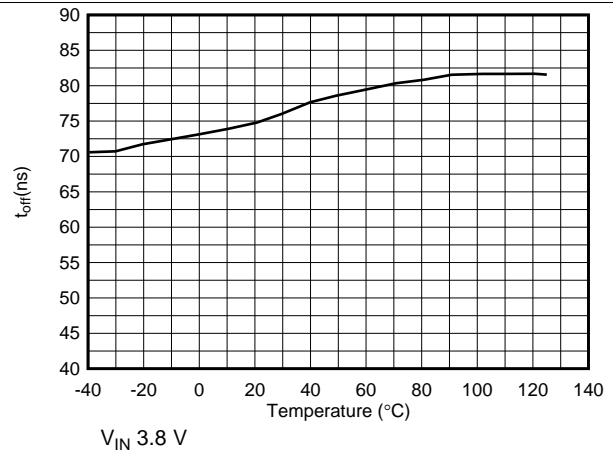


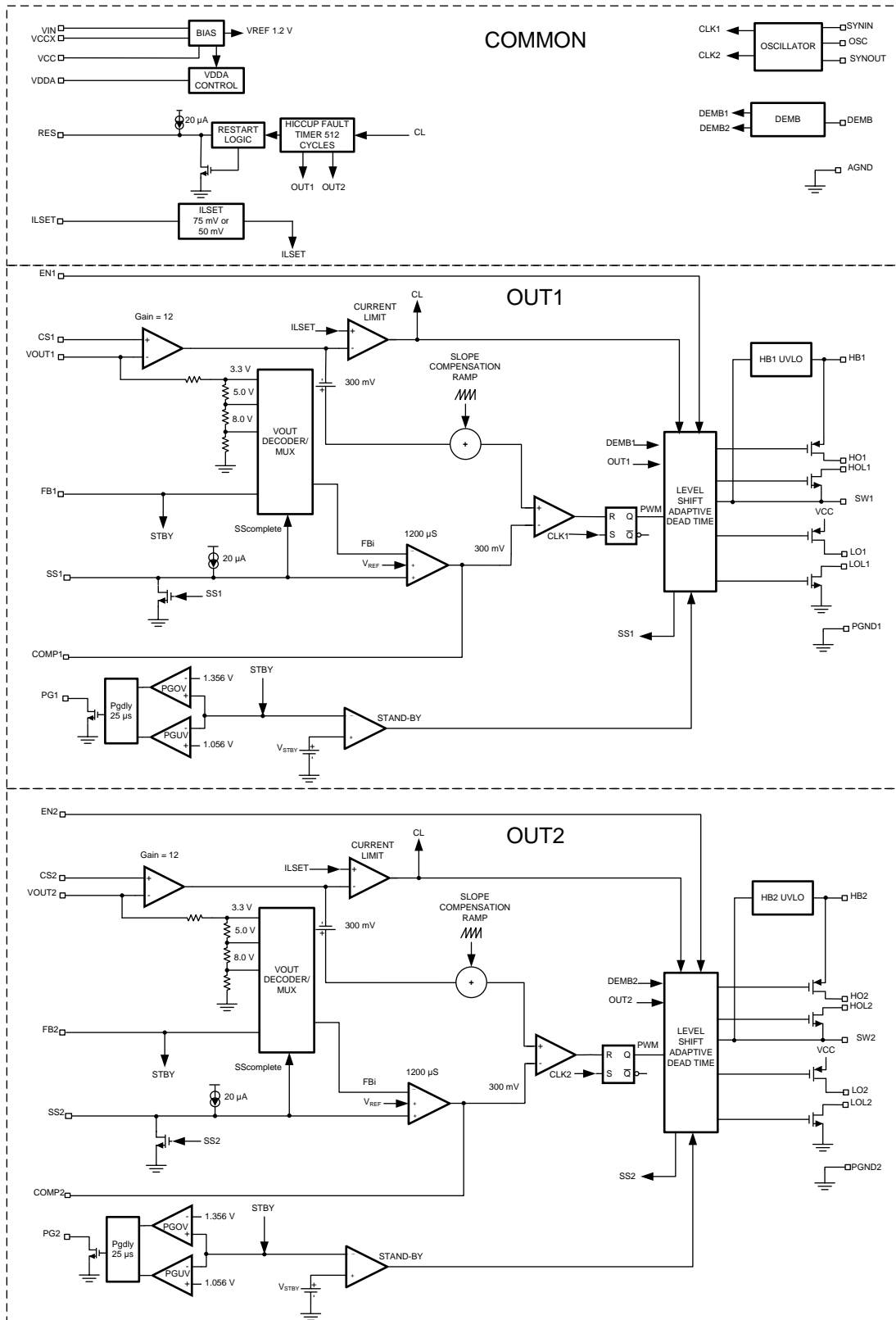
Figure 18. t_{off} Minimum vs Temperature

8 Detailed Description

8.1 Overview

The LM5140-Q1 is a dual channel switching controller which features all of the functions necessary to implement a high efficiency buck power supply that can operate over a wide input voltage range. The LM5140-Q1 is configured to provide two independent outputs. VOUT1 can be a fixed 3.3 V, 5 V, or adjustable between 1.5 V to 15 V. VOUT2 can be a fixed 5 V, 8 V, or adjustable between 1.5 V to 15 V. This easy to use controller integrates high-side and low-side MOSFET drivers capable of sourcing 3.25 A and sinking 4.25 A peak. The control method is current mode control which provides inherent line feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. With the OSC pin connected to VDD the default oscillator frequency is 2.2 MHz. With the OSC pin grounded the oscillator frequency is 440 kHz. A synchronization pin allows the LM5140-Q1 to be synchronized to an external clock. Fault protection features include current limiting, thermal shutdown, and remote shutdown capability. The LM5140-Q1 incorporates features that simplify compliance with the CISPR and Automotive EMI requirements. The LM5140-Q1 gate drivers provide adaptive slew rate control and interleaved operation (180 degree output of phase) of the two controller channels. The QFN-40L package with Wettable Flanks features an exposed pad to aid in thermal dissipation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 High Voltage Start-up Regulator

The LM5140-Q1 contains an internal high voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers for the external MOSFETs. The input pin (VIN) can be connected directly to an input voltage source up to 65 V. The output of the VCC regulator is set to 5 V. When the input voltage is below the VCC set-point level, the VCC output will track VIN with a small voltage drop.

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 70 V during line or load transients. Voltage ringing on the VIN pin that exceeds the [Absolute Maximum Ratings](#) can damage the IC. Use care during PCB board layout and high quality bypass capacitors to minimize ringing.

8.3.2 VCC Regulator

The VCC regulator output current limit is 150 mA (minimum). At power-up, the regulator sources current into the capacitors connected to the VCC pin. When the voltage on the VCC pin exceeds 3.4 V both output channels are enabled (if EN1 and EN2 are connected to a voltage source > 2.4 V) and the soft-start sequence begins. Both channels remain active unless the voltage on the VCC pin falls below the VCC_{UVLO} threshold, of 3.2 V (typical) or the enable pins are switched to a low state. The LM5140-Q1 has two VCC pins; these pins must be connected together on the PCB. It is recommended that the VCC capacitor be split between the two VCC pins and connected to the respective PGND pins. The recommended range for the VCC capacitor is from 2.2 µF to 5 µF total.

An internal 5-V linear regulator generates the VDDA bias supply. Bypass VDDA with a 100-nF or greater ceramic capacitor to ensure a low noise internal bias rail. Normally VDDA is 5 V, but there are two operating conditions where it regulates at 3.3 V. The first is in skip cycle mode with VOUT1 set to 3.3 V, and VOUT2 is disabled. The second is in a cold crank start-up where VIN is 3.8 V and VOUT1 is 3.3 V.

Internal power dissipation in the VCC Regulator can be minimized by connecting the VCCX pin to a 5 V output at VOUT1 or VOUT2 or to an external 5 V supply. If VCCX > 4.5 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. If VCCX is unused, it should be grounded. Never connect the VCCX pin to a voltage greater than 6.5 V.

8.3.3 Oscillator

The LM5140-Q1 has independent oscillators that generate the clock for each channel and can be programmed to 2.2 MHz or 440 kHz with the OSC pin. With the OSC pin connected to VDDA, both oscillators will be set to 2.2 MHz. With OSC grounded, they will both be set to 440 kHz. The state of the OSC pin is read and latched during VCC power up and thus cannot be changed until VCC drops below the VCC_{UVLO} threshold. CLK1 is the clock for channel 1; CLK2 is for channel 2. CLK1 and CLK2 are 180° out of phase. The rising edge of SYNOUT always corresponds to the rising edge of CLK2 which is 180° out of phase with CLK1.

Under low VIN conditions when either of the high-side buck switch on time exceeds the programmed oscillator period, the LM5140-Q1 will extend the oscillator period of that channel until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage. In such an event, the oscillators (CLK1 and CLK2) operate independently and asynchronously until both channels can maintain output regulation at the programmed frequency.

The approximate input voltage level where this occurs is:

$$VIN_{min} = VOUT \times \frac{t_p}{ton_{(max)}} \quad (1)$$

Where t_p = is the oscillator period, 454 ns (for 2.2 MHz operation) $ton_{(max)} = 354$ ns

For example, if VOUT1 = 3.3 V and VOUT2 = 5 V and VIN drops to 6.41 V:

$$VIN = 5.0 \text{ V} \times \frac{454 \text{ ns}}{354 \text{ ns}} = 6.41 \text{ V} \quad (2)$$

In the above example, CLK2 frequency is required to drop to maintain regulation of VOUT2 while CLK1 can remain at the programmed frequency (refer to [Figure 19](#)). If VIN continues to drop, both CLK1 and CLK2 frequencies are reduced [Figure 20](#).

Feature Description (continued)

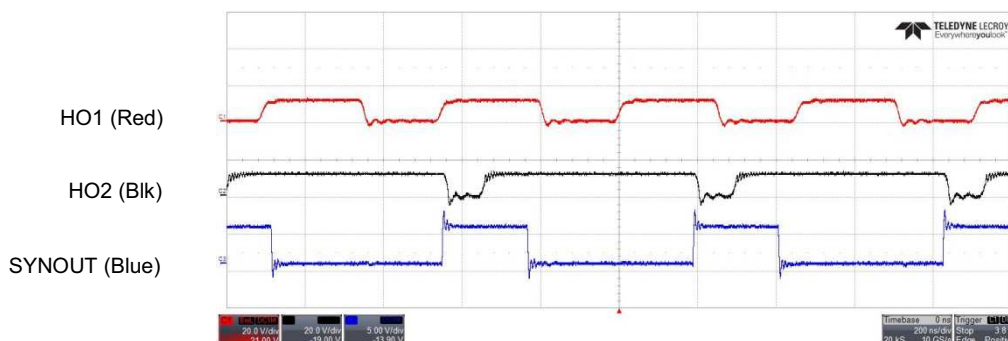


Figure 19. HO1, HO2, and SYNOUT VIN 6.41 V

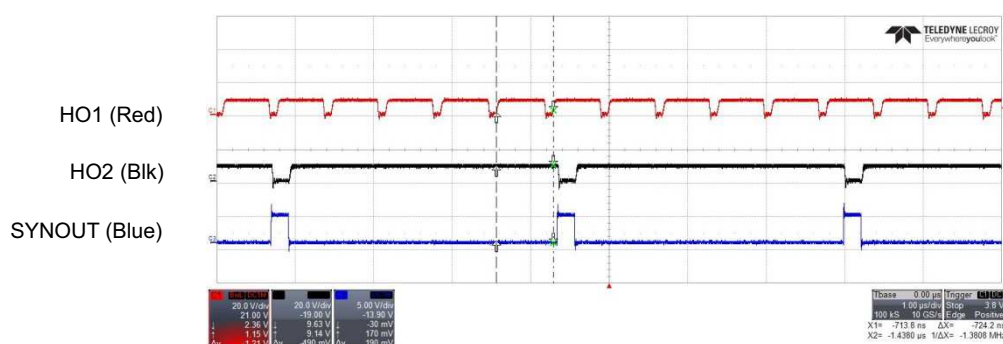


Figure 20. HO1, HO2, SYNOUT VIN 4.2 V

Under high input voltage conditions ($V_{IN} > 20V$) when the buck switch on time of either controller reaches the minimum on-time of 45ns typical, the LM5140-Q1 will reduce the oscillator frequency by skipping clock cycles for the appropriate channel.

Using the same output voltages as in the example above with VIN = 36 V, CLK1 drops to 1.1 MHz and CLK2 is 2.2 MHz, (refer to [Figure 21](#)), and SYNOUT is 2.2 MHz.

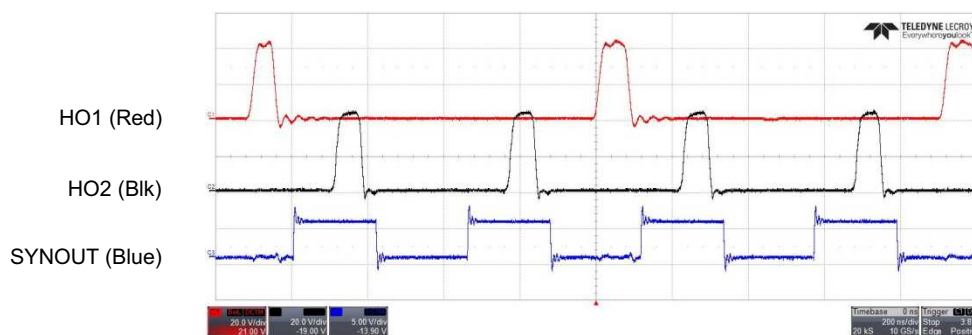


Figure 21. HO1, HO2, and SYNOUT VIN 36 V

Feature Description (continued)

8.3.4 SYNIN and SYNOUT

The SYNIN pin can be used to synchronize the LM5140-Q1 to an external clock. The synchronization range when the internal oscillator is set to 440 kHz is 374 kHz minimum to 506 kHz maximum. When the internal oscillator is set to 2.2 MHz the synchronization range is 1.87 MHz to 2.53 MHz. If the synchronization feature is not being used, the SYNIN pin should be grounded.

CLK1 starts on the rising edge of the external synchronization clock (SYNIN). The HO1 pulse will follow approximately 110ns after CLK1 due to internal delays (refer to [Figure 22](#)). Similarly, CLK2 generates the HO2 pulse after a short delay, and CLK2 is 180° out of phase with CLK1. SYNOUT always corresponds to the rising edge of CLK2.

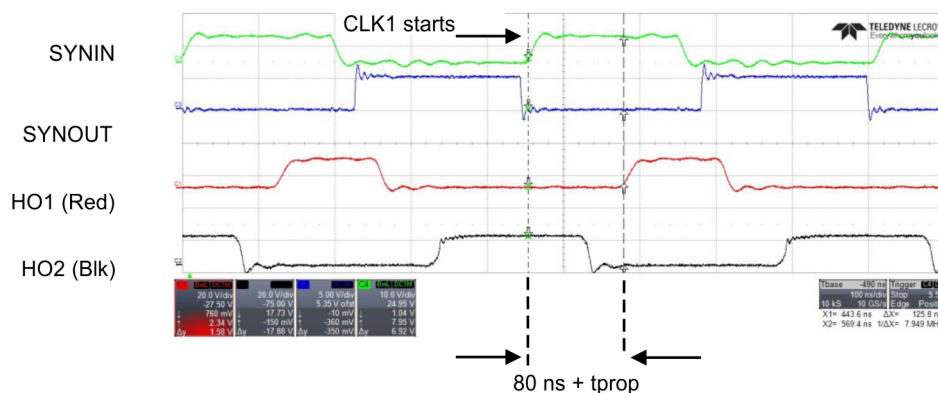


Figure 22. SYNIN and HO1 Timing (2.2 MHz)

Under low VIN conditions when the frequency must be reduced to maintain output voltage regulation, the SYNIN input function will adapt as necessary. If VOUT1 can maintain regulation at the SYNIN frequency and VOUT2 cannot, then CLK1 remains synchronized to SYNIN and the CLK2 frequency is reduced (refer to [Figure 23](#)). If VOUT1 cannot maintain regulation at the SYNIN frequency, then the SYNIN signal is ignored and channel 1 frequency is reduced to maintain regulation. Channel 2 runs at the frequency determined by OSC pin or lower if required to maintain regulation on VOUT2 (refer to [Figure 24](#)).

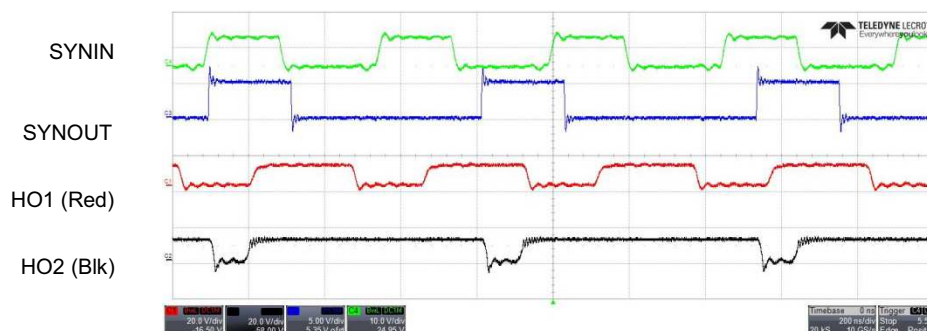


Figure 23. SYNIN (2.2 MHz) VIN 6.41 V

Feature Description (continued)

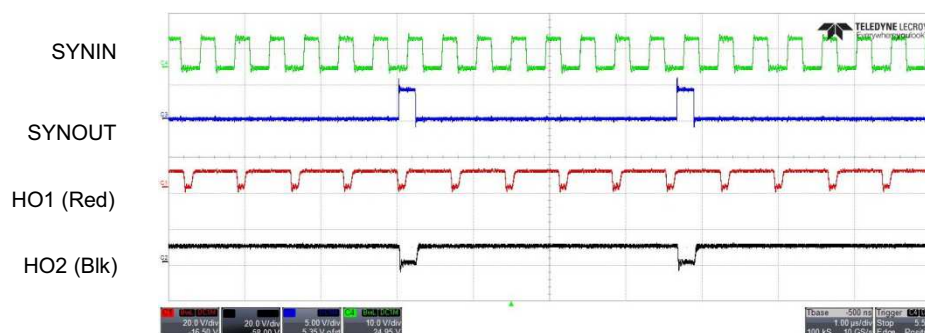


Figure 24. SYNIN (2.2 MHz) VIN 4.2 V

At high VIN when pulse skipping is necessary, HO1 drops to 1.1 MHz and HO2 remains at 2.2 MHz (refer to Figure 25), and SYNOUT is 2.2 MHz.

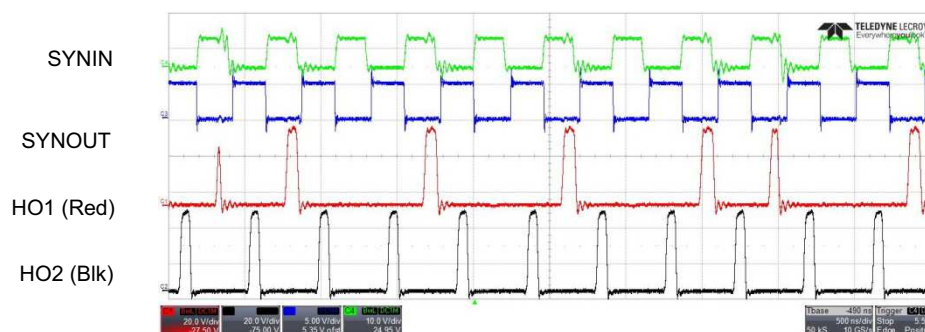


Figure 25. SYNIN (2.2 MHz) VIN 36 V

8.3.5 Enable

The LM5140-Q1 contains two enable inputs, EN1 and EN2. The enable pins allow independent start-up and shutdown control of VOUT1 (EN1) and VOUT2 (EN2). The enable pins can be connected to a voltage as high as 70 V. If the enable input is greater than 2.4 V, the respective controller output is enabled. If the enable pins is pulled below 0.4 V, the respective output will be in shutdown. If both outputs are disabled the LM5140-Q1 is in a low I_Q shutdown mode, with 9- μ A typical current drawn from the VIN pin. It is not recommended to leave either of the EN pins floating.

8.3.6 Power Good

The LM5140-Q1 includes output voltage monitoring signals for VOUT1 and VOUT2 to simplify sequencing and supervision. The power good function can be used to enable circuits that are supplied by the corresponding voltage rail or to turn-on sequenced supplies. Each power good output (PG1 and PG2) switches to a high impedance open drain state when the corresponding output voltage is in regulation. Each output switches low when the corresponding output voltage drops below the lower power good threshold (92% typical) or rises above the upper power good threshold (110% typical). A 25 μ s deglitch filter prevents any false tripping of the power good signals due to transients. Pull-up resistors of 10 k Ω (typical) are recommended from PG1 and PG2 to the relevant logic rail. PG1 and PG2 are asserted low during soft-start and when the corresponding buck converter is disabled by EN1 or EN2.

Feature Description (continued)

8.3.7 Output Voltage

The LM5140-Q1 outputs can be independently configured for one of two fixed output voltages with no external feedback resistors or adjusted to the desired voltage using external resistor dividers. VOUT1 can be configured as a 3.3-V output by connecting the FB1 pin to VDDA, or a 5-V output by connecting the FB1 pin to ground with a maximum resistance of 500 Ω. VOUT2 can be configured as either a 5-V output or 8-V output. For a 5-V output at VOUT2, connect the FB2 pin to VDDA. For a fixed 8-V output at VOUT2 connect FB2 to ground with a maximum resistance of 500 Ω. The FB1 and FB2 connections (either VDDA or GND) are detected during power-up. The configuration setting is latched and can not be changed until the LM5140-Q1 is powered down with VCC falling below V_{CC(UVLO)} (3.4 V typical) and then powered up again.

Alternative output voltages can be set external resistive dividers from output to the FB pins. The output voltage adjustment range is between 1.5 V and 15 V. The regulation threshold at the FB pin is 1.2 V (VREF). To calculate R_{FB1} and R_{FB2} use Equation 3, refer to Figure 26:

$$R_{FB2} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_{FB1} \quad (3)$$

The recommend value for R_(FB1) is between 10 kΩ to 20 kΩ.

The Thevenin equivalent impedance of the resistive divider connected to the FB pins must be greater than 5 kΩ for the LM5140-Q1 to detect the divider and set the channel to the adjustable output mode.

$$R_{TH} = \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}} > 5 \text{ k}\Omega \quad (4)$$

If a low I_Q mode is required, care should be taken when selecting the external resistors. The extra current drawn from the external divider is added to the LM5140-Q1 I_(STANDBY) current (35 μA typical). The divider current reflected to VIN is divided down by the ratio of VOUT/VIN. For example, if VOUT is set to 5.5 V with R_{FB1} 10 kΩ, and R_{FB2} = 35.8 kΩ (use 35.7 kΩ), the input current at VIN required to supply the current in the feedback resistors is:

$$I_{DIVIDER} = \frac{V_{OUT}}{R_{FB1} + R_{FB2}} \times \frac{V_{OUT}}{V_{IN}} = \frac{5.5 \text{ V}}{10 \text{ k} + 35.8 \text{ k}} \times \frac{5.5 \text{ V}}{12 \text{ V}} = 55.04 \text{ }\mu\text{A} \quad (5)$$

$$I_{VIN} \approx I_{(STANDBY)} + I_{DIVIDER} \approx 35 \text{ }\mu\text{A} + 55.04 \text{ }\mu\text{A} \approx 90.4 \text{ }\mu\text{A} \quad (6)$$

VIN = 12 V

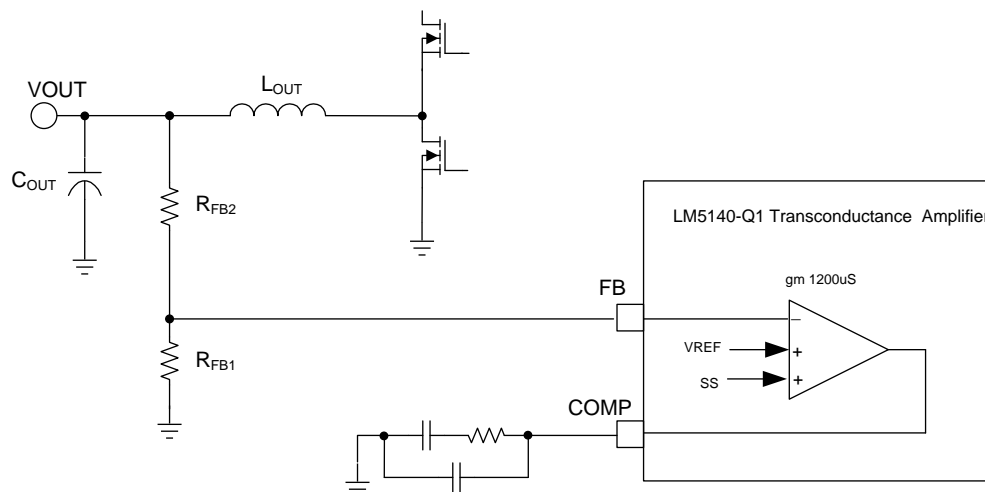


Figure 26. Voltage Feedback

Feature Description (continued)

If one output is enabled and the other disabled, VCC output will be in regulation. The HB pin voltage of the disabled channel will charge to VCC through the boot strap diode. As a result, the HO driver bias current (~3uA) can charge the disabled channel VOUT to approximately 2.2 V. If this is not desired, a load resistor (100 kΩ) can be added to the output that is disabled to maintain a low voltage off state.

8.3.8 Minimum Output Voltage Adjustment

There are two limitations to the minimum output voltage adjustment range: the LM5140-Q1 voltage reference 1.2 V and the minimum switch node pulse width, t_{SW} .

The minimum t_{SW} time limits the voltage conversion ratio (V_{OUT}/V_{IN}). For fixed-frequency PWM operation, the voltage conversion ratio should meet the following condition:

$$\frac{V_{OUT}}{V_{IN}} > t_{SW} \times F_{sw} \quad (7)$$

Where t_{SW} is 70 ns (typical) and F_{sw} is the switching frequency. If the desired voltage conversion ratio does not meet the above condition, the controller transitions from fixed frequency operation into a pulse skipping mode to maintain regulation of the output voltage.

For example if the desired output voltage is 3.3 V with a V_{IN} of 20 V and operating at 2.2 MHz, the voltage conversion ratio test is:

$$\begin{aligned} \frac{3.3 \text{ V}}{20 \text{ V}} &> 70 \text{ ns} \times 2.2 \text{ MHz} \\ 0.165 &> 0.154 \end{aligned} \quad (8)$$

For Wide V_{IN} applications and lower output voltages, an alternative is to use the LM5140-Q1 with 440-kHz oscillator frequency. Operating at 440 kHz, the limitation with the minimum t_{on} time is less significant. For example, if a 1.8-V output is required with a V_{IN} of 50 V:

$$\begin{aligned} \frac{1.8 \text{ V}}{50 \text{ V}} &> 70 \text{ ns} \times 440 \text{ kHz} \\ 0.036 &> 0.0308 \end{aligned} \quad (9)$$

8.3.9 Current Sense

There are two methods to sense the inductor current of the buck converters. The first is using current sense resistor in series with the inductor and the second is to use the dc resistance of the inductor (DCR sensing). [Figure 27](#) illustrates inductor current sensing using a current sense resistor. This configuration continuously monitors the inductor current providing accurate current-limit protection. For the best current-sense accuracy and over current protection, use a low inductance $\pm 1\%$ tolerance current-sense resistor between the inductor and output, with a Kelvin connection to the LM5140-Q1 sense amplifier.

The LM5140-Q1 provides two user selectable current limit levels of 48 mV and 73 mV. If the ILSET pin is connected to VDDA, the current limit threshold is 73 mV. When the ILSET pin is connected to ground, the current limit set point is 48 mV. The ILSET pin is monitored during power up and the setting is latched. To change the setting, V_{IN} power must be removed from the controller allowing the VCC voltage to drop below $V_{CC(UVLO)}$.

If the peak differential current signal sensed from CS to VOUT exceeds the user selectable current limit level of 48 mV or 73 mV, the current limit comparator immediately terminates the HO output for cycle-by-cycle current limiting.

$$R_{sense} = \frac{V_{CS}}{\left(I_{OUT_{max}} + \frac{\Delta I}{2} \right)} \quad (10)$$

Where: V_{CS} is user selectable threshold of 48 mV or 73 mV.

$I_{OUT_{max}}$ is the over current set point which is set higher than the maximum load current to avoid tripping the over current comparator during load transients.

ΔI is the peak-peak inductor current.

Feature Description (continued)

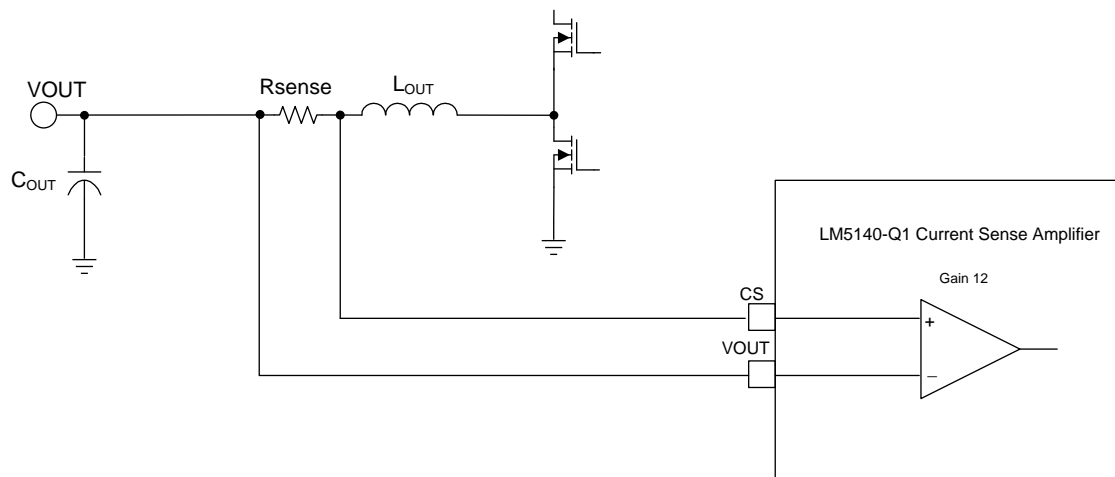


Figure 27. Current Sense

8.3.10 DCR Current Sensing

For high-power applications which do not require high accuracy current-limit protection, DCR sensing may be preferable. This technique provides lossless and continuous monitoring of the output current using an RC sense network in parallel with the inductor. Using an inductor with a low DCR tolerance, the user can achieve a typical current limit accuracy within the range of 10% to 15% at room temperature.

Components R_{SC} and C_{CS} in Figure 28 create a low-pass filter across the inductor to enable differential sensing of the voltage drop across inductor DCR. When $R_{CS} \times C_{CS}$ is equal to L_{OUT}/L_{DCR} , the voltage developed across the sense capacitor, C_{CS} , is a replica of the inductor DCR voltage waveform. Choose the capacitance of C_{CS} to be greater than 0.1 μF to maintain a low impedance sensing network, thus reducing the susceptibility of noise pickup from the switch node. Carefully observe the PCB layout guidelines to ensure the noise and DC errors do not corrupt the differential current-sense signals applied across the CS and VOUT pins.

The voltage drop across C_{CS} :

$$V_{CS} = \frac{1 + sL_{out}}{\frac{L_{DCR}}{1 + sR_{CS}C_{CS}}} I_{pk} \times L_{DCR} \quad (11)$$

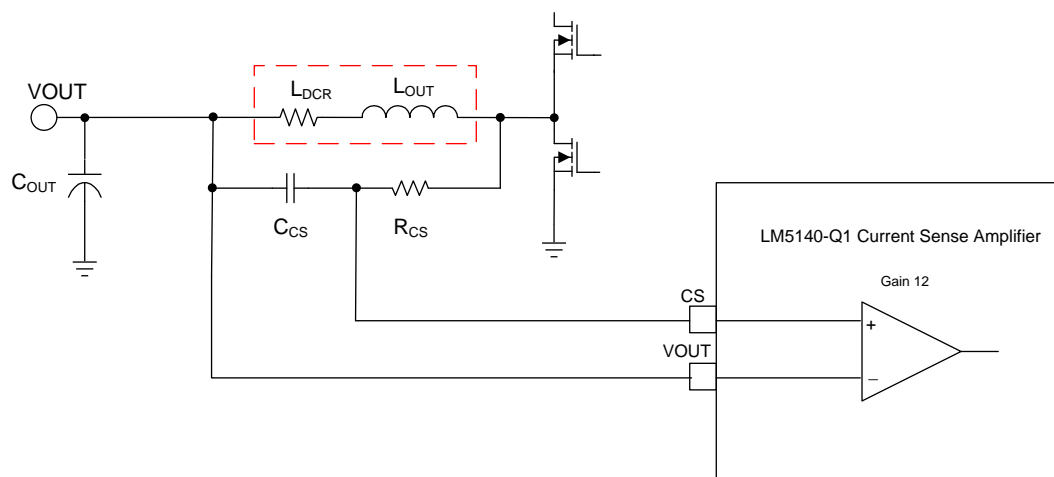


Figure 28. DCR Current Sensing

Feature Description (continued)

$R_{CS}C_{CS} = L_{OUT}/L_{DCR} \rightarrow$ accurate DC and AC current sensing.

If the RC time constant is not equal to the L_{OUT}/L_{DCR} time constant there will be an error.

$R_{CS}C_{CS} > L_{OUT}/L_{DCR} \rightarrow$ DC level still correct, the AC amplitude will be attenuated.

$R_{CS}C_{CS} < L_{OUT}/L_{DCR} \rightarrow$ DC level still correct, the AC amplitude will be amplified.

8.3.11 Error Amplifier and PWM Comparator

Each channel of the LM5140-Q1 has an independent high-gain transconductance amplifier which generates an error current proportional to the difference between the feedback voltage and an internal precision reference (1.2 V). The output of each transconductance amplifier is connected to the COMP pin allowing the user to provide external control loop compensation. Generally for current mode control a type II network is recommended.

8.3.12 Slope Compensation

The LM5140-Q1 provides internal slope compensation to ensure stable operation with duty cycle greater than 50%. To correctly use the internal slope compensation, the inductor value must be calculated based on the following guidelines:

$$L_{OUT} = \frac{V_{OUT}}{F_{sw} \times LX} \quad (12)$$

Where LX is 1 ± 0.25

- Lower inductor values increase the peak-to-peak inductor current, which minimizes size and cost and improves transient response at the cost of reduced efficiency due to higher peak currents.
- Higher inductance values decrease the peak-to-peak inductor current, which increases efficiency by reducing the RMS current at the cost of requiring larger output capacitors to meet load-transient specifications.

8.4 Device Functional Modes

8.4.1 Hiccup Mode Current Limiting

The LM5140-Q1 includes an optional hiccup mode protection function that is enabled when a capacitor is connected to the RES pin. In normal operation the RES capacitor is discharged to ground. If 512 cycles of cycle-by-cycle current limiting occur on either channel, the SS pin capacitor of that channel is pulled low and the HO and LO outputs are disabled (refer to [Figure 29](#)). A 20- μ A current source begins to charge the RES capacitor. When the RES pin charges to 1.2 V, the RES pin is pulled low and the SS capacitor begins to charge. The 512 cycle hiccup counter is reset if 4 consecutive switching cycles occur without exceeding the current limit threshold. Separate hiccup counters are provided for each channel, but the RES pin is shared by both channels. One channel can be in the hiccup protection mode while the other operates normally. In the event that both channels are in an over-current condition triggering hiccup protection, the last hiccup counter to expire will pull RES low and start the RES capacitor charging cycle. Both channels will then restart together when RES=1.2 V. If RES is connected to VDDA at power-up, the hiccup function is disabled for both channels.

The controller is in forced PWM (FPWM) continuous conduction mode when the DEMB pin is connected to VDDA. In this mode the SS pin is clamped to a level 200 mV above the feedback voltage to the internal error amplifier. This ensures that SS can be pulled low quickly during a brief overcurrent event and prevent overshoot of VOUT when the overcurrent condition is removed.

If DEMB=0 V, the controller operates in diode emulation with light loads (discontinuous conduction mode) and the SS pin is allowed to charge to VDDA. This reduces the quiescent current of the LM5140-Q1. If 32 or more cycle-by-cycle current limit events occur, the SS pin is clamped to 200 mV above the feedback voltage to the internal error amplifier until the hiccup counter is reset. Thus, if a momentary overload occurs that causes at least 32 cycles of current limiting, the SS capacitor voltage will be slightly higher than the FB voltage and will control VOUT during recovery.

Device Functional Modes (continued)

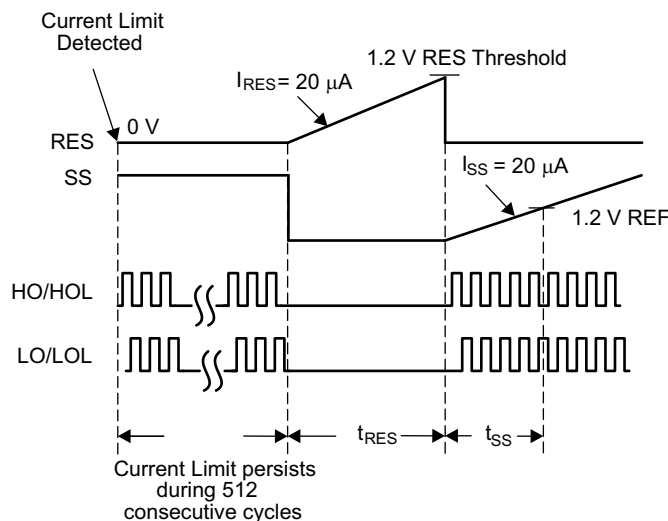


Figure 29. Hiccup Mode

8.4.2 Standby Mode

The LM5140-Q1 operates with peak current mode control such that the feedback compensation voltage is proportional to the peak inductor current. During no-load or light load conditions, the output capacitor will discharge very slowly. As a result the compensation voltage will not demand a driver output pulses on a cycle-by-cycle basis. When the LM5140-Q1 controller detects that there have been 16 missing switching cycles, it enters Standby Mode and switches to a low I_Q state to reduce the current drawn from VIN. For the LM5140-Q1 to go into a Standby Mode, the controller must be programmed for diode emulation (DEMB pin < 0.4 V). The typical I_Q in Standby Mode is 35 μ A with VOUT1 regulating at 3.3 V and VOUT2 disabled. With VOUT1 disabled and VOUT2 regulating to 5 V, the Standby Mode current is 42 μ A. With both channels in standby mode (VOUT1 = 3.3 V and VOUT2 = 5 V) the VIN current is 75 μ A. Using external feedback resistors will add additional load to VOUT and significantly increase the Standby Mode VIN current.

8.4.3 Soft-Start

The soft-start feature allows the regulator to gradually reach the steady state operating point, thus reducing startup stresses and surges. The LM5140-Q1 regulates the FB pin to the SS pin voltage or the internal 1.2-V reference, whichever is lower. At the beginning of the soft-start sequence when SS = 0 V, the internal 20- μ A soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the FB and output voltages.

The controller is in the forced PWM (FPWM) mode when the DEMB pin is connected to VDDA. In this mode, the SS pin is clamped at 200 mV above the feedback voltage to the internal error amplifier. This ensures that SS can be pulled low quickly during brief over-current events and prevent overshoot of VOUT during recovery. SS can be pulled low with an external circuit to stop switching, but this is not recommended. Pulling SS low will result in COMP being pulled down internally as well. If the controller is operating in FPWM mode (DEMB = VDDA), LO will remain on and the low-side MOSFET will discharge the VOUT capacitor resulting in large negative inductor current. When the LM5140-Q1 pulls SS low internally due to a fault condition, the LO gate driver is disabled.

8.4.4 Diode Emulation

A fully synchronous buck regulator implemented with a free-wheel MOSFET rather than a diode has the capability to sink current from the output in certain conditions such as light load, over-voltage, and pre-bias startup. The LM5140-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain to source) current flow in the low-side free-wheel MOSFET. When configured for diode emulation, the low-side MOSFET is disabled when reverse current flow is detected. The benefit of this configuration is lower power loss

Device Functional Modes (continued)

at no load or light load conditions and the ability to turn on into a pre-biased output without discharging the output. The negative effect of diode emulation is degraded light load transient response times. Enabling the diode emulation feature is recommended to allow discontinuous conduction operation. The diode emulation feature is configured with the DEMB pin. To enable diode emulation, connect the DEMB pin to ground or leave the pin floating. If continuous conduction operation is desired, the DEMB pin should be tied to VDDA.

8.4.5 High and low-side Drivers

The LM5140-Q1 contains a N-channel MOSFET gate drivers and an associated high-side level shifter to drive the external N-channel MOSFET. The high-side gate driver works in conjunction with an external bootstrap diode D_{BST} , and bootstrap capacitor C_{BST} , refer to Figure 30. During the on-time of the low-side MOSFET, the SW pin voltage is approximately 0 V and C_{BST} is charged from VCC through the D_{BST} . A 0.1- μ F or larger ceramic capacitor, connected with short traces between the BST and SW pin, is recommended.

The LO and HO outputs are controlled with an adaptive dead-time methodology which ensures that both outputs (HO and LO) are never enabled at the same time, preventing cross conduction. When the controller commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for the HO-SW voltage to drop below 2.5 V typical. LO is then enabled after a small delay (HO fall to LO rise delay). Similarly, the HO turn-on is delayed until the LO voltage has dropped below 2.5 V. HO is then enabled after a small delay (LO fall to HO rise delay). This technique ensures adequate dead-time for any size N-channel MOSFET device or parallel MOSFET configurations. Caution is advised when adding series gate resistors, as this may decrease the effective dead-time. Each of the high and low-side drivers have an independent driver source and sink output pins. This allows the user to adjust drive strength to optimize the switching losses for maximum efficiency and control the slew rate for reduced EMI. The selected N-channel high-side MOSFET determines the appropriate boost capacitance values C_{BST} in the Figure 30 according to Equation 13.

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \quad (13)$$

Where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} such that the available gate-drive voltage is not significantly degraded when determining C_{BST} . A typical range of ΔV_{BST} is 100 mV to 300 mV. The bootstrap capacitor should be a low-ESR ceramic capacitor. A minimum value of 0.1 μ F to 0.47 μ F is best in most cases. Care should be taken when choosing the high-side and low-side MOSFET devices with logic level gate thresholds.

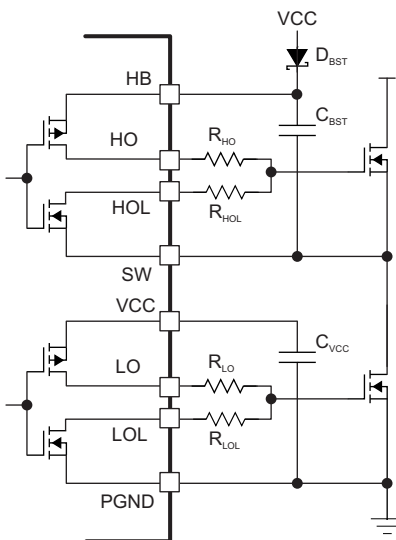


Figure 30. Drivers

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM5140-Q1 is a synchronous buck controller used to convert a higher input voltage to two lower output voltages. The following design procedure can be used to select external component values. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process. In addition to the WEBENCH software the LM5140ADESIGN-CALC.XXS quick start Excel calculator is available at www.ti.com.

9.2 Typical Application

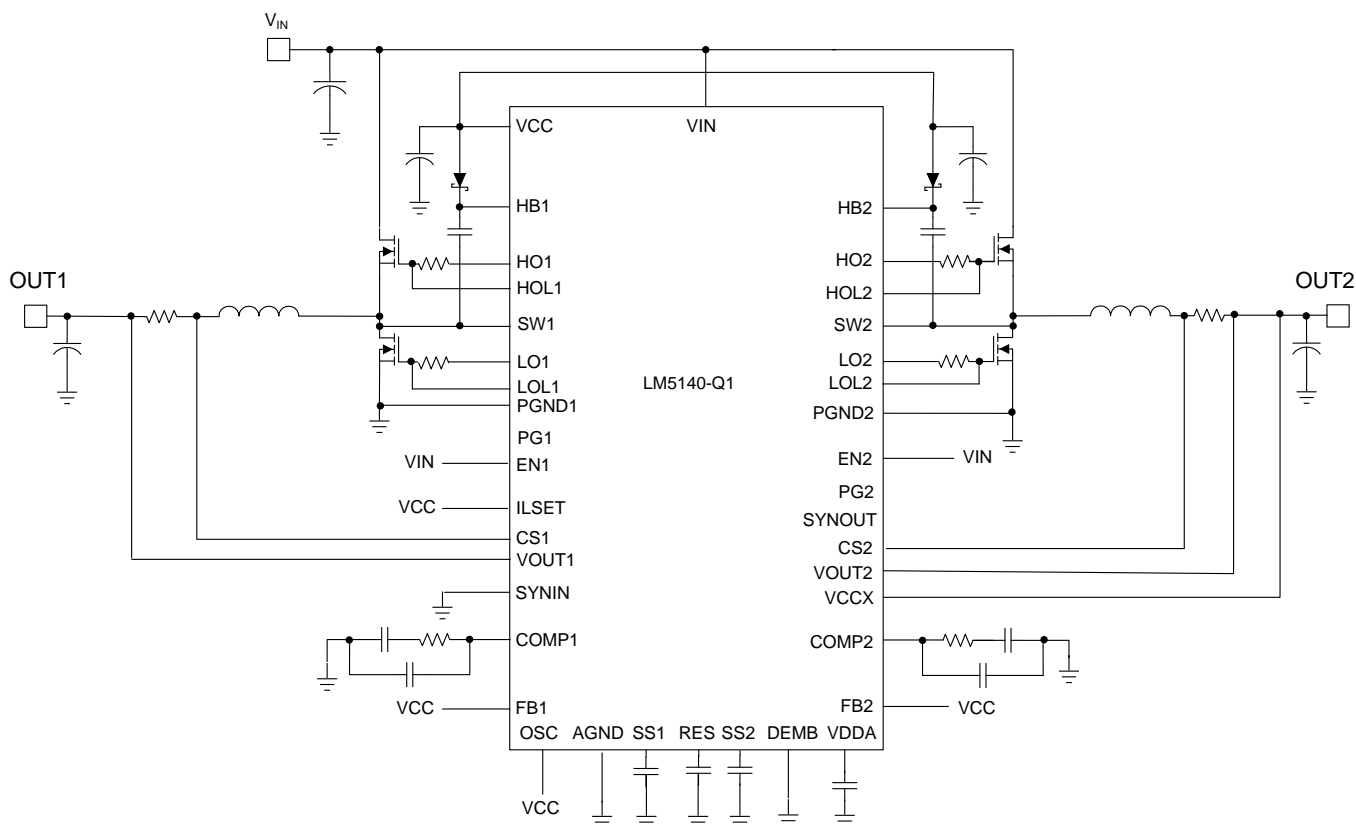


Figure 31. 12-V to 3.3-V and 5-V Converter

Typical Application (continued)

9.2.1 Design Requirements

For this design example, the intended input, output and performance parameters are shown in [Table 1](#).

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range (Steady State)	8 V to 18 V
Transient	42 V
Cold Crank	3.8 V
Output voltage	3.3 V
Output current	6 A
Operating frequency	2.2 MHz
Output voltage regulation	± 1%
Standby current, one output enabled, no-load	< 35 µA
Shutdown Current	9 µA

9.2.2 Detailed Design Procedure

- Buck Inductor calculation
- Peak inductor current calculation
- Current Sense resistor
- Output capacitor
- Input filter design
- MOSFET selection
- Control Loop design

9.2.2.1 Inductor Calculation

For design simplification, the LM5140-Q1 has internal slope compensation to eliminate sub-harmonic oscillation. For proper slope compensation, the inductor value should be calculated based on the following guidelines:

$$L_{OUT} = \frac{V_{OUT}}{F_{sw} \times LX} \quad (14)$$

Where LX is 1 ±0.25

- Lower inductor values increase the peak-to-peak inductor current, which minimizes size and cost and improves transient response at the expense of reduced efficiency due to higher peak currents.
- Higher inductance values decrease the peak-to-peak inductor current, which increases efficiency by reducing the RMS current but requires larger output capacitors to meet load-transient specifications.

$$L_{OUT} = \frac{3.3 \text{ V}}{2.2 \text{ MHz} \times 1} = 1.5 \text{ µH} \quad (15)$$

A standard inductor value of 1.5 µH is selected.

$$D_{max} = \frac{V_{OUT}}{V_{IN_{min}}} = \frac{3.3 \text{ V}}{8 \text{ V}} = 0.413 \quad (16)$$

$$D_{min} = \frac{V_{OUT}}{V_{IN_{max}}} = \frac{3.3 \text{ V}}{18 \text{ V}} = 0.183 \quad (17)$$

The maximum peak-to-peak inductor current is:

$$\Delta I = \frac{V_{IN_{max}} - V_{OUT}}{L_{OUT}} \times \frac{D_{min}}{F_{sw}} \quad (18)$$

$$\Delta I = \frac{18 \text{ V} - 3.3 \text{ V}}{1.5 \text{ µH}} \times \frac{0.183}{2.2 \text{ MHz}} = 0.815 \text{ Apk} \quad (19)$$

$$I_{pk} = I_{OUT} + \frac{\Delta I}{2} \quad (20)$$

$$I_{pk} = 6A + \frac{0.815}{2} = 6.41A_{pk} \quad (21)$$

9.2.2.2 Current Sense Resistor

When calculating the current sense resistor, the maximum output current capability ($I_{OUT_{MAX}}$) should be at least 20% higher than the required full load current to account for tolerances, ripple current, and load transients. For this example, 120% of the 6.41 A peak inductor current calculated in the previous section (I_{pk}) is 7.69 A. The current sense resistor value can be calculated using:

$$R_{sense} = \frac{V_{CS}}{I_{OUT_{max}}} \quad (22)$$

$$R_{sense} = \frac{73 \text{ mV}}{7.69 A_{pk}} = 0.00949 \Omega \quad (23)$$

Where: V_{CS} is the 73 mV current limit threshold.

The R_{sense} value selected is 9 m Ω

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the differential current sense signals between the CS and VOUT pins. Place the sense resistor close to the devices with short, direct traces, creating Kelvin-sense connections between the current-sense resistor and the LM5140-Q1.

The propagation delays through the current limit comparator, logic, and external MOSFET gate drivers allow the peak current to increase above the calculated current limit threshold. For a total propagation delay of $t_{dlyTOTAL}$, the worst case peak current through the inductor with the output is shorted can be calculated from:

$$I_{pk_{shortckt}} = \frac{V_{CS}}{R_{sense}} + \frac{V_{IN_{max}} \times t_{dlyTOTAL}}{L} \quad (24)$$

From the [Electrical Characteristics](#), $t_{dlyTOTAL}$ 40 ns. Therefore:

$$I_{pk_{shortckt}} = \frac{73 \text{ mV}}{0.009} + \frac{18 \text{ V} \times 40 \text{ ns}}{1.5 \mu\text{H}} = 8.59 A_{pk} \quad (25)$$

Once the peak current and the inductance parameters are known, the inductor can be chosen. An inductor with a saturation current greater than $I_{pk_{shortckt}}$ (8.59 A_{pk}) should be selected.

9.2.2.3 Output Capacitor

In a switch mode power supply, the minimum output capacitance is typically selected based on the capacitor ripple current rating and the load transient requirements. The output capacitor must be large enough to absorb the inductor energy and limit over voltage when transitioning from full-load to no-load, and to limit the output voltage undershoot during no-load to full load transients. The worst-case load transient from zero to full load occurs when the input voltage is at the maximum value and a current switching cycle has just finished. The total output voltage drop $V_{OUT_{UV}}$ is the sum of the voltage drop while the inductor is ramping up to support the full load and the voltage drop before the next pulse can occur.

The output capacitance required to maintain the minimum output voltage drop $V_{OUT_{UV}}$ can be calculated as follows:

$$C_{OUT_{min}} = \frac{L \times I_{STEP}^2}{2 \times V_{OUT_{UV}} \times D_{min} \times (V_{IN_{max}} - V_{OUT})} \quad (26)$$

$$C_{OUT_{min}} = \frac{1.5 \mu\text{H} \times 6 A^2}{2 \times 33 \text{ mV} \times 0.183 \times (18 \text{ V} - 3.3 \text{ V})} = 304 \mu\text{F} \quad (27)$$

Where:

- $I_{STEP} = 6A$
- $V_{OUT_{UV}} = 1\%$ of 3.3 V, or 33 mV

For this example a total of 293 μF of capacitance is used, three 82- μF aluminum capacitors for energy storage and one 47 μF low ESR ceramic capacitor to reduce high frequency noise.

Generally, when sufficient capacitance is used to satisfy the undershoot requirement, the overshoot during a full-load to no-load transient will also be satisfactory. After the output capacitance has been selected, calculate the output ripple current and verify that the ripple current is within the capacitor ripple current ratings.

For this design, the output ripple current is:

$$I_{OUT_{rms}} = \frac{\Delta I}{\sqrt{12}} \quad (28)$$

$$I_{OUT_{rms}} = \frac{0.815 A}{\sqrt{12}} = 0.235 Arms \quad (29)$$

9.2.2.4 Input Filter

A power supply input typically has a relatively high source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the buck switch on-time. When the buck switch turns on, the current drawn from the input capacitor steps from zero to the valley of the inductor current waveform, then ramps up to the peak value, and then drops to the zero at turn-off.

Average input current can be calculated from the total input power required to support the loads at VOUT1 and VOUT2:

$$P_{in} = \frac{V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2}}{\eta} \quad (30)$$

The efficiency η is assumed to be 83% for this design example, yielding total input power:

$$P_{in} = \frac{3.3 V \times 6 A + 5.0 V \times 5 A}{0.83} = 54 W \quad (31)$$

$$I_{avg} = \frac{P_{in}}{V_{IN_{min}}} \quad (32)$$

$$I_{avg} = \frac{54 W}{8 V} = 6.75 A \quad (33)$$

The ripple voltage on the input capacitors will be reduced significantly with a dual channel operation since each channel operates 180° out of phase from the other. Capacitors connected in parallel should be evaluated for their RMS current rating. The ripple current will split between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

The input capacitors should be selected with sufficient RMS current rating and the maximum voltage rating. The input ripple current with one channel operating is:

$$I_{IN(rms)} = \sqrt{\left[(I_{pk} - I_{avg})^2 + \frac{\Delta I^2}{12} \right] \times D_{max} + \left[(I_{avg})^2 \times (1 - D_{max}) \right]} \quad (34)$$

$$I_{IN(rms)} = \sqrt{\left[(6.41 - 2.98)^2 + \frac{0.815^2}{12} \right] \times 0.413 + (2.98^2 \times (1 - 0.413))} = 3.16 A \quad (35)$$

9.2.2.5 EMI Filter Design

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An under-damped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{in} = \left| -\frac{V_{IN_{min}}^2}{P_{in}} \right| \quad (36)$$

$$Z_{in} = \left| -\frac{8 \text{ V}^2}{54 \text{ W}} \right| = 1.18 \Omega \quad (37)$$

EMI Filter Design Steps:

- Calculate the required attenuation
- Capacitor C_{IN} represents the existing capacitor at the input of the switching converter
- Filter inductor L_f is usually selected between 1 μH and 10 μH (3.6 μH was used for this application), but it can be smaller to reduce losses in a high current design
- Calculate capacitor C_f

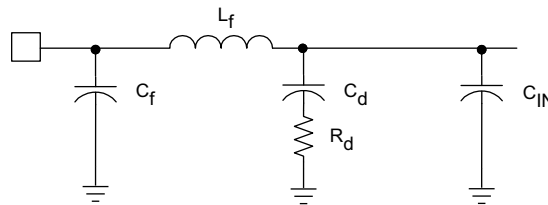


Figure 32. Input EMI Filter

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula can be derived to obtain the required attenuation:

$$|Attn| = 20 \log \left(\frac{I_{pk}}{\frac{\pi^2 \times f_{sw} \times C_{IN}}{1 \mu\text{V}}} \right) \times \sin(\pi \times D_{max}) - V_{max} \quad (38)$$

$$|Attn| = 20 \log \left(\frac{6.41}{\frac{\pi^2 \times 2.2 \text{ MHz} \times 10 \mu\text{F}}{1 \mu\text{V}}} \right) \times \sin(\pi \times 0.413) - 45 \text{ dB}\mu\text{V} = 44.06 \text{ dB} \quad (39)$$

V_{max} is the allowed dB μV noise level for the particular EMI standard, C_{IN} is the existing input capacitors of the buck converter. For this application 10 μF was selected. D_{max} is the maximum duty cycle. I_{pk} is the peak inductor current and for filter design purposes, the current at the input can be modeled as a squarewave. The EMI filter capacitor C_f is determined from:

$$C_f = \frac{1}{L_f} \left(\frac{10^{\frac{|Attn|}{40}}}{2 \times \pi \times F_{SW}} \right)^2 \quad (40)$$

$$C_f = \frac{1}{3.6 \mu\text{F}} = \left(\frac{10^{\frac{44.06}{40}}}{2 \times \pi \times 2.2 \text{ MHz}} \right)^2 = 0.25 \mu\text{F} \quad (41)$$

For this application, C_f was chosen to be 1 μF . Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. The resonant frequency of the filter is given by:

$$f_r = \frac{1}{2 \times \pi \sqrt{L_f \times C_f}} \quad (42)$$

$$f_r = \frac{1}{2 \times \pi \sqrt{1.8 \mu\text{H} \times 10 \mu\text{F}}} = 37.53 \text{ kHz} \quad (43)$$

The purpose of R_d is to reduce the peak output impedance of the filter at the resonant frequency. The capacitor C_d blocks the dc component of the input voltage to avoid excessive power dissipation in R_d . The capacitor C_d should have lower impedance than R_d at the resonant frequency with a capacitance value greater than the input capacitor C_{IN} . This will prevent C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance is high at the resonant frequency (Q of filter formed by C_{IN} and L_f is too high): An electrolytic cap C_d can be used as damping device, with the value of:

$$C_d = 4 \geq C_{IN} \quad (44)$$

$C_d = 4 \times 10 \mu\text{F}$, a 47- μF capacitor was selected and R_d is chosen using:

$$R_d = \sqrt{\frac{L_f}{C_{IN}}} \quad (45)$$

$$R_d = \sqrt{\frac{1.8 \mu\text{H}}{10 \mu\text{F}}} = 0.424 \Omega \quad (46)$$

9.2.2.6 MOSFET Selection

The LM5140-Q1 gate drivers are powered by the internal 5-V VCC bias regulator. To reduce power dissipation in the controller and improve efficiency, the VCCX pin which should be connected to 5-V output or an external 5 V bias supply. The MOSFETs used with the LM5140 require a logic-level gate threshold with on-resistance specified with $V_{GS} = 4.5 \text{ V}$ or lower.

The four MOSFETs must be chosen with a V_{DS} rating to withstand the maximum V_{IN} voltage plus supply voltage transients and spikes (ringing). For automotive applications, the maximum V_{IN} occurs during a load dump and the voltage can surge to 42 V under some conditions. A MOSFET with a V_{DS} rating of 60 V would meet most application requirements. The N-channel MOSFETs must be capable of delivering the average load current plus peak ripple current during switching.

The high-side MOSFET losses are associated with the $R_{DS(ON)}$ of the MOSFET and the switching losses.

$$P_{d_{HS}} = (I_{OUT}^2 \times R_{DS(on)} \times D_{max}) + \frac{1}{2} V_{IN} \times (t_r + t_f) \times I_{OUT} \times f_{sw} \quad (47)$$

$$P_{d_{HS}} = (6 \text{ A}^2 \times 0.026 \Omega \times 0.413) + \frac{1}{2} \times 12 \text{ V} \times (17 \text{ ns} + 17 \text{ ns}) \times 6 \text{ A} \times 2.2 \text{ MHz} = 2.69 \text{ W} \quad (48)$$

The losses in the low-side MOSFET include the $R_{DS(ON)}$ losses, the dead time losses, and losses in the MOSFETs internal body diode. The body diode conducts the inductor current during the dead time before the rising edge of the switch node. Minority carriers are injected into and stored in the body diode PN junction. As the high-side FET begins to turn-on, a negative current must first flow through the diode to remove the stored charge before the diode can be reverse biased. During this time, the high-side MOSFET drain-source voltage remains at V_{IN} until all the diode minority carriers are removed. Then the diode begins to block negative voltage and the reverse current continues to flow to charge the depletion capacitance of the body diode junction. The total charge required to reverse bias the diode is called reverse-recovery charge Q_{rr} . The power loss in the low-side MOSFET can be calculated from:

$$P_{d_{LS}} = (I_{OUT}^2 \times R_{DS(on)} \times (1 - D_{max})) + (I_{OUT} \times (t_{dr} + t_{df}) \times F_{SW} \times V_{DFET}) + (D_{Qrr} \times F_{SW} \times V_{IN}) \quad (49)$$

$$P_{d_{LO}} = 6^2 A \times 26 m\Omega \times (1 - 0.413) + (6 A \times 20 ns + 6 A \times 20 ns) \times 2.2 MHz \times 0.8 V + 105 nc \times 2.2 MHz \times 12 V = 3.744 W \quad (50)$$

Where t_{dr} and t_{df} are the switch node voltage rise and fall times (20 ns).

V_{DFET} the forward voltage drop across the low-side MOSFET internal body diode (0.8 V).

D_{Qrr} the internal body diode reverse recovery charge (105 nC).

$R_{DS(ON)}$ the on resistance of the low-side MOSFET (26 mΩ at $T_J = 125^\circ C$).

The table below provides parameters for several MOSFETs that have tested in the LM5140-Q1 evaluation module.

Manufacturer	Part Number	VDS (V)	ID (A)	Q_{gMAX} (nC) VGS = 4.5 V	$R_{DS(ON)}$ MAX (mΩ) VGS = 4.5	C_{OSS} /MAX	Application
VISHAY	SQJ850EP	60	24	30	32	215	Automotive High Power
VISHAY	SQ7414EN	60	5.6	25	36	175	Automotive Low Power
Texas Instruments	CSD18534Q5A	60	13	11.1	12.4	217	Industrial

9.2.2.7 Driver Slew Rate Control

Figure 33 shows the high current driver outputs with independent source and current sink pins for slew rate control. Slew rate control enables the user to adjust the switch node rise and fall times which can reduce the conducted EMI in the FM radio band (30 MHz to 108 MHz). Using the LM5140-Q1 EVM, conducted emission were measured in accordance with CISPR 25. Figure 34 shows the measured results without slew rate control. The conducted EMI results with slew rate control are shown in Figure 35.

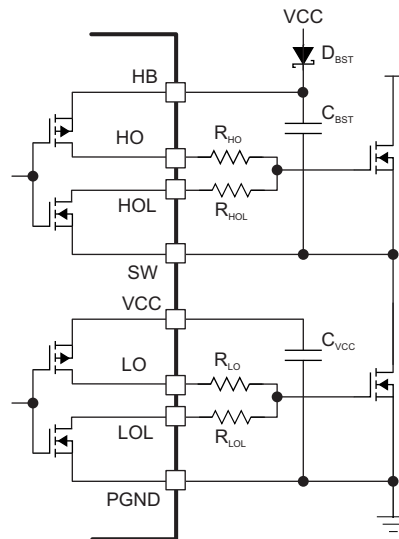


Figure 33. Drivers with Slew Rate Control

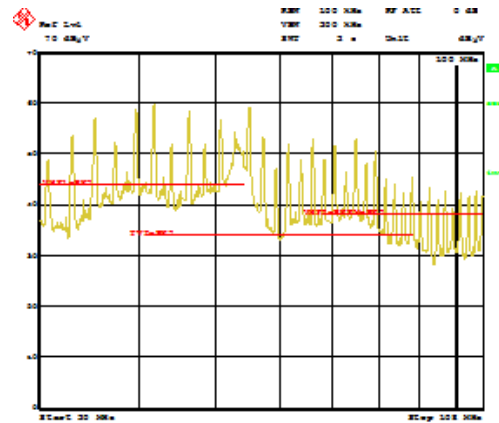


Figure 34. EMI Measurements CISPR 25, No Slew Rate Control

Referring to [Figure 34](#) and [Figure 35](#) a 10 dB reduction in conduction emissions in the FM band is attained by using slew rate control. This can reduce the size and cost of the EMI filters.

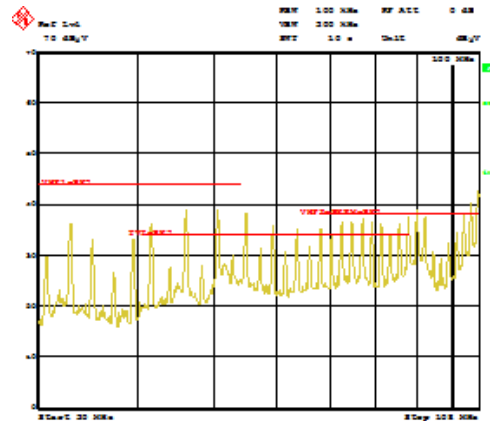


Figure 35. EMI Measurements CISPR 25 with Slew Rate Control

9.2.2.8 Sub-Harmonic Oscillation

For peak current mode control, sub-harmonic oscillation occurs with a duty cycle greater than 50% and is characterized by alternating wide and narrow pulses at the SW pin. By adding a compensating ramp equal to the down-slope of the inductor current, any tendency toward sub-harmonic oscillation is damped within one switching cycle.

In time-domain analysis, the steady-state inductor current starts and ends at the same value during one clock cycle. If the magnitude of the end-of-cycle current error, dl_1 , caused by an initial perturbation, dl_0 , is less than the magnitude of dl_0 or $dl_1/dl_0 > -1$, the perturbation naturally disappears after a few cycles, refer to [Figure 36](#). When $dl_1/dl_0 < -1$, the initial perturbation does not disappear resulting in sub-harmonic oscillation in steady-state operation. By choosing $K > 1$, sub-harmonic oscillation will be avoided.

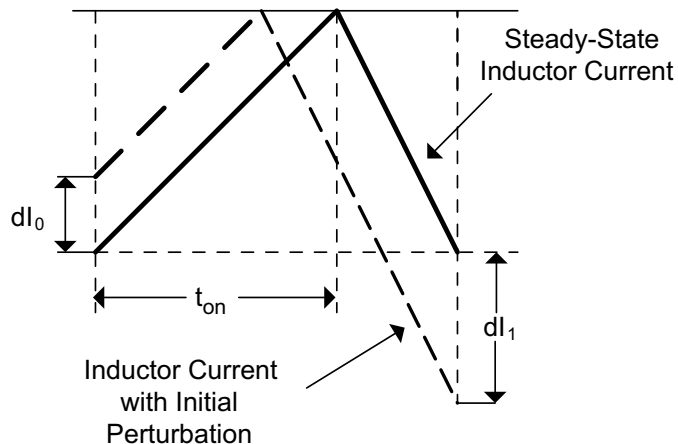


Figure 36. Sub-Harmonic Oscillation

$$\frac{dl_0}{dl_1} = 1 - \frac{1}{k}$$

(51)

The relationship between Q and K factor is illustrated graphically in [Figure 37](#).

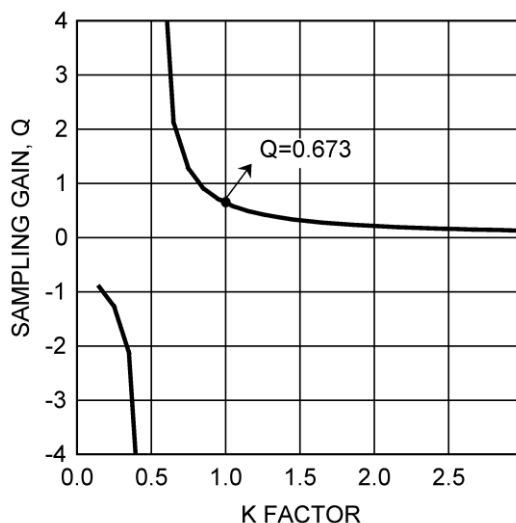


Figure 37. Sampling Gain Q vs K Factor

The minimum value of K is 0.5. This is the same as time domain analysis result. When $K < 0.5$, the regulator is unstable. High gain peaking at 0.5 results in sub-harmonic oscillation at $F_{SW}/2$. When $K = 1$, one-cycle damping is realized and Q is equal to 0.673 at this point. A higher K factor may introduce additional phase shift by moving the sampled gain inductor pole closer to the crossover frequency but will help reduce noise sensitivity in the current loop.

9.2.2.9 Control Loop

The open loop response of a buck converter is defined as the product of modulator and feedback transfer functions. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain. The modulator transfer function includes a power stage transfer function with an embedded current loop that can be simplified as one pole and a one zero system as shown in [Equation 52](#). The modulator transfer function is defined as follows:

$$\frac{V_{OUT}}{V_C} = AM \times \frac{\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_p}\right) \times \left(1 + \frac{s}{\omega_n Q} + \frac{s^2}{\omega_n^2}\right)} \quad (52)$$

$$s = 2 \times \pi \times \frac{F_{SW}}{2}$$

$$K = 1$$

$$Q = \frac{1}{\pi(K - 0.5)}$$

$$\omega_Z = \frac{1}{C_{ESR} \times C_O}$$

$$\omega_P = \frac{1}{R_{LOAD} \times C_O}$$

$$\omega_n = \pi \times \frac{F_{SW}}{2} \quad (53)$$

The equation includes the sample gain at $f_{SW}/2$ (ω_n), which is caused by sampling effect of current mode control. Refer to section [Sub-Harmonic Oscillation](#):

$$1 + \frac{s}{\omega_n Q} + \frac{s^2}{\omega_n^2} \quad (54)$$

$$AM = \frac{R_{LOAD}}{(R_{sense} + R_{DCR}) \times G_{CS}}$$

$$AM = \frac{0.471 \Omega}{(0.007 + 0.0081) \times 12} = 3.035 \quad (55)$$

$$\text{Gain in dB } 20\log(AM) \quad (56)$$

$$20 \log M(3.035) = 9.64 \quad (57)$$

G_{CS} is the current sense amplifier gain (12).

R_{LOAD} is the load resistance.

R_{DCR} is the dc resistance on the output inductor.

9.2.2.10 Error Amplifier

R_{COMP} and C_{COMP} configure the error amplifier gain characteristic to achieve a stable voltage feedback loop. One advantage of current mode control is the ability to compensate the loop with only two compensation components, R_{COMP} and C_{COMP} . The voltage loop gain is the product of the modulator gain and the error amplifier gain. For the 3.3-V output of this design example, the modulator is treated as an ideal voltage-to-current converter. The modulator gain of the LM5140-Q1 can be modeled as:

$$\frac{V_O}{V_C} = \frac{V_{REF}}{V_{OUT}} \times G_m \times R_{AMP} \times \frac{\left(1 + \frac{s}{\omega_{ZEA}}\right)}{\left(1 + \frac{s}{\omega_{PEA}}\right)} \quad (58)$$

$$\omega_{ZEA} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (59)$$

$$\omega_{PEA} \approx \frac{1}{R_{AMP} \times C_{COMP}} \quad (60)$$

Where:

V_{REF} is the feedback voltage reference (1.2 V)

G_m is the error amplifier gain transconductance (1200 μS)

R_{AMP} is the error amplifier output impedance (2.5 M Ω)

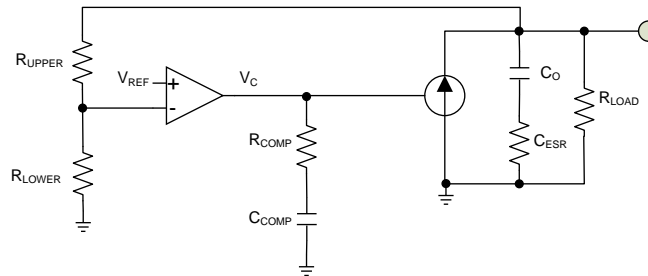


Figure 38. Transconductance Amplifier

The procedure for choosing compensation components for a stable closed loop is:

- Select the desired open loop gain crossover frequency (f_c); for this application 30 kHz was chosen
- Calculate the R_{COMP} resistor for the gain crossover frequency at 30 kHz

$$R_{COMP} = f_c \frac{V_{OUT}}{V_{REF}} \times \frac{2 \times \pi \times C_O \times R_{sense} \times G_{CS}}{G_m} \quad (61)$$

$$R_{COMP} = 30 \text{ kHz} \times \frac{3.3 \text{ V}}{1.2 \text{ V}} \times \frac{2 \times \pi \times 290 \mu F \times 0.007 \times 12}{1200 \times 10^{-6}} = 10517 \Omega \quad (62)$$

The value selected for R_{COMP} is 10 k Ω

- Calculate the C_{COMP} capacitor value to create a zero that cancels the pole ω_p ($\omega_p = 1/(R_{LOAD} \times C_O)$).

$$C_{COMP} = \frac{R_{LOAD} \times C_O}{R_{COMP}} \quad (63)$$

$$C_{COMP} = \frac{0.477 \times 290 \mu F}{10000} = 13.8 \text{ nF} \quad (64)$$

The value selected for C_{COMP} is 10 nF

9.2.3 Application Curves

Plotting the modulator gain and feedback gain, (refer to [Figure 39](#)).

The results are a gain crossover frequency of 20 kHz with 82° of phase margin, (refer to [Figure 40](#)).

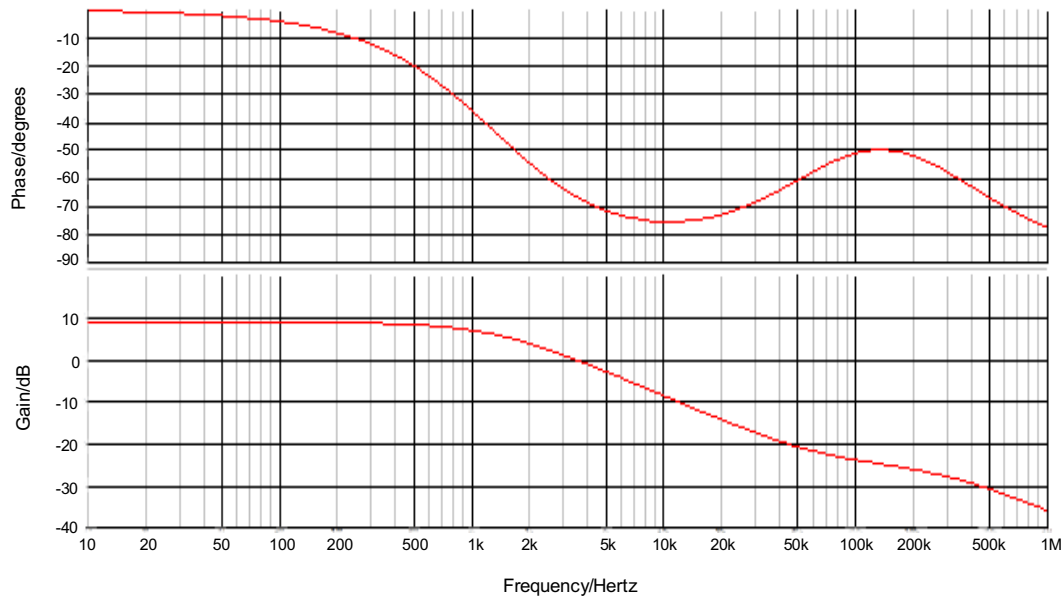


Figure 39. (V_O/V_C) Modulator Gain and Phase

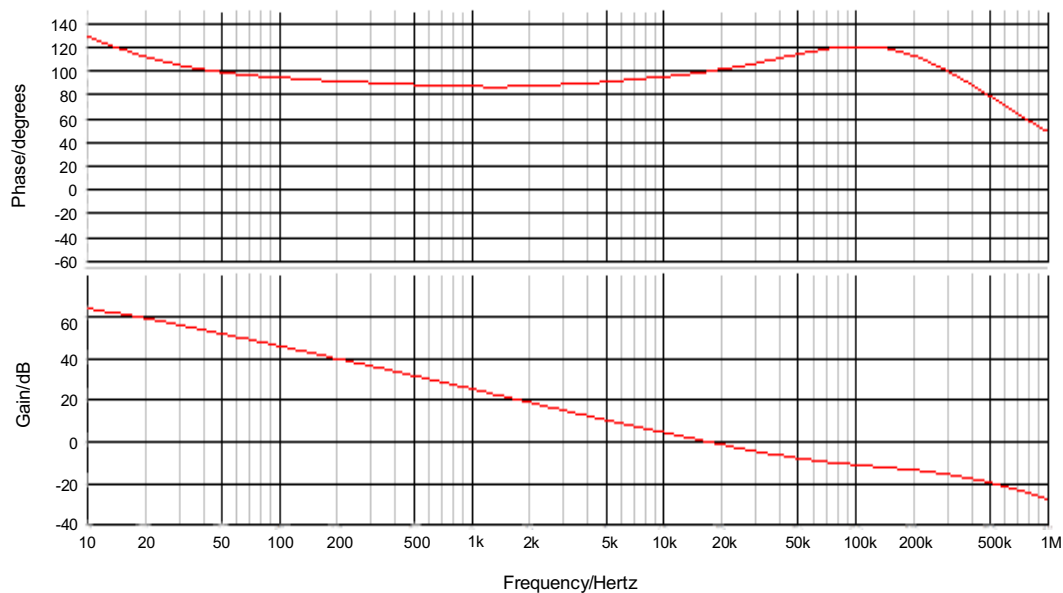


Figure 40. Open Loop Gain and Phase

10 Power Supply Recommendations

The LM5140EVM was designed to operate over an input voltage supply range between 3.8 V and 42 V. This input supply must be well regulated. If the power source is located more than a few inches from the LM5140-Q1 EVM, additional bulk capacitance and ceramic bypass capacitors may be required at the power supply input. An electrolytic capacitor with a value of 47 μ F is typically a good choice.

11 Layout

Careful PCB layout is critical to achieve low EMI and stable power supply operation. If possible, mount all the power components on the top side of the board, making the high frequency current loops as small as possible, and follow these guidelines of good layout practices:

1. Keep the high-current paths short. This practice is essential for stable, jitter-free operation.
2. Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper (2 oz) can enhance full load efficiency by 1% or more.
3. Minimize current-sensing errors by routing CS and VOUT using a kelvin sensing directly across the current-sense resistor (R_{sense}).
4. Route high-speed switching nodes (HB, HO, LO, and SW) away from sensitive analog areas (FB, CS, and VOUT).

11.1 Layout Procedure

- Place the power components first, with ground terminals adjacent to the low-side FET. If possible, make all these connections on the top layer with wide, copper-filled areas.
- Mount the controller IC as close as possible to the high and low-side MOSFETs. Make the grounds and high and low-sided drive gate drive lines as short and wide as possible. Place the series gate drive resistor as close to the MOSFET as possible to minimize gate ringing.
- Locate the gate drive components (D1 and C17) together and near the controller IC; refer to [Figure 41](#). Be aware that peak gate drive currents can be as high as 4 A. Average current up to 150 mA can flow from the VCC pin to the V_{CC} capacitor through the bootstrap diode to the bootstrap capacitor. Size the traces accordingly.
- Make the ground connections to the LM5140-Q1 controller as shown in [Figure 43](#). Create a power grounds directly connected to all high-power components and an analog ground plane for sensitive analog components. The analog ground plane (AGND) and power ground plane (PGND1, and PGND2) must be connected at a single point directly under the IC (at the die attach pad or DAP).
- [Figure 41](#) shows the schematic of the high frequency loops of one synchronous buck channel. The current flows through Q1 and Q2, through the power ground plane and back to VIN through the ceramic capacitors C11 and C12. This loop must be as small as possible to minimize EMI. Refer to [Figure 42](#) For the recommended PCB layout.

11.2 Layout Example

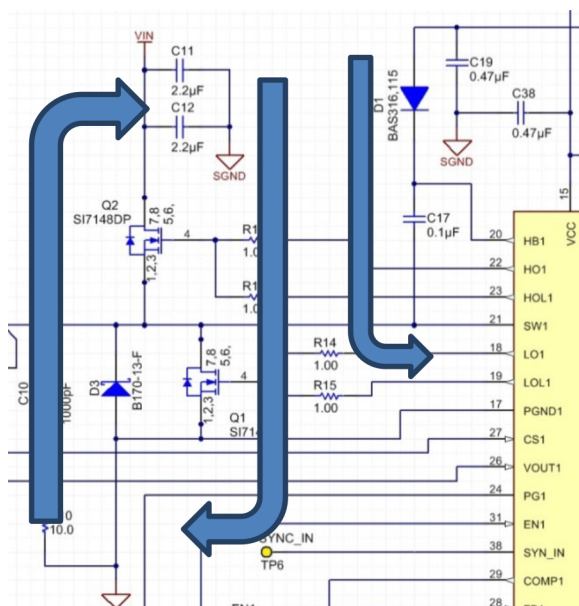


Figure 41. Synchronous Buck Power Flow

Layout Example (continued)

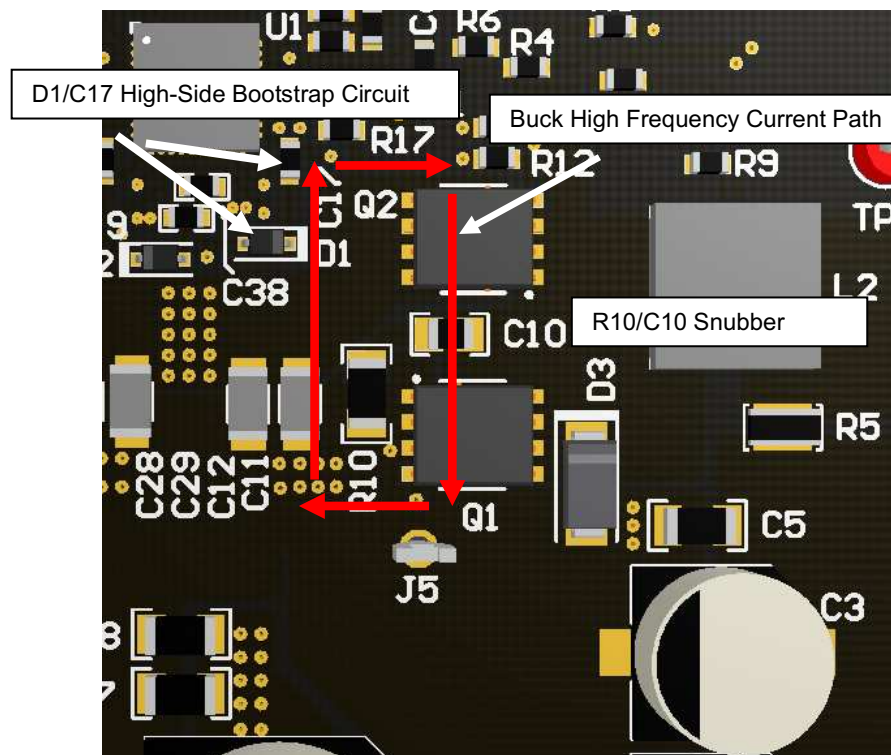


Figure 42. Synchronous Buck High Frequency Current Path

Layout Example (continued)

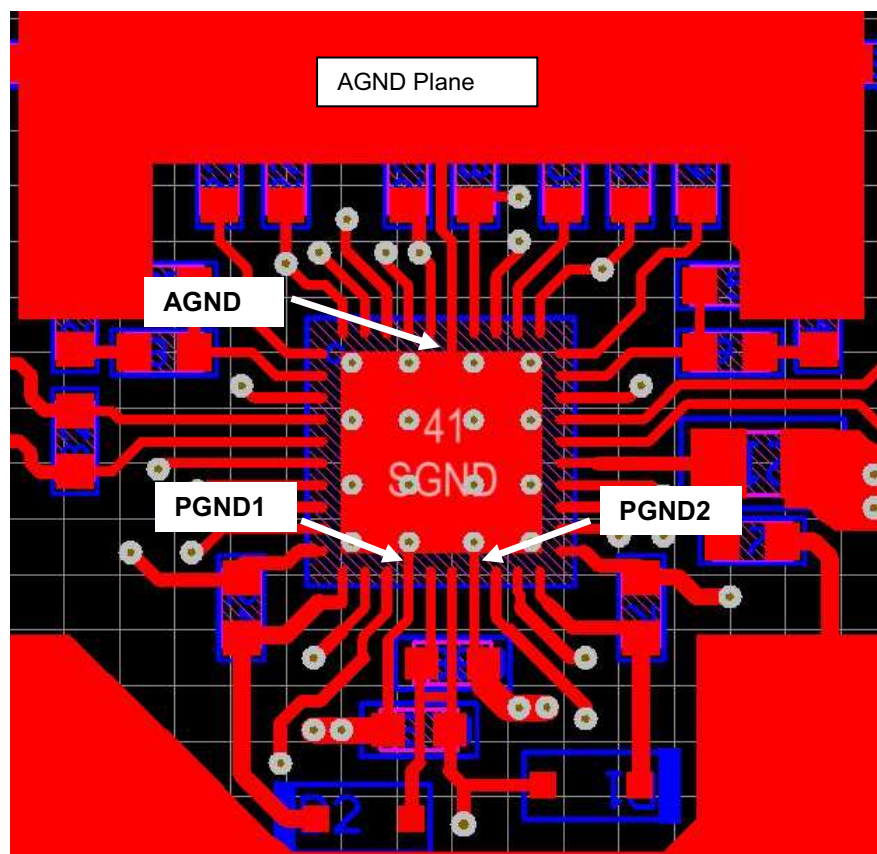


Figure 43. AGND and PGND Connections

Layout Example (continued)

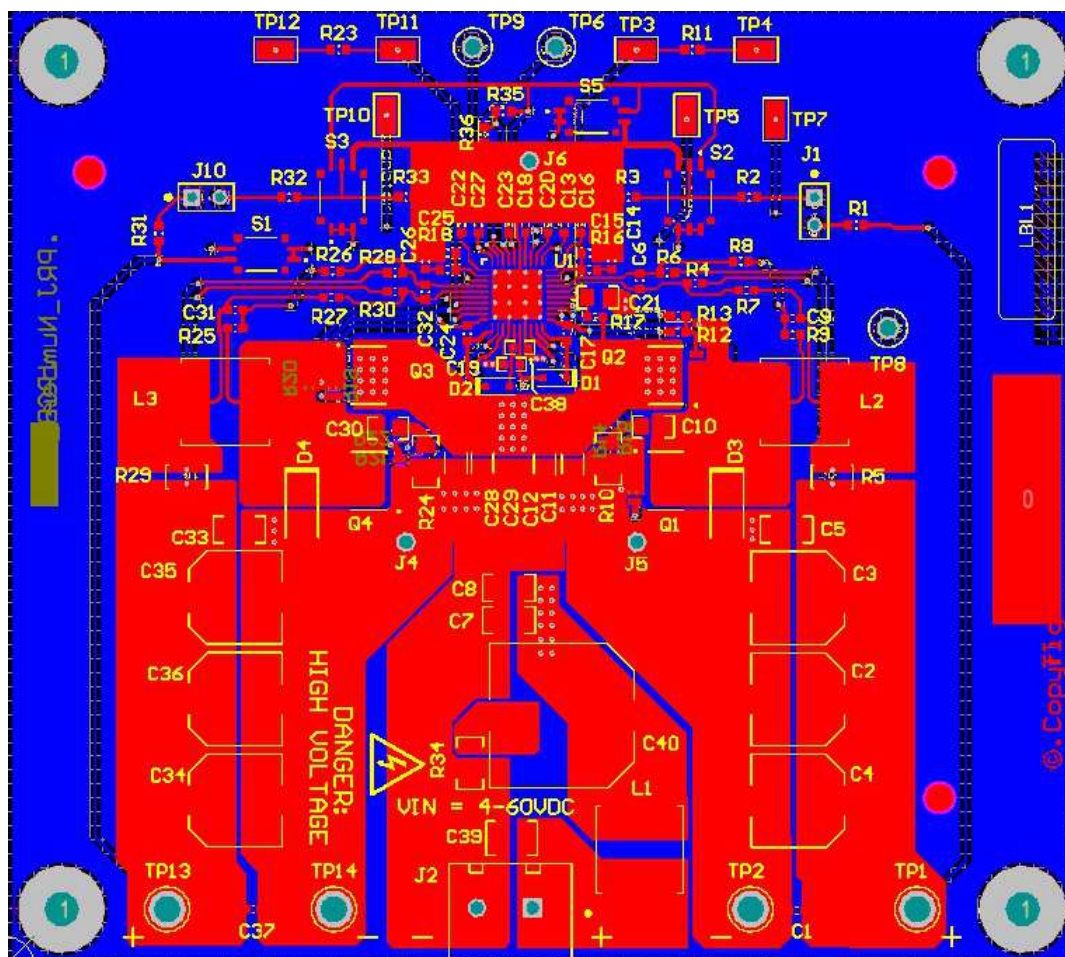


Figure 44. Top/Bottom PWM Layers

12 器件和文档支持

12.1 器件支持

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5140QRWGRQ1	Active	Production	VQFNP (RWG) 40	2500 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 150	LM5140 RWGQ1
LM5140QRWGRQ1.A	Active	Production	VQFNP (RWG) 40	2500 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 150	LM5140 RWGQ1
LM5140QRWGTQ1	Active	Production	VQFNP (RWG) 40	250 SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 150	LM5140 RWGQ1
LM5140QRWGTQ1.A	Active	Production	VQFNP (RWG) 40	250 SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 150	LM5140 RWGQ1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

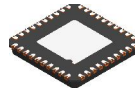
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

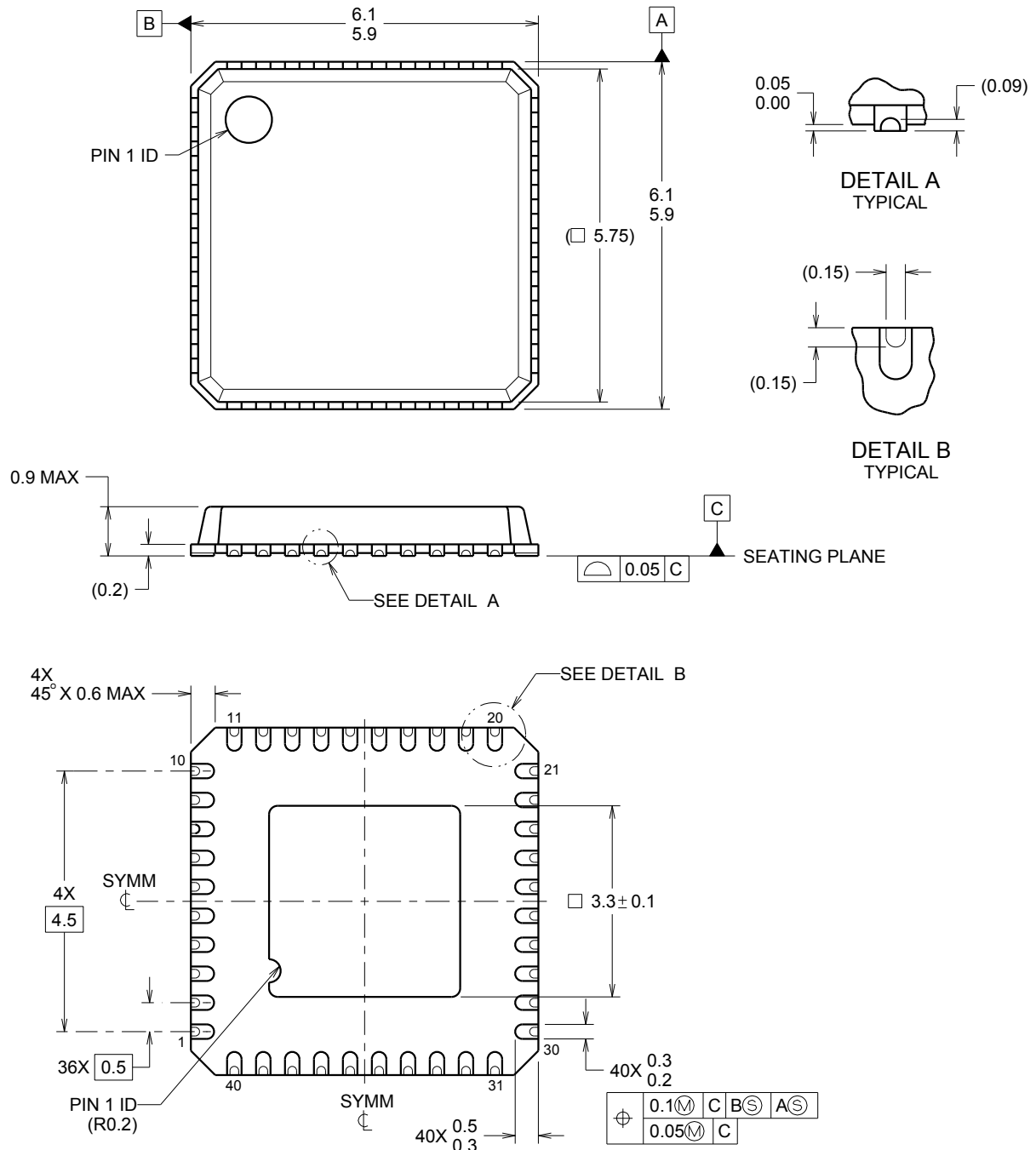
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RWG0040A**PACKAGE OUTLINE****VQFN - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4221568/A 07/2014

NOTES:

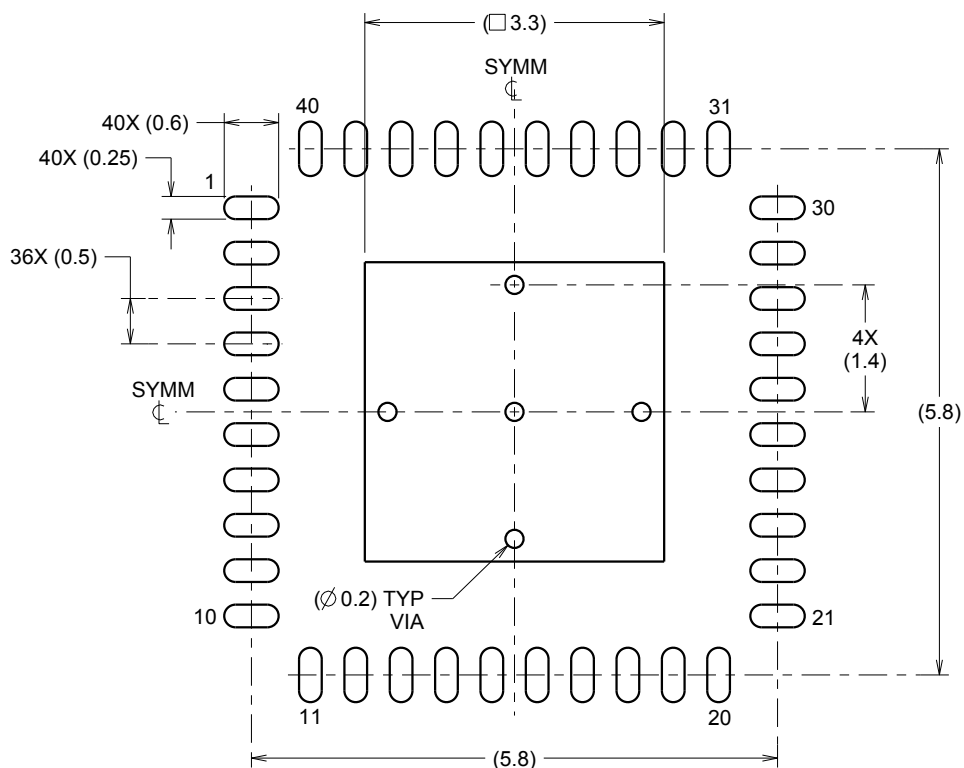
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

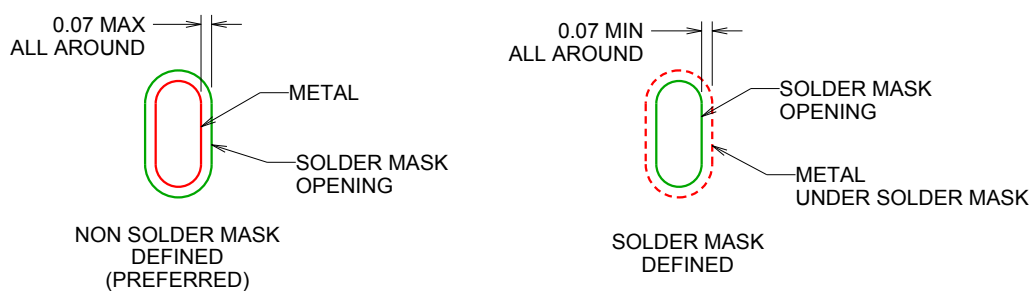
RWG0040A

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

4221568/A 07/2014

NOTES: (continued)

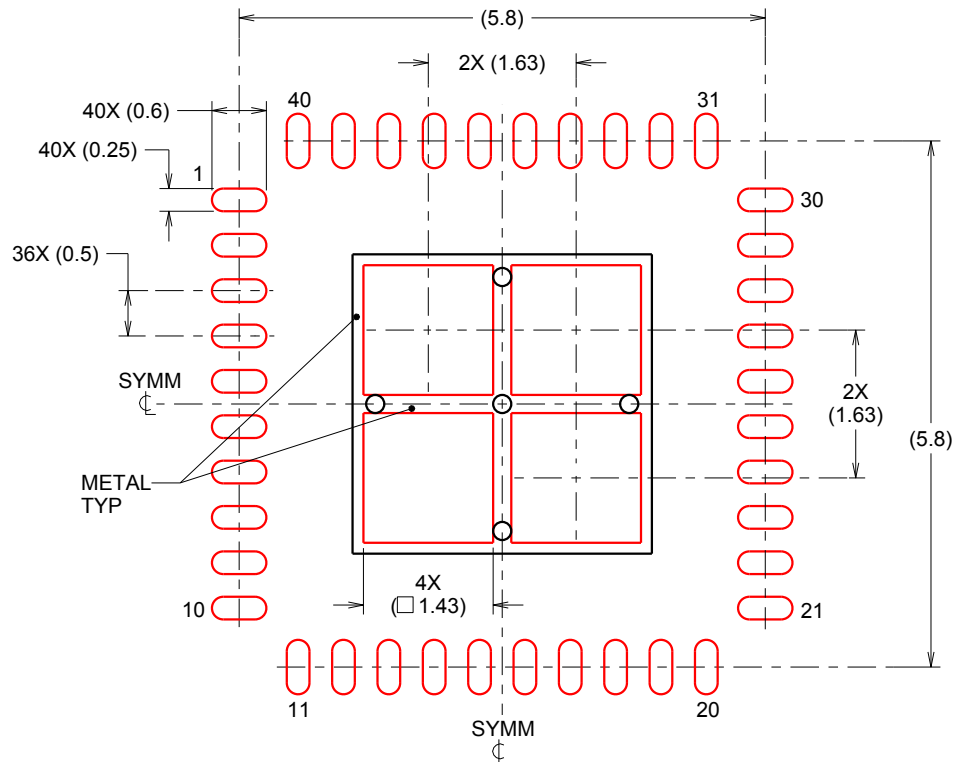
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RWG0040A

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

4221568/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司