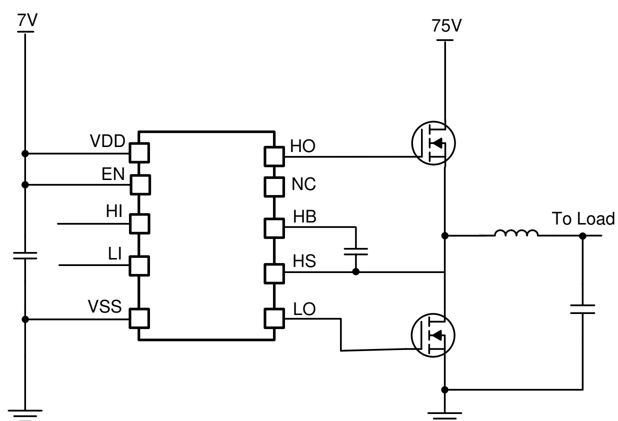
# LM5108 稳健、紧凑型 100V 半桥栅极驱动器

## 1 特性

- 可驱动两个采用高侧/低侧配置的 N 沟道 MOSFET
- 采用 3mm × 3mm 封装
- 互锁或跨导保护
- 启用/禁用功能
- HS 引脚上接受的绝对最大负电压 (–7V)
- 5V 典型欠压锁定
- 20ns 典型传播延迟
- 1000pF 负载时的上升时间为 11ns，下降时间典型值为 8ns
- 1ns 典型延迟匹配
- 2.6A 灌电流，1.6A 拉电流输出
- 绝对最大启动电压为 110V
- 禁用时消耗的电流很低 (7μA)
- 集成式自举二极管

## 2 应用

- 电机驱动器和电动工具
- 开关模式电源
- 辅助逆变器




简化版应用示意图

## 3 说明

LM5108 是一款高频半桥栅极驱动器，最大开关节点 (HS) 额定电压为 100V。借助此器件，可在基于半桥配置的拓扑（例如同步降压、全桥、有源钳位正激式、LLC 和同步升压）中控制两个 N 沟道 MOSFET。

此器件具有互锁功能，可以在两个输入都处于高电平时防止两个输出同时处于高电平。该互锁功能可提高电机驱动器和电动工具应用中的系统稳健性。使用启用和禁用功能，可以灵活、快速地控制功率级。电池供电的工具也可以使用 LM5108 的功能来减小待机电流和响应系统故障。输入与电源电压无关，并且可以具有独立的脉宽。这样即可实现极高的控制灵活性。输入和使能都具有足够的迟滞，可以在电机驱动器等易受噪声影响的应用中提高系统稳健性。

低侧和高侧输出在彼此的接通和关断之间实现了低至 1ns 的匹配。这样即可优化死区时间，进而提高效率。5V UVLO 允许驱动器使用更低的偏置电源运行，进而允许功率级以更高的开关频率运行且不会增加开关损耗。VDD 和 HB UVLO 阈值规格设计为使高侧和低侧驱动器通常在 5V 电压时接通。如果 VDD 和 HB UVLO 阈值相同，则设计器需要高于 VDD UVLO 阈值的偏置电源才能同时接通高侧和低侧驱动器。

板载自举二极管无需使用外部分立式二极管，因此提高了布板空间利用率。小型封装支持紧凑型电源设计，例如电动工具。

器件信息

| 器件型号 | 封装[(1)] | 封装尺寸（标称值） |
|---|---|---|
| LM5108 | SON (10) | 3.00mm × 3.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| **Changes from Revision * (May 2019) to Revision A (July 2023)** | **Page** |
|---|---|
| • Added transient (<100ns) for LO, HO, and HS in Absolute Maximum Ratings | 4 |


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# 5 Pin Configuration and Functions

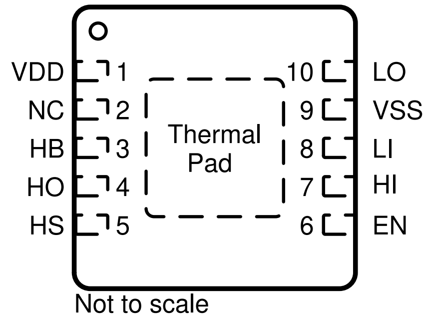


图 5-1. DRC Package 10-Pin VSON With Exposed Thermal Pad Top View

表 5-1. Pin Functions

| PIN | | I/O[(1)] | DESCRIPTION |
|---|---|---|---|
| NAME | DRC | | |
| EN | 6 | I | Enable input. When this pin is pulled high, it will enable the driver. If left floating or pulled low, it will disable the driver. 1 nF filter capacitor is recommended for high-noise systems. |
| HB | 3 | P | High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical recommended value of HB bypass capacitor is 0.1 µF, This value primarily depends on the gate charge of the high-side MOSFET. When using external boot diode, connect cathode of the diode to this pin. |
| HI | 7 | I | High-side input. |
| HO | 4 | O | High-side output. Connect to the gate of the high-side power MOSFET or one end of external gate resistor, when used. |
| HS | 5 | P | High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin. |
| LI | 8 | I | Low-side input |
| LO | 10 | O | Low-side output. Connect to the gate of the low-side power MOSFET or one end of external gate resistor, when used. |
| NC | 2 | — | Not connected internally. |
| VDD | 1 | P | Positive supply to the low-side gate driver. Decouple this pin to VSS. Typical decoupling capacitor value is 1 µF. When using an external boot diode, connect the anode to this pin. |
| VSS | 9 | G | Negative supply terminal for the device which is generally the system ground. |
| Thermal pad | | — | Connect to a large thermal mass trace (generally IC ground plane) to improve thermal performance. This can only be electrically connected to VSS. |

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

# 6 Specifications

## 6.1 Absolute Maximum Ratings

All voltages are with respect to $V_{ss}$ [1] [2]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | –0.3 | 20 | V |
| $V_{EN}$, $V_{HI}$, $V_{LI}$ | Input voltages on EN, HI and LI | | –0.3 | 20 | V |
| $V_{LO}$ | Output voltage on LO | DC | –0.3 | $V_{DD}$ + 0.3 | V |
| | | Pulses < 100ns[3] | –2 | $V_{DD}$ + 0.3 | |
| $V_{HO}$ | Output voltage on HO | DC | $V_{HS}$ – 0.3 | $V_{HB}$ + 0.3 | V |
| | | Pulses < 100ns[3] | $V_{HS}$ – 2 | $V_{HB}$ + 0.3 | |
| $V_{HS}$ | Voltage on HS | DC | –5 | 105 | V |
| | | Pulses < 100ns[3] | –7 | 105 | |
| $V_{HB}$ | Voltage on HB | | –0.3 | 110 | V |
| $V_{HB-HS}$ | Voltage on HB with respect to HS | | –0.3 | 20 | V |
| $T_J$ | Operating junction temperature | | –40 | 150 | °C |
| | Lead temperature (soldering, 10 sec.) | | | 300 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to $V_{ss}$. Currents are positive into, negative out of the specified terminal.
(3) Values are verified by characterization only.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] [3] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Pins HS, HB and HO are rated at 500V HBM

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 5.5 | 12 | 16 | V |
| $V_{EN}$, $V_{HI}$, $V_{LI}$ | Input Voltage | 0 | | $V_{DD}$ | V |
| $V_{LO}$ | Low side output voltage | 0 | | $V_{DD}$ | V |
| $V_{HO}$ | High side output voltage | $V_{HS}$ | | $V_{HB}$ | V |
| $V_{HS}$ | Voltage on HS[1] | –1 | | 100 | V |
| $V_{HB}$ | Voltage on HB | $V_{HS}$ + 5.5 | | $V_{HS}$+16 | V |
| $V_{sr}$ | Voltage slew rate on HS | | | 50 | V/ns |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) $V_{HB-HS}$ < 16V (Voltage on HB with respect to HS must be less than 16V)


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | LM5108 DRC 10 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 47.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 50.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 21.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 21.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 4.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 6.5 Electrical Characteristics

$V_{DD} = V_{HB} = V_{EN}$ =12 V, $V_{HS} = V_{SS}$ = 0 V, No load on LO or HO, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{DD}$ | VDD quiescent current | $V_{LI} = V_{HI} = 0$ | | 0.28 | 0.29 | mA |
| $I_{DDO}$ | VDD operating current | f = 500 kHz | | 2.3 | 2.4 | mA |
| $I_{HB}$ | HB quiescent current | $V_{LI} = V_{HI}$ = 0 V | | 0.13 | 0.14 | mA |
| $I_{HBO}$ | HB operating current | f = 500 kHz | | 2.5 | 2.8 | mA |
| $I_{LK}$ | Leakage current | $V_{HS} = V_{HB}$ = 110 V | | 2.0 | | μA |
| $I_{DD\_DIS}$ | $I_{DD}$ when driver is disabled | $V_{EN}$ = 0 | | 7.0 | | μA |
| **INPUT** | | | | | | |
| $V_{HIT}$ | Input rising threshold | | | | 2.3 | V |
| $V_{LIT}$ | Input falling threshold | | 1.0 | | | V |
| $V_{IHYS}$ | Input voltage Hysteresis | | | 0.7 | | V |
| $R_{IN}$ | Input pulldown resistance | | | 250 | | kΩ |
| **ENABLE** | | | | | | |
| $V_{EN}$ | Voltage threshold on EN pin to enable the driver | | | | 1.65 | V |
| $V_{DIS}$ | Voltage threshold on EN pin to disable the driver | | 1.0 | | | V |
| $V_{ENHYS}$ | Enable pin hysteresis | | | 0.12 | | V |
| $R_{EN}$ | EN pin internal pull-down resistor | | | 250 | | kΩ |
| **UNDERVOLTAGE LOCKOUT PROTECTION (UVLO)** | | | | | | |
| $V_{DDR}$ | VDD rising threshold | | 4.8 | 5.0 | 5.2 | V |
| $V_{DDF}$ | VDD falling threshold | | 4.3 | 4.5 | 4.8 | V |
| $V_{DDHYS}$ | VDD threshold hysteresis | | | 0.5 | | V |
| $V_{HBR}$ | HB rising threshold with respect to HS pin | | 3.4 | 3.7 | 4.1 | V |
| $V_{HBF}$ | HB falling threshold with respect to HS pin | | 3.1 | 3.4 | 3.8 | V |
| $V_{HBHYS}$ | HB threshold hysteresis | | | 0.3 | | V |
| **BOOTSTRAP DIODE** | | | | | | |
| $V_F$ | Low-current forward voltage | $I_{VDD-HB}$ = 100 μA | | 0.55 | | V |
| $V_{FI}$ | High-current forward voltage | $I_{VDD-HB}$ = 80 mA | | 0.9 | | V |
| $R_D$ | Dynamic resistance, $\Delta V_F/\Delta I$ | $I_{VDD-HB}$ = 100 mA and 80 mA | | 2.0 | | Ω |

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## 6.5 Electrical Characteristics (continued)

$V_{DD}$ = $V_{HB}$ = $V_{EN}$ =12 V, $V_{HS}$ = $V_{SS}$ = 0 V, No load on LO or HO, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LO GATE DRIVER** | | | | | | |
| $V_{LOL}$ | Low level output voltage | $I_{LO}$ = 100 mA | | 0.13 | | V |
| $V_{LOH}$ | High level output voltage | $I_{LO}$ = -100 mA, $V_{LOH}$ = $V_{DD}$ – $V_{LO}$ | | 0.4 | | V |
| | Peak pullup current | $V_{LO}$ = 0 V | | 1.6 | | A |
| | Peak pulldown current | $V_{LO}$ = 12 V | | 2.6 | | A |
| **HO GATE DRIVER** | | | | | | |
| $V_{HOL}$ | Low level output voltage | $I_{HO}$ = 100 mA | | 0.13 | | V |
| $V_{HOH}$ | High level output voltage | $I_{HO}$ = – 100 mA, $V_{HOH}$ = $V_{HB}$- $V_{HO}$ | | 0.4 | | |
| | Peak pullup current | $V_{HO}$ = 0 V | | 1.6 | | A |
| | Peak pulldown current | $V_{HO}$ = 12 V | | 2.6 | | A |

## 6.6 Switching Characteristics

$V_{DD}$ = $V_{HB}$ = $V_{EN}$ = 12 V, $V_{HS}$ = $V_{SS}$ = 0 V, No load on LO or HO, $T_A$ = 25°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PROPAGATION DELAYS** | | | | | | |
| $t_{DLFF}$ | $V_{LI}$ falling to $V_{LO}$ falling | See 图 6-1 | | 20 | | ns |
| $t_{DHFF}$ | $V_{HI}$ falling to $V_{HO}$ falling | See 图 6-1 | | 20 | | ns |
| $t_{DLRR}$ | $V_{LI}$ rising to $V_{LO}$ rising | See 图 6-1 | | 20 | | ns |
| $t_{DHRR}$ | $V_{HI}$ rising to $V_{HO}$ rising | See 图 6-1 | | 20 | | ns |
| **DELAY MATCHING** | | | | | | |
| $t_{MON}$ | From LO being ON to HO being OFF | See 图 6-1 | | 1 | 5 | ns |
| $t_{MOFF}$ | From LO being OFF to HO being ON | See 图 6-1 | | 1 | 5 | ns |
| **OUTPUT RISE AND FALL TIME** | | | | | | |
| $t_R$ | LO, HO rise time | $C_{LOAD}$ = 1000 pF | | 11 | | ns |
| $t_F$ | LO, HO fall time | $C_{LOAD}$ = 1000 pF | | 8 | | ns |
| **MISCELLANEOUS** | | | | | | |
| $T_{PW,min}$ | Minimum input pulse width that changes the output | | | | 40 | ns |
| | Bootstrap diode turnoff time | $I_F$ = 20 mA, $I_{REV}$ = 0.5 A | | 20 | | ns |


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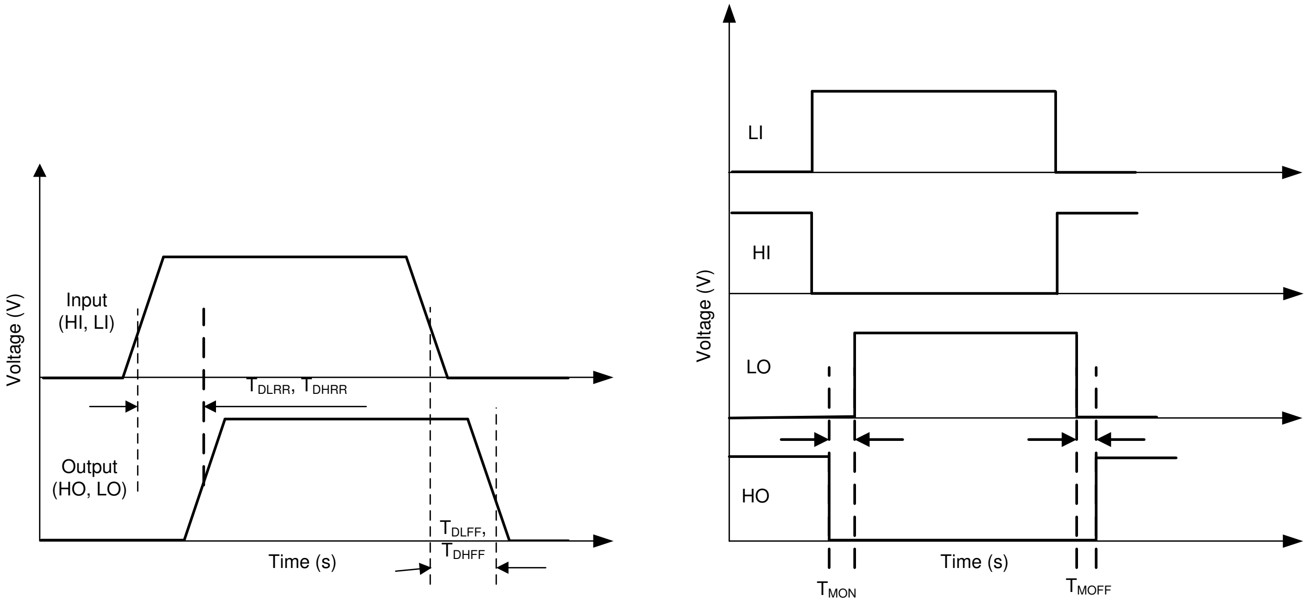
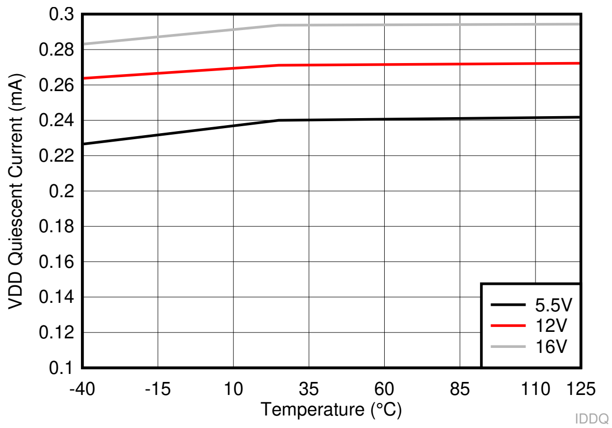



**图 6-1. Timing Diagram**

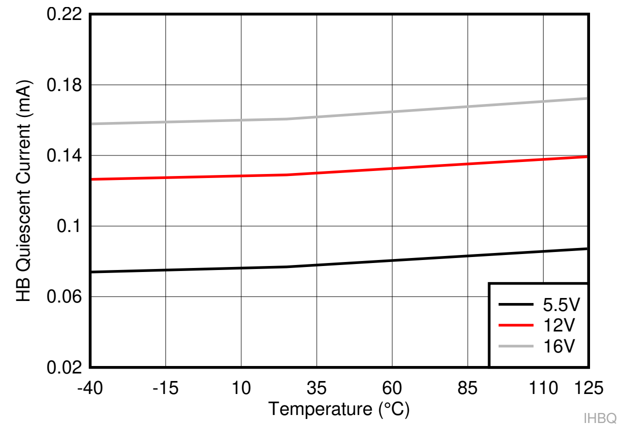
## 6.7 Typical Characteristics

Unless otherwise specified $V_{VDD}$=$V_{HB}$ = 12 V, $V_{HS}$=$V_{VSS}$ = 0 V, No load on outputs



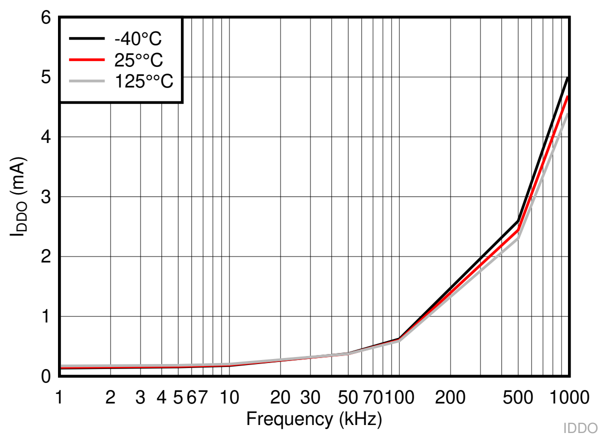

$V_{HI}$ = $V_{LI}$ = 0 V

**图 6-2. VDD Quiescent Current**



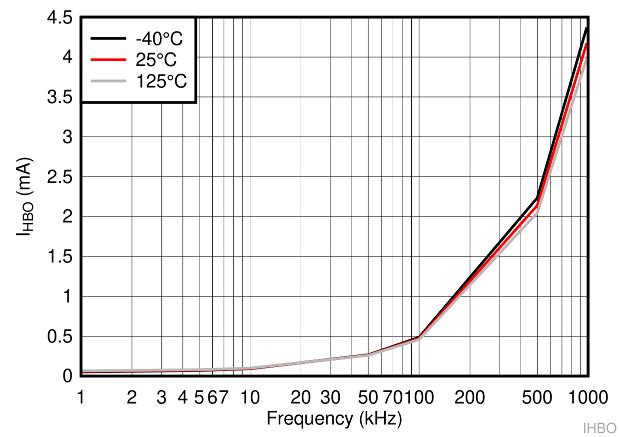

$V_{HI}$ = $V_{LI}$ = 0 V

**图 6-3. HB Quiescent Current**



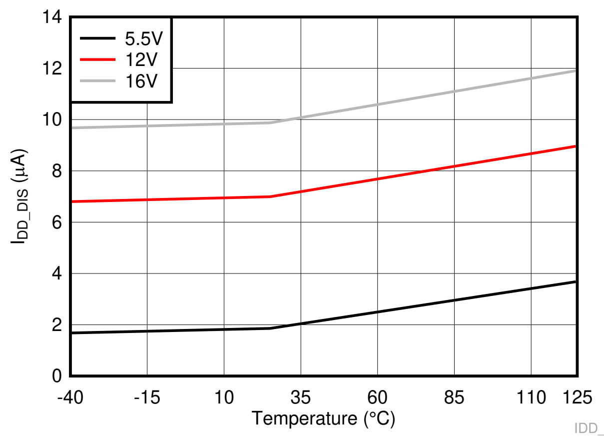

$C_L$ = 0 F $V_{DD}$ =$V_{HB}$= 12V

**图 6-4. VDD Operating Current**




$C_L$ = 0 F $V_{DD}$ =$V_{HB}$= 12V

**图 6-5. HB Operating Current**




$C_L$ = 0 F $V_{EN}$ = 0 V

**图 6-6. VDD Current When Disabled**

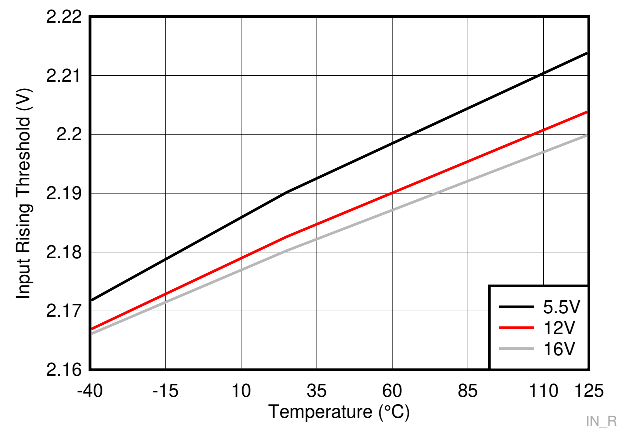



**图 6-7. Input Rising Threshold**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## 6.7 Typical Characteristics (continued)

Unless otherwise specified $V_{VDD}$=$V_{HB}$ = 12 V, $V_{HS}$=$V_{VSS}$ = 0 V, No load on outputs

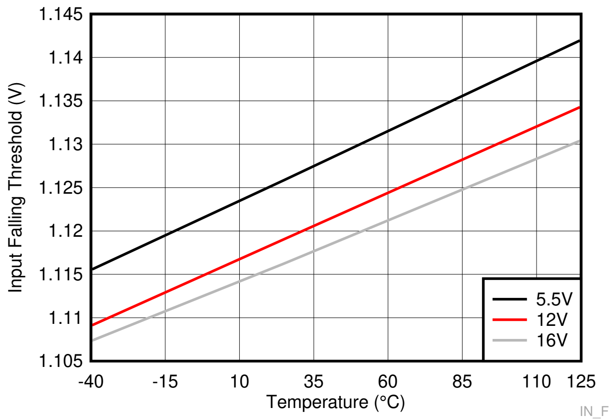


**图 6-8. Input Falling Threshold**

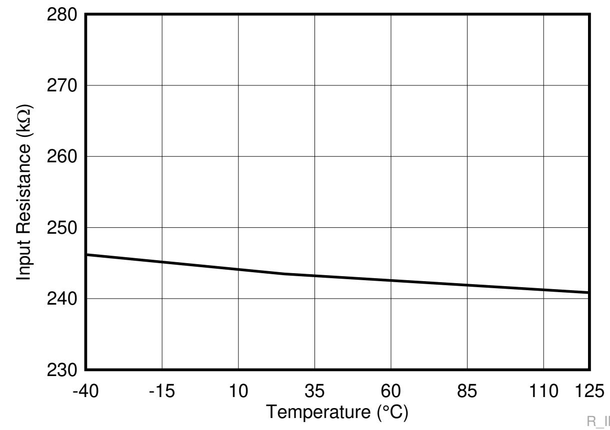


**图 6-9. Input Pull-down Resistor**

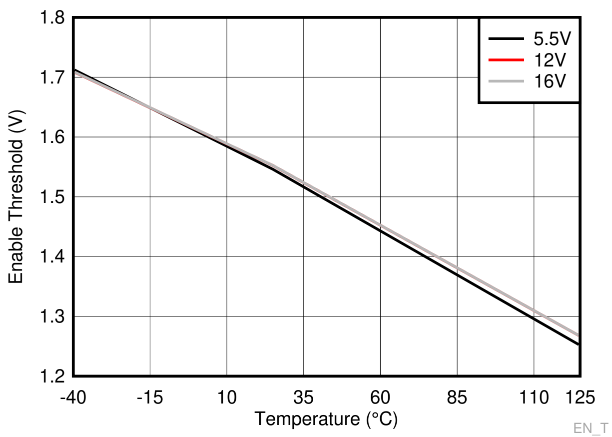


**图 6-10. Enable Threshold**

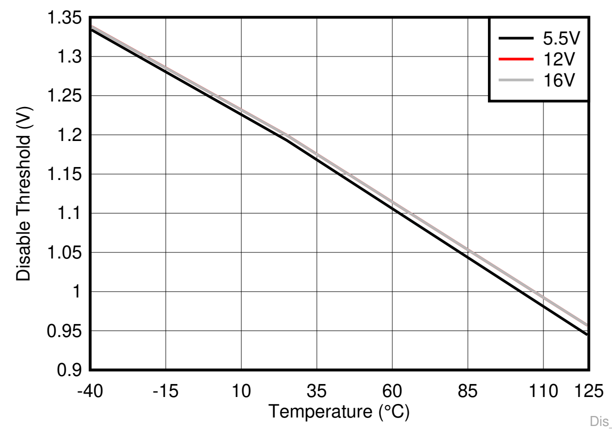


**图 6-11. Disable Threshold**

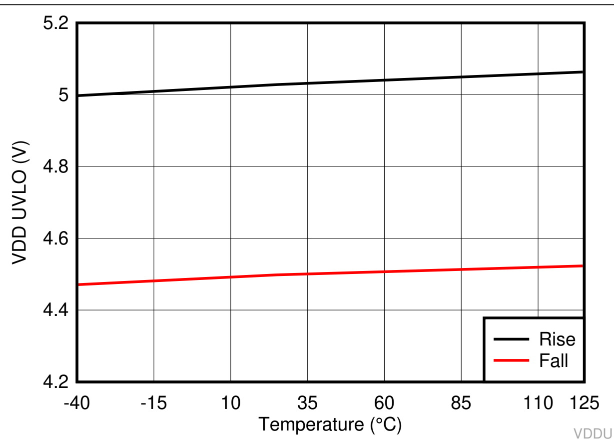


**图 6-12. VDD UVLO Threshold**

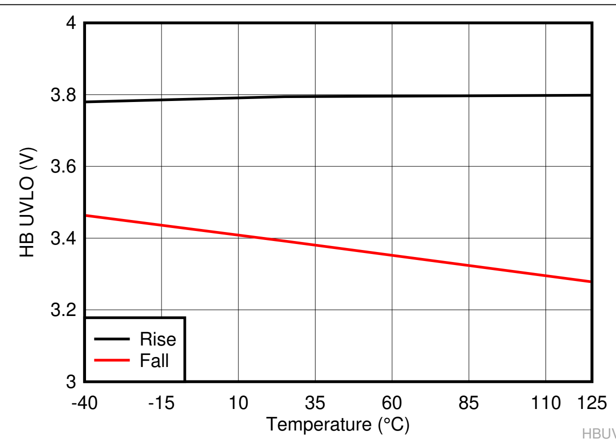


**图 6-13. HB UVLO Threshold**

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## 6.7 Typical Characteristics (continued)

Unless otherwise specified $V_{VDD}$=$V_{HB}$ = 12 V, $V_{HS}$=$V_{VSS}$ = 0 V, No load on outputs

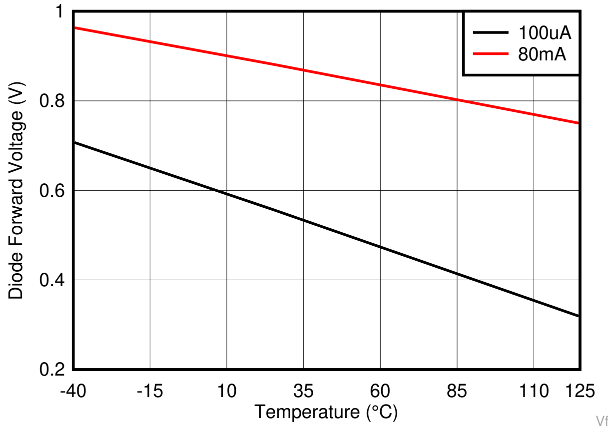



**图 6-14. Boot Diode Forward Voltage Drop**

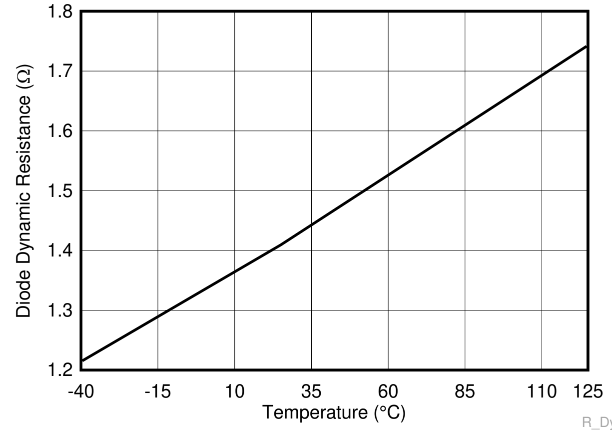
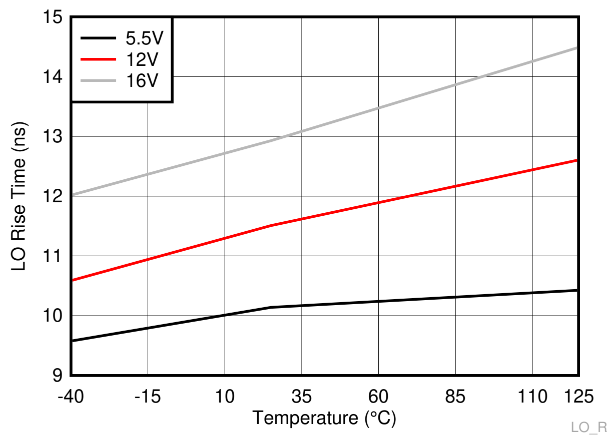
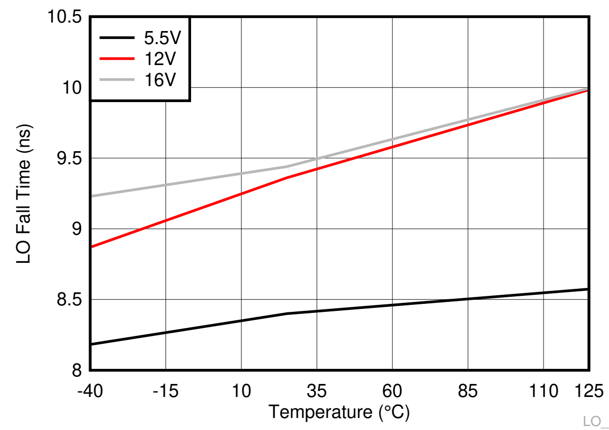



**图 6-15. Boot Diode Dynamic Resistance**



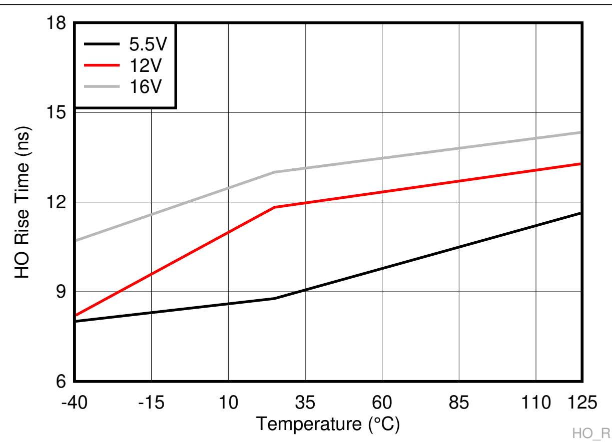

$C_L$=1000pF

**图 6-16. LO Rise Time**



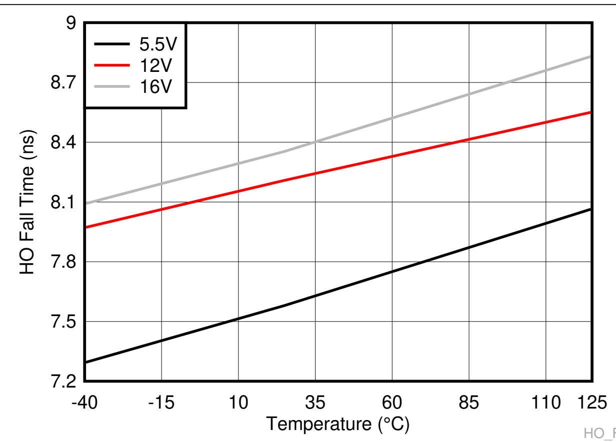

$C_L$=1000pF

**图 6-17. LO Fall Time**




$C_L$=1000pF

**图 6-18. HO Rise Time**




$C_L$=1000pF

**图 6-19. HO Fall Time**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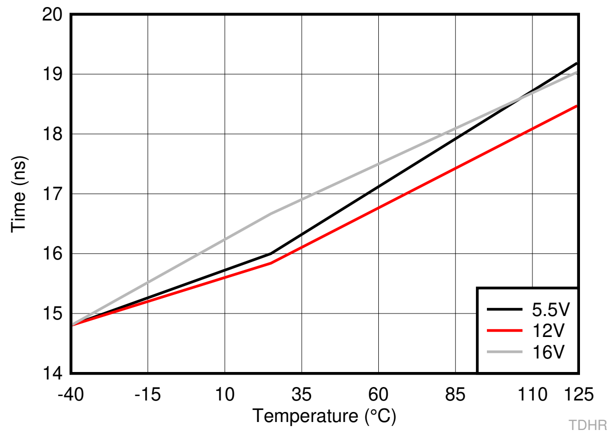
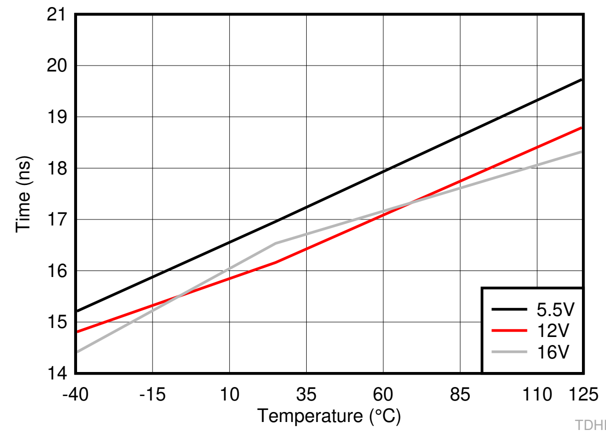
## 6.7 Typical Characteristics (continued)

Unless otherwise specified $V_{VDD}$=$V_{HB}$ = 12 V, $V_{HS}$=$V_{VSS}$ = 0 V, No load on outputs



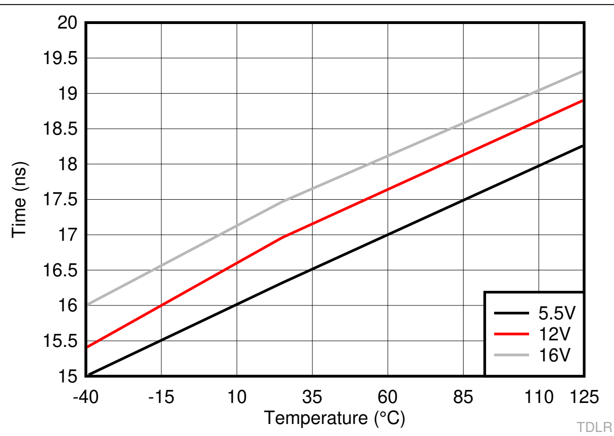

$C_L$=No Load

**图 6-20. HO Rising Propagation Delay (TDHRR)**



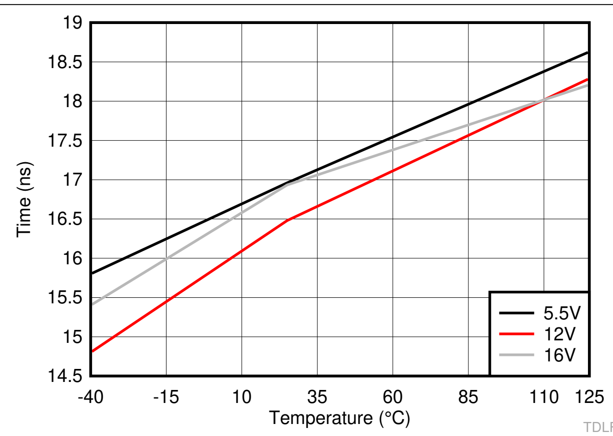

$C_L$= No Load

**图 6-21. HO Falling Propagation Delay (TDHFF)**




$C_L$= No Load

**图 6-22. LO Rising Propagation Delay (TDLRR)**




$C_L$= No Load

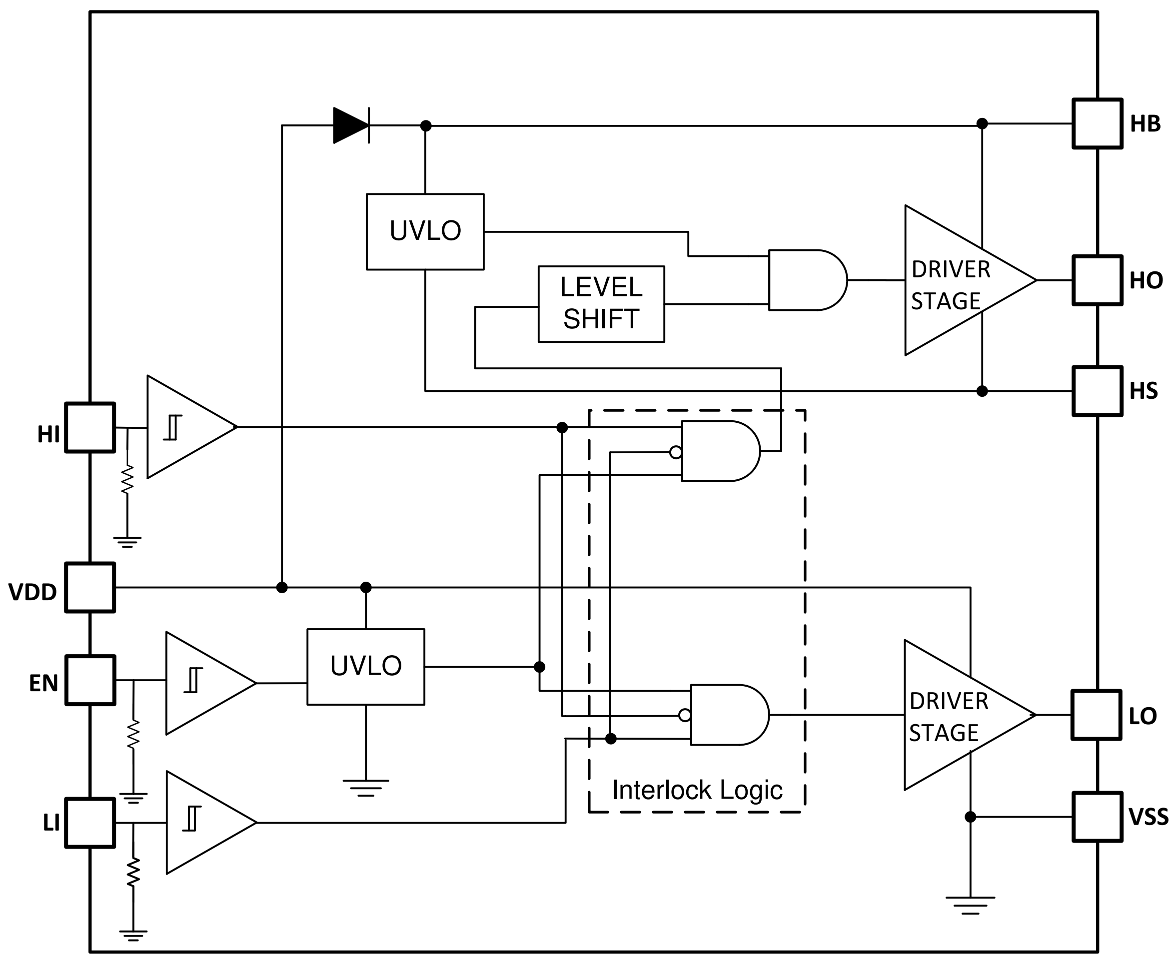
**图 6-23. LO Falling Propagation Delay (TDLFF)**

# 7 Detailed Description

## 7.1 Overview

The LM5108 is a high-voltage gate driver designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configurations. The two outputs are independently controlled with two TTL-compatible input signals. The device can also work with CMOS type control signals at its inputs as long as signals meet turn-on and turn-off threshold specifications of the LM5108. The floating high-side driver is capable of working with HS voltage up to 100 V with respect to VSS. A 100 V bootstrap diode is integrated in the LM5108 device to charge high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and provides clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails. EN pin is provided (in DRC packaged parts) to enable or disable the driver. The driver also has input interlock functionality, which shuts off both the outputs when the two inputs overlap.

## 7.2 Functional Block Diagram

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## 7.3 Feature Description

### 7.3.1 Enable

The device in DRC package has an enable (EN) pin. The outputs will be active only if the EN pin voltage is above the threshold voltage. Outputs will be held low if EN pin is left floating or pulled-down to ground. An internal 250 kΩ resistor connects EN pin to VSS pin. Thus, leaving the EN pin floating disables the device. Externally pulling EN pin to ground shall also disable the device. If the EN pin is not used, then it is recommended to connect it to VDD pin. If a pull-up resistor needs to be used then a strong pull-up resistor is recommended. For 12V supply voltage, a 10kΩ pull-up is suggested. In noise prone application, a small filter capacitor, 1nF, should be connected from the EN pin to VSS pin as close to the device as possible. An analog or a digital controller output pin could be connected to EN pin to enable or disable the device. Built-in hysteresis helps prevent any nuisance tripping or chattering of the outputs.

### 7.3.2 Start-up and UVLO

Both the high-side and the low-side driver stages include UVLO protection circuitry which monitors the supply voltage ($V_{DD}$) and the bootstrap capacitor voltage ($V_{HB-HS}$). The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs. The built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the device, both the outputs are held low until VDD exceeds the UVLO threshold, typically 5 V. Any UVLO condition on the bootstrap capacitor ($V_{HB-HS}$) disables only the high- side output (HO).

**表 7-1. VDD UVLO Logic Operation**

| CONDITION ($V_{HB-HS} > V_{HBR}$ and $V_{EN}$ > Enable Threshold) | HI | LI | HO | LO |
|---|---|---|---|---|
| $V_{DD}$-$V_{SS} < V_{DDR}$ during device start-up | H | L | L | L |
| | L | H | L | L |
| | H | H | L | L |
| | L | L | L | L |
| $V_{DD}$-$V_{SS} < V_{DDR} - V_{DDH}$ after device start-up | H | L | L | L |
| | L | H | L | L |
| | H | H | L | L |
| | L | L | L | L |

**表 7-2. HB UVLO Logic Operation**

| CONDITION ($V_{DD} > V_{DDR}$ and $V_{EN}$ > Enable Threshold) | HI | LI | HO | LO |
|---|---|---|---|---|
| $V_{HB-HS} < V_{HBR}$ during device start-up | H | L | L | L |
| | L | H | L | H |
| | H | H | L | L |
| | L | L | L | L |
| $V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up | H | L | L | L |
| | L | H | L | H |
| | H | H | L | L |
| | L | L | L | L |

### 7.3.3 Input Stages and Interlock Protection

The two inputs operate independently, with an exception that both outputs will be pulled low when both inputs are high or overlap. The independence allows for full control of two outputs compared to the gate drivers that have a single input. The device has input interlock or cross-conduction protection. Whenever both the inputs are high, the internal logic turns both the outputs off. Once the device is in shoot-through mode, when one of the inputs goes low, the outputs follow the input logic. There is no other fixed time de-glitch filter implemented in the device and therefore propagation delay and delay matching are not sacrificed. In other words, there is no built-in dead-time due to the interlock feature. Any noise on the input that could cause the output to shoot-through will be filtered by this feature and the system stays protected. Because the inputs are independent of supply voltage, they can be connected to outputs of either digital controller or analog controller. Small filter at the inputs of the driver further improves system robustness in noise prone applications. The inputs have internal pull down resistors with typical value of 250 kΩ. Thus, when the inputs are floating, the outputs are held low.

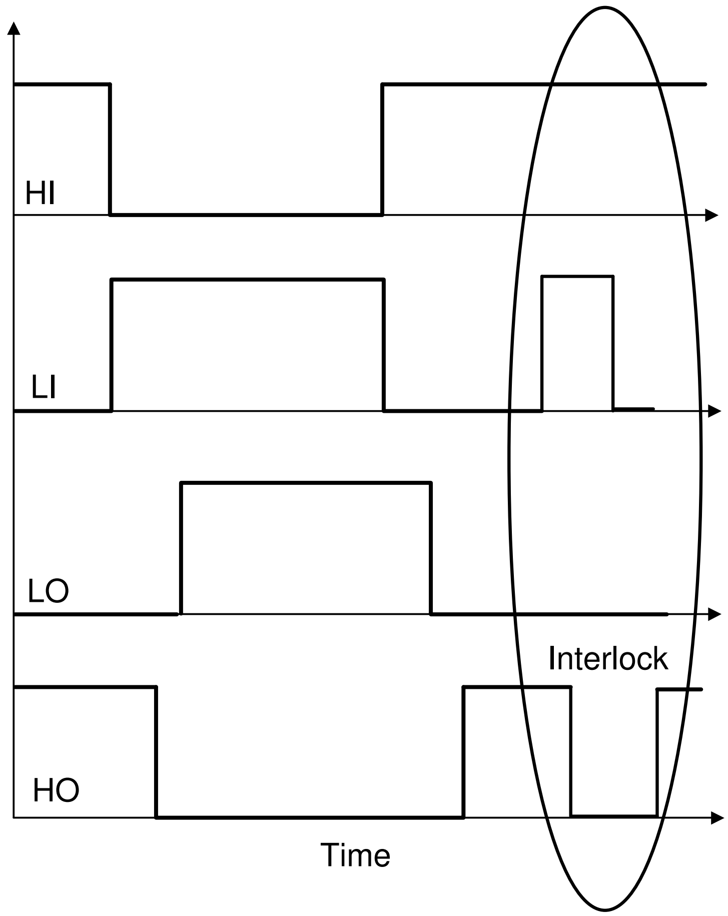


**图 7-1. Interlock or Input Shoot-through Protection**

### 7.3.4 Level Shifter

The level shift circuit is the interface from the high-side input, which is a VSS referenced signal, to the high-side driver stage which is referenced to the switch node (HS pin). The level shift allows control of the HO output which is referenced to the HS pin. The delay introduced by the level shifter is kept as low as possible and therefore the device provides excellent propagation delay characteristic and delay matching with the low-side driver output. Low delay matching allows power stages to operate with less dead time. The reduction in dead-time is very important in applications where high efficiency is required.

### 7.3.5 Output Stage

The output stages are the interface from level shifter output to the power MOSFETs in the power train. High slew rate, low resistance, and moderate peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to VSS and the high-side is referenced to HS. The device output stages are robust to handle harsh environment. The device output stages feature a pull-up structure which delivers the peak current when it is most needed, during the Miller plateau region of the power switch turn on transition. The output pull-up and pull-down structure of the device is totem pole NMOS-PMOS structure.


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### 7.3.6 Negative Voltage Transients

In most applications, the body diode of the external low-side power MOSFET clamps the HS node to ground. In some situations, board capacitances and inductances can cause the HS node to transiently swing several volts below ground, before the body diode of the external low-side MOSFET clamps this swing. When used in conjunction with the LM5108, the HS node can swing below ground as long as specifications are not violated and conditions mentioned in this section are followed.

HS must always be at a lower potential than HO. Pulling HO more negative than specified conditions can activate parasitic transistors which may result in excessive current flow from the HB supply. This may result in damage to the device. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and VSS to protect the device from this type of transient. The diode must be placed as close to the device pins as possible in order to be effective.

Ensure that the HB to HS operating voltage is 16 V or less. Hence, if the HS pin transient voltage is –5 V, then VDD (and thus HB) is ideally limited to 11 V to keep the HB to HS voltage below 16 V. Generally when HS swings negative, HB follows HS instantaneously and therefore the HB to HS voltage does not significantly overshoot.

Low ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation of the gate driver device. The capacitor should be located at the leads of the device to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor causes voltage ringing at the leads of the device which must be avoided for reliable operation.

## 7.4 Device Functional Modes

When the device is enabled, the device operates in normal mode and UVLO mode. See 节 7.3.2 for more information on UVLO operation mode. In normal mode when the $V_{DD}$ and $V_{HB-HS}$ are above UVLO threshold, the output stage is dependent on the states of the EN, HI and LI pins. The output HO and LO will be low if input state is floating.

**表 7-3. Input/Output Logic in Normal Mode of Operation**

| EN | HI | LI | HO (1) | LO (2) |
|---|---|---|---|---|
| L | H | H | L | L |
| | L | H | L | L |
| | H | L | L | L |
| | L | L | L | L |
| H | H | H | L | L |
| | L | H | L | H |
| | H | L | H | L |
| | L | L | L | L |
| H | Floating | L | L | L |
| | Floating | H | L | H |
| | L | Floating | L | L |
| | H | Floating | H | L |
| Floating | Floating | Floating | L | L |

(1) HO is measured with respect to HS
(2) LO is measured with respect to VSS

# 8 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 8.1 Application Information

Most electronic devices and applications are becoming more and more power hungry. These applications are also reducing in overall size. One way to achieve both high power and low size is to improve the efficiency and distribute the power loss optimally. Most of these applications employ power MOSFETs and they are being switched at higher and higher frequencies. To operate power MOSFETs at high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the power semiconductor devices, such as power MOSFETs, IGBTs, SiC FETs, and GaN FETs. Many of these applications require proper UVLO protection so that power semiconductor devices are turned ON and OFF optimally. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V or 5 V) in order to fully turn-on the power device, minimize conduction losses, and minimize the switching losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability and under voltage lockout protection. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also solve other problems such as minimizing the effect of high-frequency switching noise (by placing the high-current driver device physically close to the power switch), driving gate-drive transformers and controlling floating power device gates. This helps reduce power dissipation and thermal stress in controllers by moving gate charge power losses from the controller IC to the gate driver.

LM5108 gate drivers offer high voltage (100 V), small delays (20 ns), and good driving capability (1.6 A/2.6 A) in a single device. The floating high-side driver is capable of operating with switch node voltages up to 100 V. This allows for N-channel MOSFETs control in half-bridge, full-bridge, synchronous buck, synchronous boost, and active clamp topologies. LM5108 gate driver IC also has built-in bootstrap diode to help power supply designers optimize PWB area and to help reduce bill of material cost in most applications. The driver has an enable/disable functionality to be used in applications where driver needs to be enabled or disabled based on fault condition in other parts of the circuit. Interlock functionality of the device is very useful in applications where overall reliability of the system is of utmost criteria and redundant protection is desired. Each channel is controlled by its respective input pins (HI and LI), allowing flexibility to control ON and OFF state of the output. Both the outputs are forced OFF when the two inputs overlap.

Switching power devices such as MOSFETs have two main loss components; switching losses and conduction losses. Conduction loss is dominated by current through the device and ON resistance of the device. Switching losses are dominated by gate charge of the switching device, gate voltage of the switching device, and switching frequency. Applications where operating switching frequency is very high, the switching losses start to significantly impact overall system efficiency. In such applications, to reduce the switching losses it becomes essential to reduce the gate voltage. The gate voltage is determined by the supply voltage the gate driver ICs, therefore, the gate driver IC needs to operate at lower supply voltage in such applications. LM5108 gate driver has typical UVLO level of 5V and therefore, they are perfectly suitable for such applications. There is enough UVLO hysteresis provided to avoid any chattering or nuisance tripping which improves system robustness.


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## 8.2 Typical Application

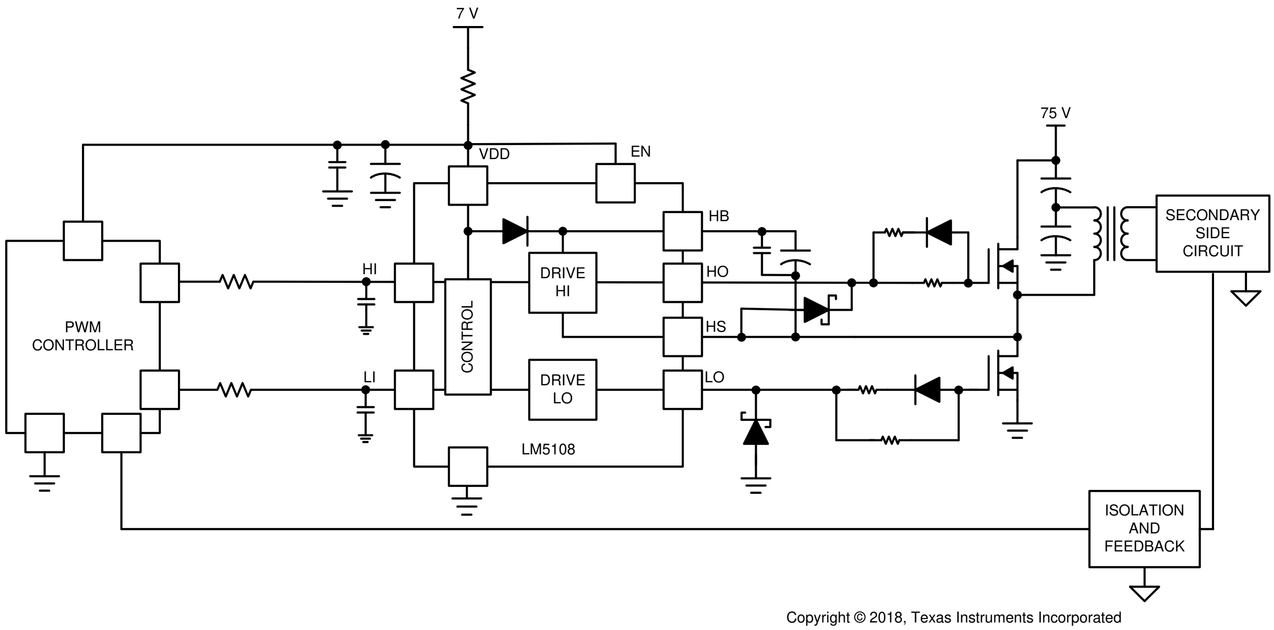


**图 8-1. Typical Application**

### 8.2.1 Design Requirements

Table below lists the system parameters. LM5108 needs to operate satisfactorily in conjunction with them.

**表 8-1. Design Requirements**

| PARAMETER | VALUE |
|---|---|
| MOSFET | CSD19535KTT |
| Maximum Bus/Input Voltage, $V_{in}$ | 75 V |
| Operating Bias Votage, $V_{DD}$ | 7 V |
| Switching Frequency, Fsw | 300 kHz |
| Total Gate Charge of FET at given VDD, $Q_G$ | 52nC |
| MOSFET Internal Gate Resistance, $R_{GFET\_Int}$ | 1.4 |
| Maximum Duty Cycle, $D_{Max}$ | 0.5 |
| Gate Driver | LM5108 |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Select Bootstrap and VDD Capacitor*

The bootstrap capacitor must maintain the $V_{HB-HS}$ voltage above the UVLO threshold for normal operation. Calculate the maximum allowable drop across the bootstrap capacitor, $\Delta V_{HB}$, with 方程式 1.

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = (7\ \mathrm{V} - 1\ \mathrm{V} - (3.7\ \mathrm{V} - 0.3\ \mathrm{V})) = 2.6\ \mathrm{V} \tag{1}$$

where

- $V_{DD}$ is the supply voltage of gate driver device
- $V_{DH}$ is the bootstrap diode forward voltage drop
- $V_{HBL}$ is the HB falling threshold ( $V_{HBR(max)}$ － $V_{HBH}$)

In this example the allowed voltage drop across bootstrap capacitor is 2.6 V.

It is generally recommended that ripple voltage on both the bootstrap capacitor and VDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value of 0.5 V.

Use 方程式 2 to estimate the total charge needed per switching cycle from bootstrap capacitor.

$$Q_{TOTAL} = Q_G + I_{LK} \times \left(\frac{D_{MAX}}{f_{SW}}\right) + \left(\frac{I_{HB}}{f_{SW}}\right) = 52\ \mathrm{nC} + 0.003\ \mathrm{nC} + 0.43\ \mathrm{nC} = 52.43\ \mathrm{nC} \tag{2}$$

where

- $Q_G$ is the total MOSFET gate charge
- $I_{LK}$ is the HB to VSS leakage current from datasheet
- $D_{Max}$ is the converter maximum duty cycle
- $I_{HB}$ is the HB quiescent current from the datasheet

The caculated total charge is 52.43 nC.

Next, use 方程式 3 to estimate the minimum bootstrap capacitor value.

$$C_{BOOT\ (min)} = \frac{Q_{TOTAL}}{\Delta V_{HB}} = \frac{52.43\ \mathrm{nC}}{2.6\ \mathrm{V}} = 20.16\ \mathrm{nF} \tag{3}$$

The calculated value of minimum bootstrap capacitor is 20.16 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100-nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the HB and HS pins as possible. Also place a small size, 0402, low value, 1000 pF, capacitor to filter high frequency noise, in parallel with main bypass capacitor.

For this application, choose a $C_{BOOT}$ capacitor that has the following specifications: 0.1 µF, 25 V, X7R


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As a general rule the local VDD bypass capacitor must be greater than the value of bootstrap capacitor value (generally 10 times the bootstrap capacitor value). For this application choose a $C_{VDD}$ capacitor with the following specifications: 1 µF , 25 V, X7R

$C_{VDD}$ capacitor is placed across VDD and VSS pin of the gate driver. Similar to bootstrap capacitors, place a small size and low value capacitor in parallel with the main bypass capacitor. For this application, choose 0402, 1000 pF, capacitance in parallel with main bypass capacitor to filter high frequency noise.

The bootstrap and bias capacitors must be ceramic types with X7R dielectric or better. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to. Choose this value because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system.

#### *8.2.2.2 Estimate Driver Power Losses*

The total power loss in gate driver device such as the LM5108 is the summation of the power loss in different functional blocks of the gate driver device. These power loss components are explained in this section.

1. 方程式 4 describes how quiescent currents ($I_{DD}$ and $I_{HB}$) affect the static power losses, $P_{QC}$.

$$P_{QC} = (V_{DD} \times I_{DD}) + (V_{DD} - V_{DH}) \times I_{HB}$$
$$= 7\ \text{V} \times 0.28\ \text{mA} + 6\ \text{V} \times 0.13\ \text{mA} = 2.74\ \text{mW} \tag{4}$$

   it is not shown here, but for better approximation, no load operating current, $I_{DDO}$ and $I_{HBO}$ can be added in above equation.

2. 方程式 5 shows how high-side to low-side leakage current ($I_{LK}$) affects level-shifter losses ($P_{ILK}$).

$$P_{ILK} = V_{HB} \times I_{LK} \times D = 82\ \text{V} \times 2\ \mu\text{A} \times 0.5 = 0.082\ \text{mW} \tag{5}$$

   where

   - D is the high-side MOSFET duty cycle
   - $V_{HB}$ is the sum of input voltage and voltage across bootstrap capacitor.

3. 方程式 6 shows how MOSFETs gate charge ($Q_G$) affects the dynamic losses, $P_{QG}$.

$$P_{QG} = 2 \times V_{DD} \times Q_G \times f_{SW} \times \frac{R_{GD\_R}}{R_{GD\_R} + R_{GATE} + R_{GFET\,(int)}}$$
$$= 2 \times 7\ \text{V} \times 52\ \text{nC} \times 300\ \text{kHz} \times 0.74 = 0.16\ \text{W} \tag{6}$$

   where

   - $Q_G$ is the total MOSFET gate charge
   - $f_{SW}$ is the switching frequency
   - $R_{GD\_R}$ is the average value of pullup and pulldown resistor
   - $R_{GATE}$ is the external gate drive resistor
   - $R_{GFET(int)}$ is the power MOSFETs internal gate resistor

Assume there is no external gate resistor in this example. For simplicity, the resistance of the pull-up MOSFET of the driver output section is considered here, which is typically 4 Ω. Substitute the application values to calculate the dynamic loss due to gate charge, which is 160 mW here.

4. 方程式 7 shows how parasitic level-shifter charge ($Q_P$) on each switching cycle affects dynamic losses, ($P_{LS}$) during high-side switching.

$$P_{LS} = V_{HB} \times Q_P \times f_{SW} \tag{7}$$

For this example and simplicity, it is assumed that value of parasitic charge $Q_P$ is 1 nC. Substituting values results in 24.6 mW as level shifter dynamic loss. This estimate is very high for level shifter dynamic losses.

The sum of all the losses is 187.42 mW as a total gate driver loss. As shown in this example, in most applications the dynamic loss due to gate charge dominates the total power loss in gate driver device. For gate drivers that include bootstrap diode, one should also estimate losses in bootstrap diode. Diode forward conduction loss is computed as product of average forward voltage drop and average forward current.

方程式 8 estimates the maximum allowable power loss of the device for a given ambient temperature.

$$P_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \tag{8}$$

where

- $P_{MAX}$ is the maximum allowed power dissipation in the gate driver device
- $T_J$ is the recommended maximum operating junction temperature
- $T_A$ is hte ambient temperature of the gate driver device
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance

To better estimate the junction temperature of the gate driver device in the application, it is recommended to first accurately measure the case temperature and then determine the power dissipation in a given application. Then use $\psi_{JT}$ to calculate junction temperature. After estimating junction temperature and measuring ambient temperature in the application, calculate $\theta_{JA(effective)}$. Then, if design parameters (such as the value of an external gate resistor or power MOSFET) change during the development of the project, use $\theta_{JA(effective)}$ to estimate how these changes affect junction temperature of the gate driver device.

The *节 6.4* table summarizes the thermal metrics for the driver package. For detailed information regarding the thermal information table, please refer to the *Semiconductor and Device Package Thermal Metrics* application report.

#### *8.2.2.3 Selecting External Gate Resistor*

In high-frequency switching power supply applications where high-current gate drivers such as the LM5108 are used, parasitic inductances, parasitic capacitances and high-current loops can cause noise and ringing on the gate of power MOSFETs. Often external gate resistors are used to damp this ringing and noise. In some applications the gate charge, which is load on gate driver device, is significantly larger than gate driver peak output current capability. In such applications external gate resistors can limit the peak output current of the gate driver. it is recommended that there should be provision of external gate resistor whenever the layout or application permits.

Use 方程式 9 to calculate the driver high-side pull-up current.

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{GATE} + R_{GFET(int)}} \tag{9}$$

where

- $I_{OHH}$ is the high-side, peak pull-up current


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- $V_{DH}$ is the bootstrap diode forward voltage drop
- $R_{HOH}$ is the gate driver internal high-side pull-up resistor. Value either directly provided in datasheet or can be calculated from test conditions ($R_{HOH}$ = $V_{HOH}/I_{HO}$)
- $R_{GATE}$ is the external gate resistance connected between driver output and power MOSFET gate
- $R_{GFET(int)}$ is the MOSFET internal gate resistance provided by MOSFET datasheet

Use 方程式 10 to calculate the driver high-side sink current.

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{GATE} + R_{GFET(int)}} \tag{10}$$

where

- $R_{HOL}$ is the gate driver internal high-side pull-down resistance

Use 方程式 11 to calculate the driver low-side source current.

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{GATE} + R_{GFET(int)}} \tag{11}$$

where

- $R_{LOH}$ is the gate driver internal low-side pull-up resistance

Use 方程式 12 to calculate the driver low-side sink current.

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{GATE} + R_{GFET(int)}} \tag{12}$$

where

- $R_{LOL}$ is the gate driver internal low-side pull-down resistance

Typical peak pull up and pull down current of the device is 1.6 A and 2.6 A respectively. These equations help reduce the peak current if needed. To establish different rise time value compared to fall time value, external gate resistor can be anti-paralleled with diode-resistor combination as shown in 图 8-1. Generally selecting an optimal value or configuration of external gate resistor is an iterative process. For additional information on selecting external gate resistor please refer to External Gate Resistor Design Guide for Gate Drivers

#### *8.2.2.4 Delays and Pulse Width*

The total delay encountered in the PWM, driver and power stage need to be considered for a number of reasons, primarily delay in current limit response. Also to be considered are differences in delays between the drivers which can lead to various concerns depending on the topology. The synchronous buck topology switching requires careful selection of dead-time between the high-side and low-side switches to avoid cross conduction as well as excessive body diode conduction.

Bridge topologies can be affected by a volt-second imbalance on the transformer if there is imbalance in the high-side and low-side pulse widths in any operating condition. The LM5108 device has typical propagation delay of 20 ns and typical delay matching of 1 ns.

Narrow input pulse width performance is an important consideration in gate driver devices, because output may not follow input signals satisfactorily when input pulse widths are very narrow. Although there may be relatively wide steady state PWM output signals from controller, very narrow pulses may be encountered under following operating conditions.

- soft-start period
- large load transients

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- short circuit conditions

These narrow pulses appear as an input signal to the gate driver device and the gate driver device need to respond properly to these narrow signals.

The LM5108 device produces reliable output pulse even when the input pulses are very narrow and bias voltages are very low. The propagation delay and delay matching do not get affected when the input pulse width is very narrow.

#### *8.2.2.5 External Bootstrap Diode*

The LM5108 incorporates the bootstrap diode necessary to generate the high-side bias for HO to work satisfactorily. The characteristics of this diode are important to achieve efficient, reliable operation. The characteristics to consider are forward voltage drop and dynamic resistance. Generally, low forward voltage drop diodes are preferred for low power loss during charging of the bootstrap capacitor. The device has a boot diode forward voltage drop rated at 0.9 V and dynamic resistance of 2 Ω for reliable charge transfer to the bootstrap capacitor. The dynamic characteristics to consider are diode recovery time and stored charge. Diode recovery times that are specified without operating conditions, can be misleading. Diode recovery times at no forward current ($I_F$) can be noticeably less than with forward current applied. The LM5108 boot diode recovery is specified as 20 ns at $I_F$ = 20 mA, $I_{REV}$ = 0.5 A. Dynamic impedance of LM5108 bootstrap diode helps limit the peak forward current.

In applications where switching frequencies are very high, for example in excess of 1 MHz, and the low-side minimum pulse widths are very small, the diode peak forward current could be very high and peak reverse current could also be very high, specifically if high bootstrap capacitor value has been chosen. In such applications it might be advisable to use external Schottky diode as bootstrap diode. It is safe to at least make a provision for such diode on the board if possible.

#### *8.2.2.6 VDD and Input Filter*

Some switching power supply applications are extremely noisy. Noise may come from ground bouncing and ringing at the inputs, (which are the HI and LI pins of the gate driver device). To mitigate such situations, the LM5108 offers wide input threshold hysteresis. If these features are not enough, then the application might need an input filter. Small filter such as 10-Ω resistor and 47-pF capacitor might be sufficient to filter noise at the inputs of the gate driver device. This RC filter would introduce delay and therefore need to be considered carefully. High frequency noise on bias supply can cause problems in performance of the gate driver device. To filter this noise it is recommended to use 1-Ω resistor in series with VDD pin as shown in 图 8-1. This resistor also acts as a current limiting element. In the event of short circuit on the bias rail, this resistor opens up and prevents further damage. This resistor can also be helpful in debugging the design during development phase.

#### *8.2.2.7 Transient Protection*

As mentioned in previous sections, high power high switching frequency power supplies are inherently noisy. High dV/dt and dI/dt in the circuit can cause negative voltage on different pins such as HO, LO, and HS. The device tolerates negative voltage on HS pin as mentioned in specification tables. If parasitic elements of the circuit cause very large negative swings, circuit might require additional protection. In such cases fast acting and low leakage type Schottky diode should be used. This diode must be placed as close to the gate driver device pin as possible for it to be effective in clamping excessive negative voltage on the gate driver device pin. Sometimes a small resistor, (for example 2 Ω, in series with HS pin) is also effective in improving performance reliability. To avoid the possibility of driver device damage due to over-voltage on its output pins or supply pins, low leakage Zener diode can be used. A 15-V Zener diode is often sufficient to clamp the voltage below the maximum recommended value of 16 V.

### 8.2.3 Application Curves

To minimize the switching losses in power supplies, turn-ON and turn-OFF of the power MOSFETs need to be as fast as possible. Higher the drive current capability of the driver, faster the switching. Therefore, the LM5108 is designed with high drive current capability and low resistance of the output stages. One of the common way to test the drive capability of the gate driver device , is to test it under heavy load. Rise time and fall time of the outputs would provide idea of drive capability of the gate driver device. There must not be any resistance in this


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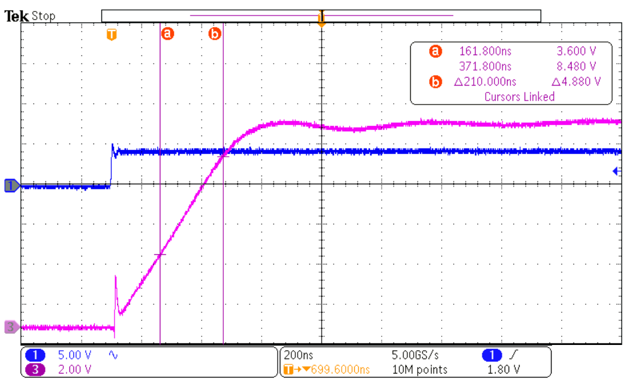
test circuit. 图 8-2 and 图 8-3 shows rise time and fall time of HO respectively of LM5108. 图 8-4 and 图 8-5 shows rise time and fall time of LO respectively of LM5108. For accuracy purpose, the VDD and HB pin of the gate driver device were connected together. HS and VSS pins are also connected together for this test.

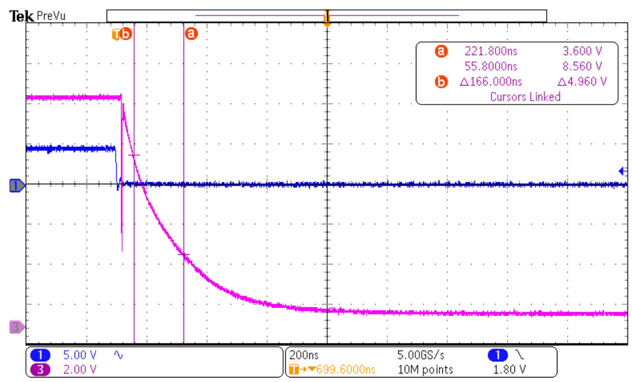
Peak current capability can be estimated using the fastest dV/dt along the rise and fall curve of the plot. This method is also useful in comparing performance of two or more gate driver devices.

As explained in 节 8.2.2.4, propagation delay plays an important role in reliable operation of many applications. 图 8-6 and 图 8-7 shows propagation delays of LM5108. In many switching power supply applications input signals to the gate driver have large amplitude high frequency noise. If there is no filter employed at the input, then there is a possibility of false signal passing through the gate driver and causing shoot-through on the output. LM5108 prevents such shoot-through. If two inputs are high at the same time, LM5108 shuts both the outputs off. 图 8-8 shows interlock feature of LM5108.



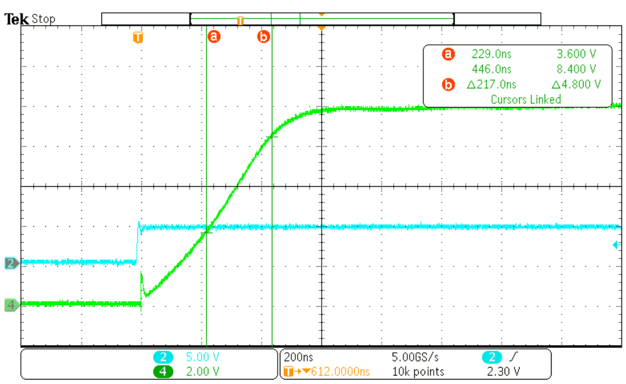

$V_{DD}$=$V_{HB}$=12 V, HS=VSS $C_{LOAD}$=68 nF Ch1=HI, Ch3=HO

**图 8-2. HO Rise Time**



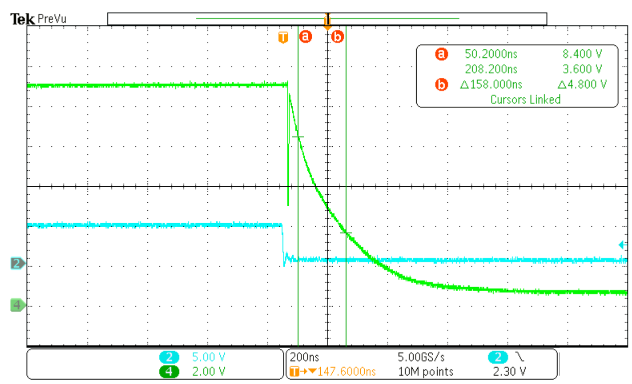

$V_{DD}$=$V_{HB}$=12 V, HS=VSS $C_{LOAD}$=68 nF Ch1=HI, Ch3=HO

**图 8-3. HO Fall Time**



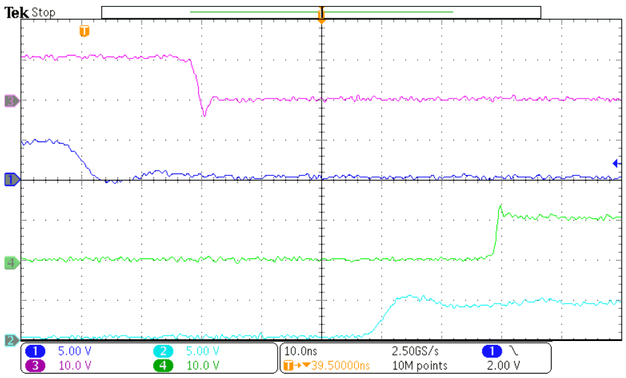

$V_{DD}$=$V_{HB}$=12 V, HS=VSS $C_{LOAD}$=68 nF Ch2=LI, Ch4=LO

**图 8-4. LO Rise Time**



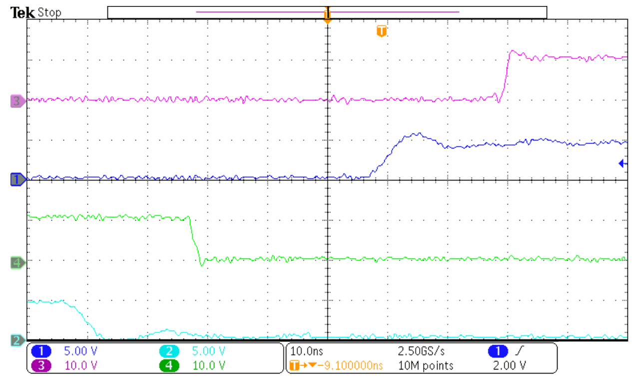

$V_{DD}$=$V_{HB}$=12 V, HS=VSS $C_{LOAD}$=68 nF Ch2=LI, Ch4=LO

**图 8-5. LO Fall Time**



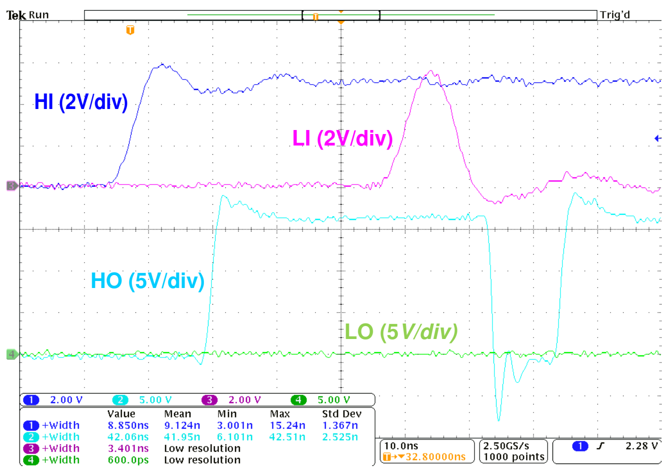
$V_{DD}$=$V_{HB}$=12 V, HS=VSS　$C_{LOAD}$=No load　Ch1=HI Ch2=LI Ch3=HO Ch4=LO

**图 8-6. Propagation Delay**



$V_{DD}$=$V_{HB}$=12 V, HS=VSS　$C_{LOAD}$=No load　Ch1=HI Ch2=LI Ch3=HO Ch4=LO

**图 8-7. Propagation Delay**




$V_{DD}$=$V_{HB}$=12 V, HS=VSS　$C_{LOAD}$=0 nF

**图 8-8. Shoot-through Protection or Interlock**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# 9 Power Supply Recommendations

The recommended bias supply voltage range for LM5108 is from 5.5 V to 16 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature, 5 V typical, of the $V_{DD}$ supply circuit block. The upper end of this range is driven by the 16-V recomended maximum voltage rating of the $V_{DD}$. It is recommended that voltage on VDD pin should be lower than maximum recommended voltage.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the $V_{DD}$ voltage drops, the device continues to operate in normal mode as far as the voltage drop do not exceeds the hysteresis specification, $V_{DDHYS}$. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 5.5-V range, the voltage ripple on the auxiliary power supply output should be smaller than the hysteresis specification of LM5108 to avoid triggering device shutdown.

A local bypass capacitor should be placed between the VDD and GND pins. This capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is recommended to use two capacitors across VDD and GND: a low capacitance ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another high capacitance value surface-mount capacitor for device bias requirements. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore, two capacitors across the HB to HS are recommended. One low value small size capacitor for high frequency filtering and another one high capacitance value capacitor to deliver HO pulses.

LM5108 has enable/disable functionality through EN pin. Therefore, signal at the EN pin should be as clean as possible. If EN pin is not used, then it is recommended to connect the pin to VDD pin. If EN pin is pulled up through a resistor, then the pull-up resistor needs to be strong. In noise prone applications, it is recommended to filter the EN pin with small capacitor, such as X7R 0402 1nF.

In power supplies where noise is very dominant and there is space on the PWB (Printed Wiring Board), it is recommended to place a small RC filter at the inputs. This allows for improving the overall performance of the design. In such applications. it is also recommended to have a place holder for power MOSFET external gate resistor. This resistor allows the control of not only the drive capability but also the slew rate on HS, which impacts the performance of the high-side circuit. If diode is used across the external gate resistor, it is recommended to use a resistor in series with the diode, which provides further control of fall time.

In power supply applications such as motor drives, there exist a lot of transients through-out the system. This sometime causes over voltage and under voltage spikes on almost all pins of the gate driver device. To increase the robustness of the design, it is recommended that the clamp diode should be used on the those pins. If user does not wish to use power MOSFET parasitic diode, external clamp diode on HS pin is recommended, which needs to be high voltage high current type (same rating as MOSFET) and very fast acting. The leakage of these diodes across the temperature needs to be minimal.

In power supply applications where it is almost certain that there is excessive negative HS voltage, it is recommended to place a small resistor between the HS pin and the switch node. This resistance helps limit current into the driver device up to some extent. This resistor will impact the high side drive capability and therefore needs to be considered carefully.

# 10 Layout

## 10.1 Layout Guidelines

To achieve optimum performance of high-side and low-side gate drivers, one must consider following printed wiring board (PWB) layout guidelines.

- Low ESR/ESL capacitors must be connected close to the device between VDD and VSS pins and between HB and HS pins to support high peak currents drawn from VDD and HB pins during the turn-on of the external MOSFETs.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground (VSS).
- In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the high-side MOSFET and the drain of the low-side MOSFET (synchronous rectifier) must be minimized.
- Overlapping of HS plane and ground (VSS) plane should be minimized as much as possible so that coupling of switching noise into the ground plane is minimized.
- Thermal pad should be connected to large heavy copper plane to improve the thermal performance of the device. Generally it is connected to the ground plane which is the same as VSS of the device. It is recommended to connect this pad to the VSS pin only.
- Grounding considerations:
  - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This confinement decreases the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. Place the gate driver as close to the MOSFETs as possible.
  - The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

## 10.2 Layout Example

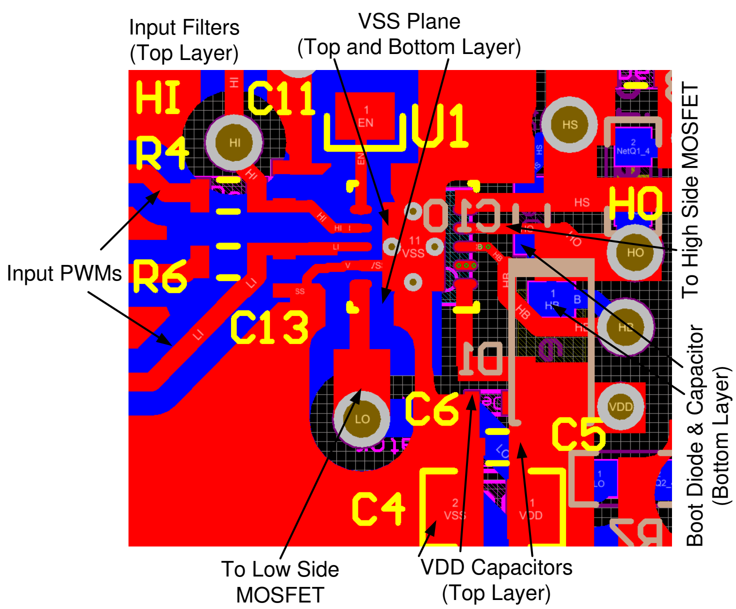


图 10-1. Layout Example


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# 11 Device and Documentation Support

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM5108DRCR | Active | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LM5108 |
| LM5108DRCR.A | Active | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LM5108 |
| LM5108DRCT | Active | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LM5108 |
| LM5108DRCT.A | Active | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LM5108 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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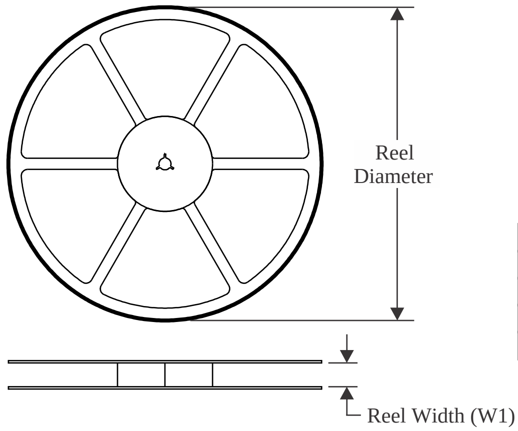
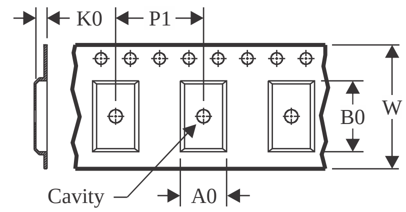
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

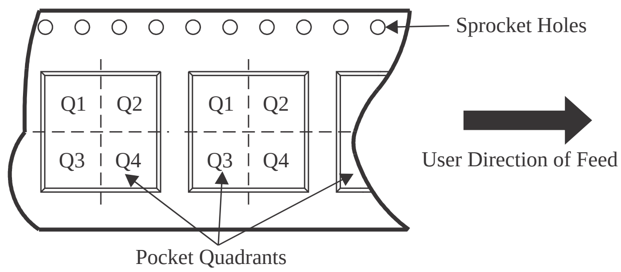



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

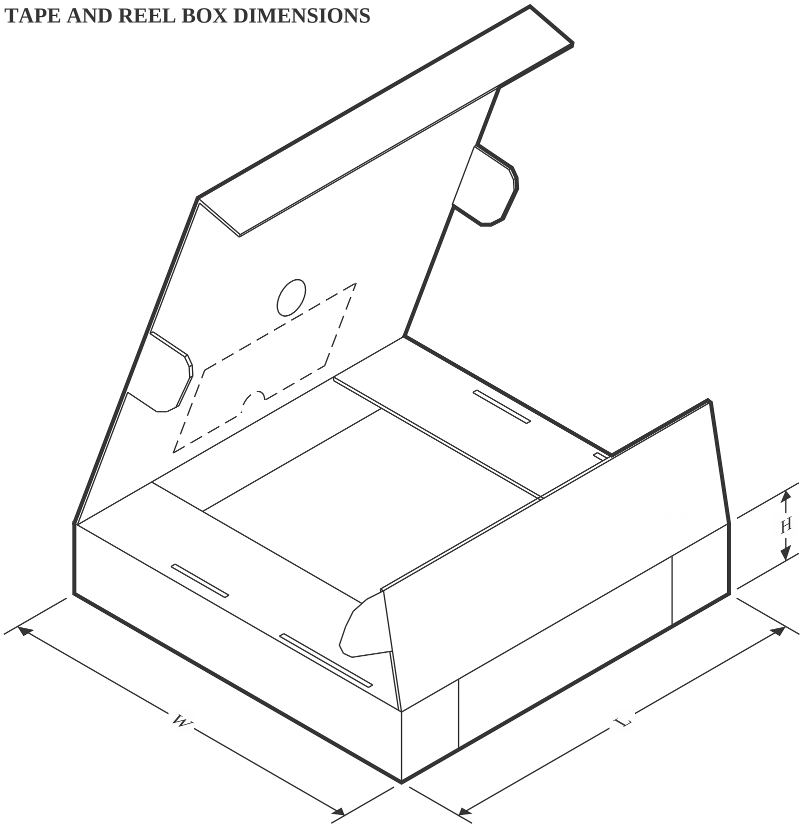
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5108DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LM5108DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM5108DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| LM5108DRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |

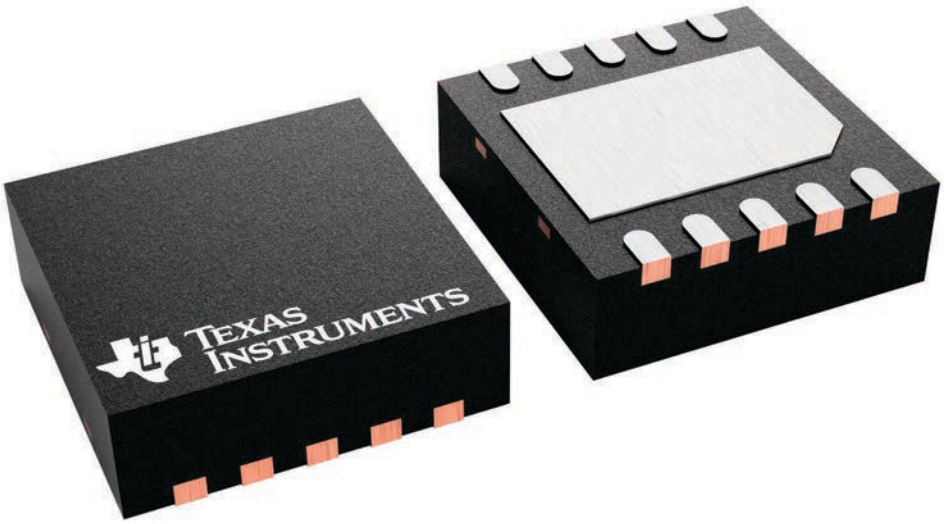
# DRC 10

**VSON - 1 mm max height**

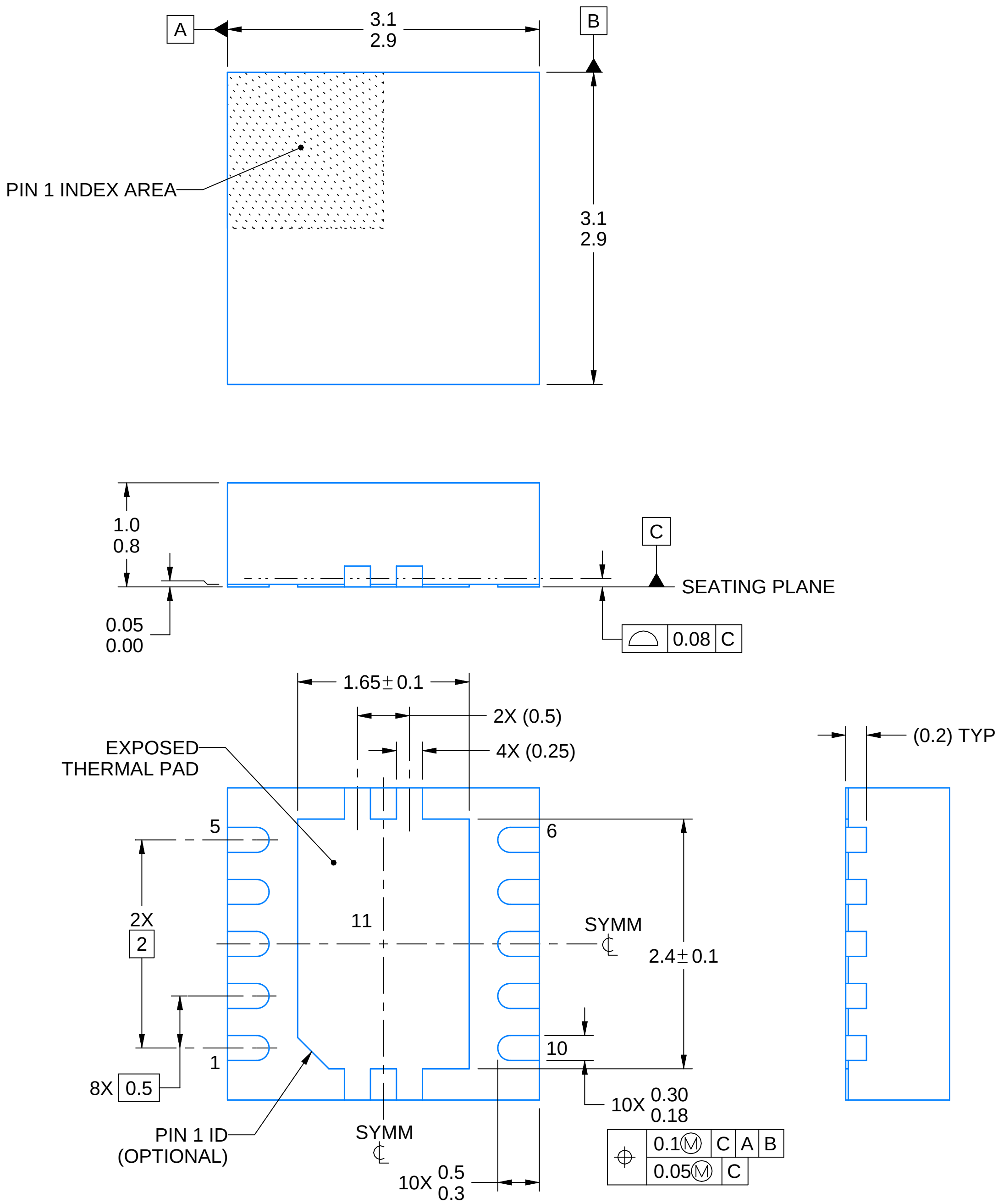
**3 x 3, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4226193/A

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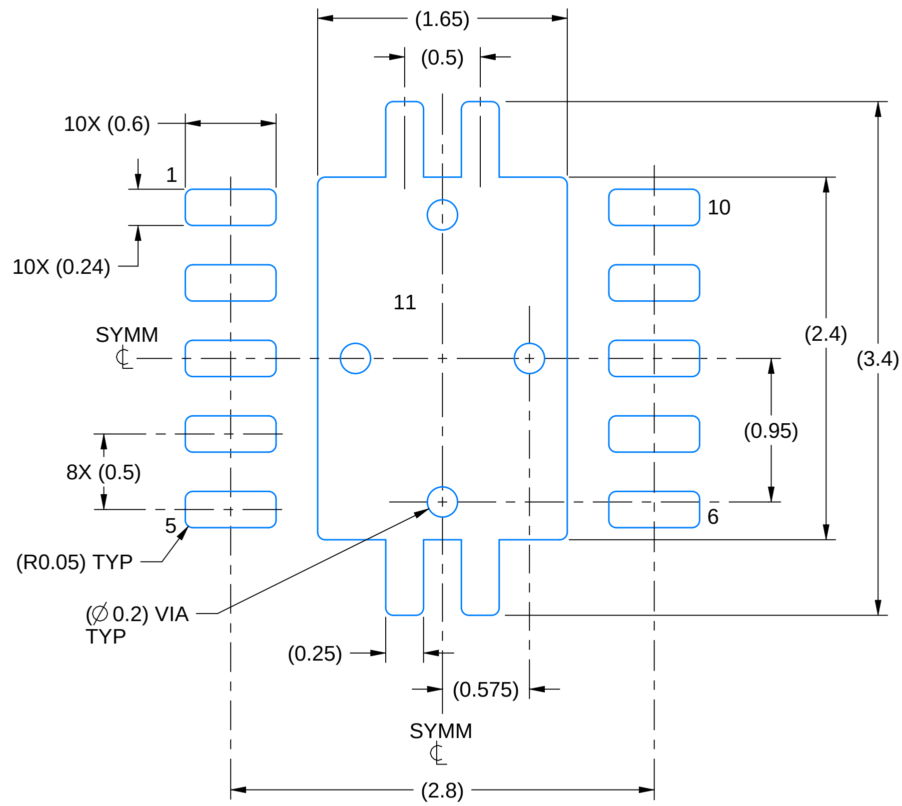
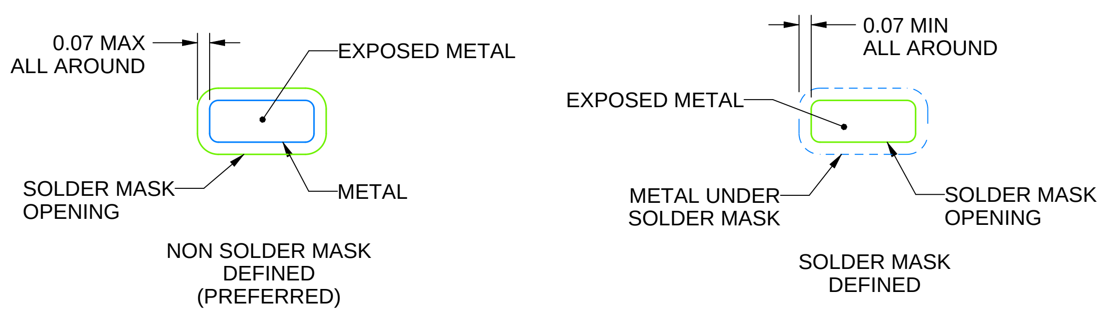
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X




SOLDER MASK DETAILS

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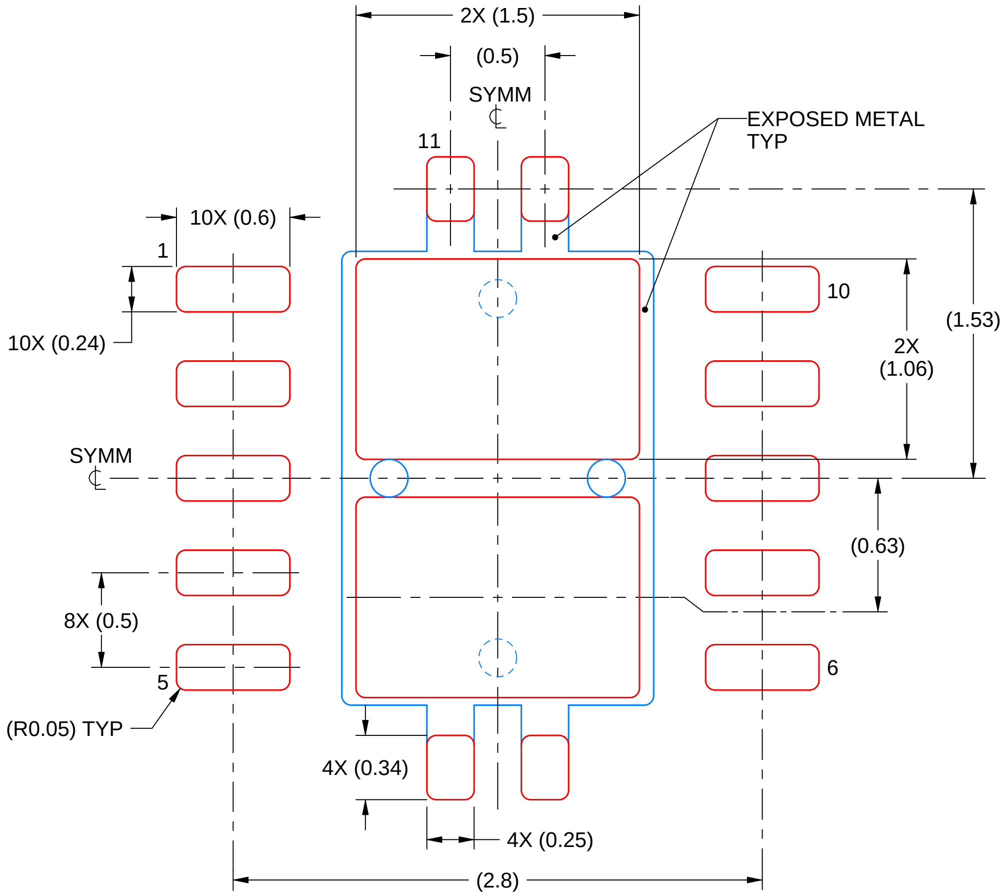
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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