LM5107 100V / 1.4-A Peak Half Bridge Gate Driver

1 Features

- Drives Both a High Side and Low Side N-Channel MOSFET
- High Peak Output Current (1.4-A Sink / 1.3-A Source)
- Independent TTL Compatible Inputs
- Integrated Bootstrap Diode
- Bootstrap Supply Voltage to 118 V DC
- Fast Propagation Times (27-ns Typical)
- Drives 1000 pF Load With 15-ns Rise and Fall Times
- Excellent Propagation Delay Matching (2-ns Typical)
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- Pin Compatible With ISL6700
- Packages:
  - SOIC
  - WSON (4 mm x 4 mm)

2 Applications

- Current Fed Push-Pull Converters
- Half and Full Bridge Power Converters
- Solid State Motor Drives
- Two Switch Forward Power Converters

3 Description

The LM5107 is a low cost high voltage gate driver, designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100-V. The outputs are independently controlled with TTL compatible input thresholds. An integrated on chip high voltage diode is provided to charge the high side gate drive bootstrap capacitor. A robust level shifter technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high side gate driver. Undervoltage lockout is provided on both the low side and the high side power rails. The device is available in the SOIC and the thermally enhanced WSON packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5107	SOIC (8)	4.90 mm × 3.91 mm
	WSON (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Block Diagram

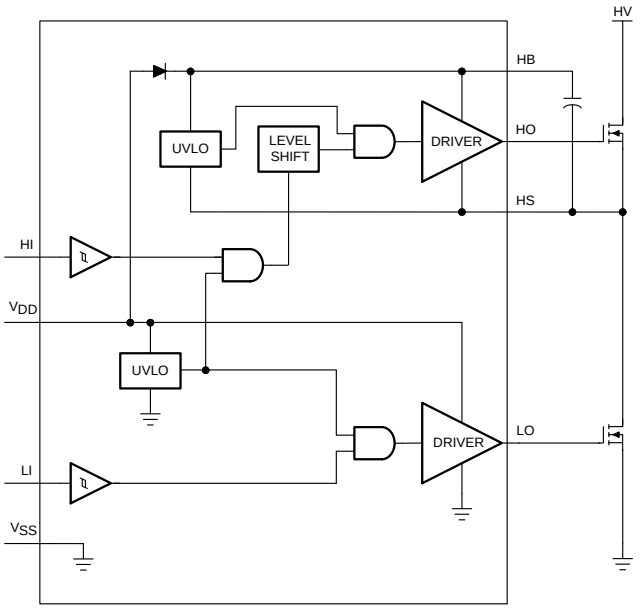


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2016) to Revision F — **Page**

- Changed *Thermal Information* table ... 4
- Added *Overview* and *Device Functional Modes* in *Detailed Description* section ... 10
- Deleted *HS Transient Voltages Below Ground* from *Application Information* section ... 12
- Added *Typical Application* section. ... 12
- Added *Power Supply Recommendations* section. ... 16
- Added *Receiving Notification of Documentation Updates* section ... 18

Changes from Revision D (March 2013) to Revision E — **Page**

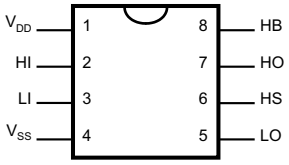
- Added *Device Information* table, *ESD Ratings*, *Pin Configuration and Functions* section, *Detailed Description* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision C (March 2013) to Revision D — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 12

5 Pin Configuration and Functions

D and NGT Packages
8-Pin SOIC, WSON
Top View



Pin Functions

PIN			DESCRIPTIONUnder	APPLICATION INFORMATION
NO.		NAME		
SOIC	WSON(1)			
1	1	V_{DD}	Positive gate drive supply	Locally decouple to V_{SS} using low ESR/ESL capacitor located as close to IC as possible.
2	2	HI	High side control input	The LM5107 HI input is compatible with TTL input thresholds. Unused HI input should be tied to ground and not left open
3	3	LI	Low side control input	The LM5107 LI input is compatible with TTL input thresholds. Unused LI input should be tied to ground and not left open.
4	4	V_{SS}	Ground reference	All signals are referenced to this ground.
5	5	LO	Low side gate driver output	Connect to the gate of the low side N-MOS device.
6	6	HS	High side source connection	Connect to the negative terminal of the bootstrap capacitor and to the source of the high side N-MOS device.
7	7	HO	High side gate driver output	Connect to the gate of the low side N-MOS device.
8	8	HB	High side gate driver positive supply rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor should be placed as close to IC as possible.

(1) For WSON package it is recommended that the exposed pad on the bottom of the LM5107 be soldered to ground plane on the PCB board and the ground plane should extend out from underneath the package to improve heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
	V_{DD} to V_{SS}	-0.3	18	V
	HB to HS	-0.3	18	V
	LI or HI to V_{SS}	-0.3	V_{DD} +0.3	V
	LO to V_{SS}	-0.3	V_{DD} +0.3	V
	HO to V_{SS}	V_{HS} − 0.3	V_{HB} + 0.3	V
	HS to V_{SS}(3)	−5	100	V
	HB to V_{SS}		118	V
T_J	Junction Temperature	-40	150	°C
T_{stg}	Storage Temperature Range	−55	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the *Electrical Characteristics* .
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} - 15V. For example, if V_{DD} = 10V, the negative transients at HS must not exceed -5V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	±2000	V

(1) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Pin 6 , Pin 7 and Pin 8 are rated at 500V.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{DD}	8		14	V
HS(1)	−1		V to 100	V
HB	V_{HS} + 8		V_{HS} + 14	V
HS Slew Rate	< 50			V/ns
Junction Temperature	−40		125	°C

(1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} - 15V. For example, if V_{DD} = 10V, the negative transients at HS must not exceed -5V.

6.4 Thermal Information

THERMAL METRIC(1)		LM5107		UNIT
		D (SOIC)	NGT (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	109.6	38.9(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	37.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.4	15.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.1	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.8	16.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	5	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report.
(2) The θ_{JA} is not a constant for the package and depends on the printed circuit board design and the operating conditions.
(3) 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

6.5 Electrical Characteristics

Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO. Typical limits are for T_J = +25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to +125°C).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V		0.3	0.6	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		2.1	3.4	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	0.2	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.6	3	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 100V		0.1	10	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.5		mA
INPUT PINS LI and HI						
V_{IL}	Low Level Input Voltage Threshold		0.8	1.8		V
V_{IH}	High Level Input Voltage Threshold			1.8	2.2	V
R_I	Input Pulldown Resistance		100	180	500	kΩ
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold	V_{DDR} = V_{DD} - V_{SS}	6	6.9	7.4	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold	V_{HBR} = V_{HB} - V_{HS}	5.7	6.6	7.1	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA V_{DL} = V_{DD} - V_{HB}		0.58	0.9	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA V_{DH} = V_{DD} - V_{HB}		0.82	1.1	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8	1.5	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA V_{OHL} = V_{LO} – V_{SS}		0.28	0.45	V
V_{OHL}	High-Level Output Voltage	I_{LO} = −100 mA, V_{OHL} = V_{DD}– V_{LO}		0.45	0.75	V
I_{OHL}	Peak Pullup Current	V_{LO} = 0V		1.3		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12V		1.4		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA V_{OLH} = V_{HO}– V_{HS}		0.28	0.45	V
V_{OHH}	High-Level Output Voltage	I_{HO} = −100 mA V_{OHH} = V_{HB}– V_{HO}		0.45	0.75	V
I_{OHH}	Peak Pullup Current	V_{HO} = 0V		1.3		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12V		1.4		A

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

6.6 Switching Characteristics

Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO. Typical limits are for T_J = +25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to +125°C).

Parameter		CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			27	56	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			27	56	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			29	56	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			29	56	ns
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off			2	15	ns
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On			2	15	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15	–	ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 100 mA, I_R = 100 mA		105		ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

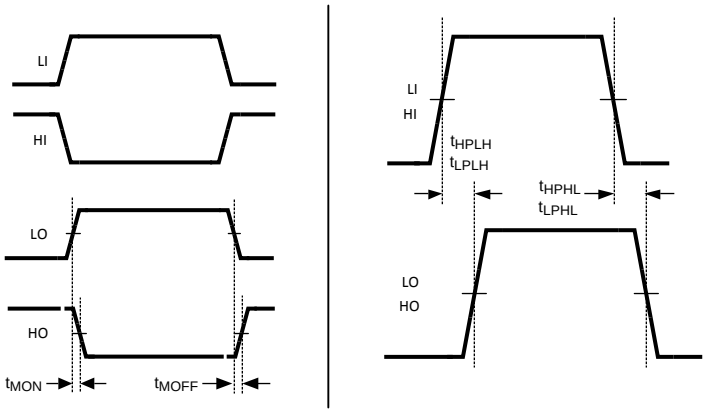


Figure 1. Timing Diagram

6.7 Typical Performance Characteristics

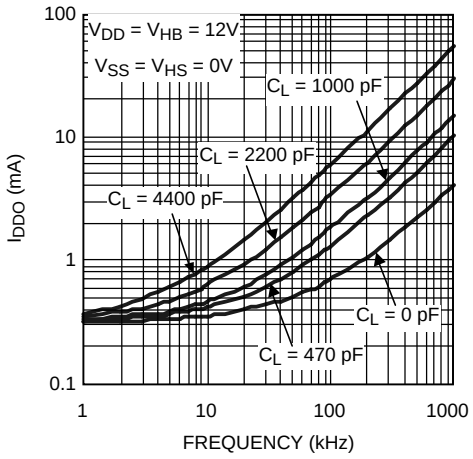


Figure 2. V_{DD} Operating Current vs Frequency

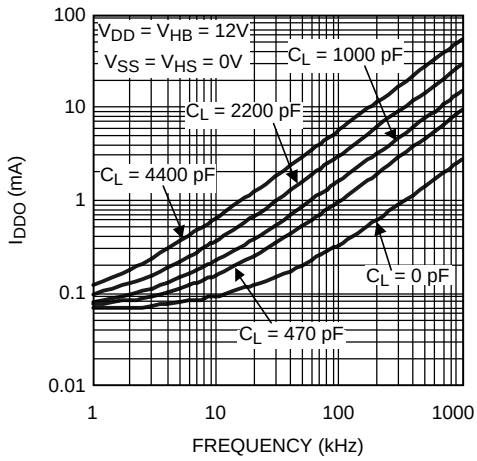


Figure 3. HB Operating Current vs Frequency

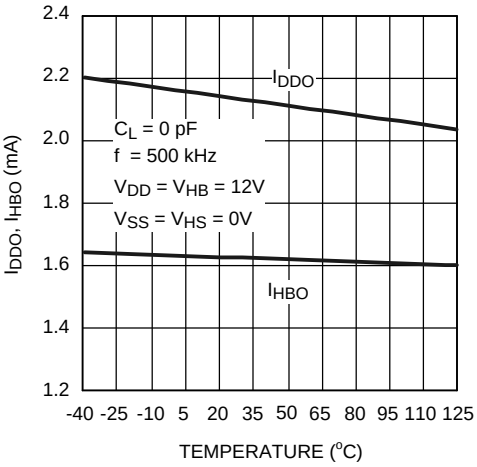


Figure 4. Operating Current vs Temperature

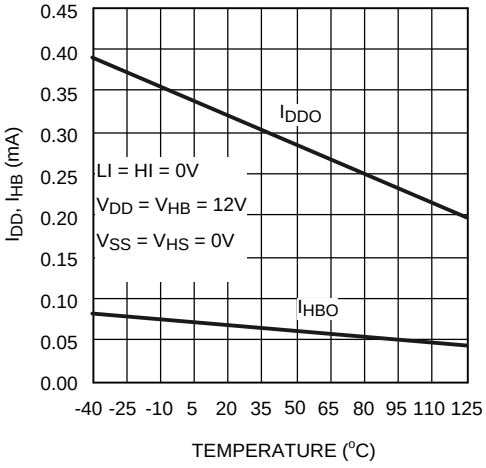


Figure 5. Quiescent Current vs Temperature

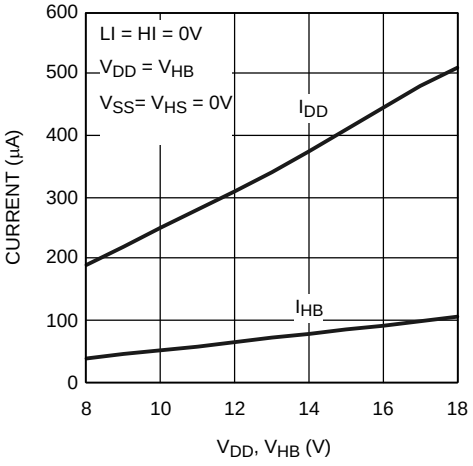


Figure 6. Quiescent Current vs Voltage

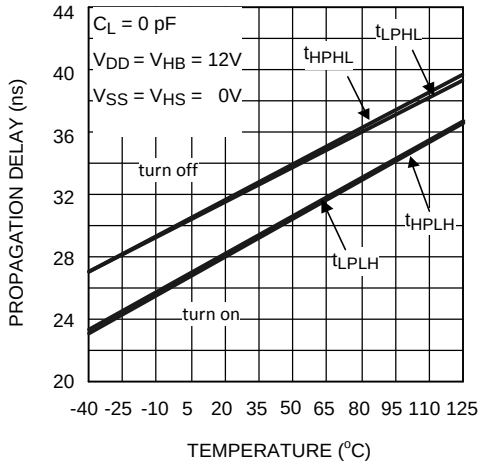


Figure 7. Propagation Delay vs Temperature

Typical Performance Characteristics (continued)

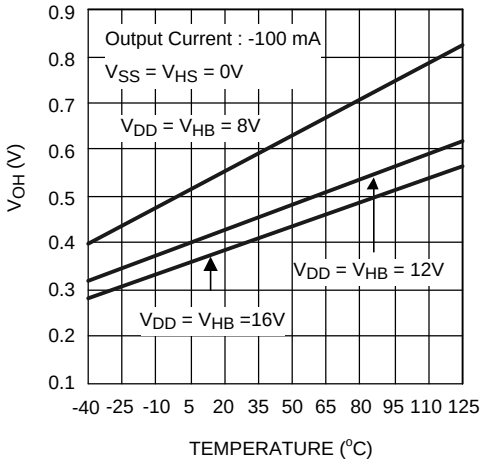


Figure 8. LO and HO High Level Output Voltage vs Temperature

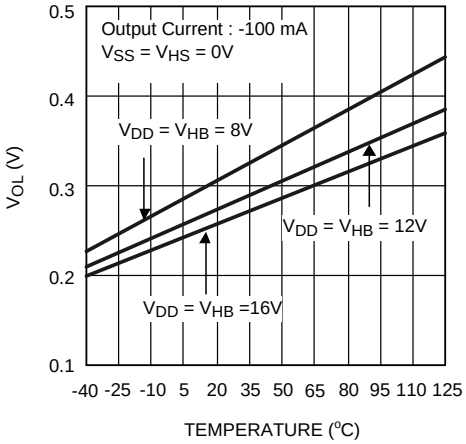


Figure 9. LO and HO Low Level Output Voltage vs Temperature

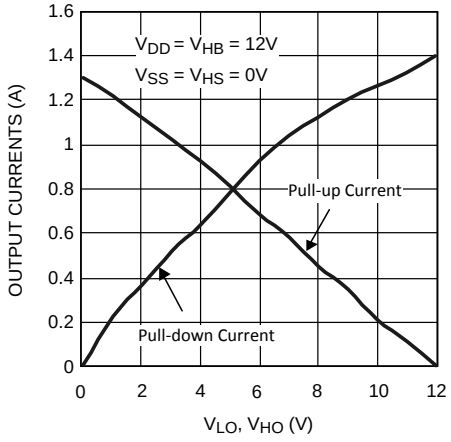


Figure 10. HO and LO Peak Output Current vs Output Voltage

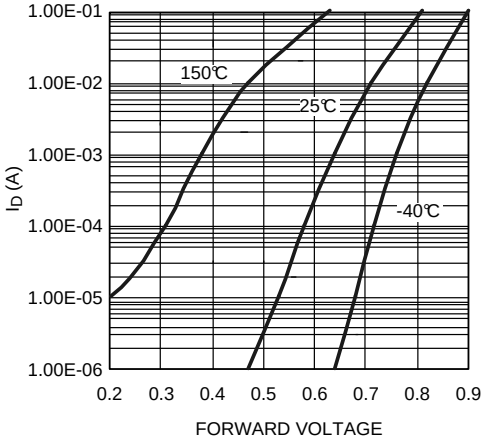


Figure 11. Doide Forward Voltage

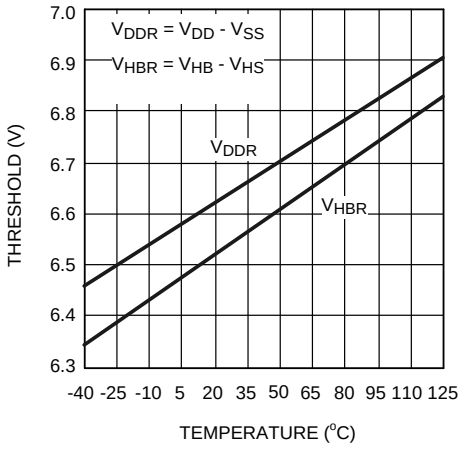


Figure 12. Undervoltage Rising Thresholds vs Temperature

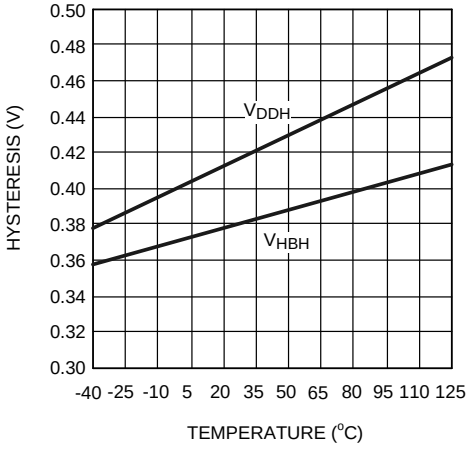


Figure 13. Undervoltage Hysteresis vs Temperature

Typical Performance Characteristics (continued)

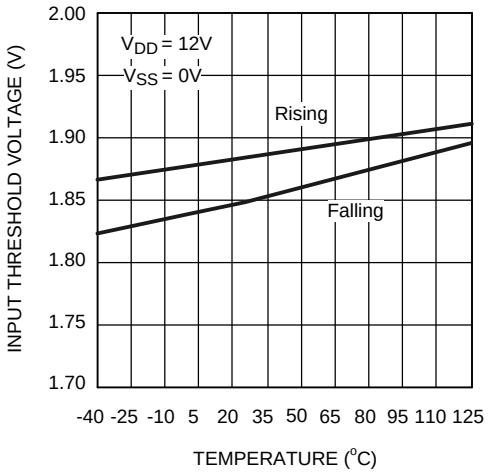


Figure 14. Input Thresholds vs Temperature

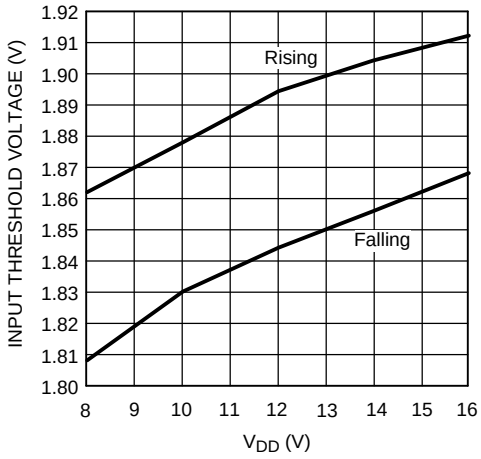


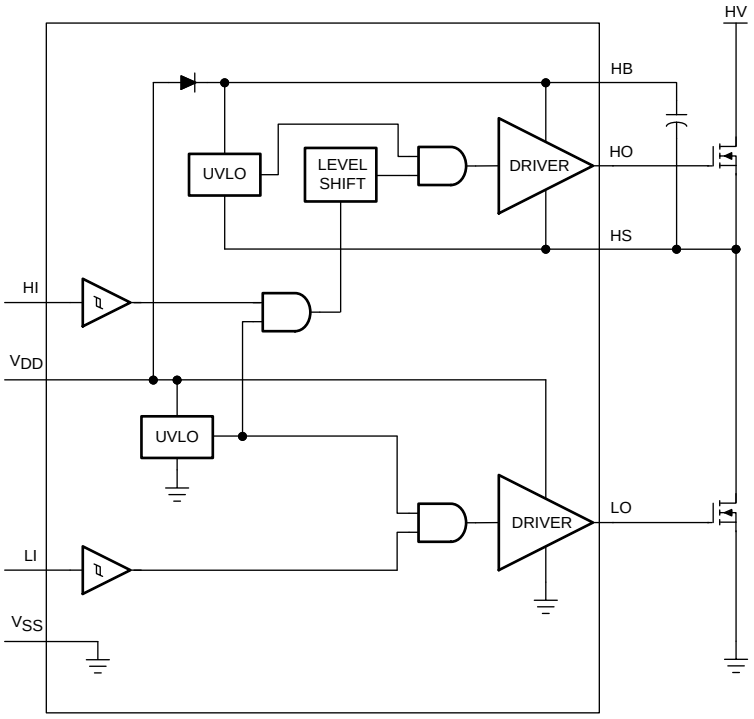
Figure 15. Input Thresholds vs Supply Voltage

7 Detailed Description

7.1 Overview

The LM5107 is designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The outputs are independently controlled with TTL input thresholds. The floating high-side driver is capable of working with supply voltages up to 100 V. An integrated high voltage diode is provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Undervoltage lockout is provided on both the low side and the high side power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start-up and UVLO

Both high and low-side drivers include under voltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage ($V_{HB–HS}$) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the V_{DD} pin of the LM5107, the outputs of the low-side and high-side are held low until V_{DD} exceeds the UVLO threshold, typically about 6.9 V. Any UVLO condition on the bootstrap capacitor will disable only the high-side output (HO).

7.3.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

Feature Description (continued)

7.3.3 Bootstrap Diode

The bootstrap diode necessary to generate the high-side bias is included in the LM5107. The diode anode is connected to V_{DD} and cathode connected to V_{HB}. With the V_{HB} capacitor connected to HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

7.3.4 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from V_{DD} to V_{SS} and the high-side is referenced from V_{HB} to V_{HS}.

7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See *Start-up and UVLO* for more information on UVLO operation mode. In normal mode, the output stage is dependent on the states of the HI and LI pins.

Table 1. Input/Output Logic Table

HI	LI	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to the HS.
(2) LO is measured with the respect to the VSS.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LM5107 is a high voltage gate driver that is designed to drive both the high-side and low-side N-Channel MOSFETs in a half-bridge/full bridge configuration or in a synchronous buck circuit. The floating high side driver is capable of operating with supply voltages up to 100 V. This allows for N-Channel MOSFET control in half-bridge, full-bridge, push-pull, two switch forward and active clamp topologies. The outputs are independently controlled. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control on and off state of the output.

8.2 Typical Application

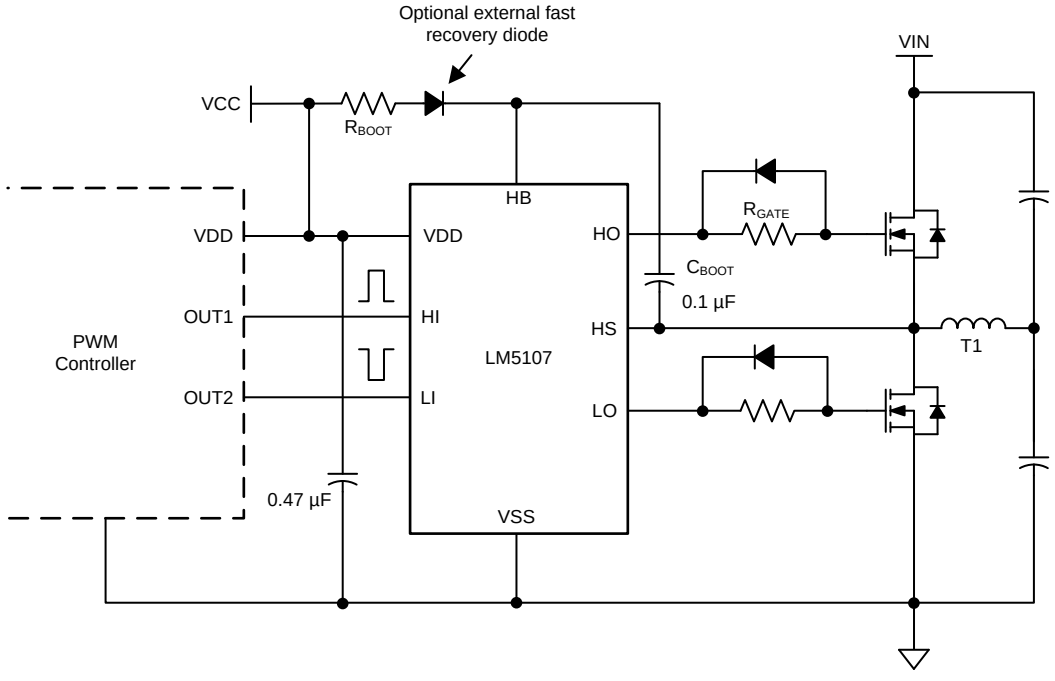


Figure 16. LM5107 Driving MOSFETs in Half-Bridge Configuration

Typical Application (continued)

8.2.1 Design Requirements

See Table 2 for the parameter and values.

Table 2. Operating Parameters

PARAMETER	VALUE
Gate Driver	LM5107
MOSFET	CSD18531Q5A
VDD	10 V
Qgmax	43 nC
Fsw	100 kHz
Dmax	95%
I_{HBS}	10 µA
V_{DH}	1.0 V
V_{HBR}	7.1 V
V_{HBH}	0.4 V

8.2.2 Detailed Design Procedure

8.2.2.1 Select Bootstrap and VDD capacitor

The bootstrap capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit in any circumstances during normal operation. Calculate the maximum allowable drop across the bootstrap capacitor with Equation 1.

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = 10\ V - 1.0\ V - 6.7\ V = 2.3\ V \quad (1)$$

where

- V_{DD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- $V_{HBL} = V_{HBR} - V_{HBH}$ = 6.7 V, HB falling threshold

The quiescent current of the bootstrap circuit is 10 µA, which is negligible compared to the Qgs of the MOSFET (see Equation 2 and Equation 3).

$$Q_{TOTAL} = Q_{gmax} + I_{HBS}\frac{D_{MAX}}{F_{SW}} = 43\ nC + 10\ \mu A\frac{0.95}{100\ kHz} = 43.01\ nC \quad (2)$$

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{HB}} = \frac{43.01\ nC}{2.3\ V} = 18.7\ nF \quad (3)$$

In practice the value for the CBOOT capacitor should be greater than that calculated to allow for situations where the power stage may skip pulse due to load transients. It is recommended to place the bootstrap capacitor as close to the HB and HS pins as possible.

$$C_{BOOT} = 100\ nF \quad (4)$$

As a general rule the local VDD bypass capacitor should be 10 times greater than the value of CBOOT.

$$C_{VDD} = 10 \times C_{BOOT} = 1\ \mu F \quad (5)$$

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum VDD to allow for loss of capacitance once the devices have a DC bias voltage across them and to ensure long-term reliability of the devices.

8.2.2.2 Select External Bootstrap Diode and Resistor

The bootstrap capacitor is charged by the VDD through the internal bootstrap diode every cycle when low side MOSFET turns on. The charging of the capacitor involves high peak currents, and therefore transient power dissipation in the internal bootstrap diode may be significant and dependent on its forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver and need to be considered in the gate driver IC power dissipation.

For high frequency and high capacitive loads, it may be necessary to consider using an external bootstrap diode placed in parallel with internal bootstrap diode to reduce power dissipation of the driver.

Bootstrap resistor R_{BOOT} is selected to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of HB-HS. It is recommended that R_{BOOT} is between 2 Ω and 10 Ω. For this design, a current limiting resistor of 2.2 Ω is selected to limit inrush current of bootstrap diode.

$$I_{DBOOT(pk)} = \frac{V_{DD} - V_{DBOOT}}{R_{BOOT}} = \frac{10\ V - 0.6\ V}{2.2\ \Omega} = 4.27\ A \quad (6)$$

8.2.2.3 Select Gate Driver Resistor

Resistor R_{GATE} is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver. For this design 7.5-Ω resistors were selected for this design. Maximum HO and LO drive current are calculated by Equation 7 through Equation 10.

$$I_{HOH} = \frac{V_{DD} - V_{DH} - V_{OH}}{R_{GATE}} = \frac{10\ V - 1\ V - 0.45\ V}{7.5\ \Omega} = 1.14\ A \quad (7)$$

$$I_{LOH} = \frac{V_{DD} - V_{OH}}{R_{GATE}} = \frac{10\ V - 0.45\ V}{7.5\ \Omega} = 1.27\ A \quad (8)$$

$$I_{HOL} = \frac{V_{DD} - V_{DH} - V_{OL}}{R_{GATE}} = \frac{10\ V - 1\ V - 0.25\ V}{7.5\ \Omega} = 1.17\ A \quad (9)$$

$$I_{LOL} = \frac{V_{DD} - V_{OH}}{R_{GATE}} = \frac{10\ V - 0.25\ V}{7.5\ \Omega} = 1.30\ A$$

where

- I_{HOH} = Maximum HO source current
- I_{LOH} = Maximum LO source current
- I_{HOL} = Maximum HO sink current
- I_{LOH} = Maximum HO sink current
- V_{OH} = High-Level output voltage drop across HB to HO or VDD to LO
- V_{OL} = Low-Level output voltage drop across HO to HS or LO to GND (10)

8.2.3 Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 11.

$$P_{DISS} = P_{DC} + P_{SW} \quad (11)$$

Use Equation 12 to calculate the DC portion of the power dissipation (PDC).

$$PDC = I_Q \times V_{DD}$$

where

- I_Q is the quiescent current for the driver. (12)

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage VG, which is very close to input bias supply voltage VDD)
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 13.

$$EG = ½C_{LOAD} \times V_{DD}^2$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver (13)

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by Equation 14.

$$PG = C_{LOAD} \times V_{DD}^2 \times f_{SW}$$

where

- f_{SW} is the switching frequency (14)

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when switching a capacitor which is calculated using the equation $Q_G = C_{LOAD} \times V_{DD}$ to provide Equation 15 for power.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (15)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

8.2.4 Application Curves

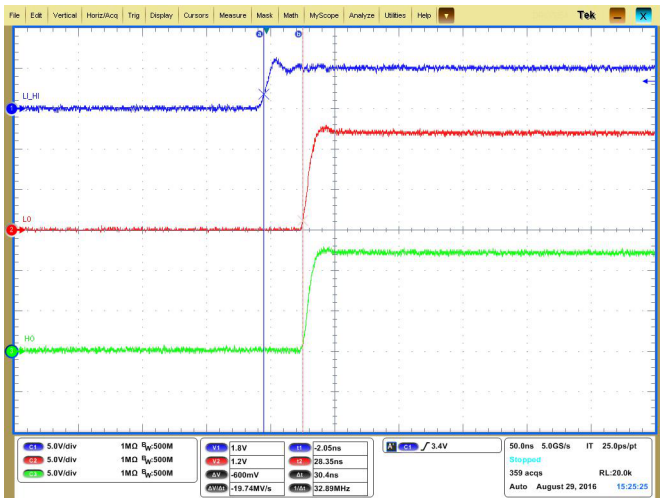


Figure 17. LI/HI to LO/HO Turn On Propagation Delay

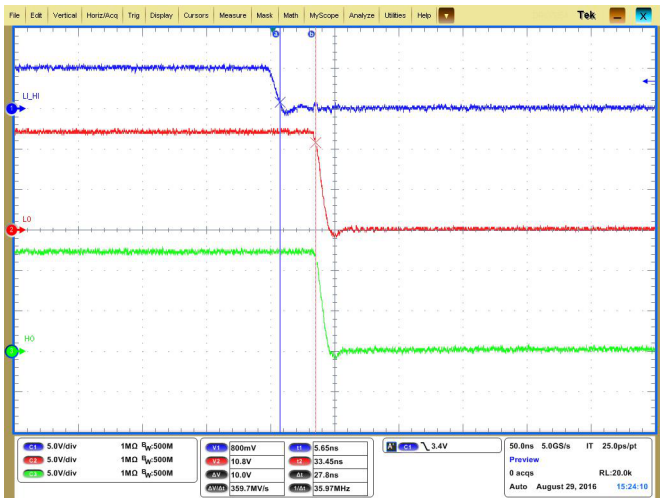


Figure 18. LI/HI to LO/HO Turn Off Propagation Delay

9 Power Supply Recommendations

The bias supply voltage range for which the device is rated to operate is from 8 V to 14 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the VDDR supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 18-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 4-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 14 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDDH. Therefore, ensuring that, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the threshold (V_{DDR} – V_{DDH}), which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start up, the device does not begin operation until the VDD pin voltage has exceeded above the V_{DDR} threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Keep in mind that the charge for source current pulses delivered by the LO pin is also supplied through the same VDD pin. As a result, every time a current is sourced out of the LO pin a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that a local bypass capacitor is provided between the VDD and GND pins and located as close as possible to the device for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is necessary. TI recommends using two capacitors between VDD and GND: a 100-nF ceramic surface-mount capacitor that can be nudged very close to the pins of the device and another surface-mount capacitor in the range 0.22 µF to 10 µF added in parallel. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore, a 0.022-µF to 1-µF local decoupling capacitor is recommended between the HB and HS pins.

10 Layout

10.1 Layout Guidelines

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR / ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
   – The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   – The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

10.2 Layout Example

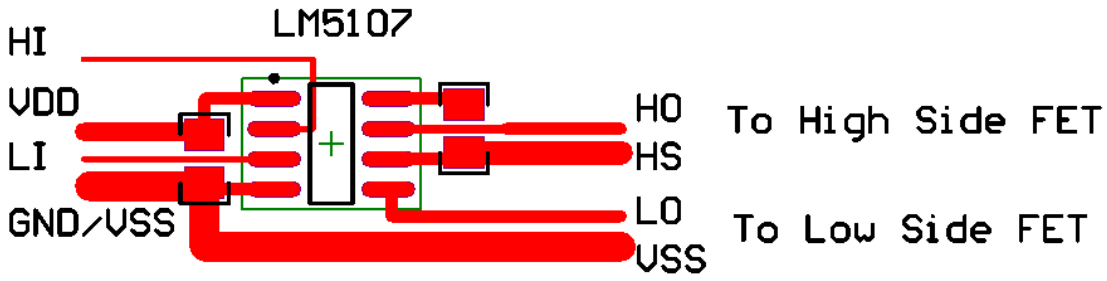


Figure 19. Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following:

AN-1187 Leadless Leadframe Package (LLP) (SNOA401).

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5107MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107 MA
LM5107MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107 MA
LM5107MA/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107 MA
LM5107MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107 MA
LM5107MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107 MA
LM5107MAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107 MA
LM5107SD/NOPB	Active	Production	WSON (NGT) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107SD
LM5107SD/NOPB.A	Active	Production	WSON (NGT) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107SD
LM5107SD/NOPB.B	Active	Production	WSON (NGT) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L5107SD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

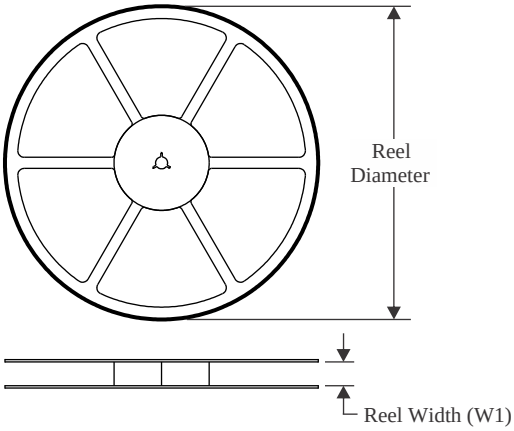
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

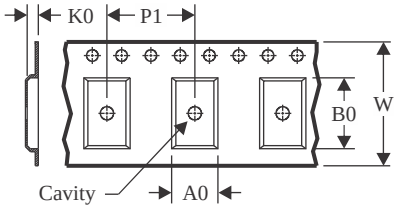
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

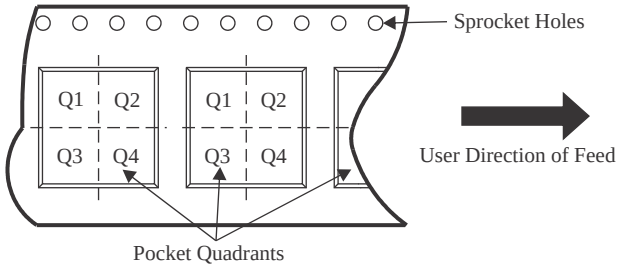


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

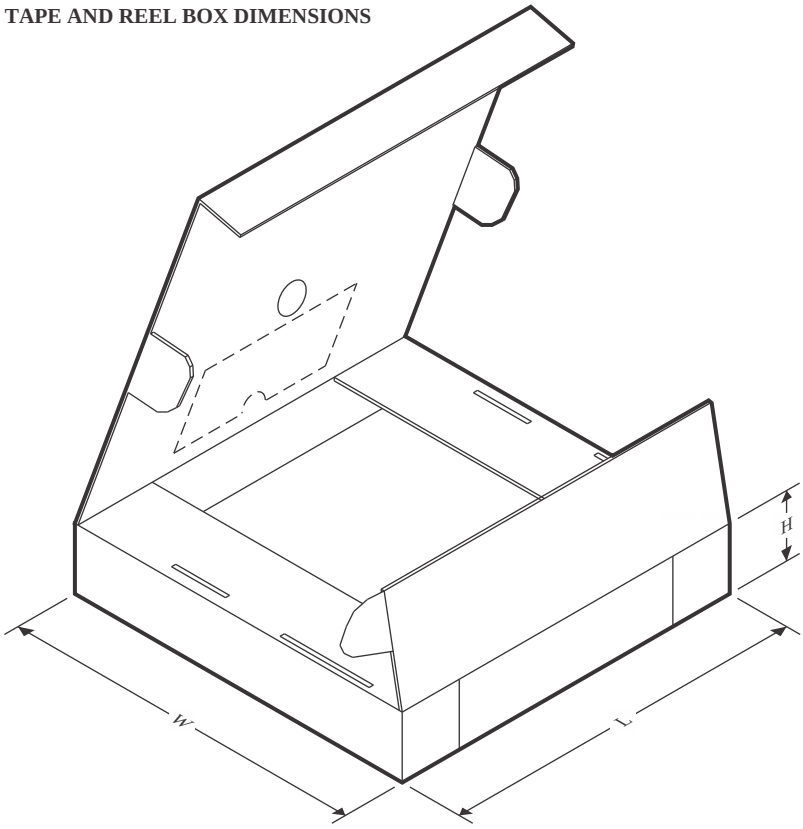
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5107MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5107SD/NOPB	WSON	NGT	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1

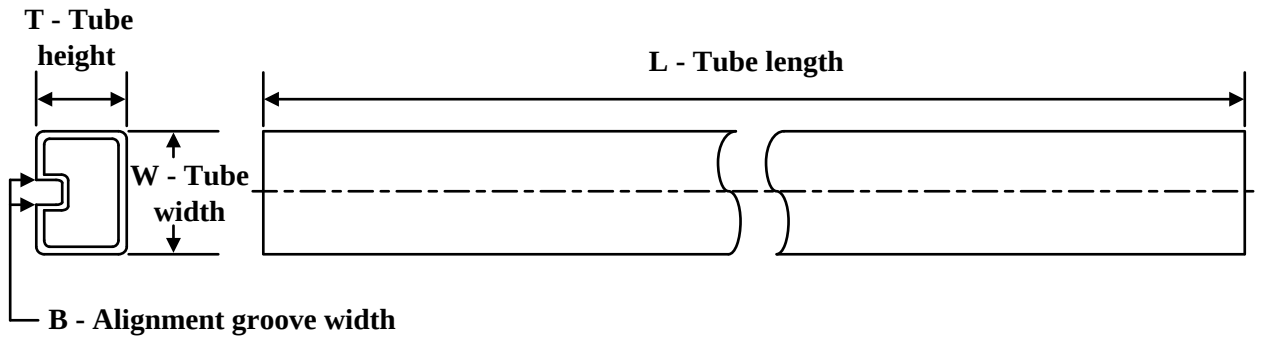
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5107MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5107SD/NOPB	WSON	NGT	8	1000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

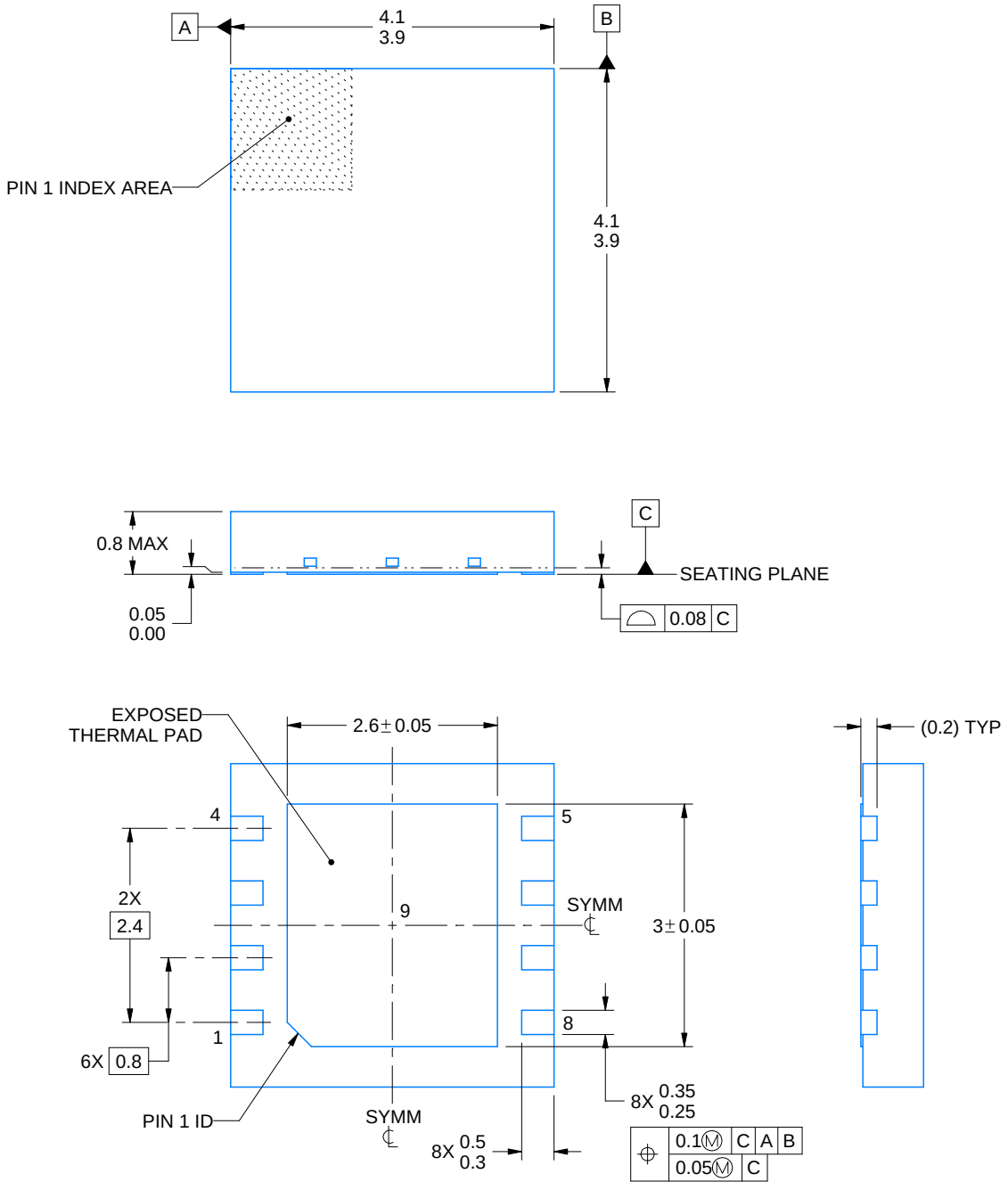
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5107MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5107MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM5107MA/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

NGT0008A

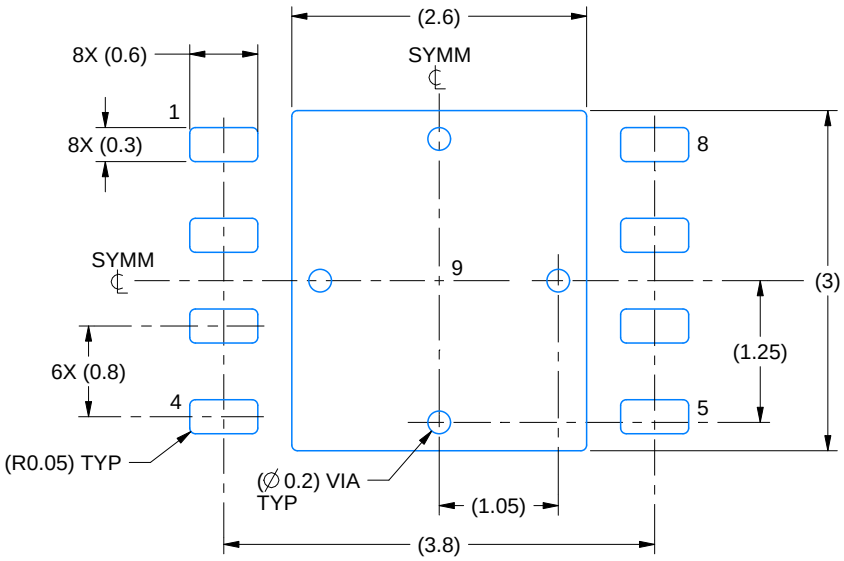
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

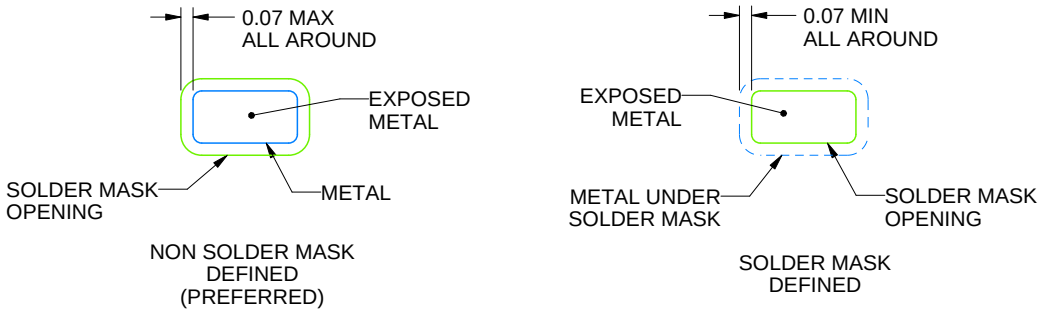


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

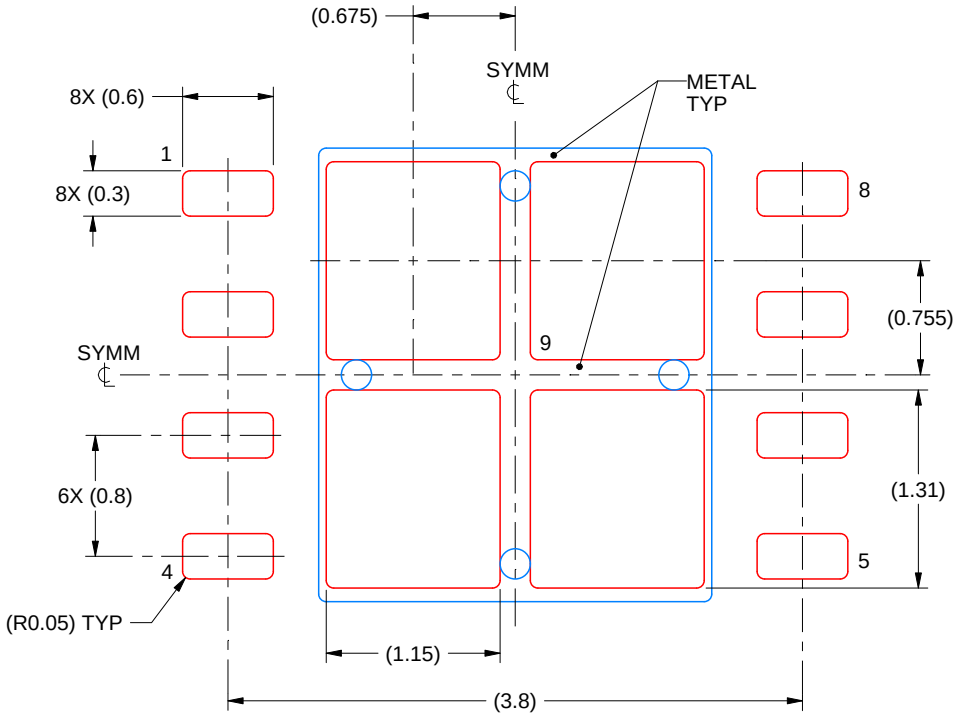


SOLDER MASK DETAILS

4214935/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



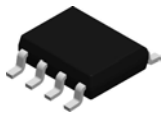
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214935/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

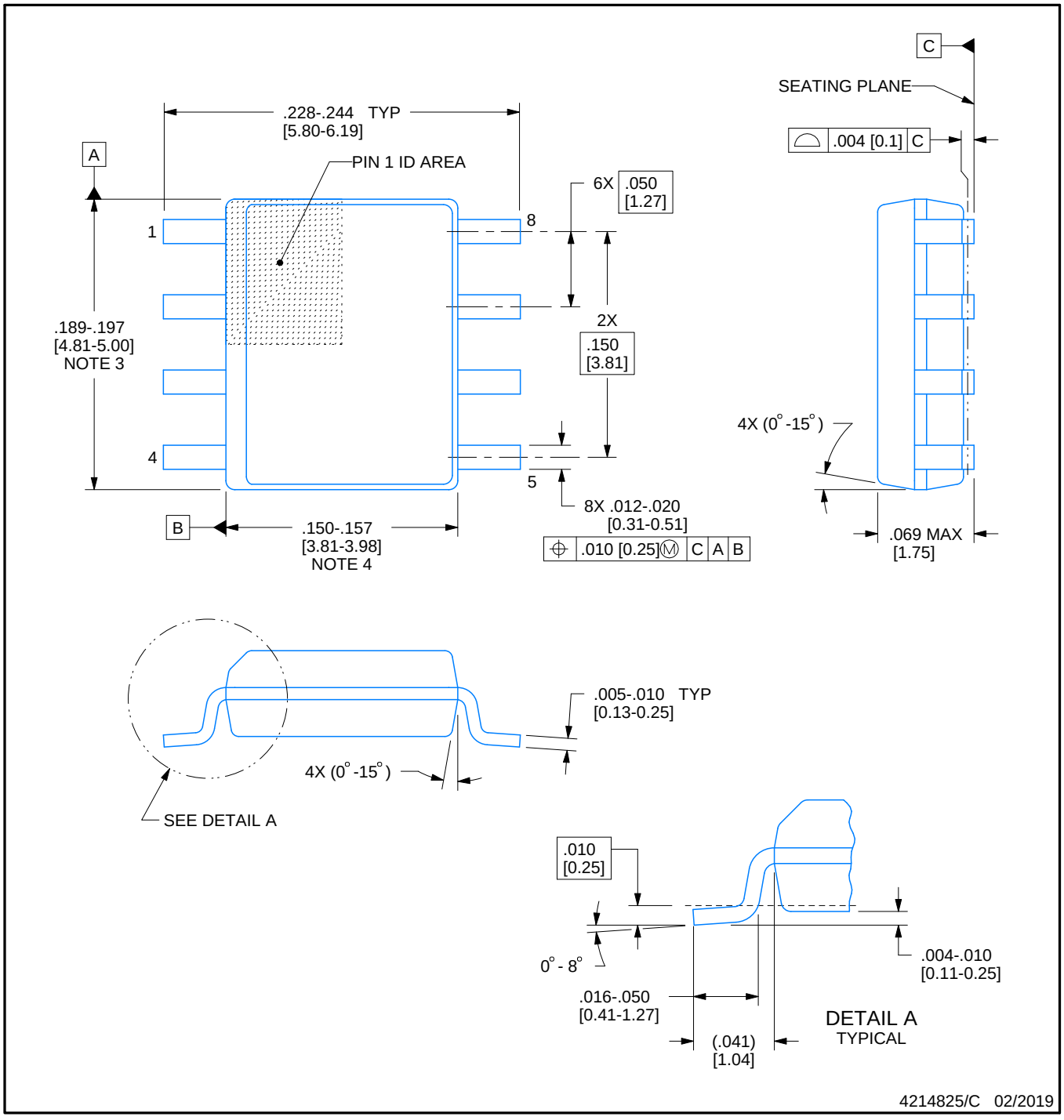


PACKAGE OUTLINE

D0008A

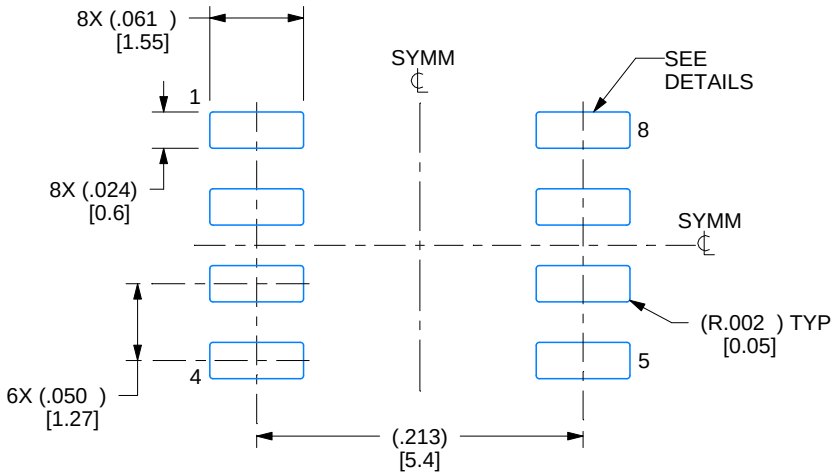
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

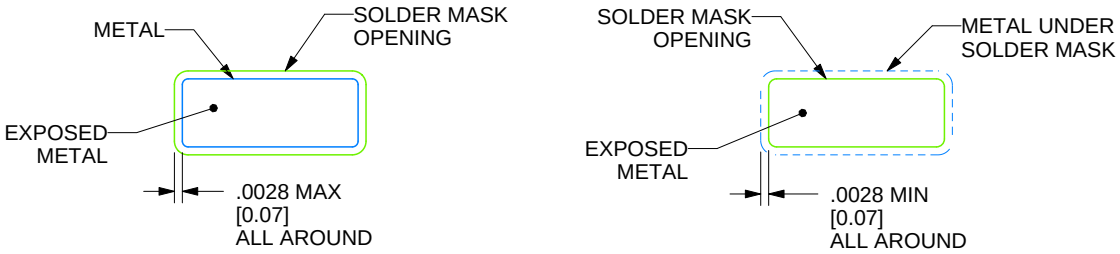


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

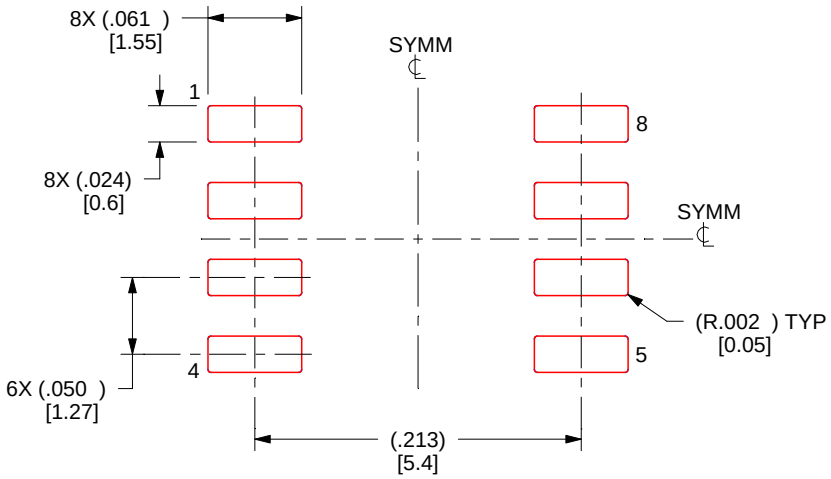
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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