LM5100 /LM5101 High Voltage High Side and Low Side Gate Driver

Check for Samples: LM5100, LM5101

FEATURES

- **Drives Both a High Side and Low Side N-Channel MOSFET**
- **Independent High and Low Driver Logic Inputs (TTL for LM5101 or CMOS for LM5100)**
- **Bootstrap Supply Voltage Range up to 118V DC**
- **Fast Propagation Times (25 ns Typical)**
- **Drives 1000 pF Load with 15 ns Rise and Fall Times**
- **Excellent Propagation Delay Matching (3 ns Typical)**
- **Supply Rail Under-voltage Lockouts**
- **Low Power Consumption**
- **Pin Compatible with HIP2100/HIP2101**

TYPICAL APPLICATIONS

- **Current Fed Push-pull Converters**
- **Half and Full Bridge Power Converters**
- **Synchronous Buck Converters**
- **Two Switch Forward Power Converters**
- **Forward with Active Clamp Converters**

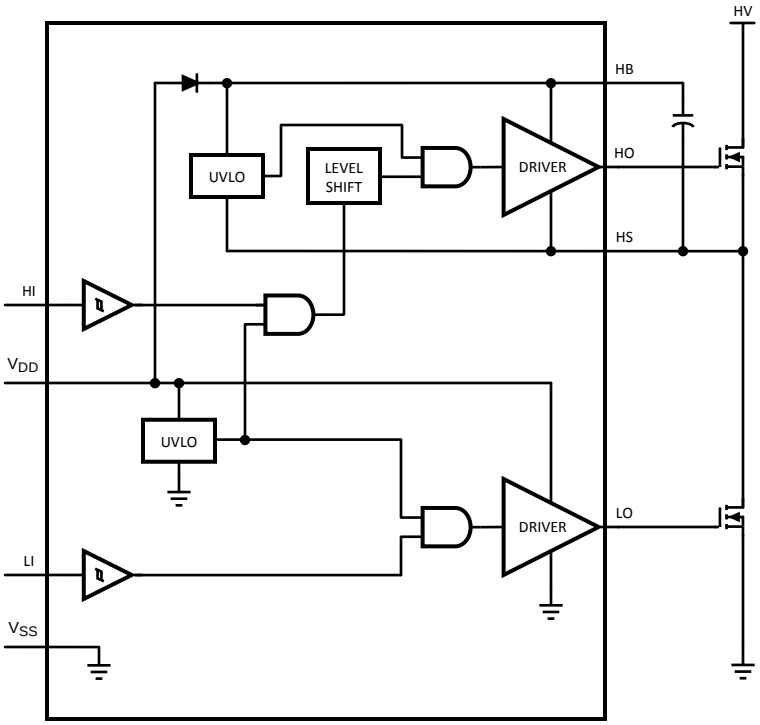
PACKAGE

- **SOIC-8**
- **WSON-10 (4 mm x 4 mm)**

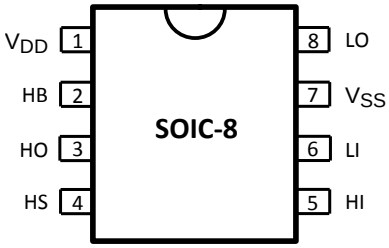
DESCRIPTION

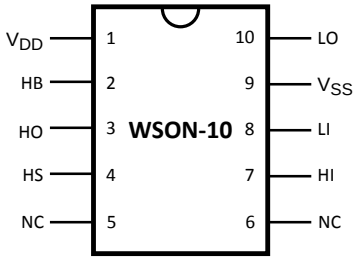
The LM5100/LM5101 High Voltage Gate Drivers are designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The outputs are independently controlled with CMOS input thresholds (LM5100) or TTL input thresholds (LM5101). An integrated high voltage diode is provided to charge the high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. This device is available in the standard SOIC-8 pin and the WSON-10 pin packages.

Simplified Block Diagram



Connection Diagrams





PIN DESCRIPTION (1)

Pin #		Name	Description	Application Information
SO-8	WSON-10			
1	1	V_{DD}	Positive gate drive supply	Locally decouple to V_{SS} using low ESR/ESL capacitor located as close to IC as possible.
2	2	HB	High side gate driver bootstrap rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The Bootstrap capacitor should be place as close to IC as possible.
3	3	HO	High side gate driver output	Connect to gate of high side MOSFET with a short low inductance path.
4	4	HS	High side MOSFET source connection	Connect to bootstrap capacitor negative terminal and the source of the high side MOSFET.
5	7	HI	High side driver control input	The LM5100 inputs have CMOS type thresholds. The LM5101 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
6	8	LI	Low side driver control input	The LM5100 inputs have CMOS type thresholds. The LM5101 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7	9	V_{SS}	Ground return	All signals are referenced to this ground.
8	10	LO	Low side gate driver output	Connect to the gate of the low side MOSFET with a short low inductance path.

(1) **Note: For WSON-10 package, it is recommended that the exposed pad on the bottom of the LM5100 / LM5101 be soldered to ground plane on the PC board, and the ground plane should extend out from beneath the IC to help dissipate the heat. Pins 5 and 6 have no connection.**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_{DD} to V_{SS}	−0.3V to +18V
V_{HB} to V_{HS}	−0.3V to +18V
LI or HI Inputs	−0.3V to V_{DD} +0.3V
LO Output	−0.3V to V_{DD} +0.3V
HO Output	V_{HS} −0.3V to V_{HB} +0.3V
V_{HS} to V_{SS}	−1V to +100V
V_{HB} to V_{SS}	118V
Junction Temperature	+150°C
Storage Temperature Range	−55°C to +150°C
ESD Rating HBM(3)	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 500V.

Recommended Operating Conditions

V_{DD}	+9V to +14V
HS	−1V to 100V
HB	V_{HS} +8V to V_{HS} +14V
HS Slew Rate	< 50 V/ns
Junction Temperature	−40°C to +125°C

Electrical Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO .

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Units
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V (LM5100)		0.1	**0.2**	mA
		LI = HI = 0V (LM5101)		0.25	**0.4**	
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		1.5	**3**	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.3	**3**	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 100V		0.05	**10**	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.08		mA
INPUT PINS						
V_{IL}	Low Level Input Voltage Threshold (LM5100)		**3**	5.0		V
V_{IL}	Low Level Input Voltage Threshold (LM5101)		**0.8**	1.8		V
V_{IH}	High Level Input Voltage Threshold (LM5100)			5.5	**8**	V
V_{IH}	High Level Input Voltage Threshold (LM5101)			1.8	**2.2**	V
V_{IHYS}	Input Voltage Hysteresis (LM5100)			0.5		V
R_I	Input Pulldown Resistance		**100**	200	**500**	kΩ
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		**6.0**	6.9	**7.4**	V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO .

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Units
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.6	**0.9**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.85	**1.1**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8	**1.5**	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.23	**0.4**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = −100 mA, V_{OHL} = V_{DD}–V_{LO}		0.35	**0.55**	V
I_{OHL}	Peak Pullup Current	V_{LO} = 0V		1.6		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12V		1.8		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.23	**0.4**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = −100 mA V_{OHH} = V_{HB}–V_{HO}		0.35	**0.55**	V
I_{OHH}	Peak Pullup Current	V_{HO} = 0V		1.6		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12V		1.8		A
THERMAL RESISTANCE						
θ_{JA}(2)	Junction to Ambient	SOIC-8		170		°C/W
		WSON-10(3)		40		

(2) The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.
(3) 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187 (SNOA401).

Switching Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Units
LM5100						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			24	**45**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			24	**45**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			24	**45**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			24	**45**	ns
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off			2	**10**	ns
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On			2	**10**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_R, t_F	Either Output Rise/Fall Time (3V to 9V)	C_L = 0.1 µF		0.6		µs
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

Switching Characteristics (continued)

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min (1)	Typ	Max (1)	Units
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns
LM5101						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			25	**56**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			25	**56**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			25	**56**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			25	**56**	ns
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off			2	**10**	ns
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On			2	**10**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_R, t_F	Either Output Rise/Fall Time (3V to 9V)	C_L = 0.1 µF		0.6		µs
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns

Typical Performance Characteristics

LM5100 I_{DD} vs Frequency

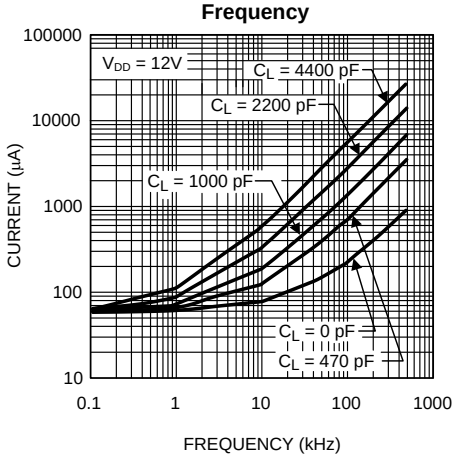


Figure 1.

LM5101 I_{DD} vs Frequency

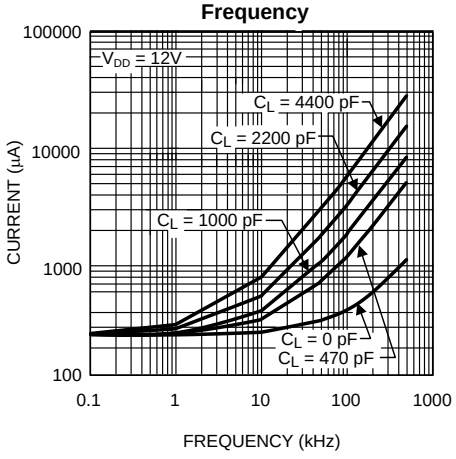


Figure 2.

LM5100/LM5101 Operating Current vs Temperature

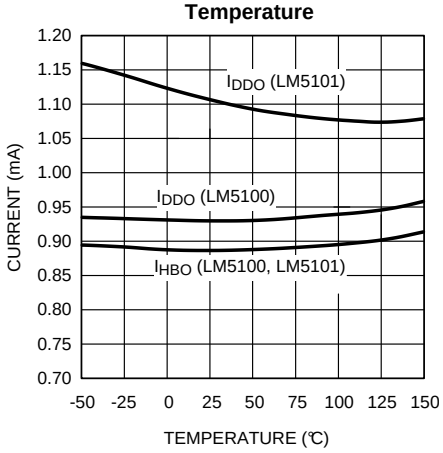


Figure 3.

IHB vs Frequency

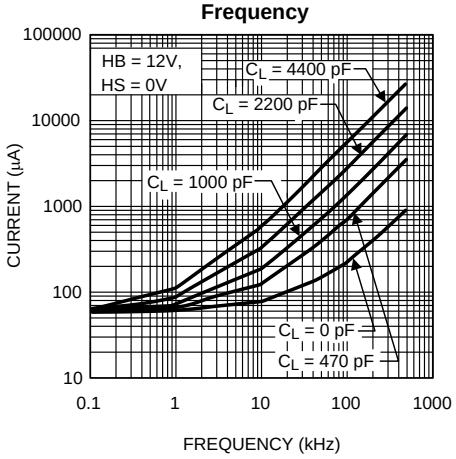


Figure 4.

Quiescent Current vs Supply Voltage

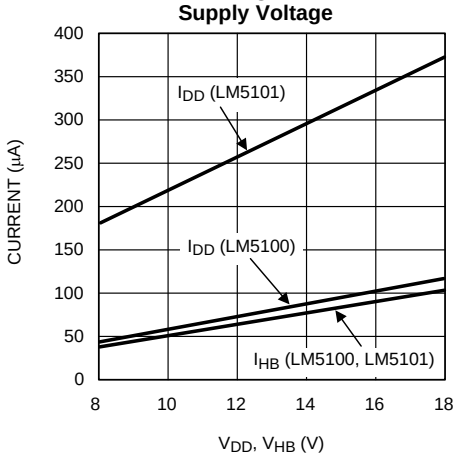


Figure 5.

LM5100/LM5101 Quiescent Current vs Temperature

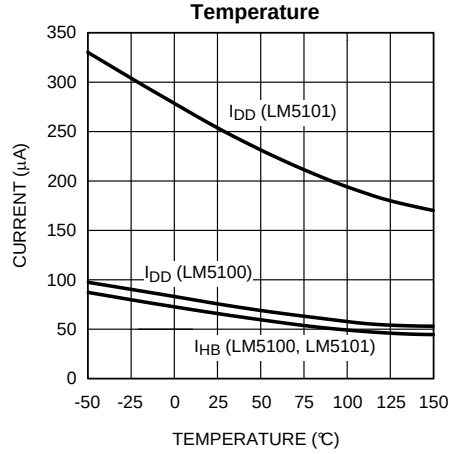


Figure 6.

Typical Performance Characteristics (continued)

Undervoltage Rising Thresholds vs Temperature

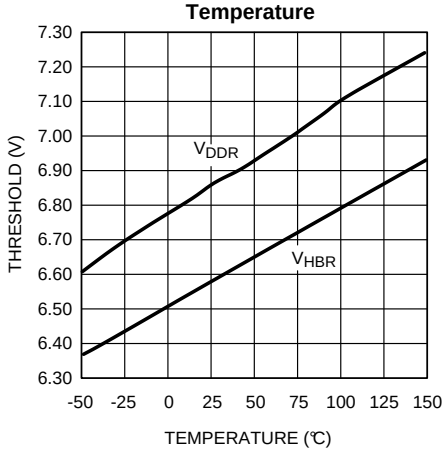


Figure 7.

LM5100 Undervoltage Threshold Hysteresis vs Temperature

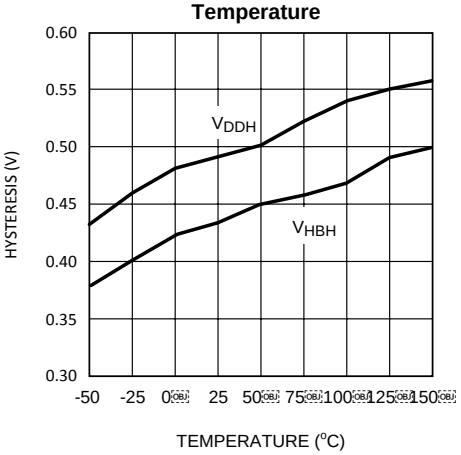


Figure 8.

Bootstrap Diode Forward Voltage

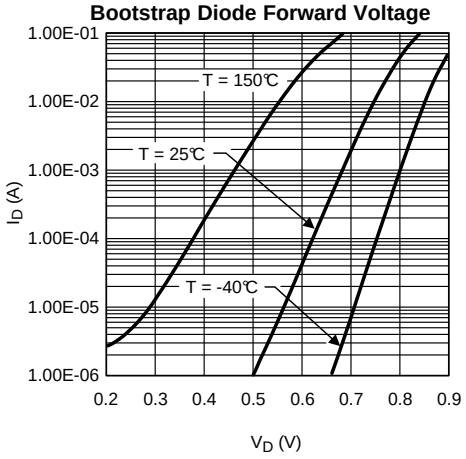


Figure 9.

HO and LO Peak Output Current vs Output Voltage

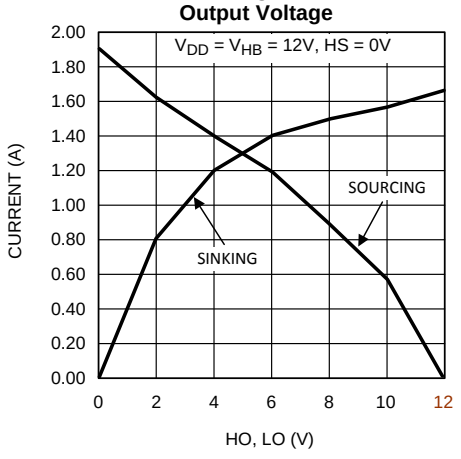


Figure 10.

LO and HO Gate Drive—High Level Output Voltage vs Temperature

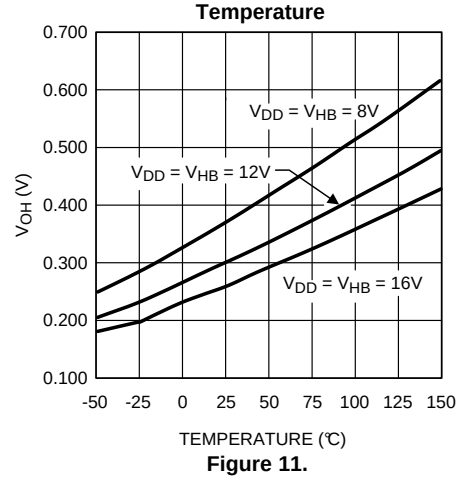


Figure 11.

LO and HO Gate Drive—Low Level Output Voltage vs Temperature

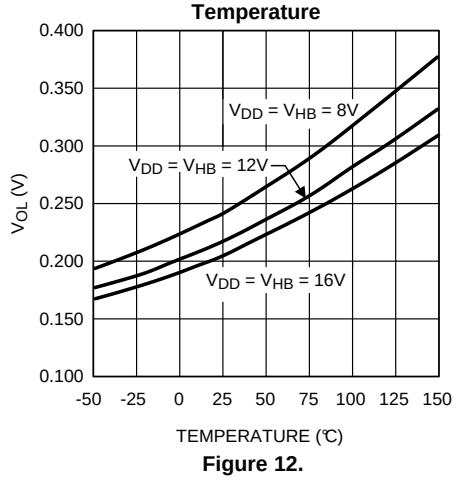


Figure 12.

Typical Performance Characteristics (continued)

LM5100 Propagation Delay vs Temperature

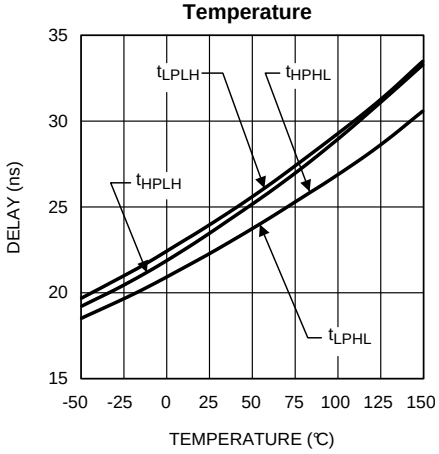


Figure 13.

LM5101 Propagation Delay vs Temperature

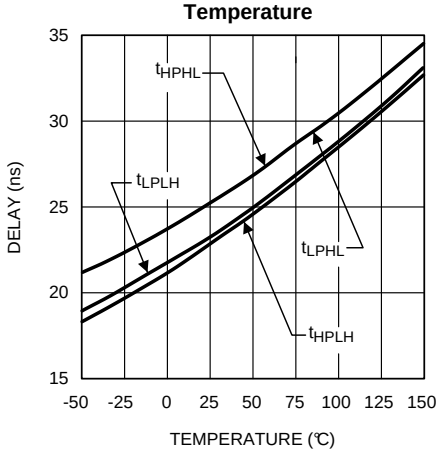


Figure 14.

Timing Diagram

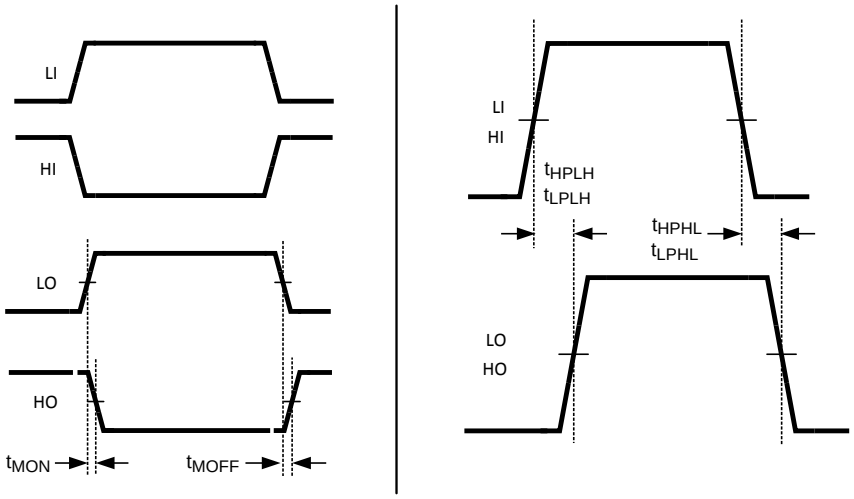


Figure 15.

LAYOUT CONSIDERATIONS

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR / ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
   - a) The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   - b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

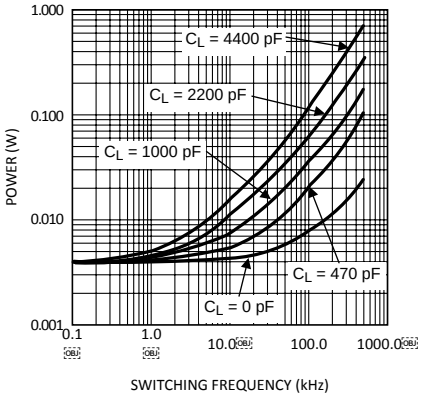


Figure 16. Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12V, Neglecting Diode Losses

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

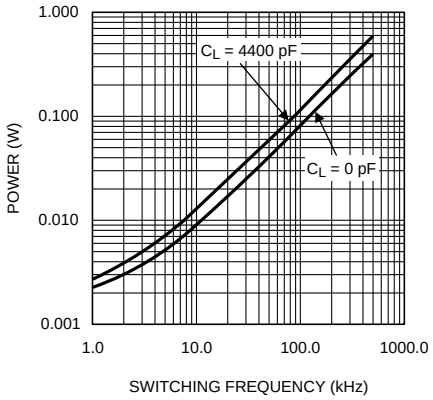


Figure 17. Diode Power Dissipation V_{IN} = 80V

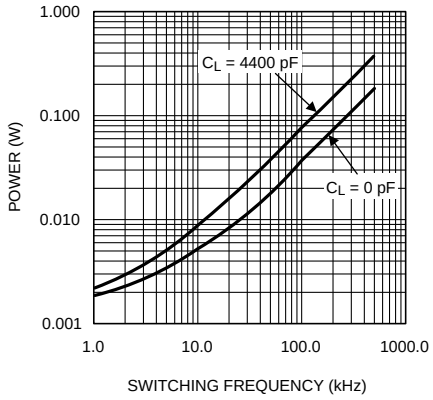


Figure 18. Diode Power Dissipation V_{IN} = 40V

The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel (refer to Figure 19) with the internal bootstrap diode can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

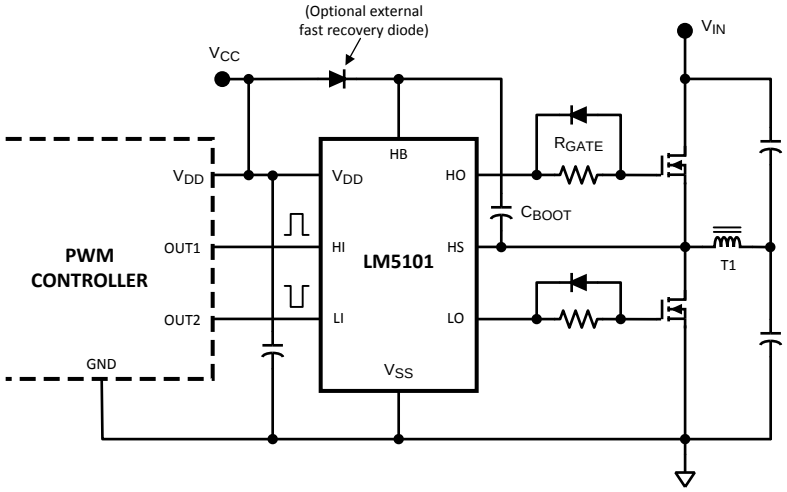


Figure 19. LM5101 Driving MOSFETs Connected in Half-Bridge Configuration

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5101M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-	5101 M
LM5101M/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See LM5101M/NOPB	5101 M
LM5101M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	See LM5101M/NOPB	5101 M
LM5101MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-	5101 M
LM5101MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See LM5101MX/NOPB	5101 M
LM5101MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See LM5101MX/NOPB	5101 M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

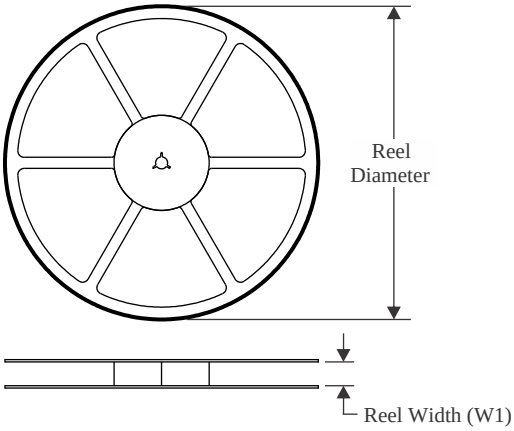
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

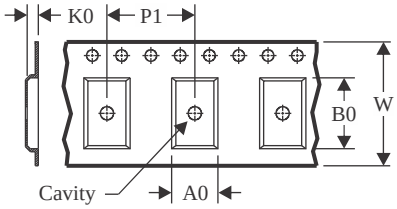
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

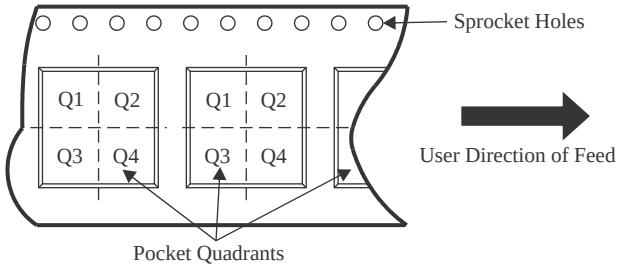


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

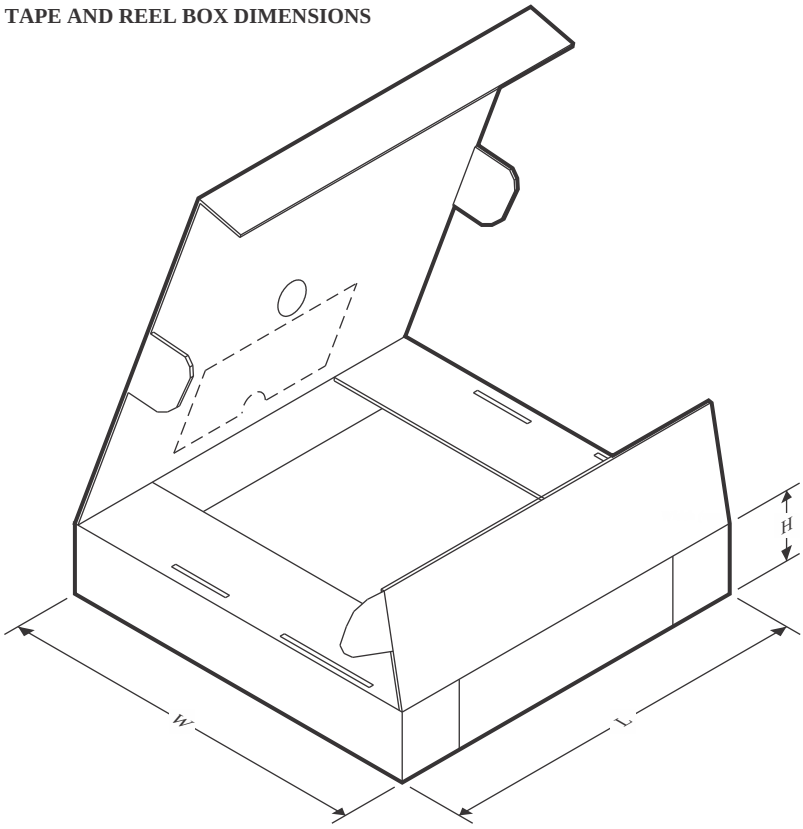
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5101MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

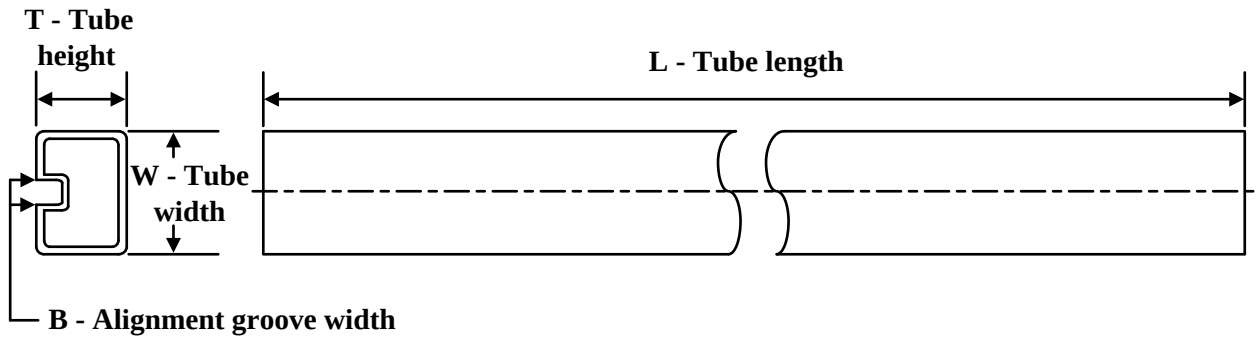
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

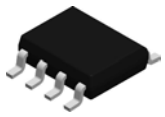
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5101MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5101M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5101M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM5101M/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

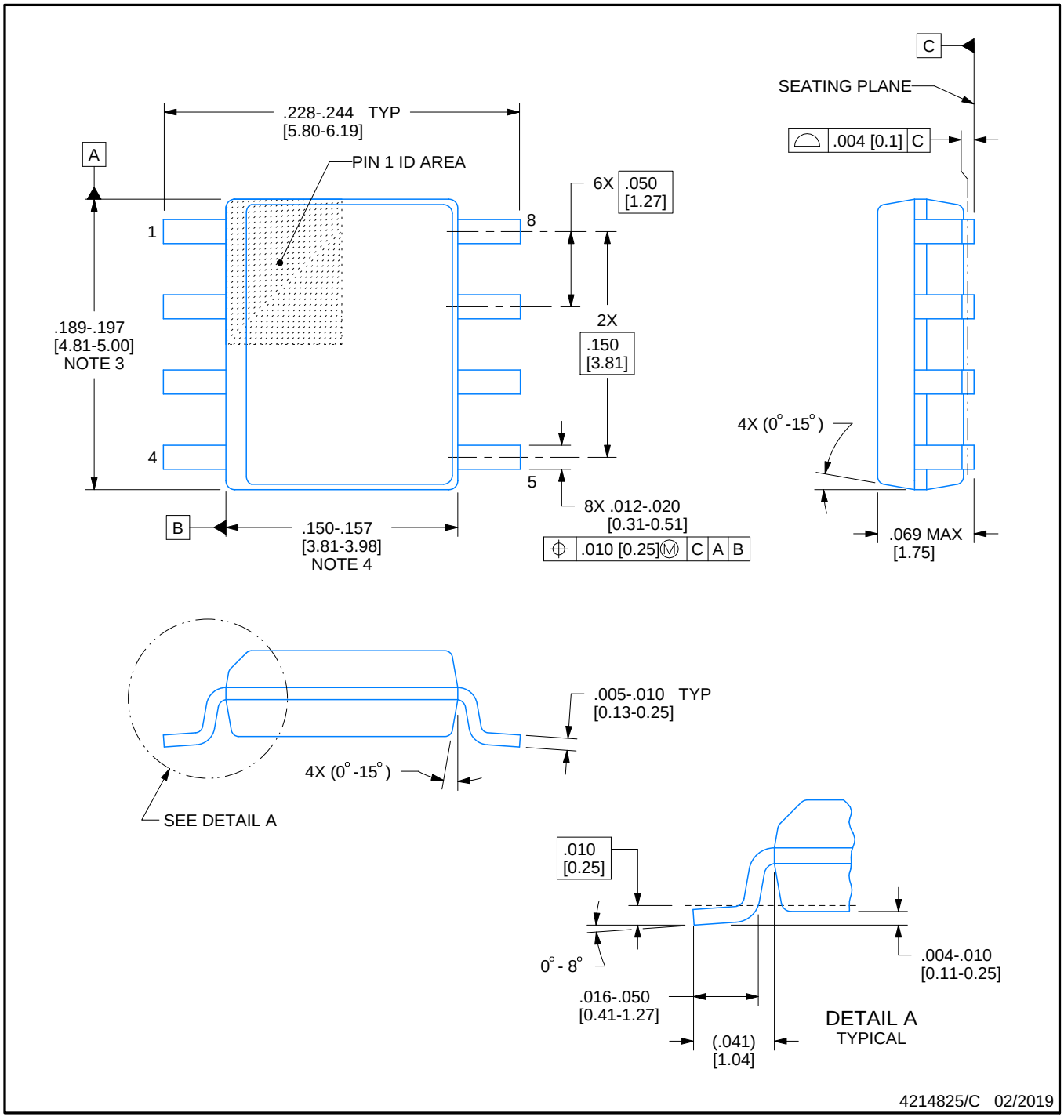


PACKAGE OUTLINE

D0008A

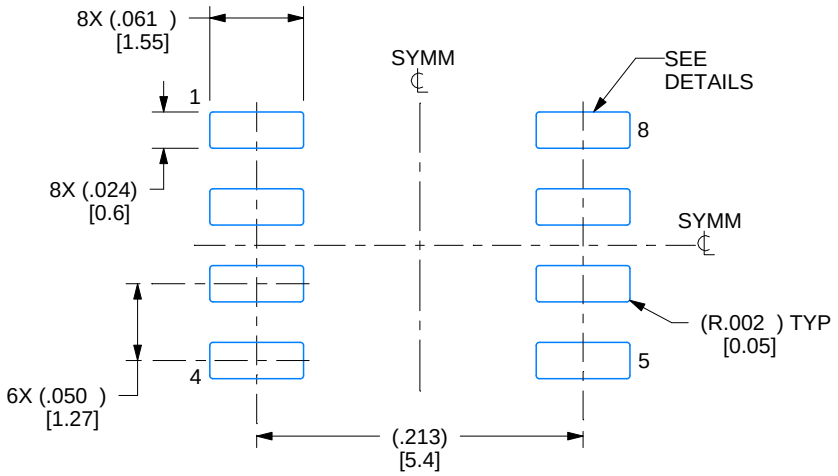
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

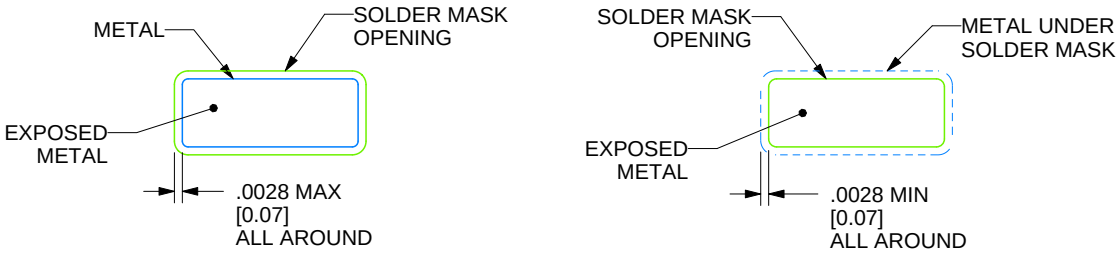


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

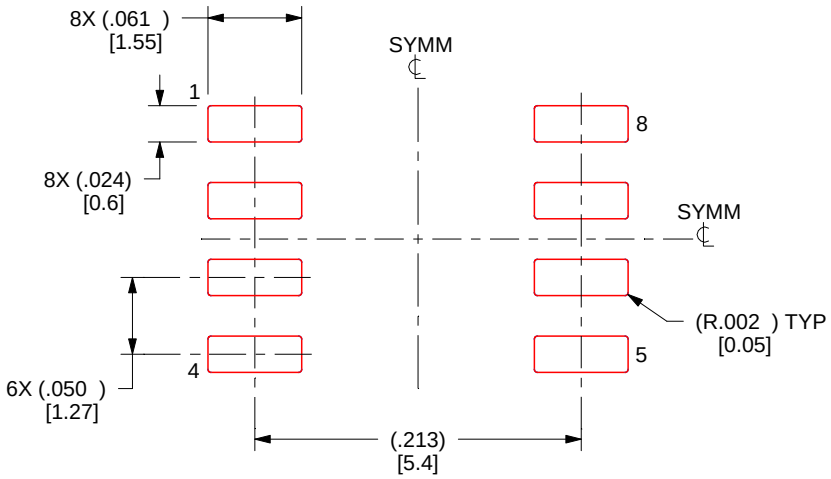
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265