LM118-N/lm218-N/LM318-N Operational Amplifiers

Check for Samples: LM118-N, LM218-N, LM318-N

FEATURES

- **15 MHz Small Signal Bandwidth**
- **Ensured 50V/μs Slew Rate**
- **Maximum Bias Current of 250 nA**
- **Operates from Supplies of ±5V to ±20V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protected**
- **Pin Compatible with General Purpose Op Amps**

DESCRIPTION

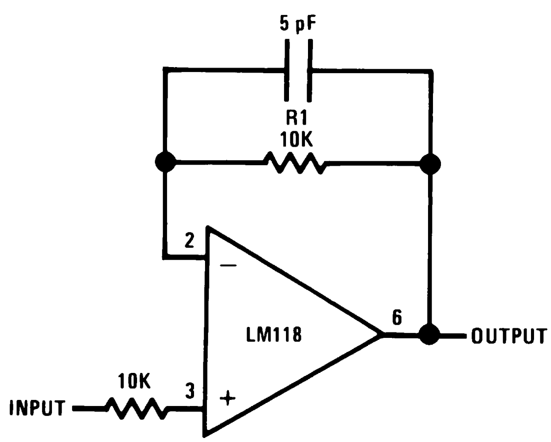
The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM218-N is identical to the LM118 except that the LM218-N has its performance specified over a −25°C to +85°C temperature range. The LM318-N is specified from 0°C to +70°C.

Fast Voltage Follower



Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage	±20V
Power Dissipation [3]	500 mW
Differential Input Current [4]	±10 mA
Input Voltage [5]	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
lm118-n	−55°C to +125°C
LM218-N	−25°C to +85°C
LM318-N	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-99 Package	300°C
PDIP Package	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
SOIC Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Tolerance [6]	2000V

(1) Refer to RETS118X for LM118H and LM118J military specifications.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum junction temperature of the lm118-n is 150°C, the LM218-N is 110°C, and the LM318-N is 110°C. For operating at elevated temperatures, devices in the LMC package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
(4) The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
(5) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(6) Human body model, 1.5 kΩ in series with 100 pF.

Electrical Characteristics [1]

Parameter	Conditions	LM118-N/LM218-N			LM318-N			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C		2	4		4	10	mV
Input Offset Current	T_A = 25°C		6	50		30	200	nA
Input Bias Current	T_A = 25°C		120	250		150	500	nA
Input Resistance	T_A = 25°C	1	3		0.5	3		MΩ
Supply Current	T_A = 25°C		5	8		5	10	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, R_L ≥ 2 kΩ	50	200		25	200		V/mV
Slew Rate	T_A = 25°C, V_S = ±15V, A_V = 1 [2]	50	70		50	70		V/μs
Small Signal Bandwidth	T_A = 25°C, V_S = ±15V		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA

(1) These specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C (lm118-n), −25°C ≤ T_A ≤ +85°C (LM218-N), and 0°C ≤ T_A ≤ +70°C (LM318-N). Also, power supplies must be bypassed with 0.1 μF disc capacitors.
(2) Slew rate is tested with V_S = ±15V. The lm118-n is in a unity-gain non-inverting configuration. V_{IN} is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and specified to exceed 50V/μs.

Electrical Characteristics [1] (continued)

Parameter	Conditions	LM118-N/LM218-N			LM318-N			Units
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current				500			750	nA
Supply Current	T_A = 125°C		4.5	7				mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L ≥ 2 kΩ	25			20			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 2 kΩ	±12	±13		±12	±13		V
Input Voltage Range	V_S = ±15V	±11.5			±11.5			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

TYPICAL PERFORMANCE CHARACTERISTICS

LM118-N, LM218-N

Input Current

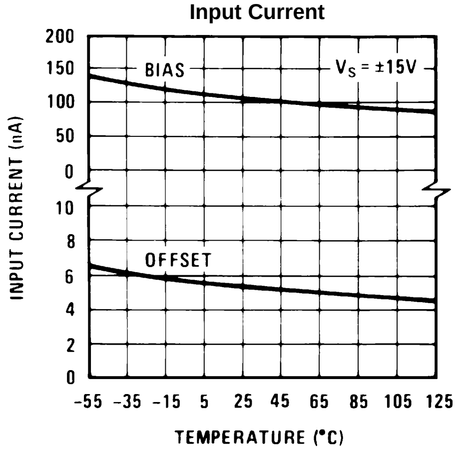


Figure 1.

Voltage Gain

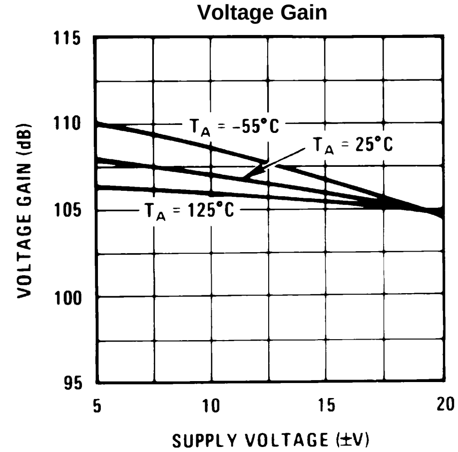


Figure 2.

Power Supply Rejection

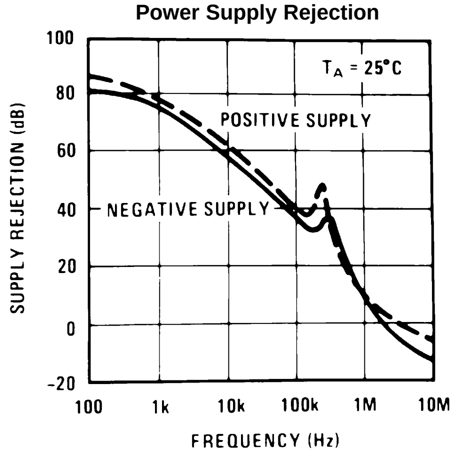


Figure 3.

Input Noise Voltage

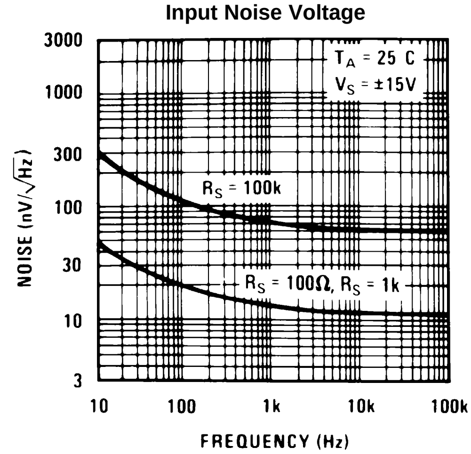


Figure 4.

Common Mode Rejection

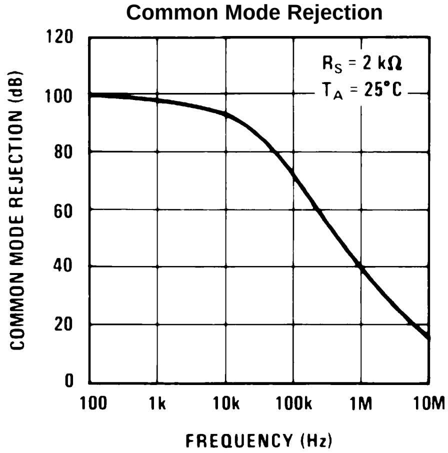


Figure 5.

Supply Current

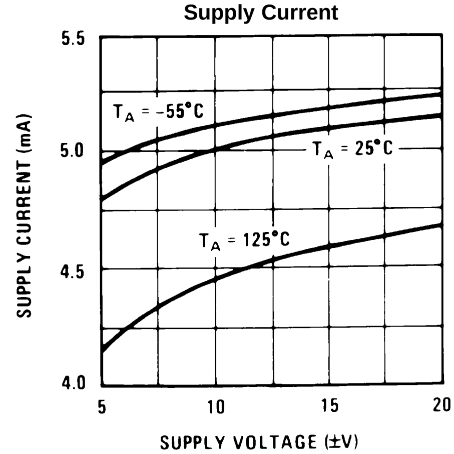


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

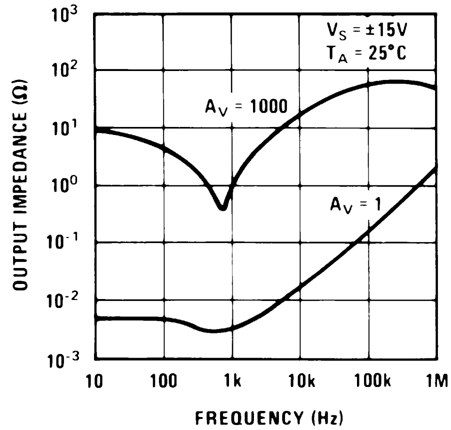


Figure 7.

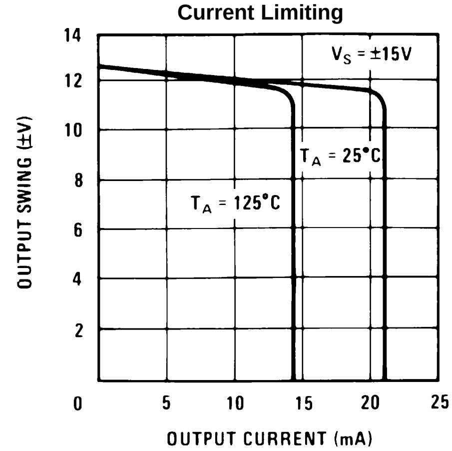


Figure 8.

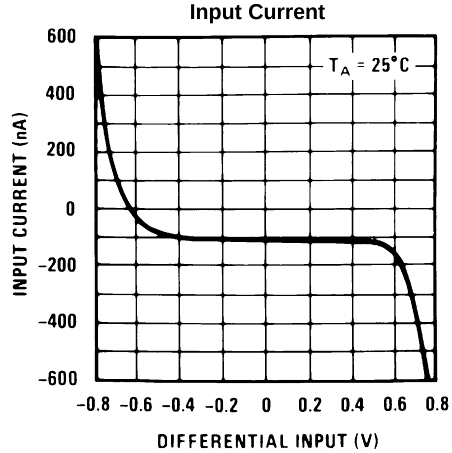


Figure 9.

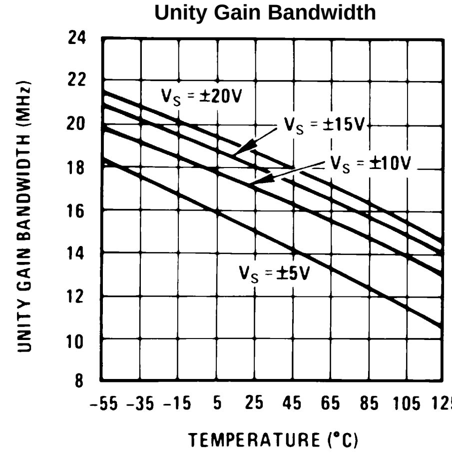


Figure 10.

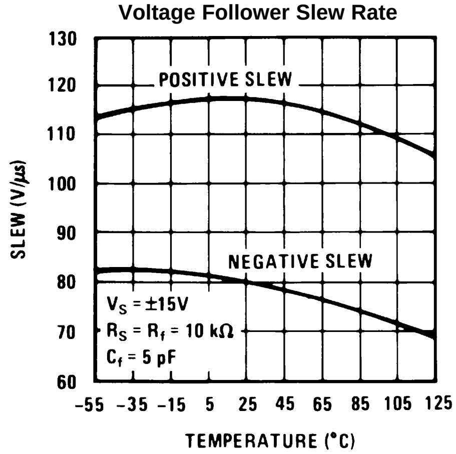


Figure 11.

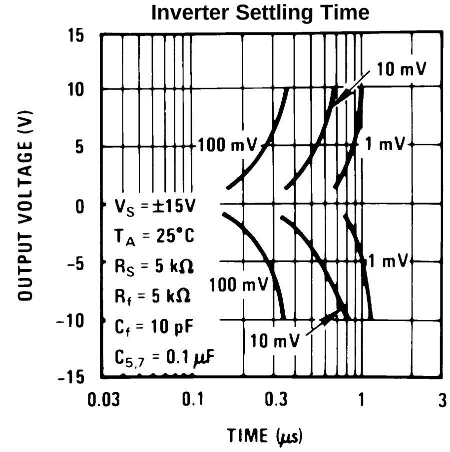


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

Large Signal Frequency Response

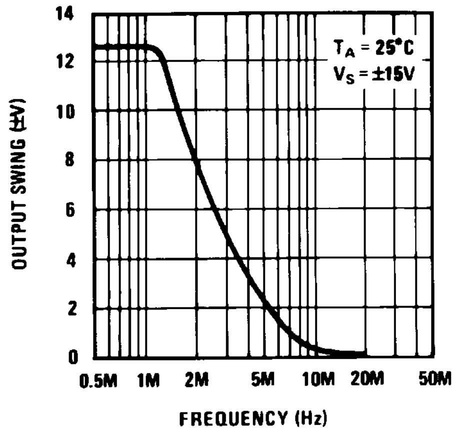


Figure 13.

Open Loop Frequency Response

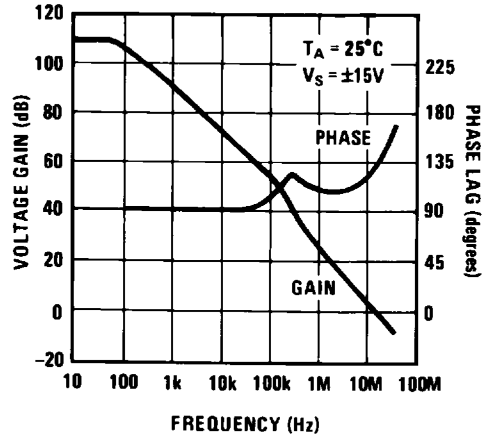


Figure 14.

Voltage Follower Pulse Response

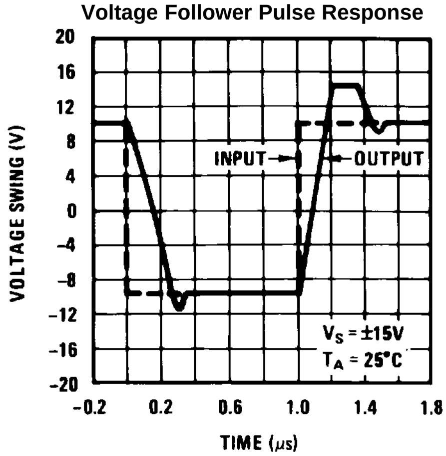


Figure 15.

Large Signal Frequency Response

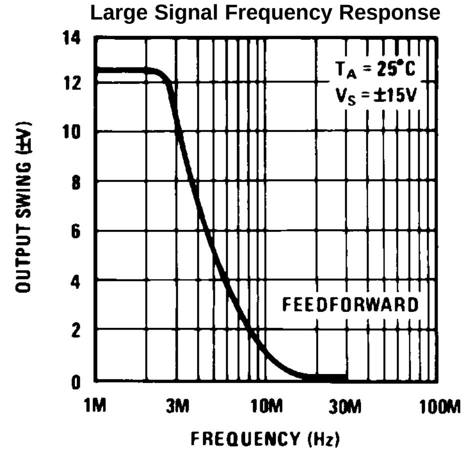


Figure 16.

Open Loop Frequency Response

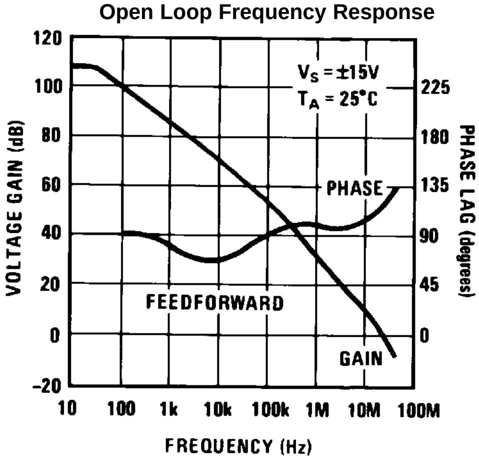


Figure 17.

Inverter Pulse Response

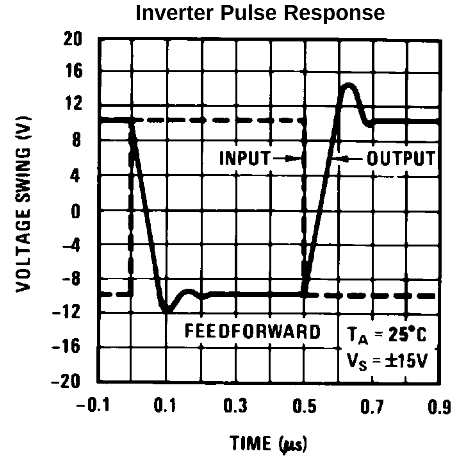


Figure 18.

Typical Performance Characteristics

LM318-N

Input Current

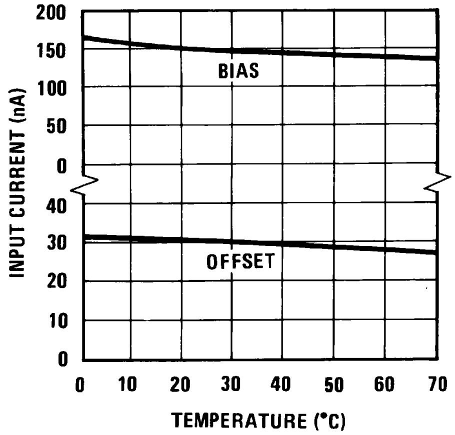


Figure 19.

Voltage Gain

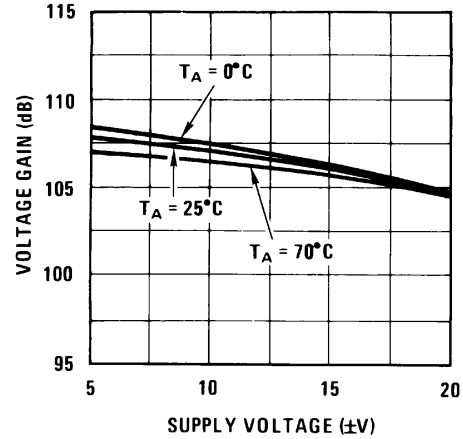


Figure 20.

Power Supply Rejection

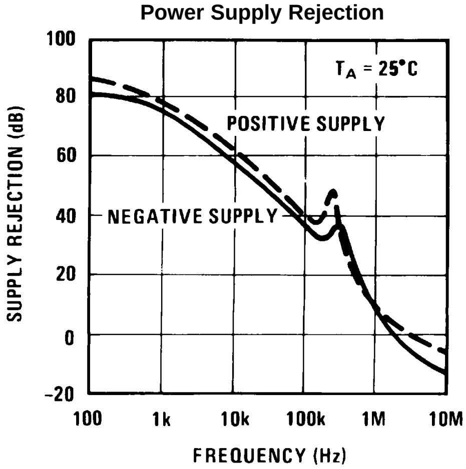


Figure 21.

Input Noise Voltage

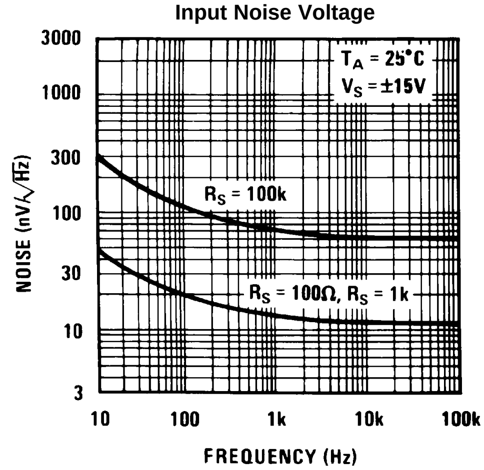


Figure 22.

Common Mode Rejection

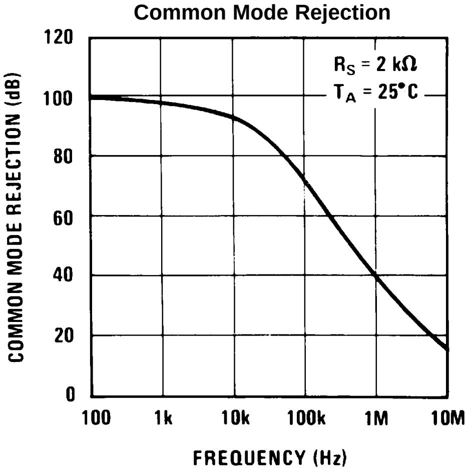


Figure 23.

Supply Current

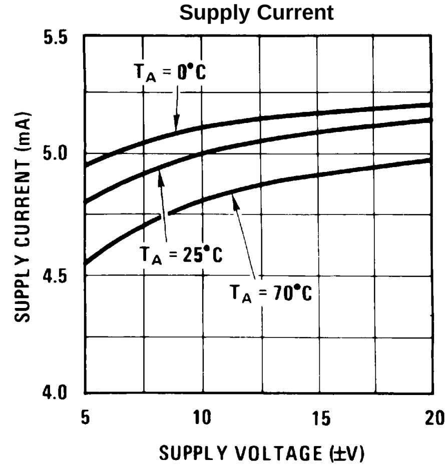


Figure 24.

Typical Performance Characteristics (continued)

LM318-N

Closed Loop Output Impedance

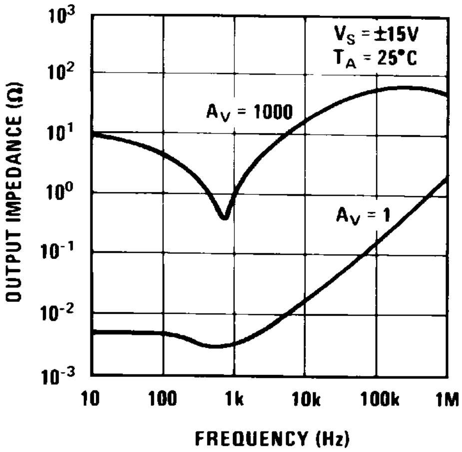


Figure 25.

Current Limiting

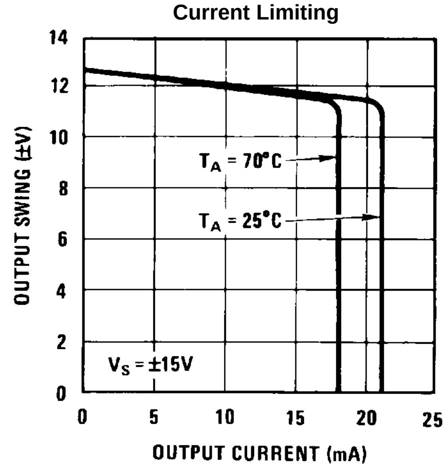


Figure 26.

Input Current

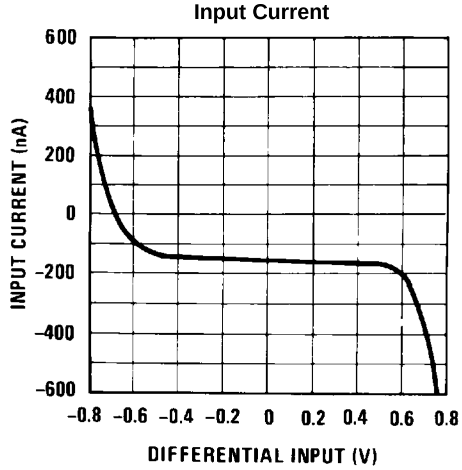


Figure 27.

Unity Gain Bandwidth

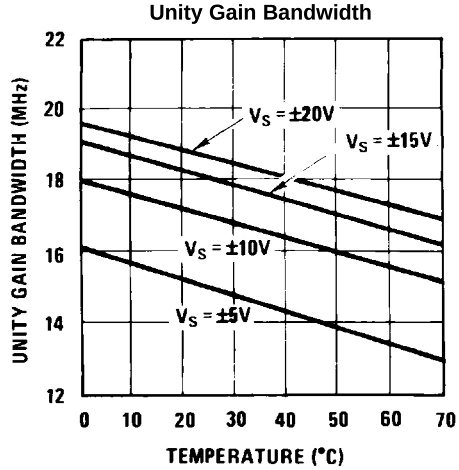


Figure 28.

Voltage Follower Slew Rate

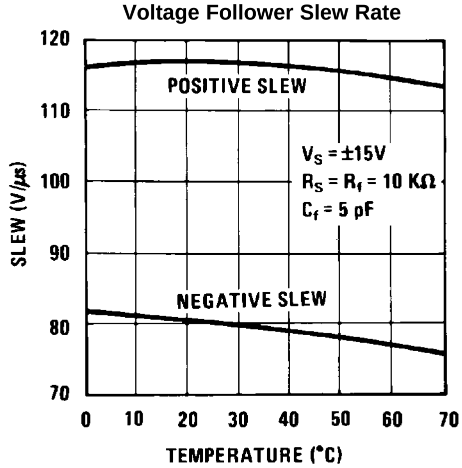


Figure 29.

Inverter Settling Time

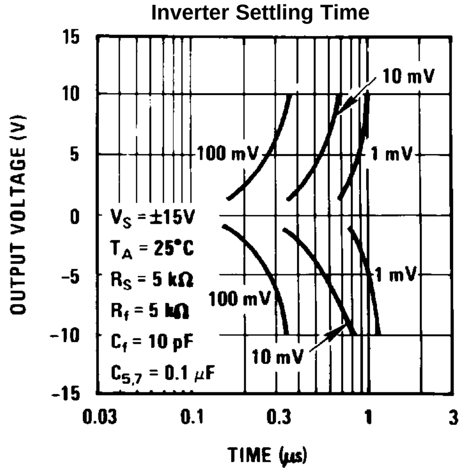


Figure 30.

Typical Performance Characteristics (continued)

LM318-N

Large Signal Frequency Response

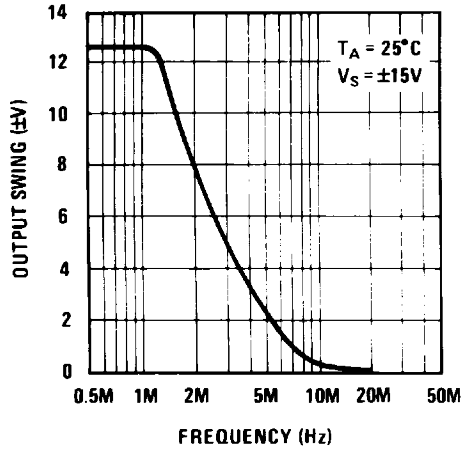


Figure 31.

Open Loop Frequency Response

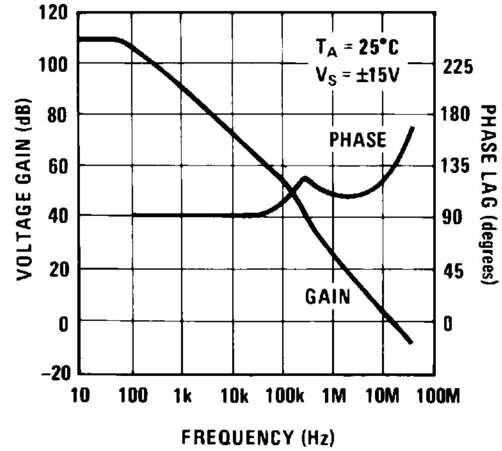


Figure 32.

Voltage Follower Pulse Response

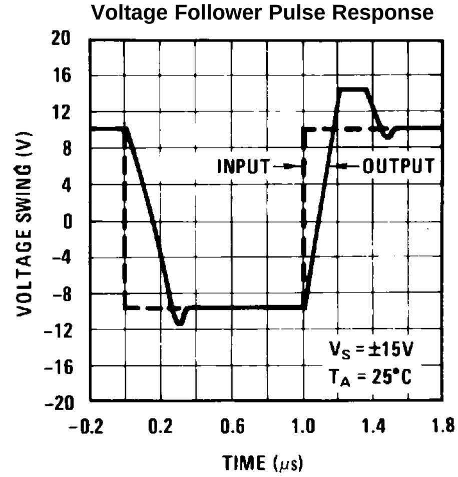


Figure 33.

Large Signal Frequency Response

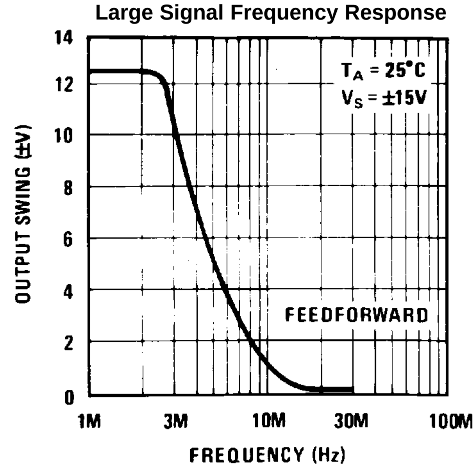


Figure 34.

Open Loop Frequency Response

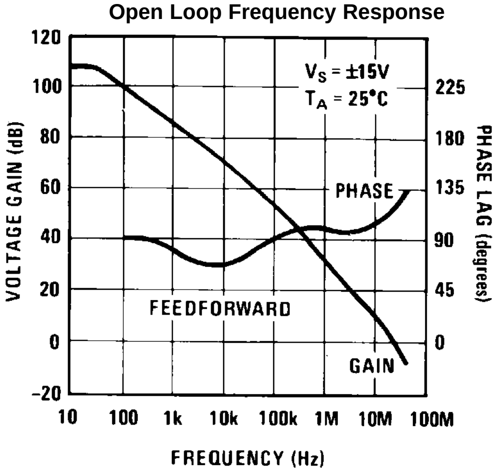


Figure 35.

Inverter Pulse Response

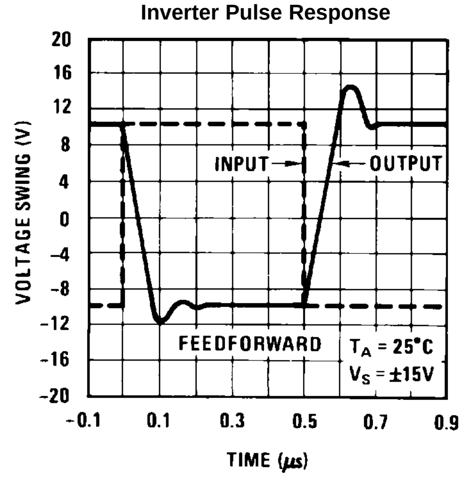
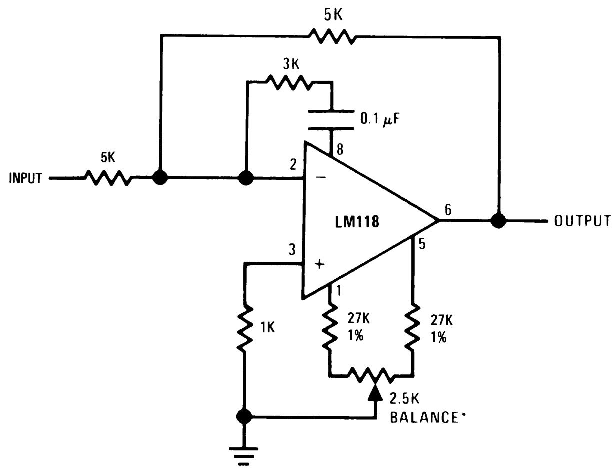


Figure 36.

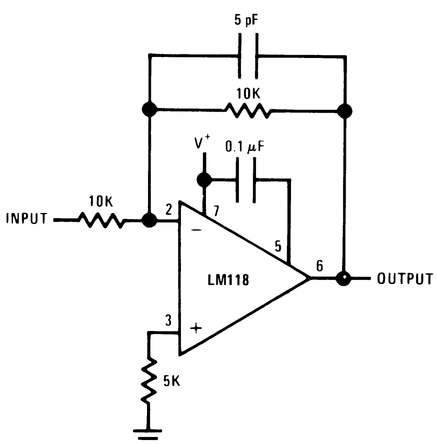
AUXILIARY CIRCUITS



*Balance circuit necessary for increased slew.

Slew rate typically 150V/μs.

Figure 37. Feedforward Compensation for Greater Inverting Slew Rate



Slew and settling time to 0.1% for a 10V step change is 800 ns.

Figure 38. Compensation for Minimum Settling Time

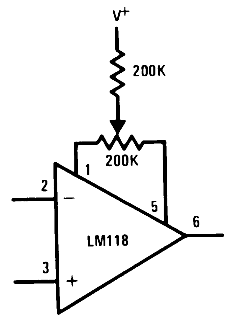


Figure 39. Offset Balancing

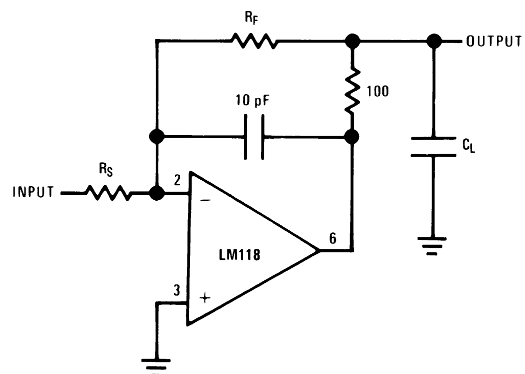


Figure 40. Isolating Large Capacitive Loads

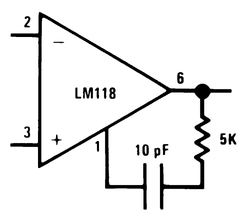
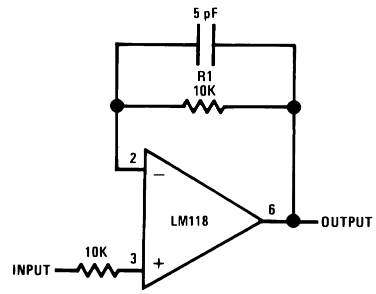


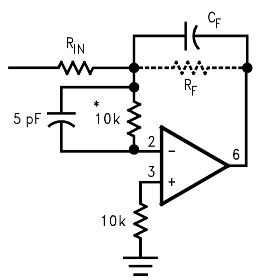
Figure 41. Overcompensation

TYPICAL APPLICATIONS



Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Figure 42. Fast Voltage Follower



C_F = Large
(C_F ≥ 50 pF)
*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Figure 43.

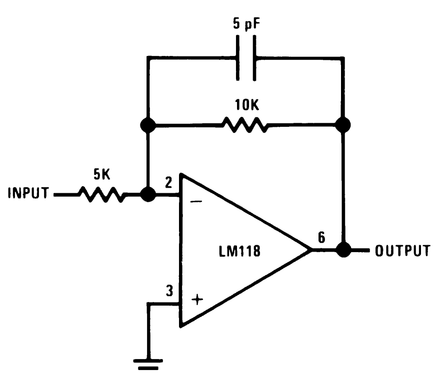


Figure 44. Fast Summing Amplifier

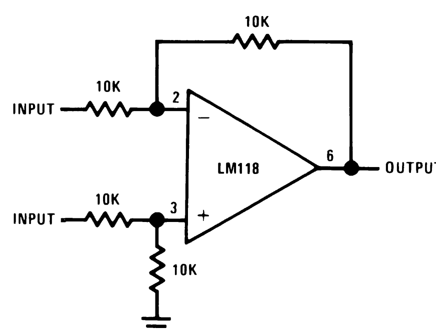


Figure 45. Differential Amplifie

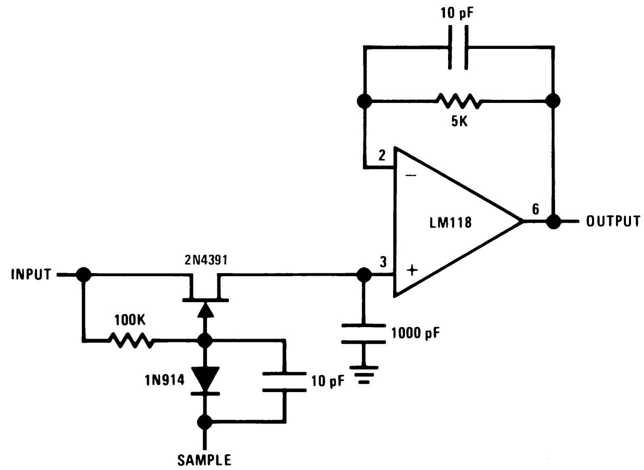
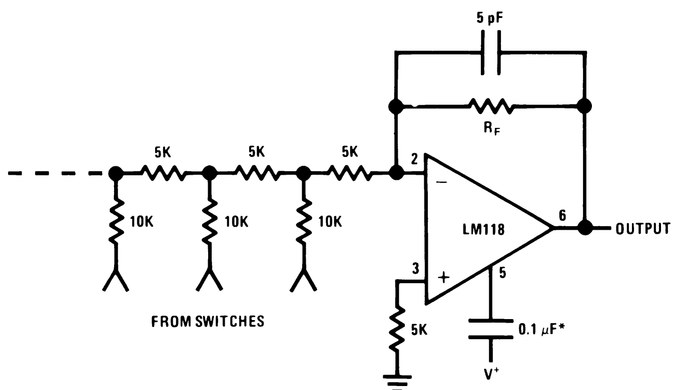
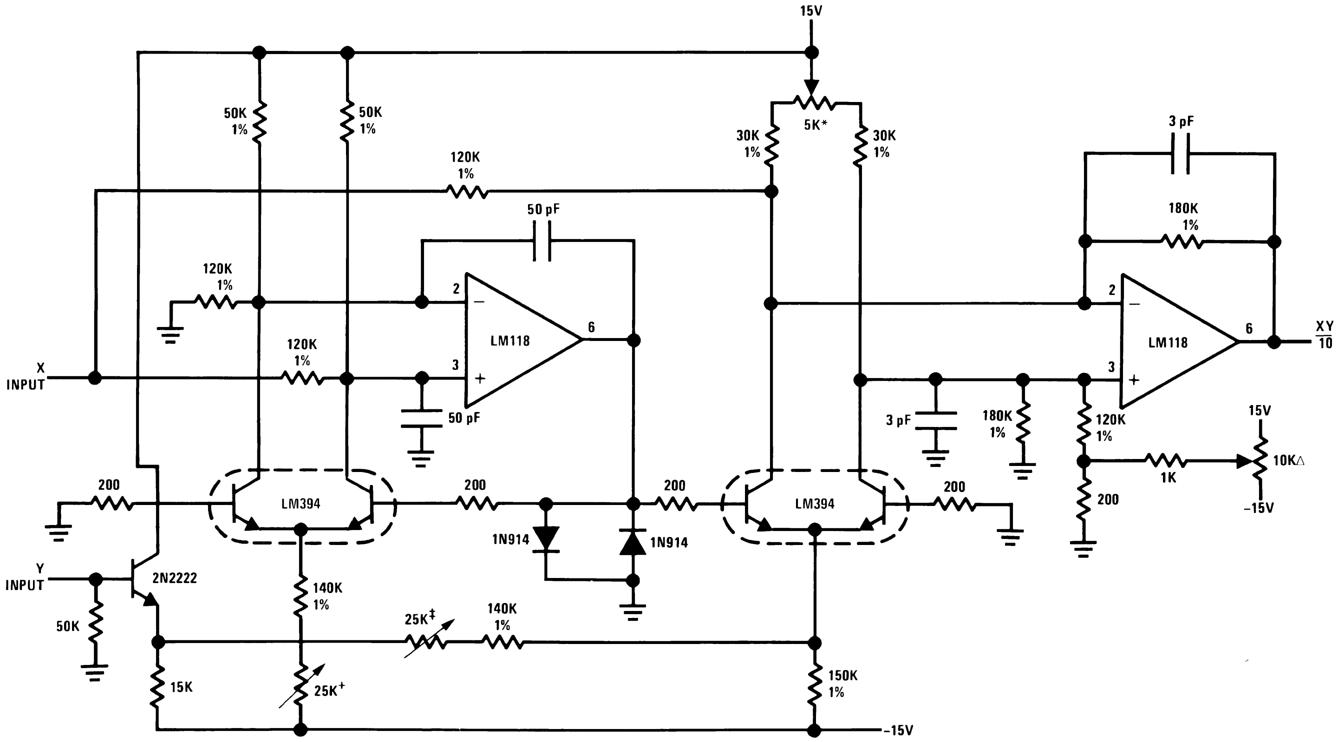


Figure 46. Fast Sample and Hold



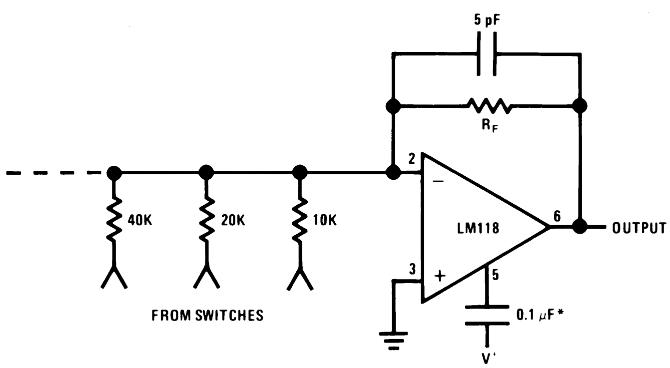
*Optional—Reduces settling time.

Figure 47. D/A Converter Using Ladder Network



ΔOutput zero.
*"Y" zero
+"X" zero
‡Full scale adjust.

Figure 48. Four Quadrant Multiplier



*Optional—Reduces settling time.

Figure 49. D/A Converter Using Binary Weighted Network

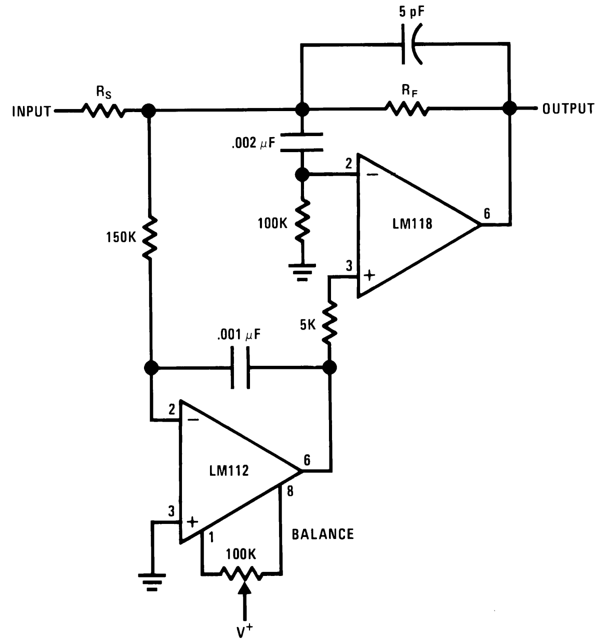


Figure 50. Fast Summing Amplifier with Low Input Current

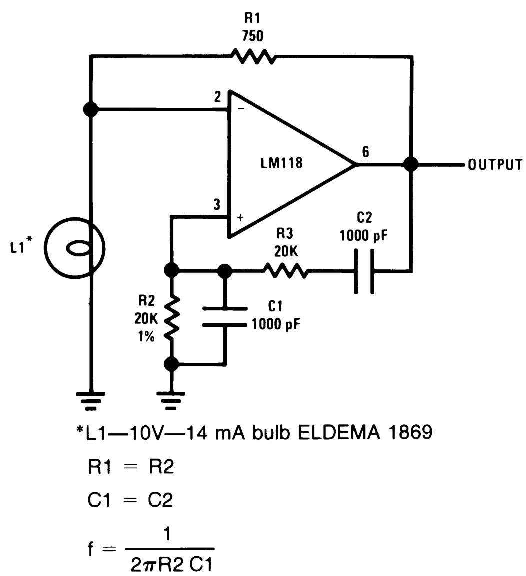


Figure 51. Wein Bridge Sine Wave Oscillator

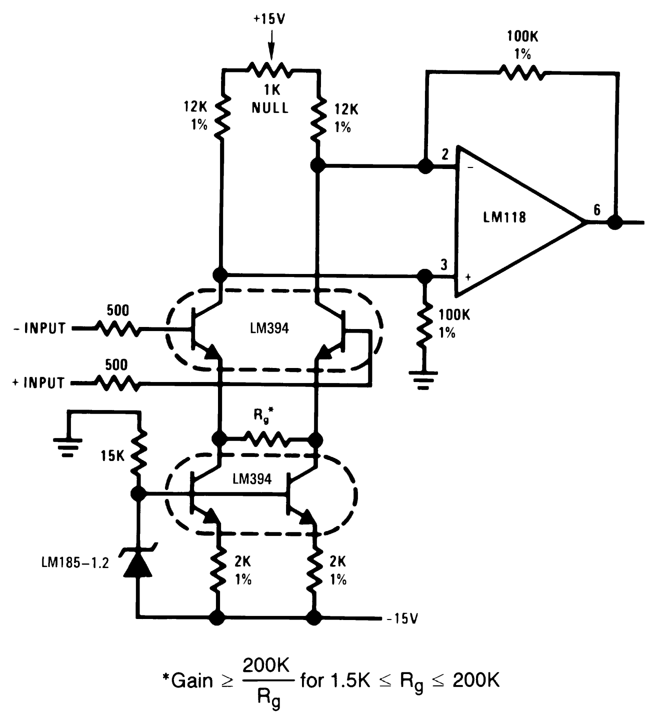
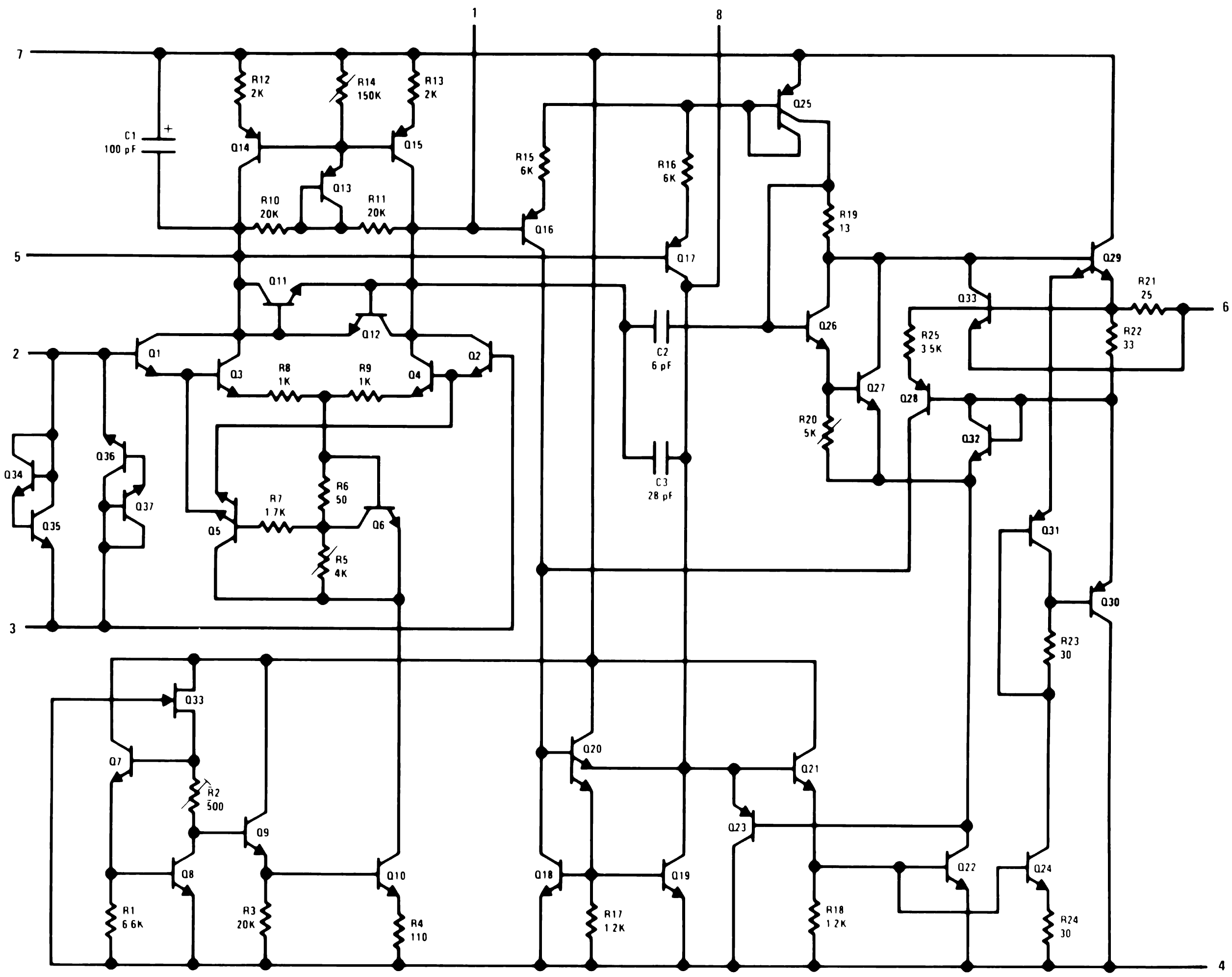
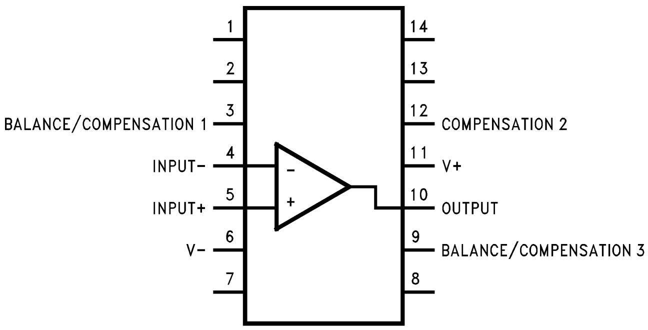


Figure 52. Instrumentation Amplifier

Schematic Diagram

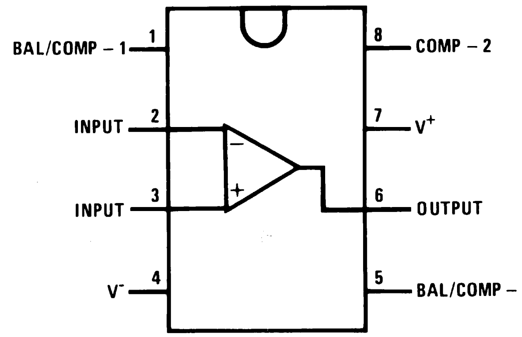


Pin Diagram



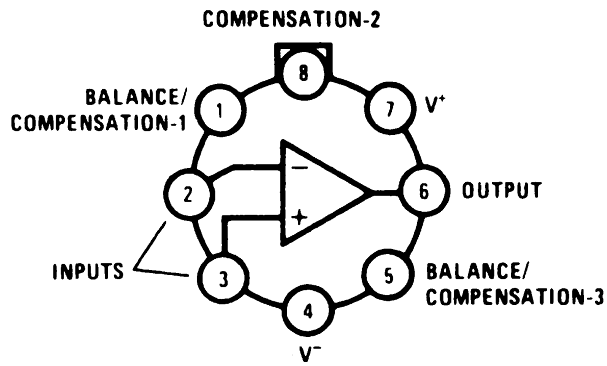
Available per JM38510/10107.

Dual-In-Line Package
(Top View)
See Package Number J (R-GDIP-T14)



Available per JM38510/10107.

Dual-In-Line Package
(Top View)
See Package Number NAB008A, D (R-PDSO-G8), or P (R-PDIP-T8)



Pin connections shown on schematic diagram and typical applications are for TO-99 package.

TO-99 Package
(Top View)
See Package Number LMC (O-MBCY-W8)

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM118H	Active	Production	TO-99 (LMC) | 8	500 | OTHER	No	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM118H, LM118H)
LM118H/NOPB	Active	Production	TO-99 (LMC) | 8	500 | TRAY NON-STD	Yes	SNAGCU	Level-1-NA-UNLIM	-55 to 125	(LM118H, LM118H)
LM318M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 318M
LM318M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 318M
LM318MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 318M
LM318MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 318M
LM318N/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 318N
LM318N/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 318N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

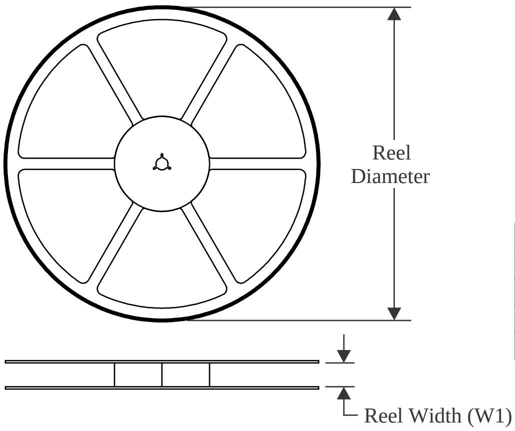
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

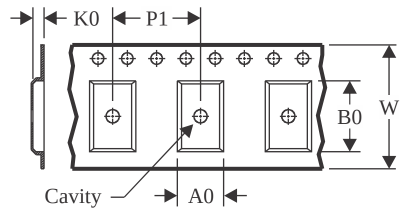
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

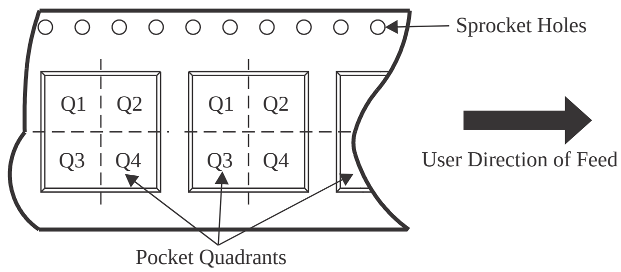


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

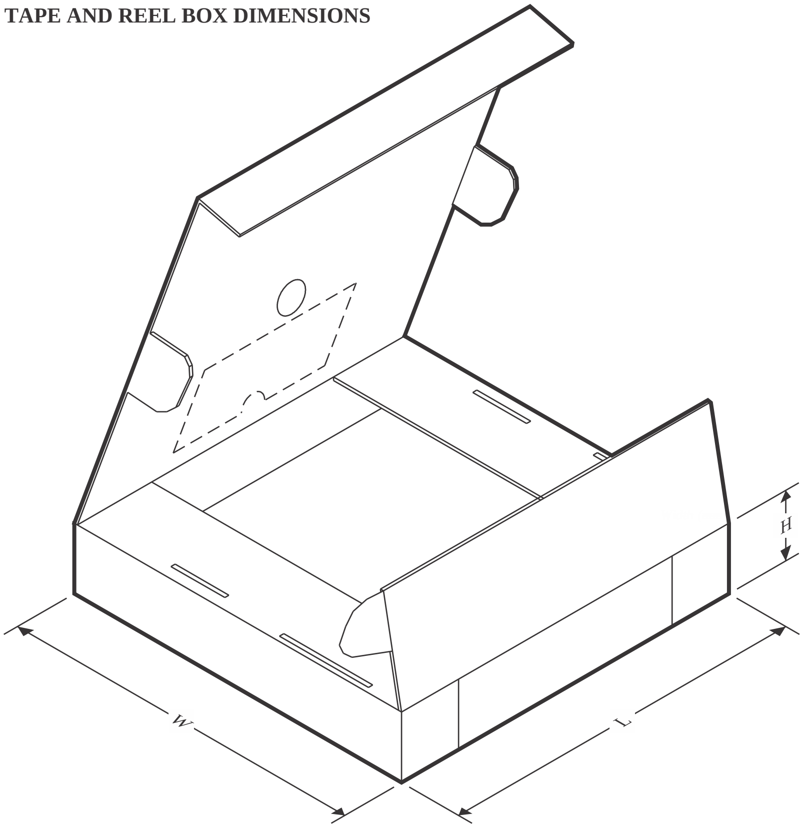
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM318MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

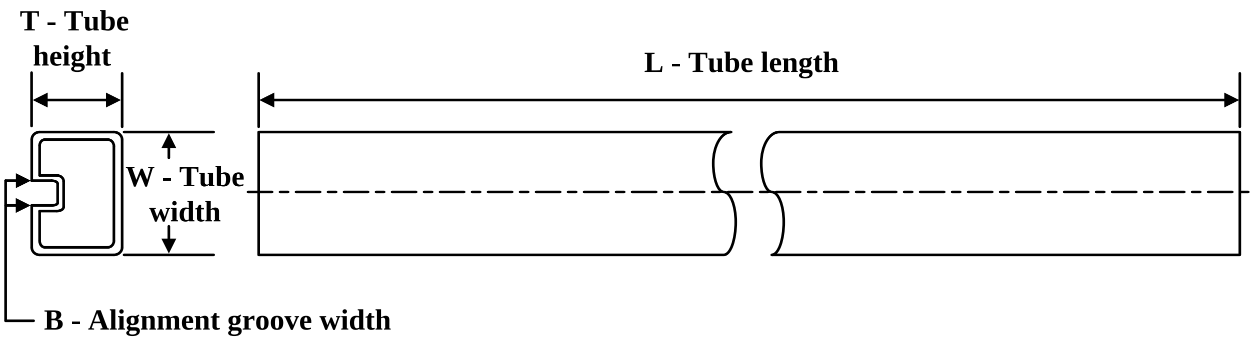
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

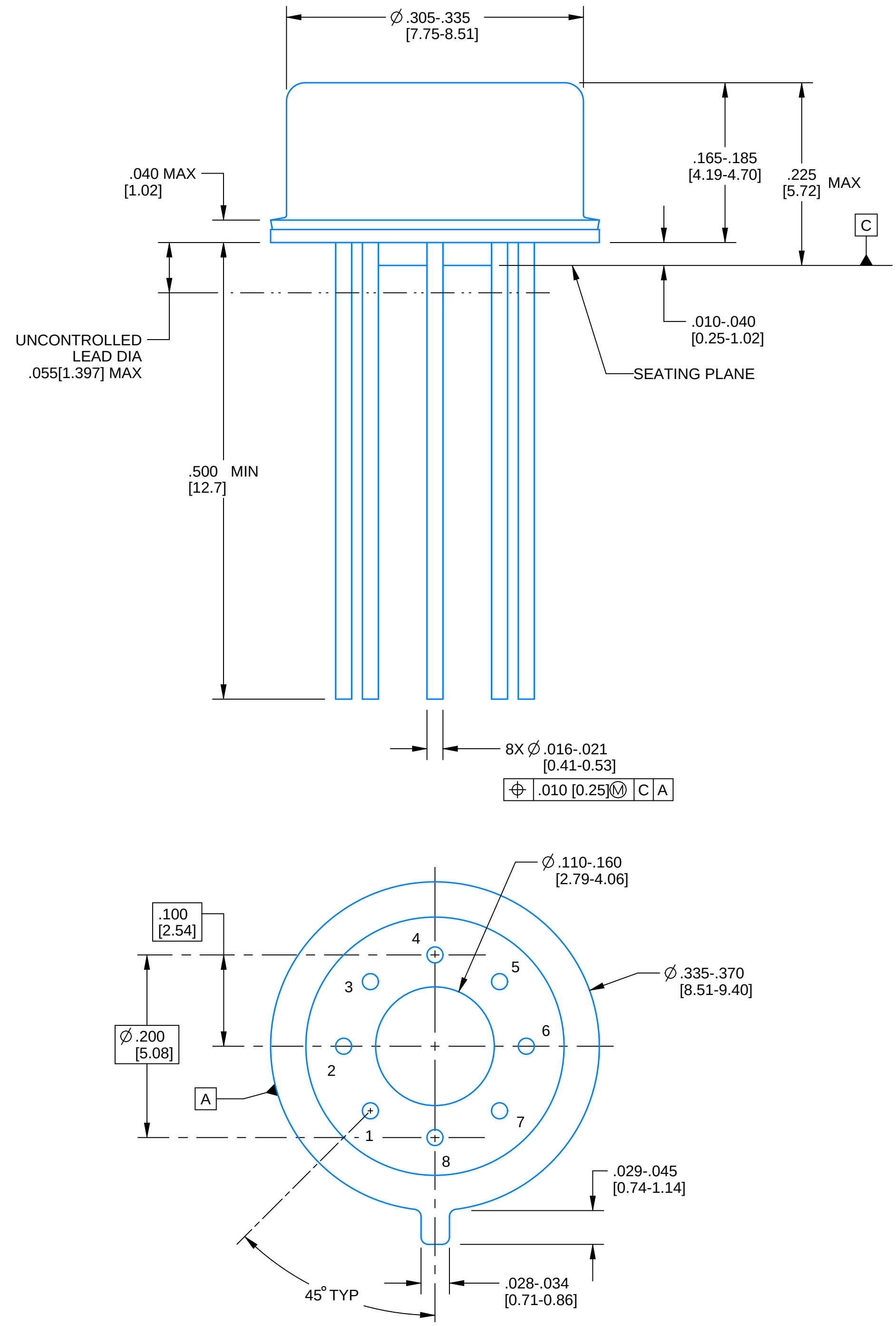
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM318MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

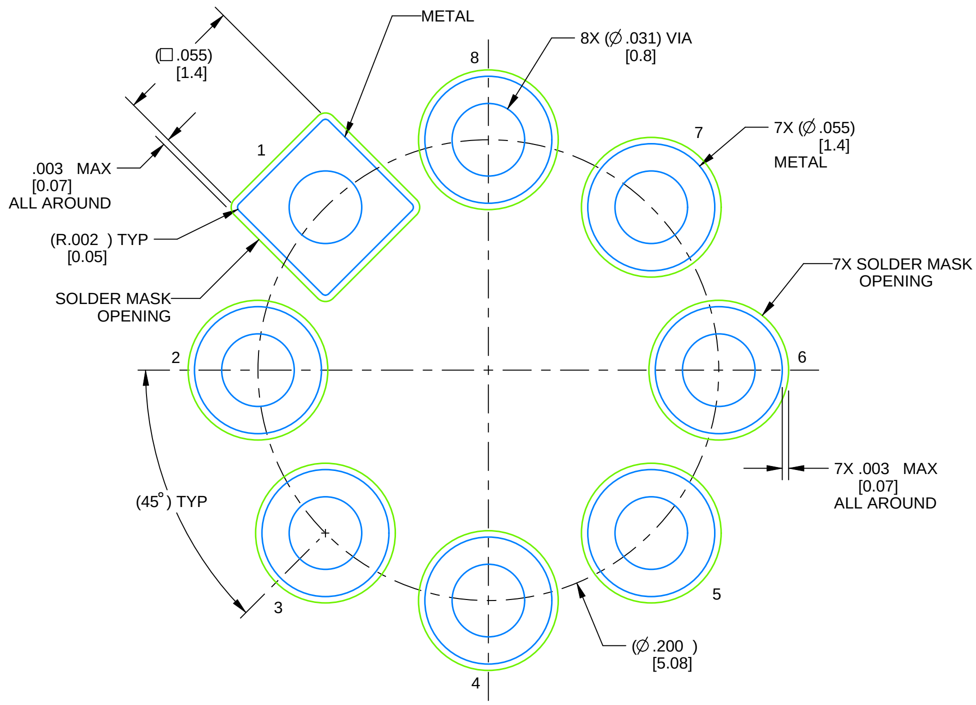
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM318M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM318M/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM318N/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM318N/NOPB.B	P	PDIP	8	40	502	14	11938	4.32



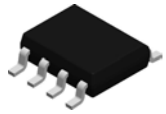
4220610/B 09/2024

NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

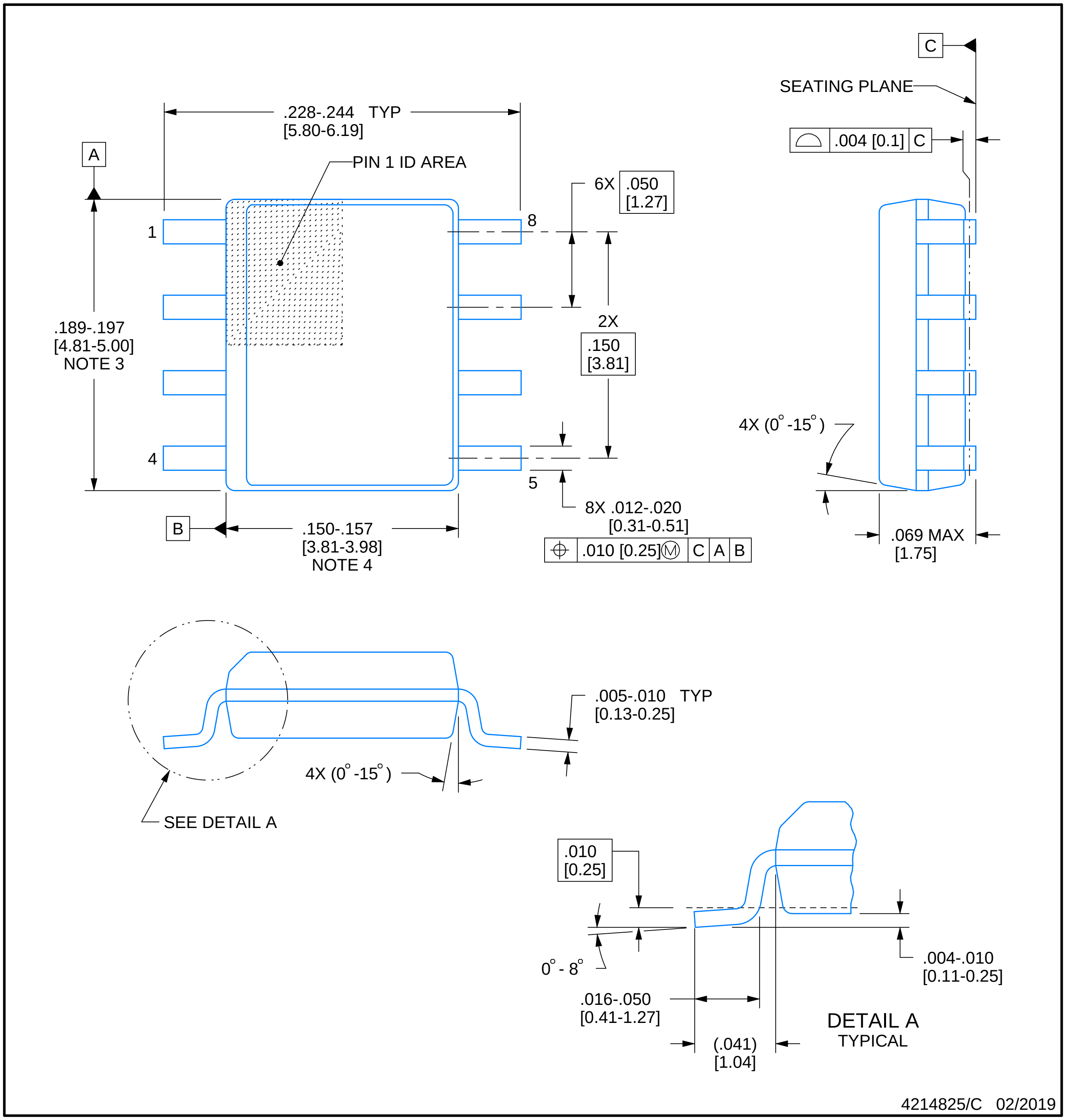


PACKAGE OUTLINE

D0008A

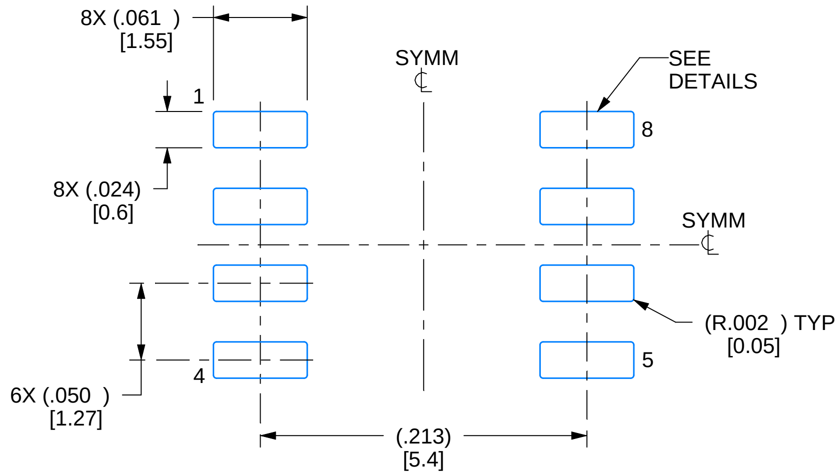
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

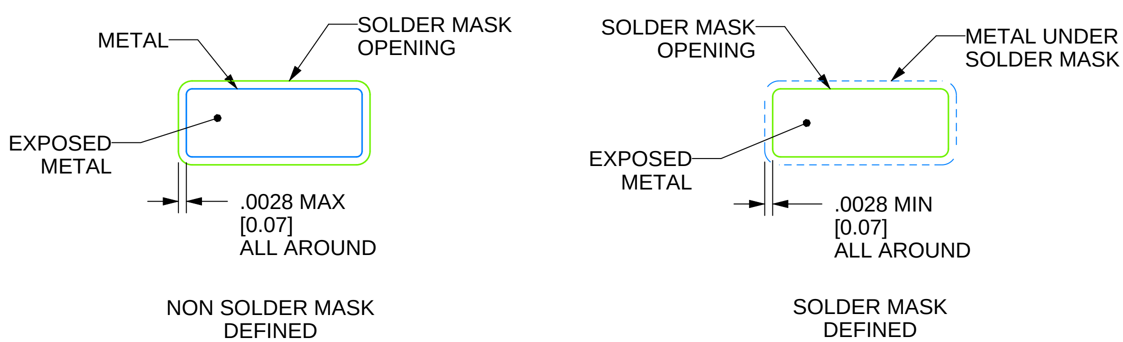


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

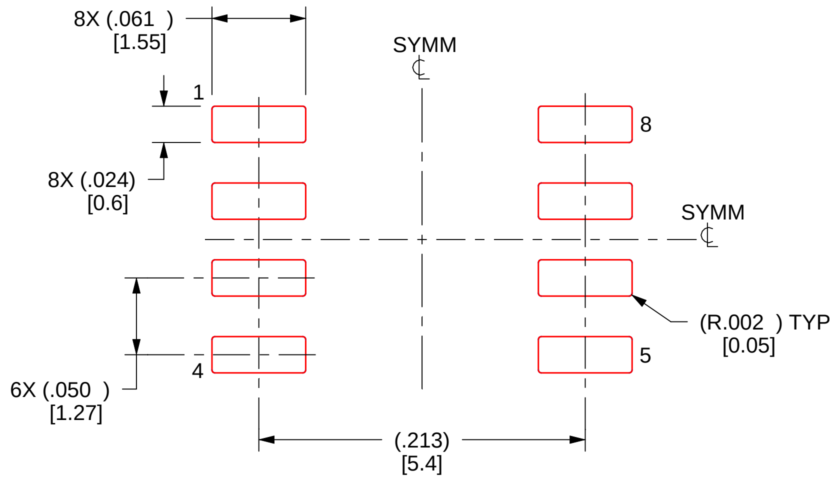


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



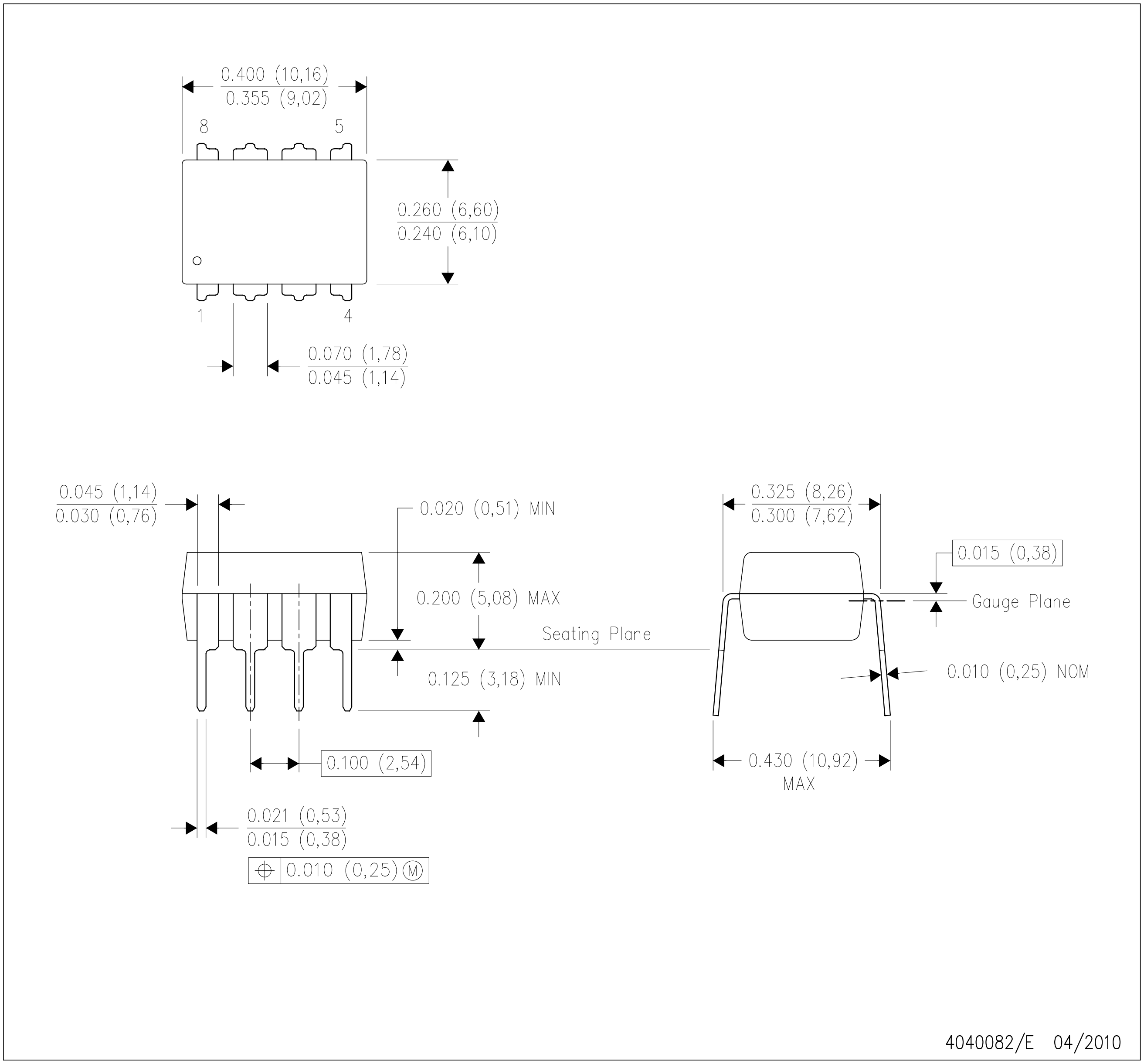
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.