

LM118, LM218, LM318 FAST GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

The LM118 and LM218 are obsolete and are no longer supplied.

SLOS063B – JUNE 1976 – REVISED DECEMBER 2002

- Small Signal Bandwidth . . . 15 MHz Typ
- Slew Rate . . . 50 V/μs Min
- Bias Current . . . 250 nA Max (LM118, LM218)
- Supply Voltage Range . . . ±5 V to ±20 V
- Internal Frequency Compensation
- Input and Output Overload Protection
- Same Pin Assignments as General-Purpose Operational Amplifiers

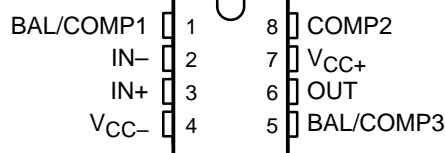
description/ordering information

The LM118, LM218, and LM318 are precision, fast operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor-of-ten increase in speed over general-purpose devices without sacrificing dc performance.

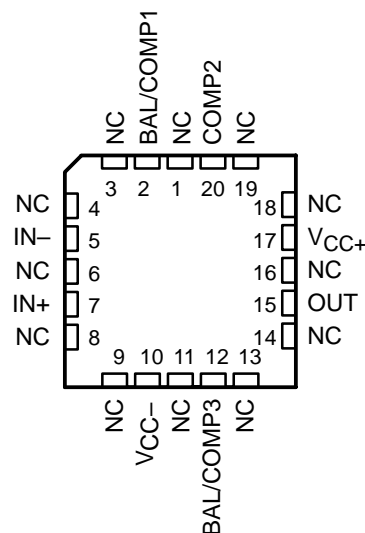
These operational amplifiers have internal unity-gain frequency compensation. This considerably simplifies their application because no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation boosts the slew rate to over 150 V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the settling time for 0.1% error band to under 1 μs.

The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample-and-hold circuits, and general-purpose amplifiers.

LM118 . . . JG PACKAGE
LM218 . . . D OR P PACKAGE
LM318 . . . D, P, OR PS PACKAGE
(TOP VIEW)



LM118 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T _A	V _{IO} max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	10 mV	PDIP (P)	Tube of 50	LM318P	LM318P
		SOIC (D)	Tube of 75	LM318D	LM318
			Reel of 2500	LM318DR	
		SOP (PS)	Reel of 2000	LM318PSR	LM18

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

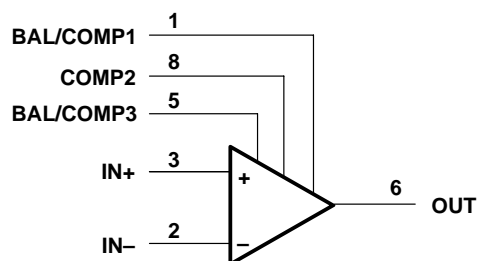
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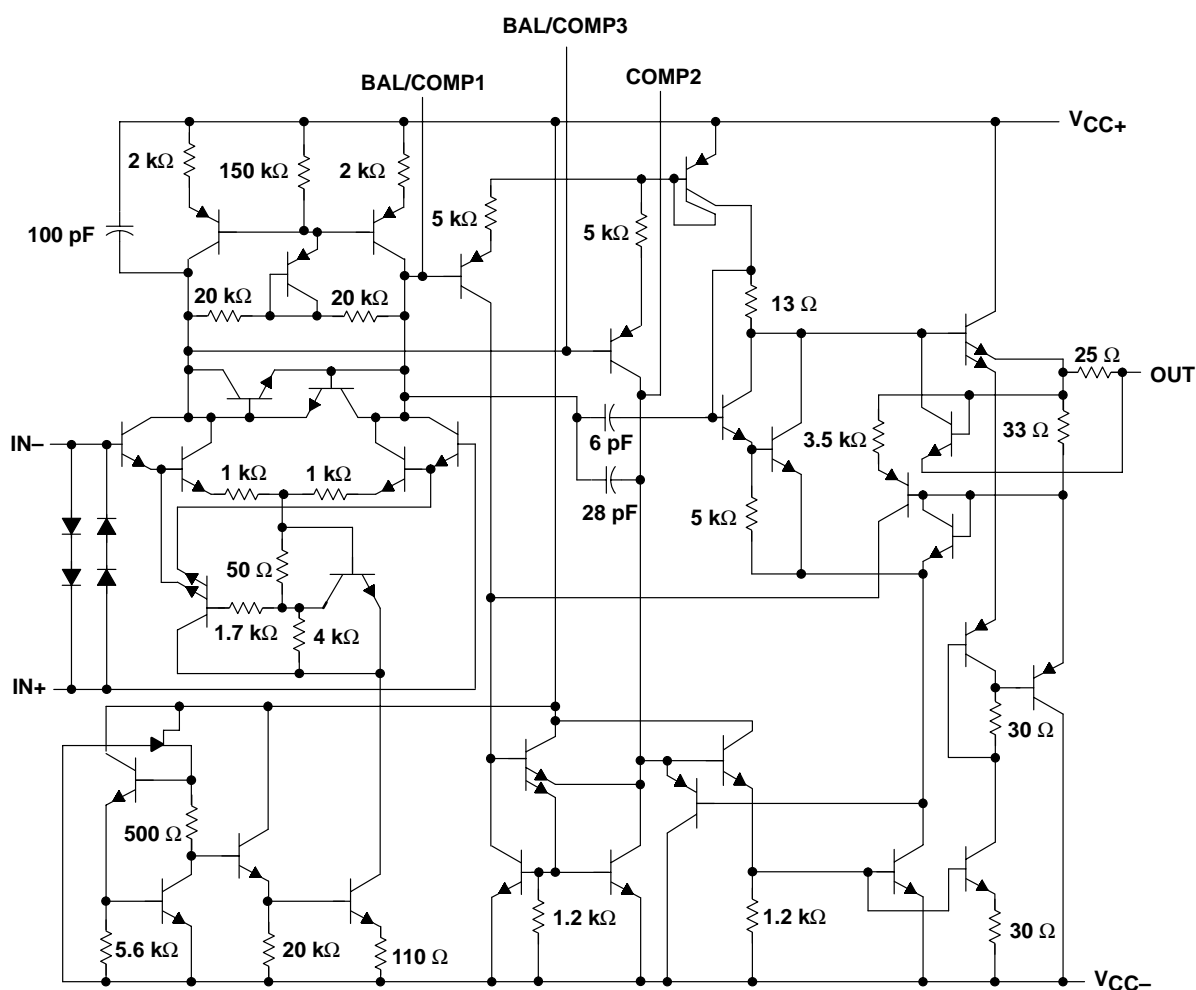
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symbol



Pin numbers shown are for the D, JG, P, and PS packages.

schematic



Component values shown are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1)	20 V
V_{CC-} (see Note 1)	–20 V
Input voltage, V_I (either input, see Notes 1 and 2)	±15 V
Differential input current, V_{ID} (see Note 3)	±10 V
Duration of output short circuit (see Note 4)	Unlimited
Operating virtual junction temperature, T_J	150°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package	97°C/W
P package	85°C/W
PS package	95°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8): FK package	5.61°C/W
JG package	14.5°C/W
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, P, PS, or PW package	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 3. The inputs are shunted with two opposite-facing base-emitter diodes for overvoltage protection. Therefore, excessive current flows if a different input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
 4. The output can be shorted to ground or either power supply. For the LM118 and LM218 only, the unlimited duration of the short circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.
 5. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 6. The package thermal impedance is calculated in accordance with JESD 51-7.
 7. Maximum power dissipation is a function of $T_J(\max)$, θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 8. The package thermal impedance is calculated in accordance with MIL-STD-883.

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electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER	TEST CONDITION†	TA‡	LM118, LM218			LM318			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
VIO Input offset voltage	VO = 0	25°C		2	4		4	10	mV
		Full range			6			15	
IIO Input offset current	VO = 0	25°C		6	50		30	200	nA
		Full range			100			300	
IIB Input bias current	VO = 0	25°C		120	250		150	500	nA
		Full range			500			750	
VICR Common-mode input voltage range	VCC± = ±15 V	Full range	±11.5			±11.5			V
VOM Maximum peak output voltage swing	VCC± = ±15 V, RL = 2 kΩ	Full range	±12 ±13			±12 ±13			V
AVD Large-signal differential voltage amplification	VCC± = ±15 V, VO = ±10 V, RL ≥ 2 kΩ	25°C	50	200		25	200		V/mV
		Full range	25			20			
B1 Unity-gain bandwidth	VCC± = ±15 V	25°C	15			15			MHz
ri Input resistance		25°C	1*	3		0.5	3		MΩ
CMRR Common-mode rejection ratio	VIC = VICRmin	Full range	80	100		70	100		dB
kSVR Supply-voltage rejection ratio (ΔVCC/ΔVIO)		Full range	70	80		65	80		dB
ICC Supply current	VO = 0, No load	25°C	5 8			5 10			mA

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† All characteristics are measured under open-loop conditions with common-mode input voltage, unless otherwise specified.

‡ Full range for LM118 is –55°C to 125°C, full range for LM218 is –25°C to 85°C, and full range for LM318 is 0°C to 70°C.

NOTE 9: Unless otherwise noted, VCC = ±5 V to ±20 V. All typical values are at VCC± = ±15 V and TA = 25°C.

operating characteristics, VCC± = ±15 V, TA = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	ΔVI = 10 V, CL = 100 pF, See Figure 1	50*	70		V/μs

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION

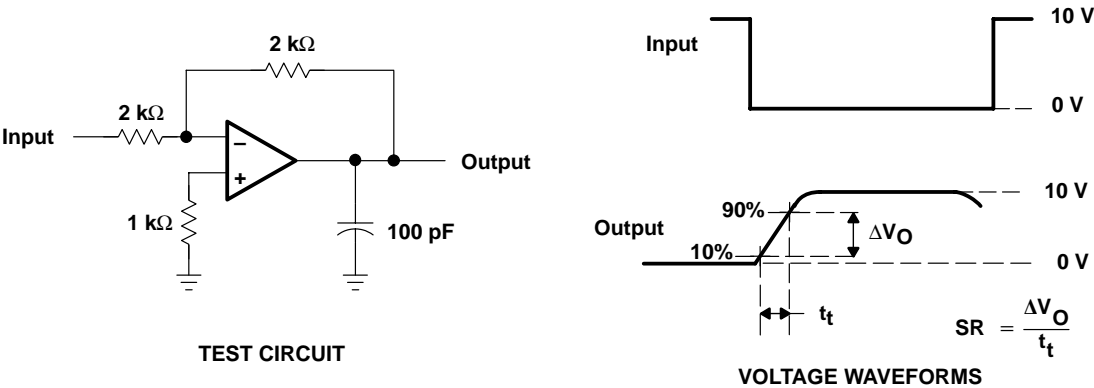


Figure 1. Slew Rate

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM318D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318
LM318D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318
LM318DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318
LM318DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318
LM318P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM318P
LM318P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM318P
LM318PE4	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	Call TI	0 to 70	
LM318PSR	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L318
LM318PSR.A	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L318

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM318DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM318PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM318DR	SOIC	D	8	2500	353.0	353.0	32.0
LM318PSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM318D	D	SOIC	8	75	507	8	3940	4.32
LM318D.A	D	SOIC	8	75	507	8	3940	4.32
LM318P	P	PDIP	8	50	506	13.97	11230	4.32
LM318P.A	P	PDIP	8	50	506	13.97	11230	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

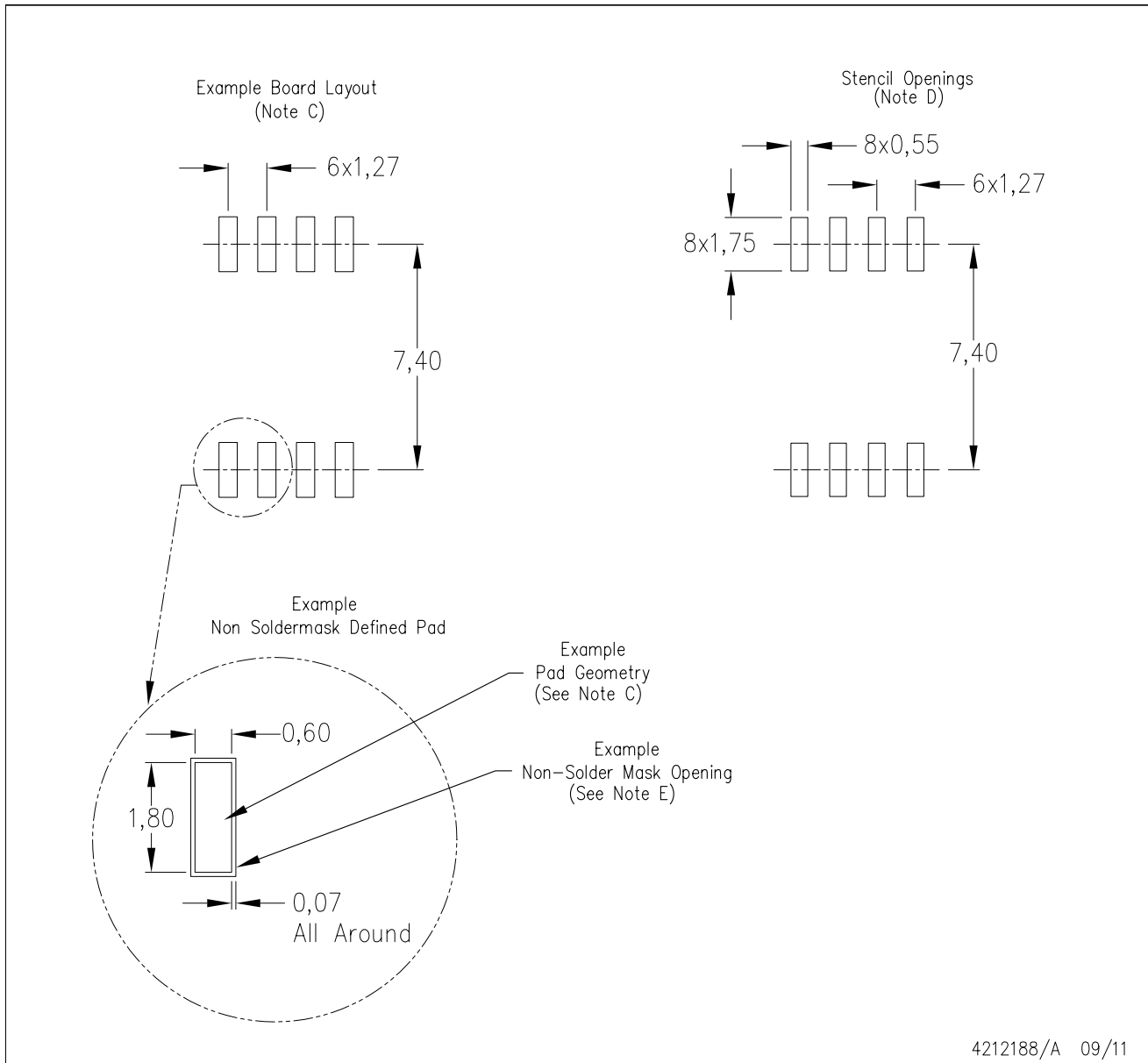


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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