LM10011 用于负载点稳压器且具有可调节启动电流的 6/4 位 VID 可编程电流 DAC

1 特性

- 1.0% 输出电流精度（0°C 至 100°C）
- 1.25% 输出电流精度（-40℃ 至 125℃）
- 输入电压范围：2.97V 至 5.5V
- 引脚可选 VID 格式（6 位或 4 位）
- 16 种可选的启动电流
- 精密使能端支持自定义 UVLO
- SON-10 3mm × 3mm 封装尺寸、0.5mm 间距
- 封装与 LM10010 兼容

2 应用

- 宽带、网络互联及无线通信
- 笔记本电源解决方案
- 便携式仪器
- 电池供电类设备
- 为具有 6 位或 4 位 4 引脚 VID 接口的数字负载供电

3 说明

LM10011 是一款用于控制直流/直流 (DC/DC) 转换器输出电压的精密数字可编程器件。 LM10011 输出的直流电流与 6 位或 4 位输入字成正比。 通过将 IDAC_OUT 引脚连接至稳压器的反馈节点，可以将稳压器输出电压调整为用户设置的范围和分辨率。 随着输入字递增计数，根据转换器中反馈电阻的值适当调高输出电压。

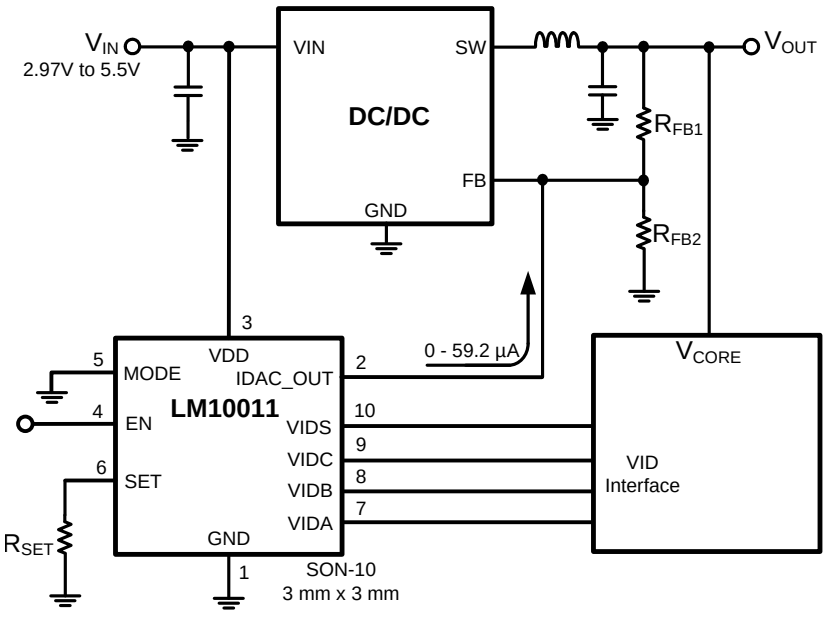
可通过外部电阻来编程 IDAC_OUT 引脚的启动电流，以覆盖 0 至 56.4μA 电流范围（分辨率为 4 位）。 MODE 引脚允许通过 4 位并行 VID 接口或 6 位接口（包含高 3 位和低 3 位 VID 代码）对器件进行编程。 LM10011 专用于针对 VID（电压识别）应用编程各类德州仪器 (TI) DC/DC 转换器。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM10011	WSON (10)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路



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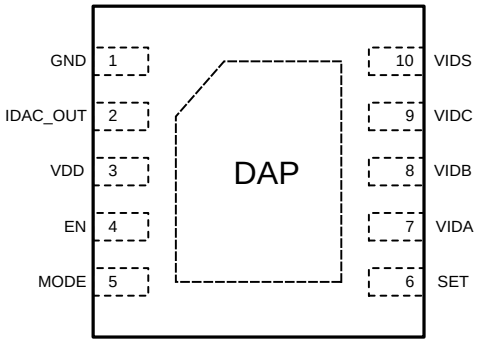
4 修订历史记录

Changes from Original (December 2012) to Revision A **Page**

- 已添加 *引脚配置和功能*部分，*处理额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

5 Pin Configuration and Functions

10-PIN
WSON PACKAGE
TOP VIEW



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
GND	1	–	Ground
IDAC_OUT	2	O	Output pin of the current DAC that connects to the feedback node of the regulator.
VDD	3	I	Positive supply input. Operating voltage is 2.97 V to 5.5 V. It is recommended to add a small 1-nF or greater bypass capacitor from this pin to GND.
EN	4	I	Precision enable input. The LM10011 will operate when the EN pin voltage exceeds 1.34 V.
MODE	5	–	MODE will set the VID operating mode. Connecting MODE to VDD will select a 4-bit parallel interface. Connecting MODE to GND will select a 4-pin, 6-bit interface.
SET	6	–	A resistor connected from SET to GND will set the start-up code (current) at the IDAC_OUT pin. There are 16 different start-up codes to select from.
VIDA	7	I	VID digital input. In 6-bit mode: Bit 0 when VIDS transitions low; Bit 3 when VIDS transitions high. In 4-bit mode: Bit 0.
VIDB	8	I	VID digital input. In 6-bit mode: Bit 1 when VIDS transitions low; Bit 4 when VIDS transitions high. In 4-bit mode: Bit 1.
VIDC	9	I	VID digital input. In 6-bit mode: Bit 2 when VIDS transitions low; Bit 5 when VIDS transitions high. In 4-bit mode: Bit 2.
VIDS	10	I	VID select line. In 6-bit mode: transition low selects lower 3 bits, transition high selects upper 3 bits and updates the IDAC_OUT current to reflect the present VID code. In 4-bit mode: Bit 3.
DAP	DAP	–	Die Attach Pad. Not electrically connected to device, connect to system ground plane for reduced thermal resistance.

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VDD, EN, IDAC_OUT, MODE	–0.3	6	V
VIDA, VIDB, VIDC, VIDS	–0.3	6	V
Junction Temperature		150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) If Military- or Aerospace-specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VDD	2.97	5.5	V
IDAC_OUT	–0.3	VDD – 1.75	V
VIDA, VIDB, VIDC, VIDS, EN, MODE	–0.3	5.5	V
Junction Temperature	−40	125	°C
Ambient Temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM10011 DSC 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	52.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	30.6	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	26.8	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	26.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(7)	7.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY, UVLO, AND ENABLE						
IQ	Quiescent current	VDD = 5.0 V, V_{EN} = 2.0 V		260	300	µA
IQ_FS	Quiescent current, IDAC_OUT = IFS_6	VDD = 5.0 V, V_{EN} = 2.0 V, IFS_6		382		µA
IQ_DIS	Quiescent current disabled	VDD = 5.0 V, V_{EN} = 0.0 V		45	65	µA
VUVLO_R	Undervoltage rising threshold	VDD rising		2.65	2.95	V
VUVLO_F	Undervoltage falling threshold	VDD falling	2.2	2.45		V
VUVLO_HYS	Hysteresis			200		mV
VEN	Enable rising threshold	V_{EN} rising	1.20	1.34	1.45	V
VEN_HYS	Enable hysteresis		50	100	180	mV
IEN	Enable pullup current			2		µA
IDAC_OUT						
ACC	Accuracy	Measured at full scale	–1.25		1.25	%
ACC	Accuracy	Measured at full scale, 0°C to 100°C	–1.0		1.0	%
LSB_6	DAC step size, 6-bit mode	IFS_6 / (2^6 – 1)		940		nA
LSB_4	DAC step size, 4-bit mode	IFS_4 / (2^4 – 1)		3.76		µA
IFS_6	Full-scale output current (6-bit mode)	VID[5:0] = 000000b		59.2		µA
IFS_4	Full-scale output current (4-bit mode)	VID[3:0] = 0000b		56.4		µA
INL	Integral non-linearity		–1		1	LSB_6
DNL	Differential non-linearity		–0.25		0.25	LSB_6
OFFSET	Offset current	VID[5:0] = 111111b (6-bit), VID[3:0] = 1111b (4-bit)		60		nA
VOUT_MAX	IDAC_OUT compliance voltage	VDD = 3 V, VDD-V_{IDAC_OUT}			1.75	V
START-UP SET CURRENT						
VSETFSR	SET pin voltage FSR		1.12	1.2	1.23	V
SETRES	SET ADC resolution			4		bits
SETRNG	SET ADC current full-scale range			56.4		µA
ISET	SET Current		4.75	5.1	5.40	µA
SET0	Start-up DAC error, code 0	R_{SET} = 0 Ω, I_{DAC_OUT} = 56.4 µA	0		0	LSB
SET1	Start-up DAC error, code 1	R_{SET} = 21.0 kΩ(3), I_{DAC_OUT} = 52.7 µA	0		0	LSB
SET2	Start-up DAC error, code 2	R_{SET} = 35.7 kΩ(3), I_{DAC_OUT} = 48.9 µA	0		0	LSB
SET3	Start-up DAC error, code 3	R_{SET} = 51.1 kΩ(3), I_{DAC_OUT} = 45.2 µA	0		0	LSB
SET4	Start-up DAC error, code 4(4)	R_{SET} = 71.5 kΩ(3), I_{DAC_OUT} = 41.4 µA	0		1	LSB
SET5	Start-up DAC error, code 5(4)	R_{SET} = 86.6 kΩ(3), I_{DAC_OUT} = 37.7 µA	0		1	LSB
SET6	Start-up DAC error, code 6(4)	R_{SET} = 105 kΩ(3), I_{DAC_OUT} = 33.9 µA	0		1	LSB
SET7	Start-up DAC error, code 7(4)	R_{SET} = 118 kΩ(3), I_{DAC_OUT} = 30.1 µA	0		1	LSB
SET8	Start-up DAC error, code 8(4)	R_{SET} = 140 kΩ(3), I_{DAC_OUT} =26.4 µA	0		1	LSB
SET9	Start-up DAC error, code 9(4)	R_{SET} = 154 kΩ(3), I_{DAC_OUT} = 22.6 µA	0		1	LSB
SET10	Start-up DAC error, code 10(4)	R_{SET} = 169 kΩ(3), I_{DAC_OUT} = 18.8 µA	0		1	LSB
SET11	Start-up DAC error, code 11(4)	R_{SET} = 182 kΩ(3), I_{DAC_OUT} = 15.1 µA	0		1	LSB
SET12	Start-up DAC error, code 12(4)	R_{SET} = 200 kΩ(3), I_{DAC_OUT} = 11.3 µA	0		1	LSB
SET13	Start-up DAC error, code 13(4)	R_{SET} = 215 kΩ(3), I_{DAC_OUT} = 7.59 µA	0		1	LSB
SET14	Start-up DAC error, code 14(4)	R_{SET} = 237 kΩ(3), I_{DAC_OUT} = 3.80 µA	0		1	LSB
SET15	Start-up DAC error, code 15	R_{SET} = 301 kΩ(3), I_{DAC_OUT} = 0.06 µA	0		0	LSB

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \times R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in the *Thermal Information* section.
(3) R_{SET} is based on 1% E96 standard resistor values.
(4) "+1" LSB implies a positive step in CODE. LSB is in reference to LSB_4.

Electrical Characteristics (接下页)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VID LOGIC INPUTS(5)						
V_{IL}	Input voltage low				0.75	V
V_{IH}	Input voltage high		1.0			V
I_{IL}	Input current low		–3.5			µA
I_{IH}	Input current high				5	µA
$t_{DEGLITCH}$	Input deglitch time			3.6		µs
t_1	Input delay time	VIDS rising edge			1	µs
t_2	Input hold time VIDA, VIDB, VIDC valid	VIDS falling edge	20			µs
t_3	Input delay time	VIDS falling edge			1	µs
t_4	Input hold time VIDA, VIDB, VIDC valid	VIDS rising edge	20			µs
t_5	Delay to beginning of IDAC_OUT transition	Measured from VIDS rising edge		6.3	10	µs
t_6	IDAC_OUT transition time	Time constant for exponential rise		40		µs
t_7	Minimum hold time in 4-bit mode	VIDA, VIDB, VIDC, VIDS		4.4		µs

(5) For VID timing, see 图 1.

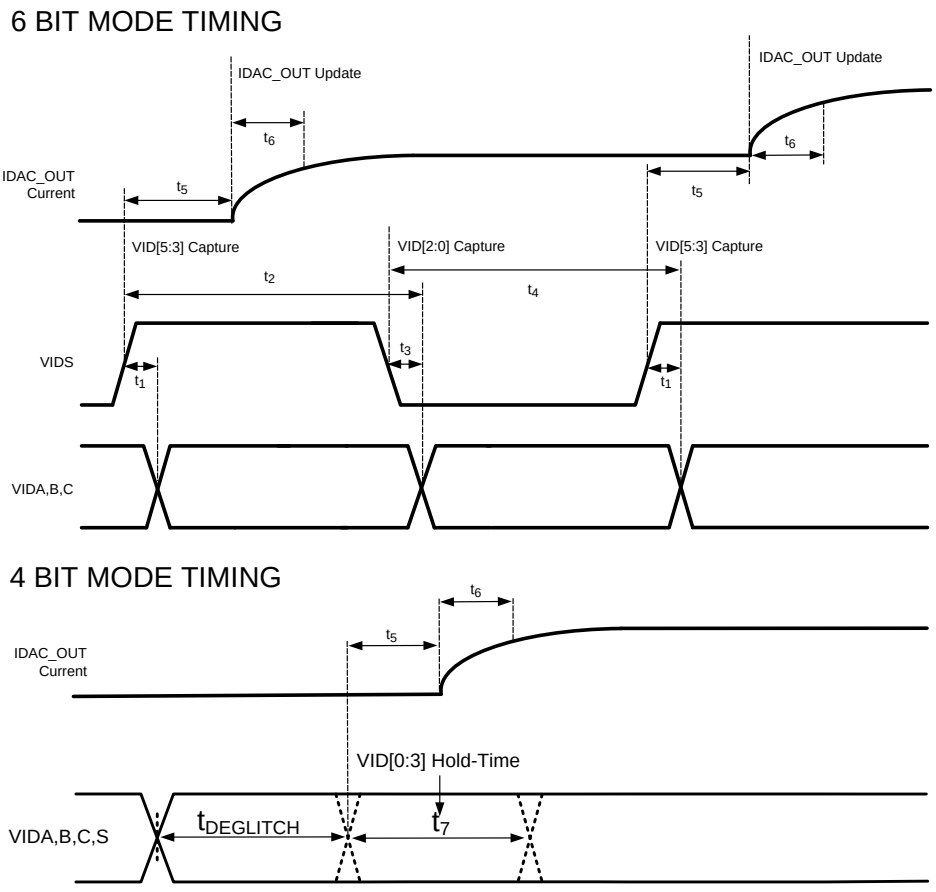


图 1. Timing Diagram for LM10011 Communications

6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_J = 25°C, VDD = 5 V. All graphs show junction temperature.

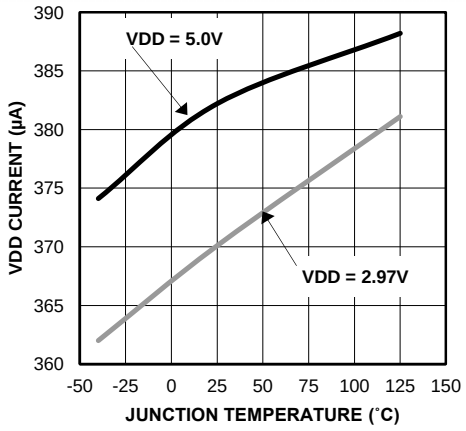


图 2. Supply Current Maximum Output Current VID = [000000]

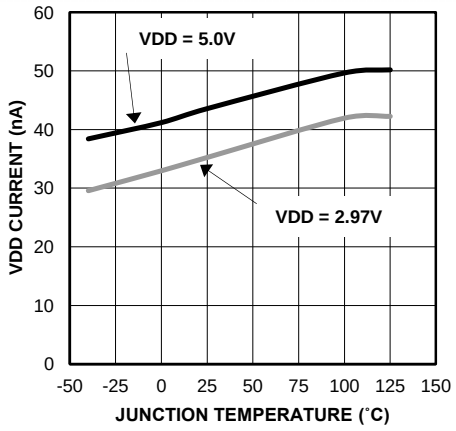


图 3. Supply Current (EN LOW)

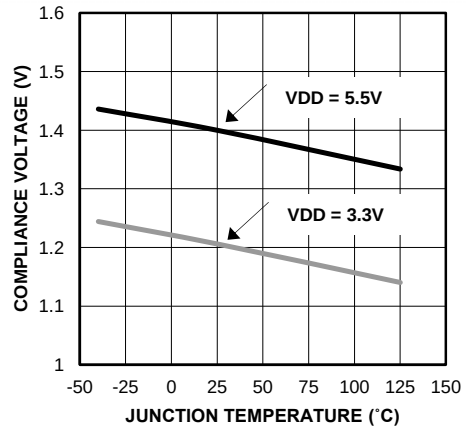


图 4. Output Compliance to Positive Rail (VDD-V_{IDAC_OUT})

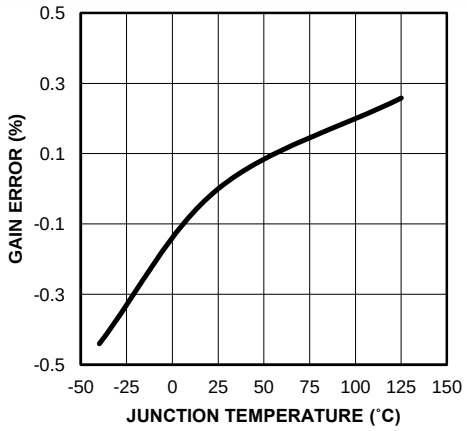


图 5. Gain Error

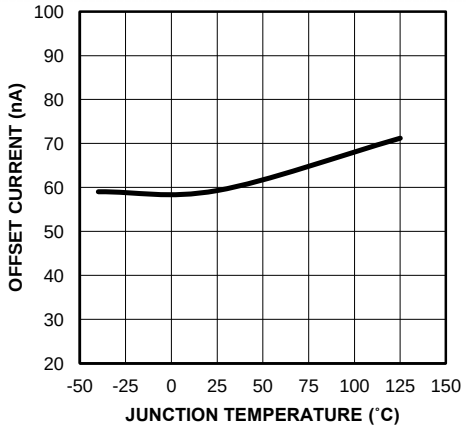


图 6. IDAC_OUT Offset Current VID = [111111]

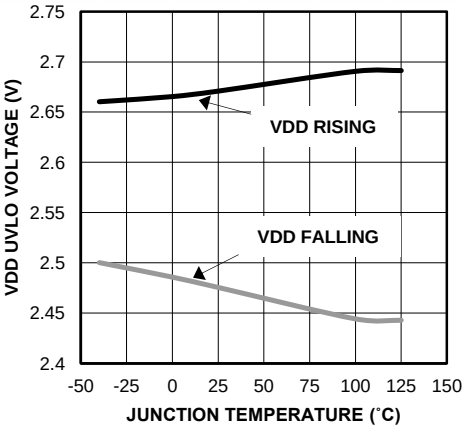


图 7. UVLO Thresholds

Typical Characteristics (接下页)

Unless otherwise specified, the following conditions apply: T_J = 25°C, VDD = 5 V. All graphs show junction temperature.

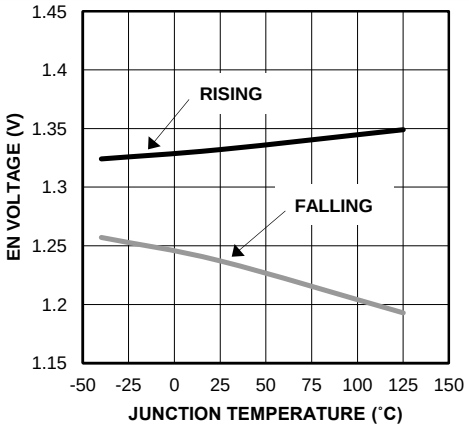


图 8. Enable (EN) Threshold

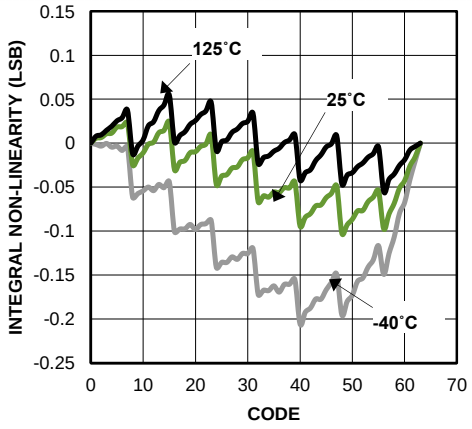


图 9. Integral Non-Linearity

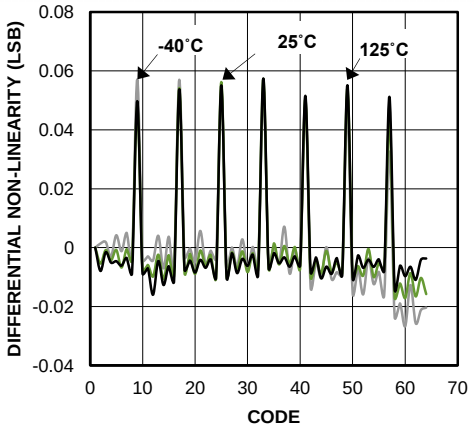


图 10. Differential Non-Linearity

7 Detailed Description

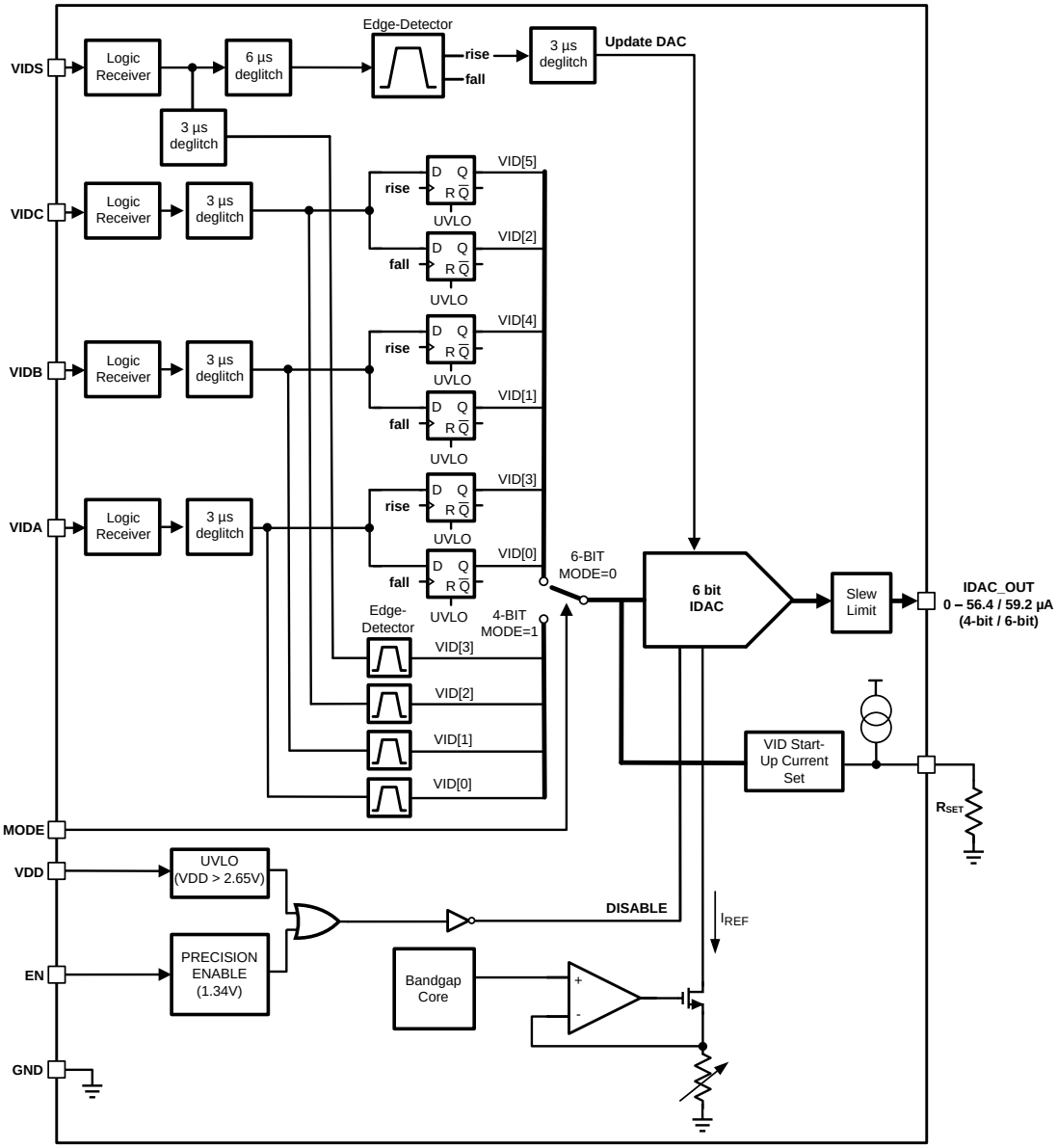
7.1 Overview

The LM10011 is a precision current DAC used for controlling any point of load regulator with an adjustable resistor feedback network. Four VID communication lines (VIDA, VIDB, VIDC, and VIDS) are used to write a 6-bit or 4-bit VID value. The output of the IDAC (IDAC_OUT) is used to inject a precision current into the feedback node of a regulator, thus adjusting the output voltage. With this method, it is possible to precisely control the output voltage of the regulator.

An enable pin (EN) is provided to allow for a reduced quiescent current when not in use. Also, the VDD line is monitored so that an undervoltage event will shutdown the LM10011 (IDAC_OUT = 0.0 µA).

The device is available in a 10-pad No-Pullback Package (SON-10). The LM10011 can be used in numerous applications with regulators from 2.97-V to 5.5-V supplies.

7.2 Functional Block Diagram



7.3 Feature Description

The LM10011 can be treated as a D/A converter, converting digital VID codes to analog outputs. The LM10011 DAC analog output is a current that flows out of the IDAC_OUT pin. The IDAC_OUT pin is intended to be connected to the feedback node of a voltage regulator as shown in 图 11. In a typical voltage regulator, the current in R_{FB2} is constant by virtue of the regulator feedback loop maintaining the reference voltage at the feedback node. The current flowing through R_{FB2} is the same current flowing through R_{FB1}. When current is injected into the feedback node by the LM10011, less current is required from the R_{FB1} resistor. The consequence of this is that the output voltage of the regulator will decrease to maintain the total amount of current in R_{FB2} to regulate at the correct feedback (reference) voltage.

Each VID code corresponds to a different IDAC_OUT current and thus a different output voltage. Increasing the VID code lowers the IDAC_OUT current and raises the output voltage. Decreasing the VID code raises the IDAC_OUT current and lowers the output voltage. All VID codes are decoded into a 6-bit or 4-bit current DAC output whether the MODE equals 0 (connected to GND) or 1 (connected to VDD), respectively.

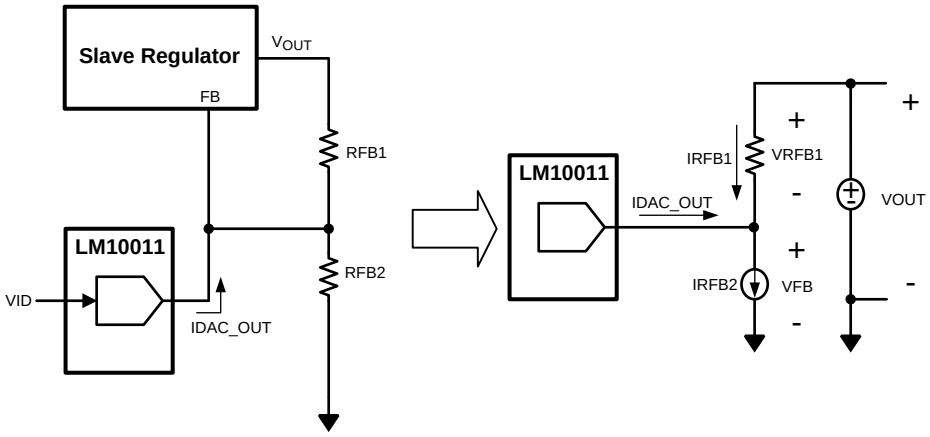


图 11. Output Voltage (V_{OUT}) is Controlled Via Current Injection into the Feedback Node

7.3.1 Current DAC

The LM10011 current DAC is based on a low-voltage bandgap reference setting a current through a precision adjustable resistor. This bandgap is trimmed for precision and gives excellent performance over temperature. The output current has a maximum full-scale range [VID = 000000b] of 59.2 µA and is adjustable with a 6- or 4-bit VID word. This allows for 64 or 16 settings with a resolution of 940 nA or 3.76 µA, respectively. The current DAC also has a slew limit to prevent abrupt changes in the output. The slew limit is represented as a time constant, t_6 = 40 µs, in the *Electrical Characteristics* table. A deglitch filter for the VID inputs provides noise immunity and effectively adds a small delay from the transition of a VID line to the change in IDAC_OUT current.

7.3.2 Enable Pin and UVLO

The enable (EN) pin allows the output of the device to be enabled or disabled (IDAC_OUT = 0.0 µA) with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.34 V. The EN pin has 100 mV of hysteresis and will disable the output when the enable voltage falls below 1.23 V. If EN is not used, it can be left open, and will be pulled high by an internal 2-µA current source. Since the EN pin has a precise turn-on threshold it can be used along with an external resistor divider network from VDD to configure the device to turn on at a precise input voltage.

The LM10011 has a built-in undervoltage lockout (UVLO) protection circuit that keeps the device from operating until the input voltage reaches 2.65 V (typical). The UVLO threshold has 200 mV of hysteresis that keeps the LM10011 from responding to power-on glitches during start-up. Note that descending below the EN voltage and/or the UVLO voltage are functionally the same as a reset. Bringing the device back from a low enable setting or from a VDD UVLO event will reset the IDAC_OUT current to its start-up R_{SET} setting.

7.4 Device Functional Modes

表 1 lists the functional modes of the LM10011 device.

表 1. Mode Pin Summary

MODE PIN CONNECTION	LOGIC STATE	DESCRIPTION
GND	0	6-bit mode
VDD	1	4-bit mode

7.5 Programming

7.5.1 VID Programming, 6-Bit Mode

Four pins are used to communicate with the LM10011. In 6-bit mode (MODE = 0), VIDA, VIDB, and VIDC are data lines, while VIDS is a latching strobe that programs in the LM10011 data. As shown in the 6-bit mode timing diagram of 图 1, the falling edge of VIDS latches in the data from VIDA, VIDB, and VIDC as the lower three LSB of the IDAC_OUT value, [2:0]. After a minimum hold time (t_2), the rising edge of VIDS latches in the data from VIDA, VIDB, and VIDC as the upper three LSB of the IDAC_OUT value, [5:3]. Internally, a delay (t_3,t_1) on VIDS allows for the setting of all VIDA, VIDB, and VIDC lines to change simultaneously as VIDS rises or falls.

7.5.2 VID Programming, 4-Bit Mode

The LM10011 includes a 4-bit mode to facilitate parallel VID communication. In 4-bit mode (MODE = 1), VIDC, VIDB, VIDA, and VIDS are all parallel data lines. As shown in the 4-bit mode timing diagram in 图 1, a changing edge of any of the VID communication lines will change the IDAC_OUT current to the corresponding new 4-bit value found on the data lines. There is a 3-µs deglitch filter to eliminate spurious noise events. The data must overcome the deglitch time and the minimum hold time (t_7) or else the IDAC_OUT pin current may not reflect the value indicated at the VID data inputs. During the hold time, no other data line can be transitioned.

As mentioned in a previous section, for both the 4-bit and 6-bit mode, the VID data word is set so that the lowest output current is seen at the highest VID data word (59.2 µA at a code of 0d in 6-bit mode and 56.4 µA in 4-bit mode). Conversely, the lowest current is seen at the highest VID data word (0.06 µA at 63d or 15d). During VID operation with the regulator, this will translate to the lowest output voltage with the lowest VID word, 0d, and the highest output voltage with the highest VID word, 63d or 15d. The communications pins can be used with a low-voltage microcontroller with a maximum V_{IL} of 0.75 V and a minimum V_{IH} of 1.0 V.

7.5.3 Programming the Start-Up Current

Depending on the value of R_{SET} during start-up (when VDD > VUVLO_R and EN > VEN), the output current on the IDAC_OUT pin will take on 1 of 16 discrete values corresponding to the currents available in the 4-bit mode. These discrete start-up currents can be programmed by connecting a resistor (R_{SET}) from the SET pin to GND. If the EN voltage is toggled or a UVLO is triggered during operation, the current will default back to the value set by the R_{SET} resistor. It takes only one VID command transition in either 4-bit or 6-bit mode to change the current to something other than the pre-programmed start-up current. The required R_{SET} resistors and their corresponding start-up currents codes can be found in 表 2.

表 2. Start-Up–4-Bit Mode Currents with Corresponding R_{SET} Values and Output Currents

VID CODE	NOMINAL IDAC_OUT CURRENT (µA)	R_{SET} (kΩ)
0000b (0d)	56.4	0
0001b (1d)	52.7	21.0
0010b (2d)	48.9	35.7
0011b (3d)	45.2	51.1
0100b (4d)	41.4	71.5
0101b (5d)	37.7	86.6
0110b (6d)	33.9	105
0111b (7d)	30.1	118
1000b (8d)	26.4	140
1001b (9d)	22.6	154

Programming (接下页)

表 2. Start-Up–4-Bit Mode Currents with Corresponding R_{SET} Values and Output Currents (接下页)

VID CODE	NOMINAL IDAC_OUT CURRENT (µA)	R_{SET} (kΩ)
1010b (10d)	18.8	169
1011b (11d)	15.1	182
1100b (12d)	11.3	200
1101b (13d)	7.59	215
1110b (14d)	3.80	237
1111b (15d)	0.06	301

Codes 0100b (4d) through 1110b (14d) will start-up into either the selected code or 1 code higher. This means that the output voltage of the POL may start-up into the selected output voltage or 1 LSB higher.

7.5.4 IDAC_OUT Current Values

表 3. IDAC_OUT Currents and Corresponding VID Codes

VID CODE (6-BIT [4-BIT])	IDAC CURRENT (µA)
0d	59.2
1d	58.3
2d	57.4
3d [0d]	56.4
4d	55.5
5d	54.6
6d	53.6
7d [1d]	52.7
8d	51.7
9d	50.8
10d	49.8
11d [2d]	48.9
12d	48.0
13d	47.0
14d	46.1
15d [3d]	45.2
16d	44.2
17d	43.3
18d	42.3
19d [4d]	41.4
20d	40.5
21d	39.5
22d	38.6
23d [5d]	37.7
24d	36.7
25d	35.7
26d	34.8
27d [6d]	33.9
28d	33.0
29d	32.0
30d	31.1
31d [7d]	30.1

表 3. IDAC_OUT Currents and Corresponding VID Codes (接下页)

VID CODE (6-BIT [4-BIT])	IDAC CURRENT (µA)
32d	29.2
33d	28.2
34d	27.3
35d [8d]	26.4
36d	25.4
37d	24.5
38d	23.6
39d [9d]	22.6
40d	21.6
41d	20.7
42d	19.8
43d [10d]	18.8
44d	17.9
45d	17.0
46d	16.0
47d [11d]	15.1
48d	14.1
49d	13.2
50d	12.3
51d [12d]	11.3
52d	10.4
53d	9.50
54d	8.52
55d [13d]	7.59
56d	6.60
57d	5.70
58d	4.74
59d [14d]	3.80
60d	2.87
61d	1.93
62d	1.00
63d [15d]	0.06

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LM10011 is a precision, digitally programmable device used for controlling the dc-dc converter output voltage. The LM10011 GUI design tool is available at www.ti.com/product/LM10011 and can be used to program any voltage regulator output to a desired range and resolution. The GUI enables changing the output voltage of the on-board POL based on direct user input. It is also able to assist the power designer in selecting the correct external components needed for any given application.

8.2 Typical Application

In this example, an LM21215A-1 is used as the voltage regulator and the desired range of output voltage operation is 0.7 V to 1.1 V. The LM10011 can provide control of the output voltage within this range with 6 bits or 4 bits of resolution. For this example, the 400 mV of voltage range translates to a V_{OUT_LSB} of 400 mV / 63 = 6.4 mV (26.7 mV in 4-bit mode) at the regulator output. In this calculation, 1% resistor values are used. A schematic for this example is shown in 图 12.

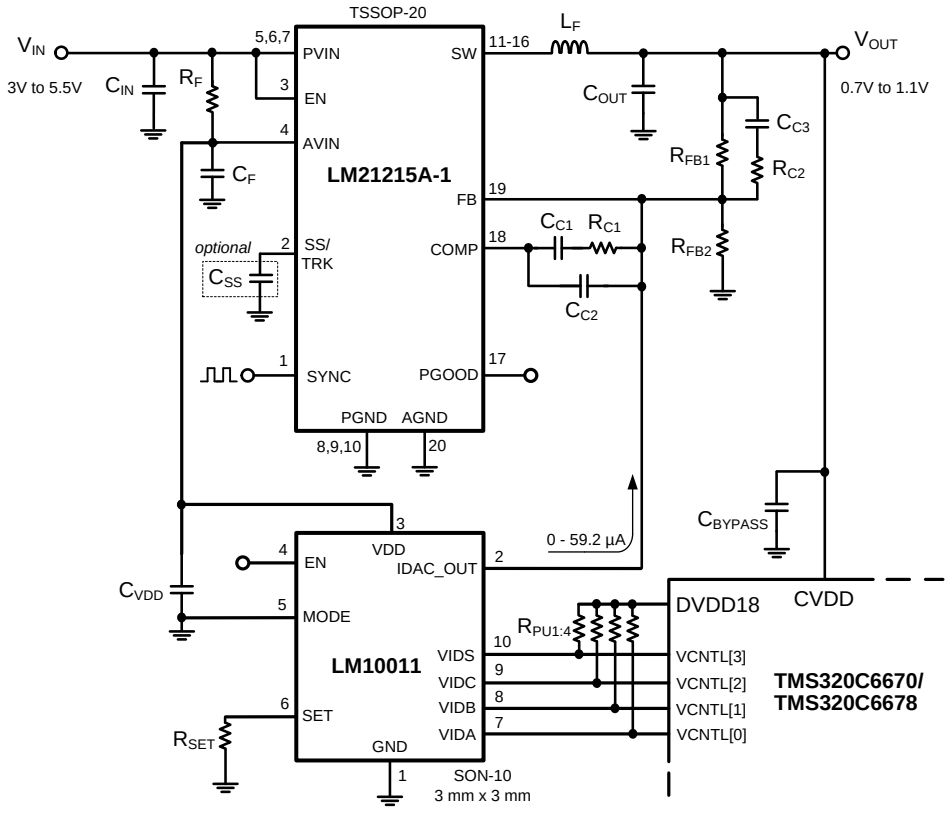


图 12. 6-Bit Mode Design Example

Typical Application (接下页)

8.2.1 Design Requirements

表 4 lists the design parameters.

表 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage range	0.7 V to 1.1 V
Startup voltage	1.1 V
Mode	0

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the V_{OUT} Range and LSB

Looking at the Typical Application Circuit in 图 12, the following equation defines V_{OUT} of a given regulator (valid for $V_{OUT} > V_{FB}$):

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) - IDAC\_OUT \times R_{FB1} \quad (1)$$

Here, the output voltage is a function of the resistor divider from R_{FB1} and R_{FB2}. Using the LM10011, there is a current supplied by the IDAC_OUT pin that helps drive current through the feedback resistor R_{FB2}, thus lowering the necessary current supplied through R_{FB1}, and hence lowering V_{OUT}. To calculate the nominal (maximum) V_{OUT}, use an IDAC_OUT value of 0 µA.

The change in the output voltage can be analyzed based on the resolution of the current DAC from the LM10011 compared to the desired resolution of the output swing of the regulator. R_{FB1} is designed to provide the desired V_{OUT_LSB} with the equation:

$$V_{OUT\_LSB} = LSB \times R_{FB1} \quad (2)$$

Where LSB = LSB_6 (940 nA) from the electrical characteristics table (see *Electrical Characteristics*). Based on the desired nominal V_{OUT} (with IDAC_OUT = 0 µA) and the calculated R_{FB1} from 公式 2, R_{FB2} can be solved using 公式 1.

8.2.2.2 4-Bit Mode Design Example

Designing with the LM10011 in 4-bit mode is similar to designing in 6-bit mode. The only differences are the LSB value (LSB = LSB_4 = 3.76 µA) in 公式 2 and full-scale current range (IDAC_OUT = 56.4 µA).

8.2.2.3 Setting the Start-Up Voltage with R_{SET}

R_{SET} is chosen depending on the required start-up voltage for the particular application. The user must use 公式 3 and solve for the required IDAC_OUT by inputting the known values of R_{FB1} and R_{FB2}, V_{FB}, and the desired start-up output voltage, V_{OUT}. Once IDAC_OUT is solved for, choose an R_{SET} based on 表 2 to select a start-up code to yield a current closely matching the calculated result. Use the equation below to solve for the required IDAC_OUT value at start-up.

$$IDAC\_OUT = \frac{1}{R_{FB1}} \left(V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) - V_{OUT}\right) \quad (3)$$

8.2.2.4 Example Solution

While in 6-bit mode, assuming a 400-mV output range, 64 VID codes, and an IDAC LSB of 0.940 µA, it is desired to have a V_{OUT} with an LSB of 6.4 mV and a default value of 1.1 V with a 1.05-V start-up voltage using an LM21215A-1 regulator (V_{FB} = 0.6 V):

$$6.4mV = 0.940\mu A \times R_{FB1} \quad (4)$$

$$R_{FB1} = 6.8k\Omega \quad (5)$$

Using 1% standard resistor values, R_{FB1} can be set to 6.81 kΩ. Now calculate R_{FB2} based on R_{FB1} and the maximum V_{OUT} of 1.1 V using 公式 1.

$$1.1V = .6V \times \left(1 + \frac{6.81k\Omega}{R_{FB2}}\right) - 0V \quad (6)$$

$$R_{FB2} = 8.1k\Omega \quad (7)$$

Using 1% standard resistor values, R_{FB2} can be set to 8.06 kΩ. This will yield a regulator output range of 0.704 V (CODE 0d) to 1.107 V (CODE 63d). Values calculated here will be dependent on the accuracy of the regulator, the LM10011 IDAC_OUT, and the resistor values used in the circuit.

表 5 shows the codes and some of the resultant values of the IDAC current and the corresponding regulator output voltage for the previous example.

表 5. 6-Bit VID Codes with IDAC Current and Regulator Voltage for the Example in 图 12.

VID CODE	IDAC_OUT CURRENT (µA)	REGULATOR VOLTAGE (V)
000000b (0d)	59.2	0.704
000001b (1d)	58.3	0.710
000010b (2d)	57.4	0.716
000011b (3d)	56.4	0.729
....	....	....
111100b (60d)	2.87	1.087
111101b (61d)	1.93	1.094
111110b (62d)	1.00	1.100
111111b (63d)	0.06	1.107

The required IDAC_OUT value during start-up can be calculated based on the desired start-up voltage of 1.05 V and the R_{FB1} and R_{FB2} resistors found in the previous calculations. Using 公式 3 to solve for the required start-up IDAC_OUT current results in a start-up current of 8.36 µA.

$$IDAC\_OUT = \frac{1}{6.81k\Omega}\left(0.6V \times \left(1 + \frac{6.81k\Omega}{8.06k\Omega}\right) - 1.05V\right) = 8.36\mu A \quad (8)$$

Choose a resistor in 表 2 that selects a start-up code that produces a current close to 8.36 µA. An R_{SET} of 215 kΩ selects a nominal start-up code of 13d yielding a current of 7.59 µA and start-up voltage of 1.054 V.

注

Using an R_{SET} of 215 kΩ may also select a code of 14d (+1 LSB) yielding a current of 3.80 µA and a start-up voltage of 1.081 V.

8.2.3 Application Curves

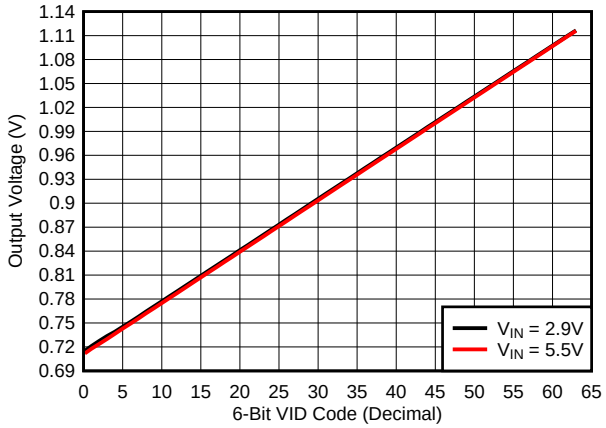


图 13. Output Voltage vs. Code for LM21k with LM10011

9 Power Supply Recommendations

The LM10011 can be driven from a PWM controller V_{DD} pin or from the V_{IN} supply pin as shown in 图 12. To ensure reliable operation, the LM10011 V_{DD} input power supply must be limited to 6 V maximum.

10 Layout

10.1 Layout Guidelines

The following guidelines should be followed when designing the PC board for the LM10011:

- Place the LM10011 close to the regulator feedback pin to minimize the FB trace length.
- Place a small capacitor, C_{VDD}, (1 nF) directly adjacent to the VDD and GND pins of the LM10011 to help minimize transients which may occur on the input supply line.
- The high-current path from the board input to the load and the return path should be parallel and close to each other to minimize loop inductance.
- The ground connections for the various components around the LM10011 should be connected directly to each other, and to the LM10011 GND pins, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high-current ground line.
- For additional information about the operation of the regulator, please consult the respective data sheet and application notes on the respective evaluation boards.

10.2 Layout Example

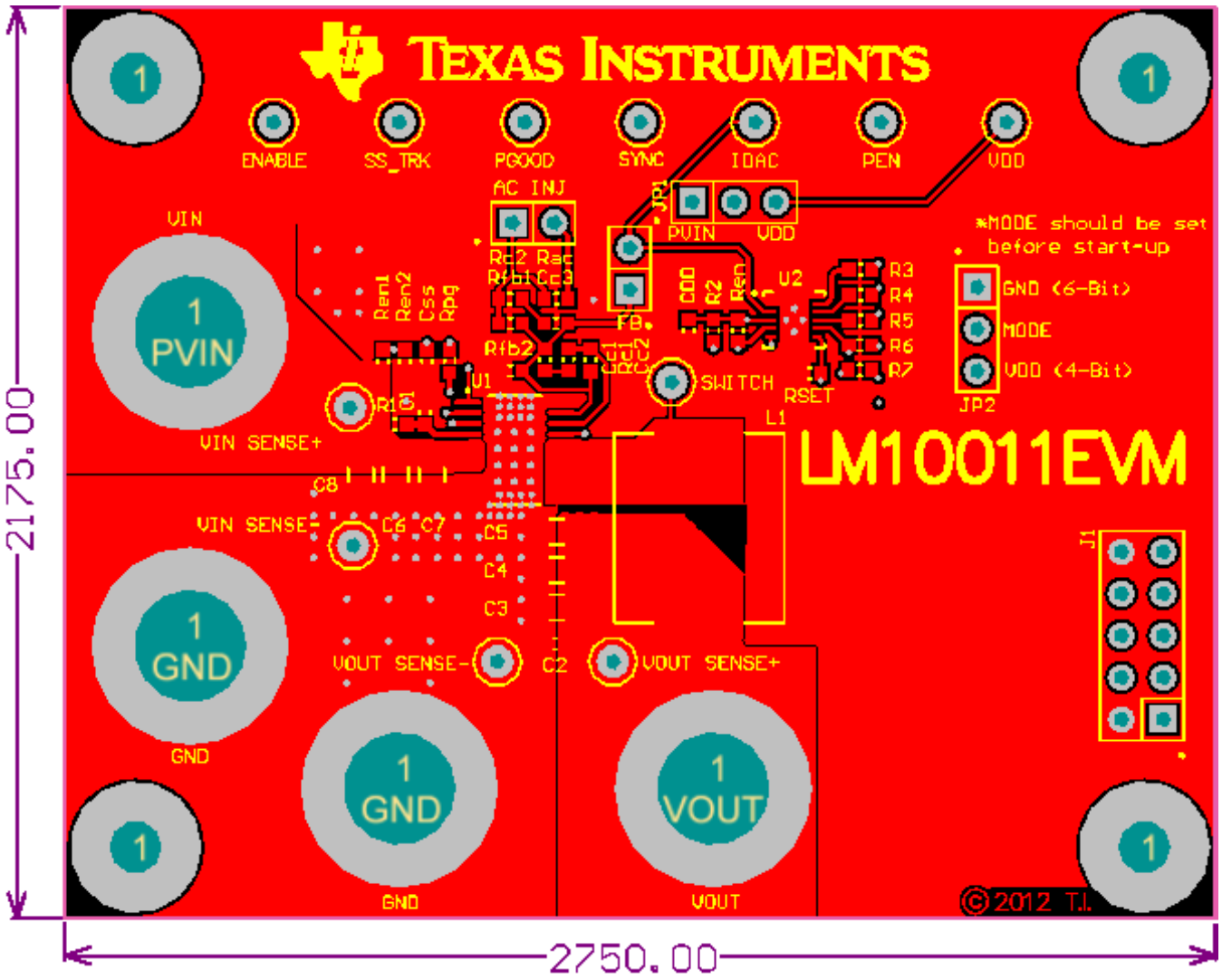


图 14. Typical Top Layer Layout

11 器件和文档支持

11.1 商标

All trademarks are the property of their respective owners.

11.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM10011SD/NOPB	Active	Production	WSON (DSC) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L271B
LM10011SD/NOPB.A	Active	Production	WSON (DSC) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L271B
LM10011SDX/NOPB	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L271B
LM10011SDX/NOPB.A	Active	Production	WSON (DSC) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L271B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

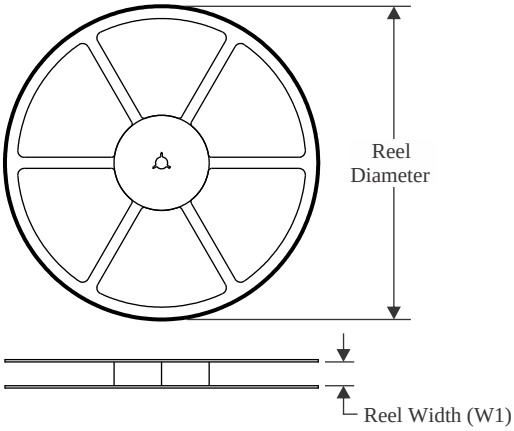
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

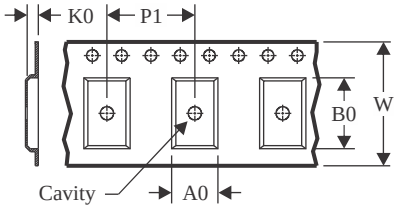
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

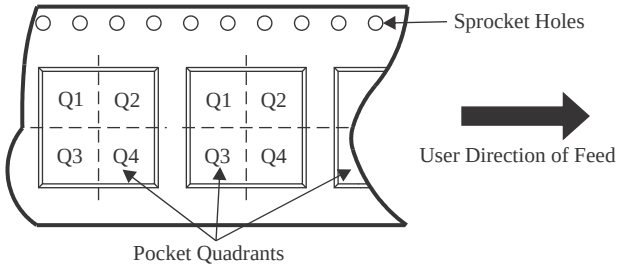


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

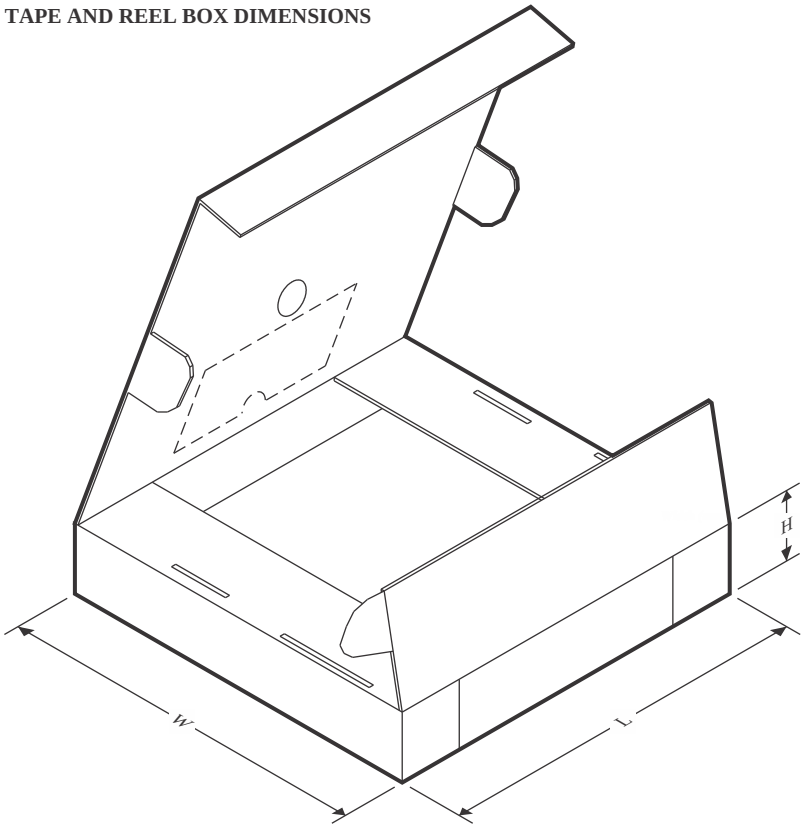
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10011SD/NOPB	WSON	DSC	10	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM10011SDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

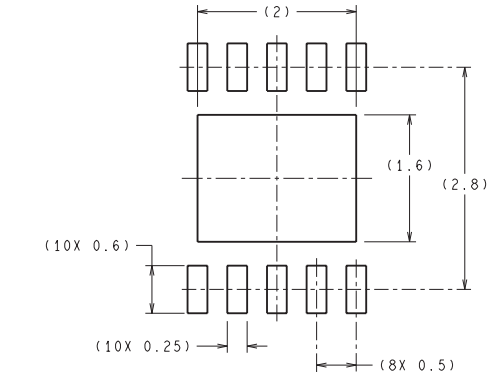
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

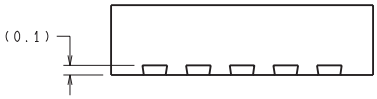
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10011SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM10011SDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

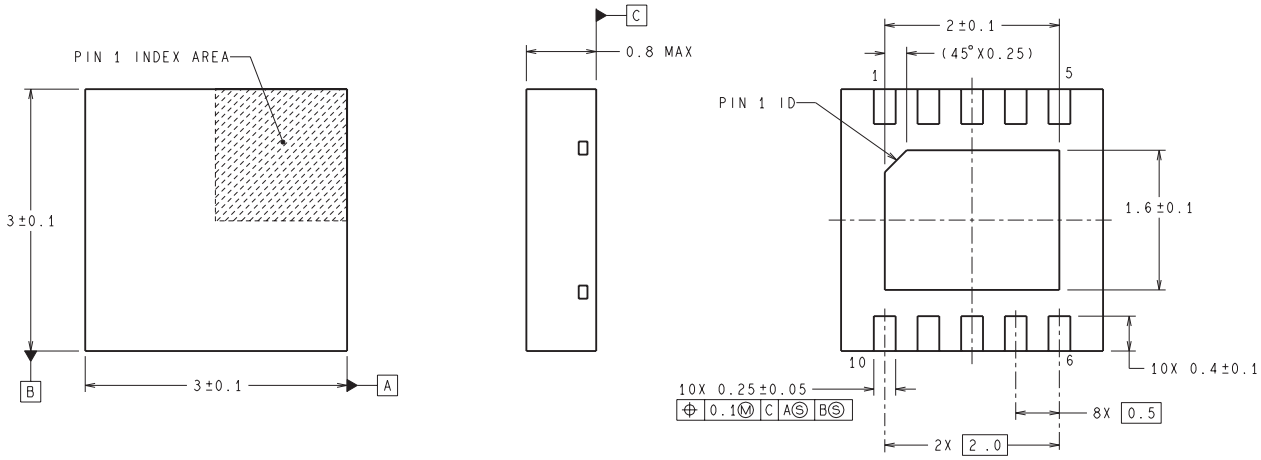
DSC0010A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





SDA10A (Rev A)

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