LF353 Wide-Bandwidth JFET-Input Dual Operational Amplifier

1 Features

- Low Input Bias Current 50 pA Typical
- Low Input Noise Current 0.01 pA/√Hz Typical
- Low Supply Current 3.6 mA Typical
- High Input Impedance 10^{12} Ω Typical
- Internally-Trimmed Offset Voltage
- Gain Bandwidth 3 MHz Typical
- High Slew Rate 13 V/µs Typical

2 Applications

- Motor Integrated Systems: UPS
- Drives and Control Solutions: AC Inverter and VF Drives
- Renewables: Solar Inverters
- Pro Audio Mixers
- Oscilloscopes

3 Description

This LF353 device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF353 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

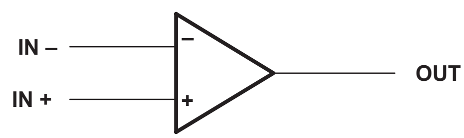
The LF353 is characterized for operation from 0°C to 70°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LF353D	SOIC (8)	4.90 mm × 3.91 mm
LF353P	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Symbol



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4 Revision History

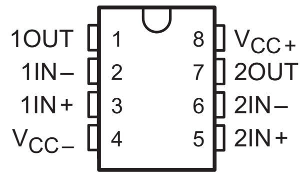
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 1994) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

5 Pin Configuration and Functions

D or P Package
8-Pin SOIC or PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1OUT	1	O	Output
1IN-	2	I	Inverting input
1IN+	3	I	Noninverting input
V_{CC-}	4	—	Negative supply voltage
2IN+	5	I	Noninverting input
2IN-	6	I	Inverting input
2OUT	7	O	Output
V_{CC+}	8	—	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{CC+}	Supply voltage		18	V
V_{CC-}	Supply voltage		–18	V
VID	Differential input voltage		±30	V
VI	Input voltage[(2)]		±15	V
	Duration of output short circuit	Unlimited		s
	Continuous total power dissipation		500	mW
	Lead temperature 1.6 mm (1/16 inch) from case for 10 s		260	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	3.5	18	V
V_{CC-}	Supply voltage	–3.5	–18	V
V_{CM}	Common-mode voltage	$V_{CC-} + 4$	$V_{CC+} - 4$	V
T_A	Operating temperature	0	70	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		LF353		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.6	55.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.5	32.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.8	22.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.1	32.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 0°C to 70°C, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ	T_A = 25°C		5	10	mV
			Full range[1]			13	
α_{VIO}	Average temperature coefficient of inputs offset voltage	V_{IC} = 0, R_S = 10 kΩ			10		µV/°C
I_{IO}	Input offset current[2]	V_{IC} = 0	T_A = 25°C		25	100	pA
			T_A = 70°C			4	nA
I_{IB}	Input bias current[2]	V_{IC} = 0	T_A = 25°C		50	200	pA
			T_A = 70°C			8	nA
V_{ICR}	Common-mode input voltage range	Lower limit of range		–11	–12		V
		Upper limit of range		11	15		
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	100		V/mV
			Full range[1]	15			
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ		70	100		dB
k_{SVR}	Supply-voltage rejection ratio	See [3]		70	100		dB
I_{CC}	Supply current				3.6	6.5	mA

(1) Full range is 0°C to 70°C
(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
(3) Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

6.6 Switching Characteristics

$V_{CC\pm}$ = ±15 V, T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/µs
B1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 20 Ω		18		$nV/\sqrt{Hz}$
I_n	Equivalent input noise current	f = 1 kHz		0.01		$pA/\sqrt{Hz}$

6.7 Typical Characteristics

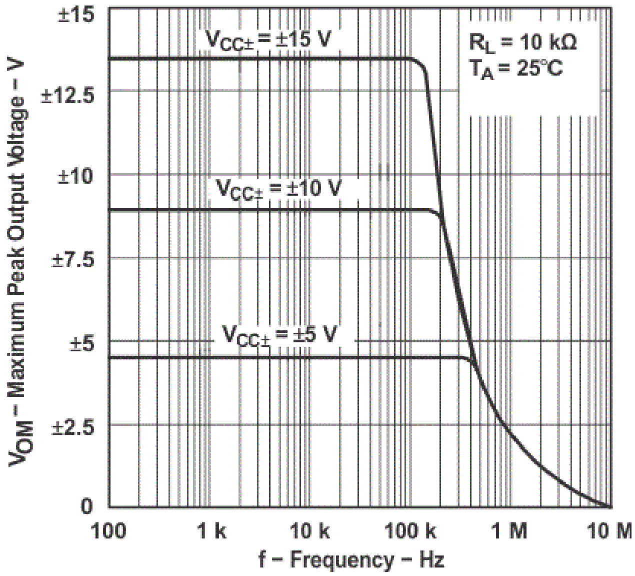


Figure 1. Maximum Peak Output Voltage vs Frequency

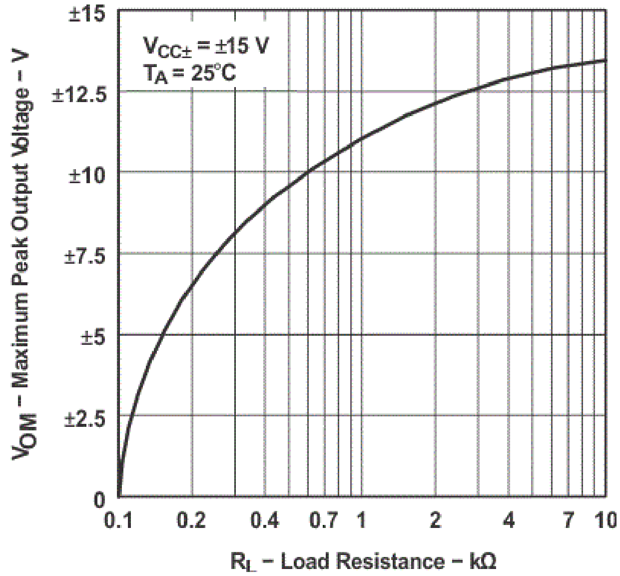


Figure 2. Maximum Peak Output Voltage vs Load Resistance

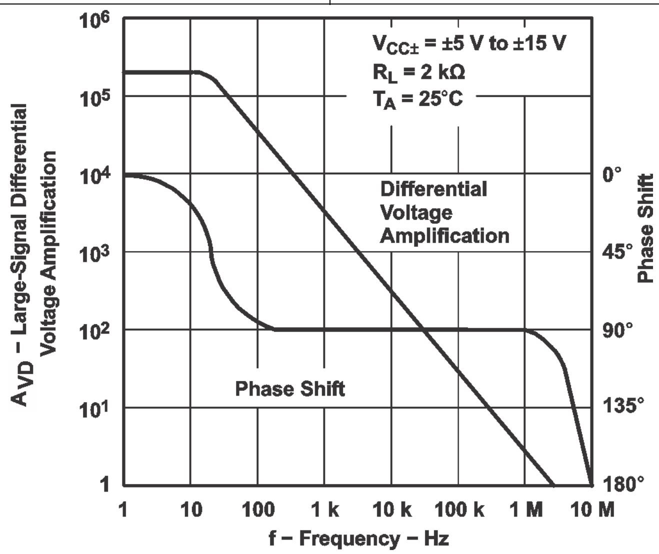


Figure 3. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

7 Parameter Measurement Information

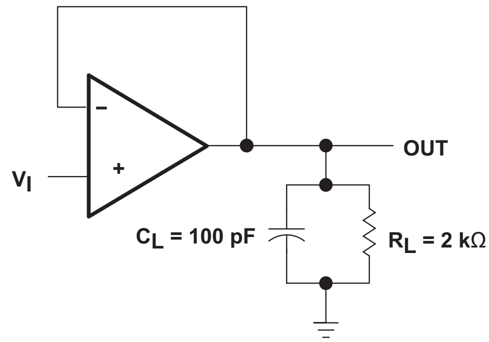


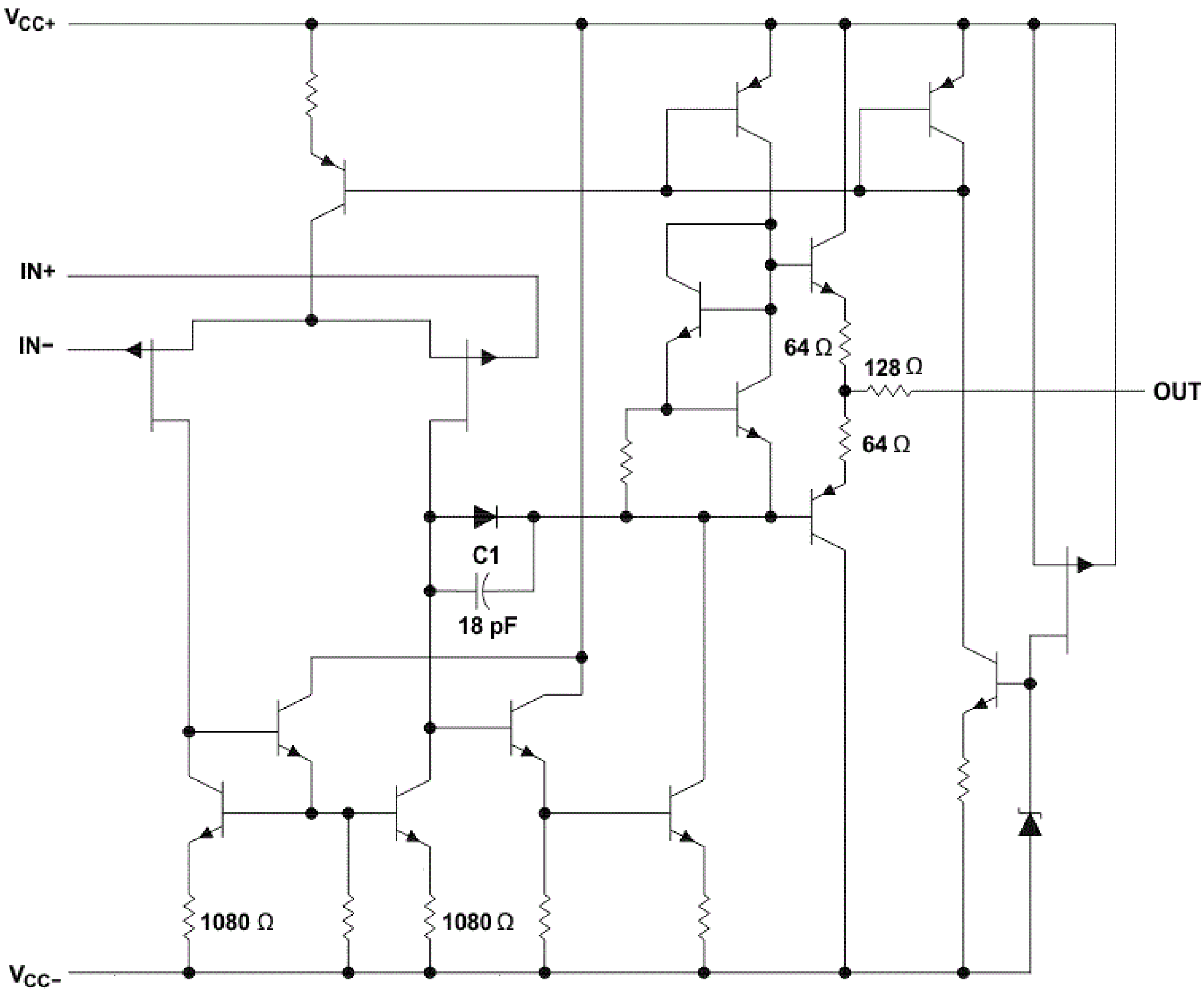
Figure 4. Unity-Gain Amplifier

8 Detailed Description

8.1 Overview

The LF353 device is a JFET-input operational amplifier with low input bias and offset currents and fast slew rate. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip. The output is protected against shorts due to the resistive 200-Ω output impedance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LF353 has two independent amplifiers that have very low input bias current which allow using higher resistance resistors in the feedback network. The upper input common mode range goes to the upper supply rail. The lower common mode range does not include the negative supply rail. Output resistance is 200 ohms to protect the device from accidental shorts.

9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage. In the same manner, it also makes negative voltages positive.

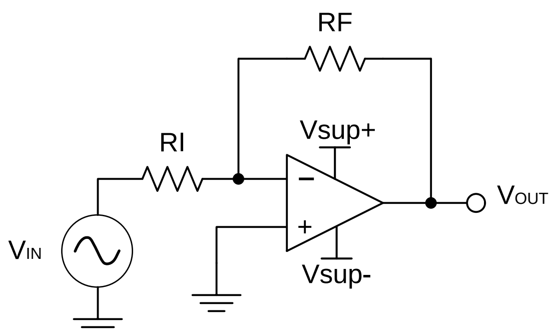


Figure 5. Inverting Amplifier

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2.

$$A_V = \frac{VOUT}{VIN} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit uses currents in the mA range. This ensures the part does draw too much current. For this example, choose 10 kΩ for RI and 36 kΩ for RF, as shown in Equation 3.

$$A_V = -\frac{RF}{RI} \tag{3}$$

Typical Application (continued)

9.2.3 Application Curve

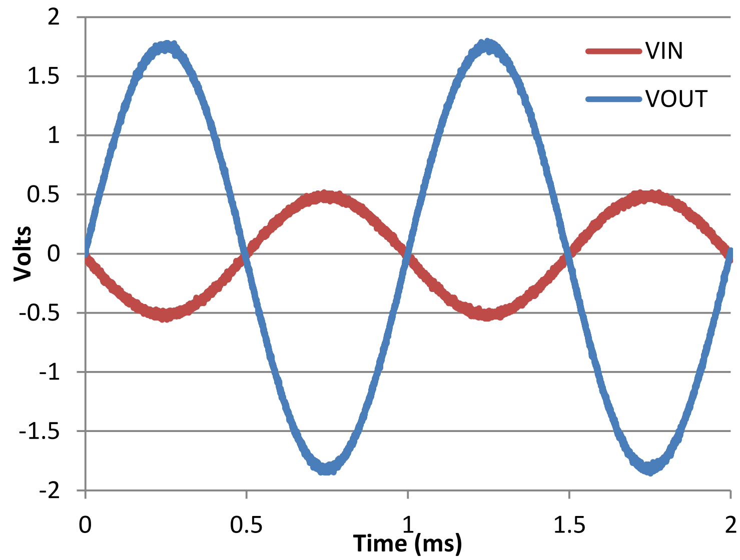


Figure 6. Input and Output Voltages of the Inverting Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Example*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use the following layout guidelines:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

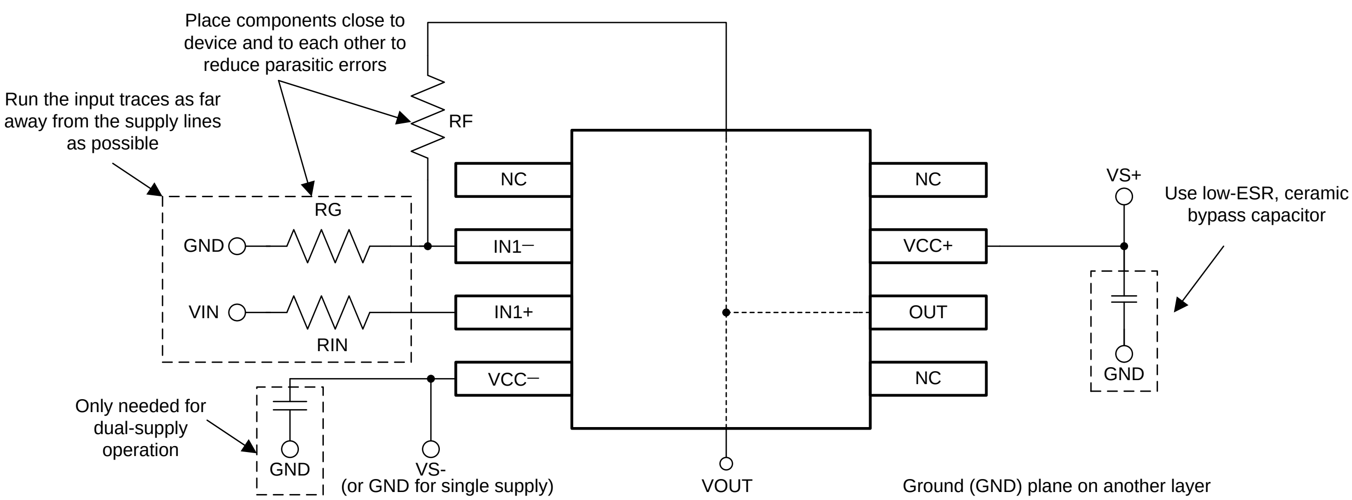


Figure 7. Operational Amplifier Board Layout for Noninverting Configuration

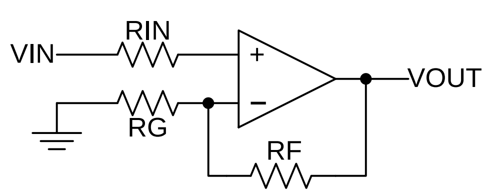


Figure 8. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see *Circuit Board Layout Techniques* (SLOA089).

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF353DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF353
LF353DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF353
LF353P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF353P
LF353P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LF353P
LF353PE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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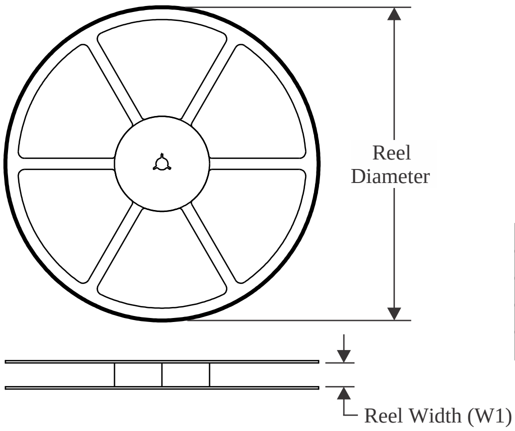
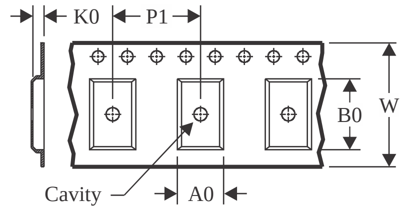
TAPE AND REEL INFORMATION

REEL DIMENSIONS

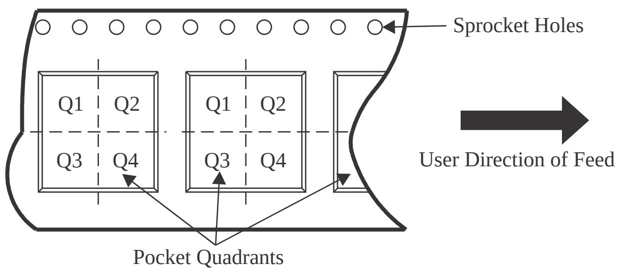


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

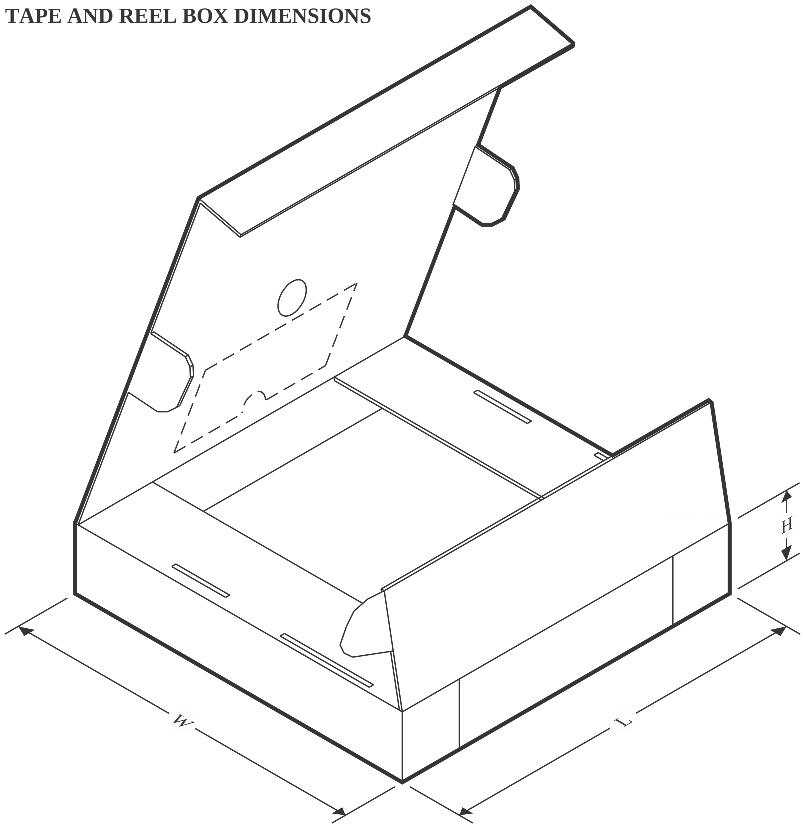
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF353DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

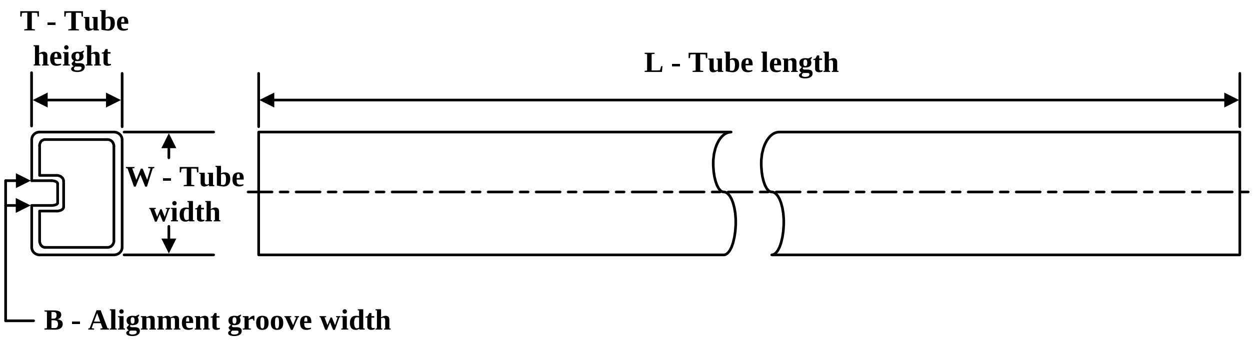
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

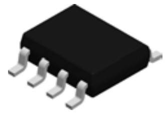
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF353DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LF353P	P	PDIP	8	50	506	13.97	11230	4.32
LF353P.A	P	PDIP	8	50	506	13.97	11230	4.32

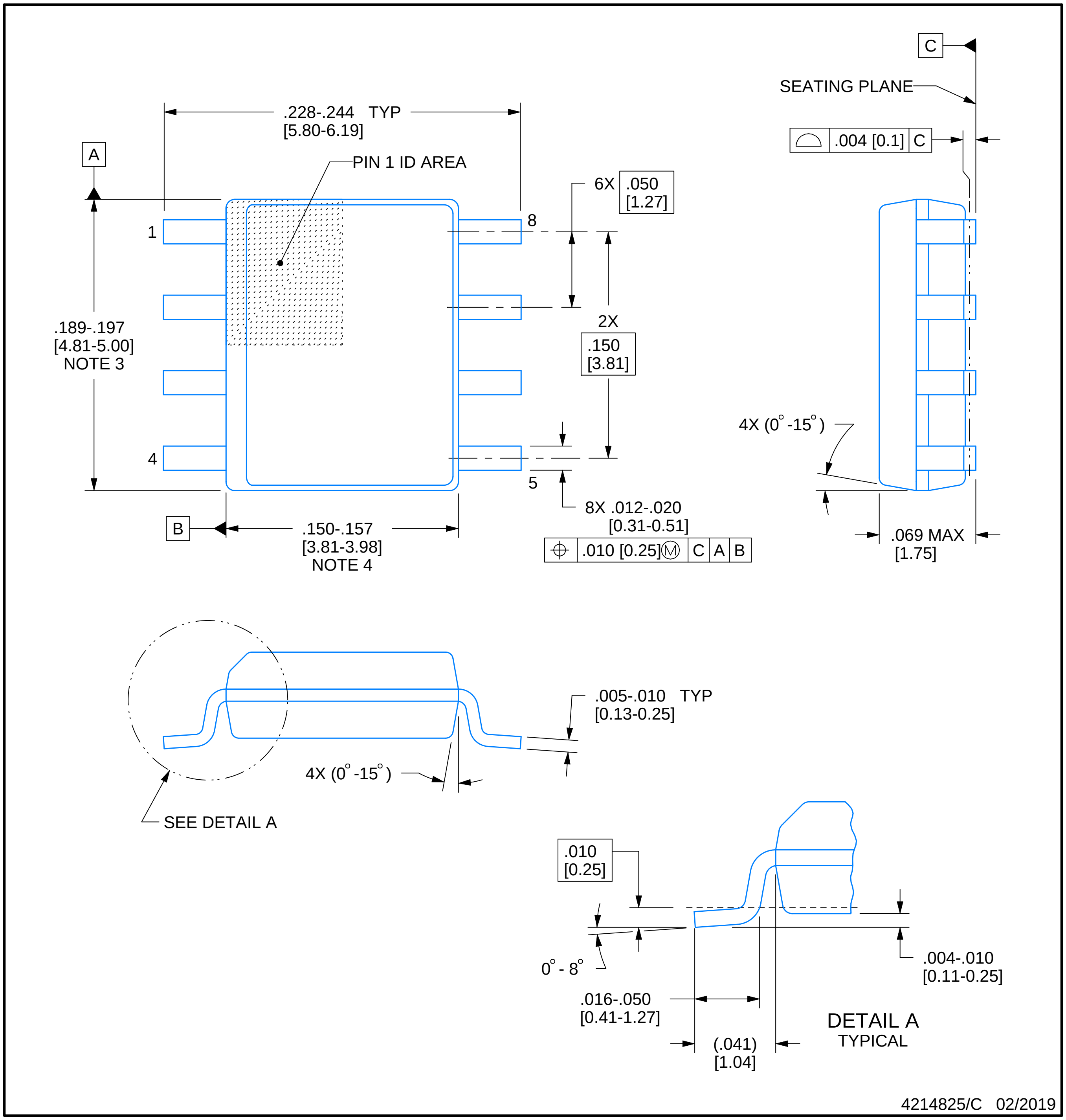


PACKAGE OUTLINE

D0008A

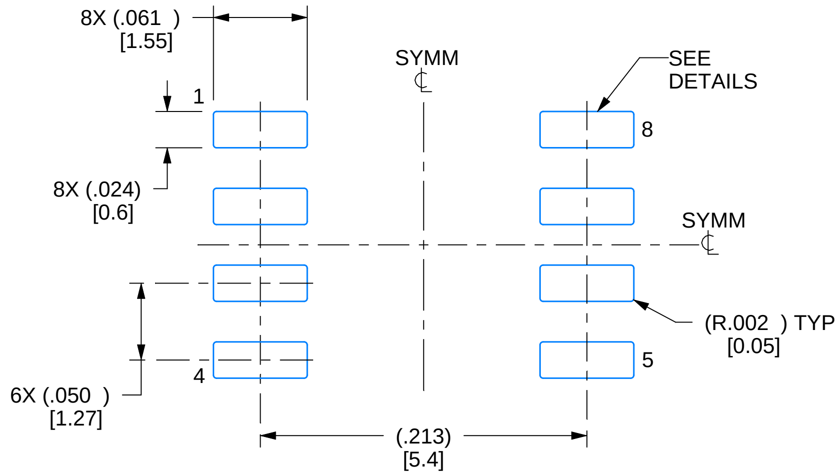
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

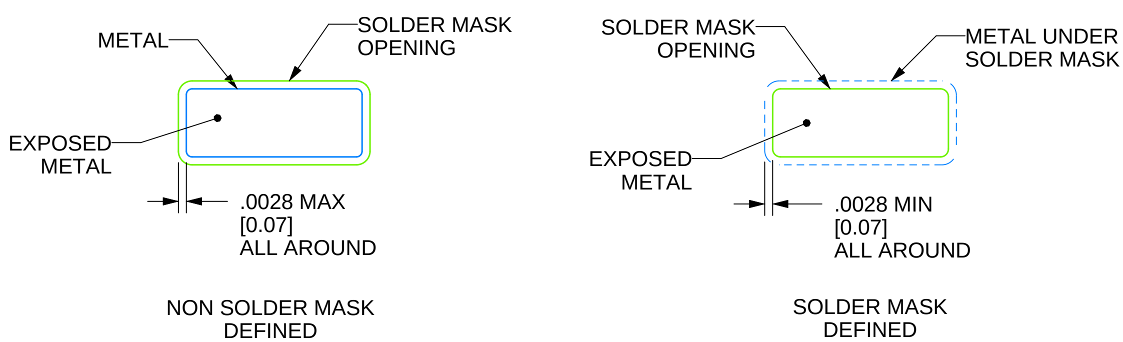


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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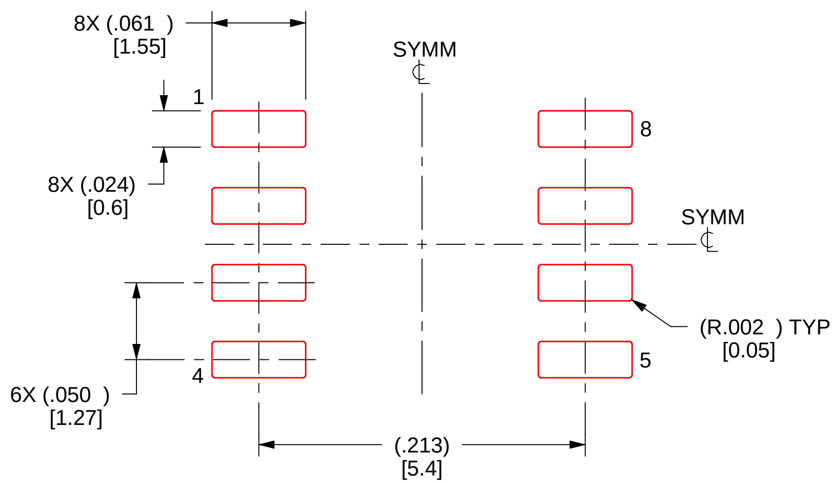
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



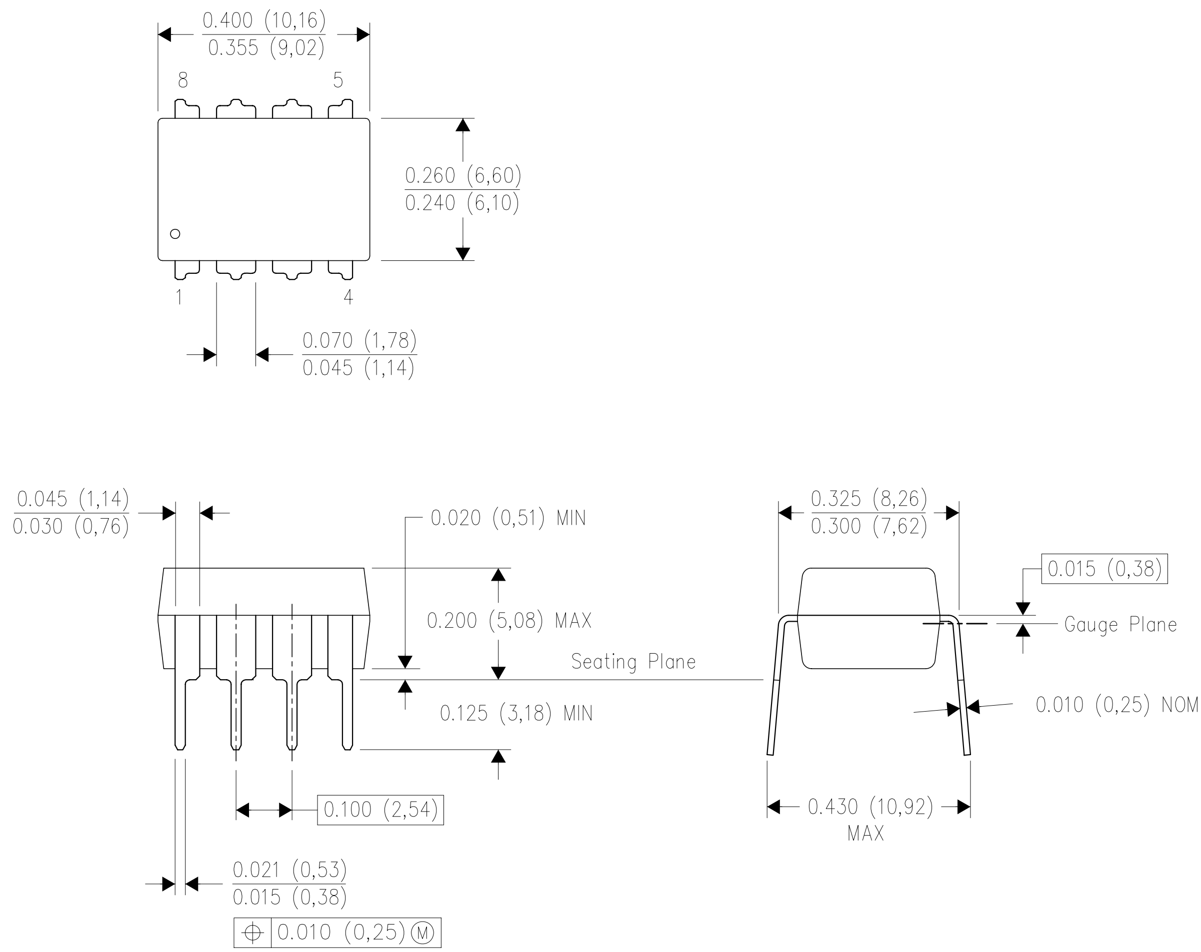
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

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