LDC1041：8 位 Rp，24 位 L 电感数字转换器，具有串行外设接口 (SPI)

1 特性

- 远程传感器放置（从恶劣环境中将 LDC 去耦合）
- 高耐久性（借助于遥控操作）
- 针对系统设计的更高灵活性（将线圈或弹簧用作传感器）
- 对于非导电环境干扰（诸如尘土、灰尘和油等）不敏感
- 无磁体操作
- 亚微米高精度
- 电源电压：典型值 5V
- 电源电压，IO：1.8V 至 5.5V
- 待机电流：典型值 250uA
- Rp 分辨率：8 位
- L 分辨率：24 位
- LC 频率范围：5kHz 至 5MHz

2 应用范围

- 水平感测
- 邻近感测
- 弹簧运动感测
- 横向和角位置感测
- 金属成分检测

3 说明

电感感测是一种非接触式、短程感测技术，此技术可实现对导电目标的高分辨率和低成本位置感测，即使在恶劣的环境中也是如此。 通过将一个线圈或弹簧用作传感器，LDC1041 电感数字转换器为系统设计人员提供了一个方法，用低于其他竞争解决方案的系统成本实现高性能和可靠性。

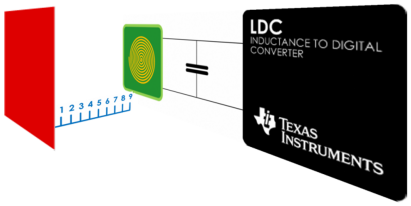
LDC1041 与 LDC1000（16 位 / 24 位 L）和 LDC1051（8 位 Rp）引脚兼容。 此器件系列根据系统设计人员的应用和系统要求为他们提供不同的分辨率选项。

LDC1041 采用 5mm x 4mm 超薄小外形尺寸无引线 (WSON)-16 封装。 经由 SPI 的器件编程可使用微控制器实现轻松配置。

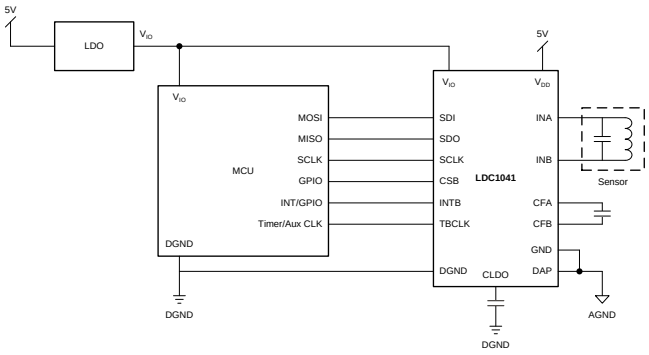
器件信息

订货编号	封装	封装尺寸
LDC1041NHRT	WSON (16)	5mm x 4mm
LDC1041NHRR	WSON (16)	5mm x 4mm
LDC1041NHRJ	WSON (16)	5mm x 4mm

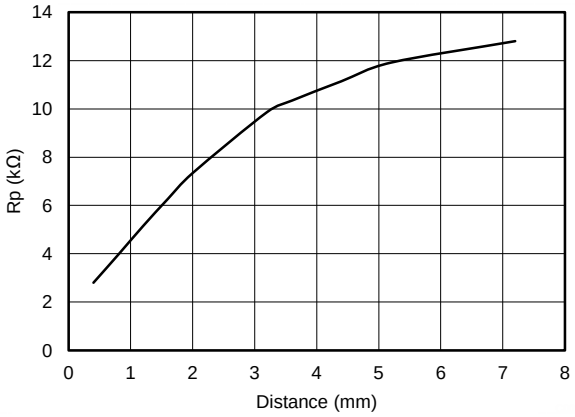
轴距感测应用



应用电路原理图



使用 **14mm** 印刷电路板 **(PCB)** 线圈时 **Rp** 与距离之间的关系



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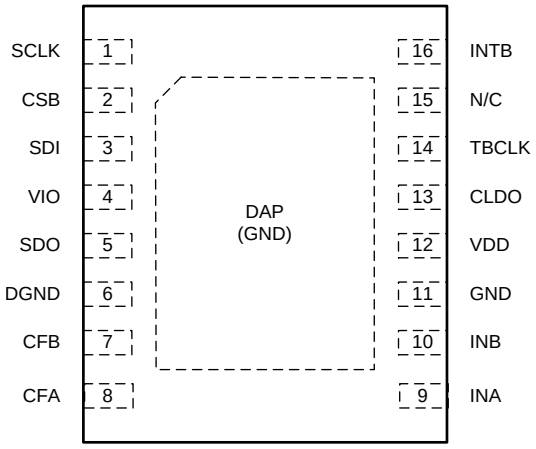
4 修订历史记录

日期	修订版本	注释
2014 年 3 月	*	最初发布。

5 Terminal Configuration and Functions

WSON-16
Top View



Terminal Description

TERMINAL NAME	TERMINAL NO.	TERMINAL TYPE (1)	FUNCTION
SCLK	1	DO	SPI clock input. SCLK is used to clock-out/clock-in the data from/into the chip
CSB	2	DI	SPI CSB(Chip Select Bar). Multiple devices can be connected on the same SPI bus and CSB can be used to select the device to be communicated with
SDI	3	DI	SPI Slave Data In (Master Out Slave In). This should be connected to the Master Out Slave In of the master
VIO	4	P	Digital IO Supply
SDO	5	DO	SPI Slave Data Out (Master In Slave Out).It is high impedance when CSB is high
DGND	6	P	Digital ground
CFB	7	A	LDC filter capacitor
CFA	8	A	LDC filter capacitor
INA	9	A	External LC Tank. Connect to external LC tank
INB	10	A	External LC Tank. Connect to external LC tank
GND	11	P	Analog ground
VDD	12	P	Analog supply
CLDO	13	A	LDO bypass capacitor. A 56nF capacitor should be connected from this Terminal to GND
TBCLK	14	DI	External time-base clock
N/C	15	N/C	No Connection
INTB	16	DO	Configurable interrupt. This Terminal can be configured to behave in 3 different ways by programing the INT Terminal mode register. Either threshold detect, wakeup, or DRDYB
DAP	17	P	Connect to GND

(1) DO: Digital Output, DI: Digital Input, P: Power, A: Analog

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Analog Supply Voltage (V_{DD} – GND)		6	V
IO Supply Voltage (V_{IO} – GND)		6	V
Voltage on any Analog Terminal	–0.3	V_{DD} + 0.3	V
Voltage on any Digital Terminal	–0.3	V_{IO} + 0.3	V
Input Current on INA and INB		8	mA
Junction Temperature, T_J(2)		150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of TJ(MAX), θJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) - TA)/ θJA. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage Temperature Range	-65	150	°C
V_{ESD}(1)	Human Body Model (HBM) ESD stress voltage (2)	1k	1k	V
	Charge Device Model (CDM) ESD stress voltage(3)	250	250	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Analog Supply Voltage (V_{DD} – GND)	4.75	5.25	V
IO Supply Voltage (V_{IO} – GND)	1.8	5.25	V
V_{DD}-V_{IO}	0		V
Operating Temperature, T_A	-40	125	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

6.4 Thermal Information

THERMAL METRIC(1)		NHR (16-TERMINALS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	28	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics(1)

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$, $V_{DD} = 5$ V, $V_{IO} = 3.3$ V(2)

PARAMETER		TEST CONDITIONS	MIN(3)	TYP(4)	MAX(3)	UNIT
POWER						
V_{DD}	Analog supply voltage		4.75	5	5.25	V
V_{IO}	IO supply voltage	$V_{IO} \le V_{DD}$	1.8	3.3	5.25	V
I_{DD}	Supply current, V_{DD}	Does not include sensor current.(5)		1.7	2.3	mA
I_{VIO}	IO supply current	Static current			14	µA
I_{DD_LP}	Stand-by mode supply current			250		µA
t_{START}	Start-Up Time	From POR to ready-to-convert.		2		ms
LDC						
f_{sensor_MIN}	Minimum sensor frequency			5		kHz
f_{sensor_MAX}	Maximum sensor frequency			5		MHz
A_{sensor_MIN}	Minimum sensor amplitude			1		V_{PP}
A_{sensor_MAX}	Maximum sensor amplitude			4		V_{PP}
t_{REC}	Recovery time	Oscillation start-up time after Rp under-range condition		10		$1/f_{sensor}$
Rp Min	Minimum sensor Rp range			798		Ω
Rp Max	Maximum Sensor Rp range			3.93		MΩ
Rp Res	Rp measurement resolution			8		Bits
L Res	Inductance measurement resolution			24		Bits
t_{S_MIN}	Minimum response time	Minimum programmable settling time of digital filter		192 × 1 / f_{sensor}		s
t_{S_MAX}	Maximum response time	Maximum programmable settling time of digital filter		6144 × 1 / f_{sensor}		s
EXTERNAL CLOCK						
f	External clock frequency				8	MHz
DIGITAL I/O CHARACTERISTICS						
V_{IH}	Logic 1 input voltage		0.8 × V_{IO}			V
V_{IL}	Logic 0 input voltage				0.2 × V_{IO}	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 400 µA		V_{IO} – 0.3		V
V_{OL}	Logic 0 output voltage	I_{SINK} = 400 µA			0.3	V
I_{IOHL}	Digital IO leakage current		–500		500	nA

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) The maximum power dissipation is a function of TJ(MAX), θJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) - TA)/ θJA. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.
(3) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(5) LC tank current depends on the Q-factor of the tank, distance and material of the target.

6.6 Timing Requirements

Unless otherwise noted, all limits specified at T_A = 25°C, V_{DD} = 5, V_{IO} = 3.3, 10 pF capacitive load in parallel with a 10 kΩ load on the SDO terminal. Specified by design; not production tested.

PARAMETER			MIN	TYP	MAX	UNIT
f_{SCLK}	Serial Clock Frequency				4	MHz
t_{PH}	SCLK Pulse Width High	f_{SCLK} = 4 MHz	0.4 / f_{SCLK}			s
t_{PL}	SCLK Pulse Width Low	f_{SCLK} = 4 MHz	0.4 / f_{SCLK}			s
t_{SU}	SDI Setup Time		10			ns
t_H	SDI Hold Time		10			ns
t_{ODZ}	SDO Driven-to-Tristate Time	Measured at 10% / 90% point			20	ns
t_{OZD}	SDO Tristate-to-Driven Time	Measured at 10% / 90% point			20	ns
t_{OD}	SDO Output Delay Time				20	ns
t_{CSS}	CSB Setup Time		20			ns
t_{CSH}	CSB Hold Time		20			ns
t_{IAG}	Inter-Access Gap		100			ns
t_{DRDYB}	Data ready pulse width	Data ready pulse at every 1 / ODR if no data is read	1 / f_{sensor}			s

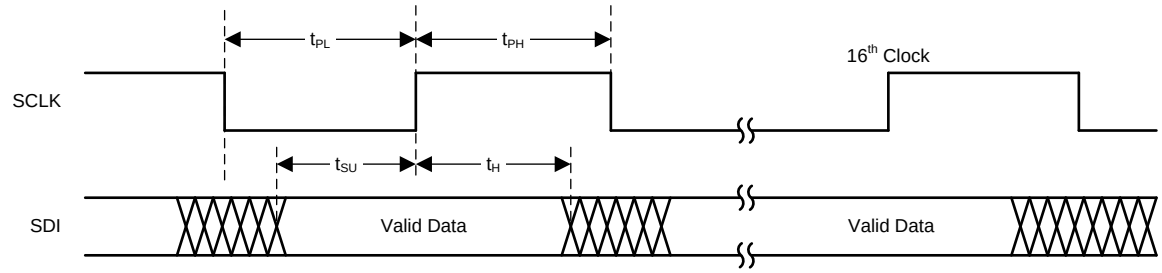


Figure 1. Write Timing Diagram

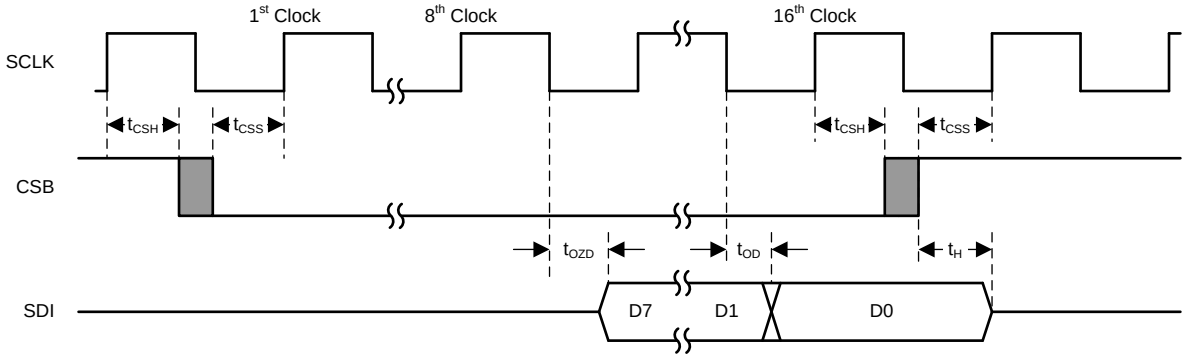
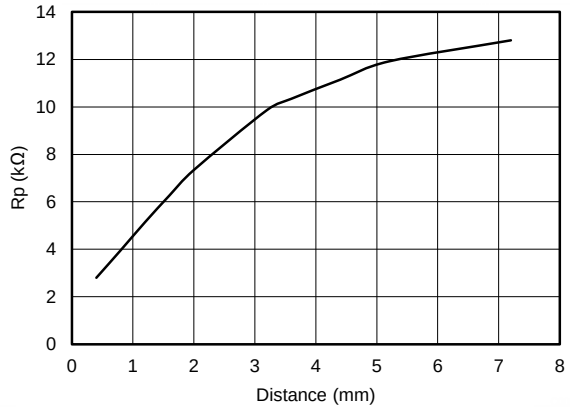


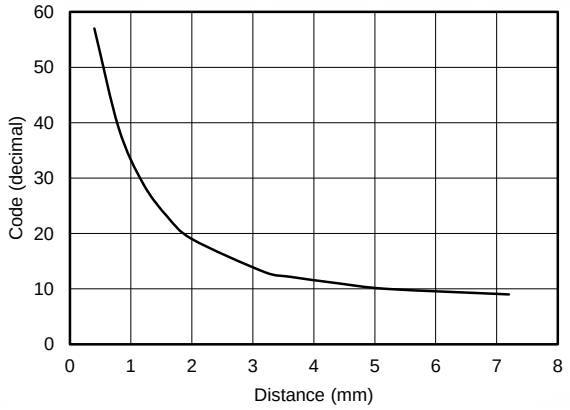
Figure 2. Read Timing Diagram

6.7 Typical Characteristics



Sensor Details:	Table 19	Rp_MIN:	1.347 kΩ
Target Material:	Stainless Steel	Rp_MAX:	38.785 kΩ

Figure 3. Rp vs Distance



Sensor Details:	Table 19	Rp_MIN:	1.347 kΩ
Target Material:	Stainless Steel	Rp_MAX:	38.785 kΩ

Figure 4. Proximity Data vs Distance

7 Detailed Description

7.1 Overview

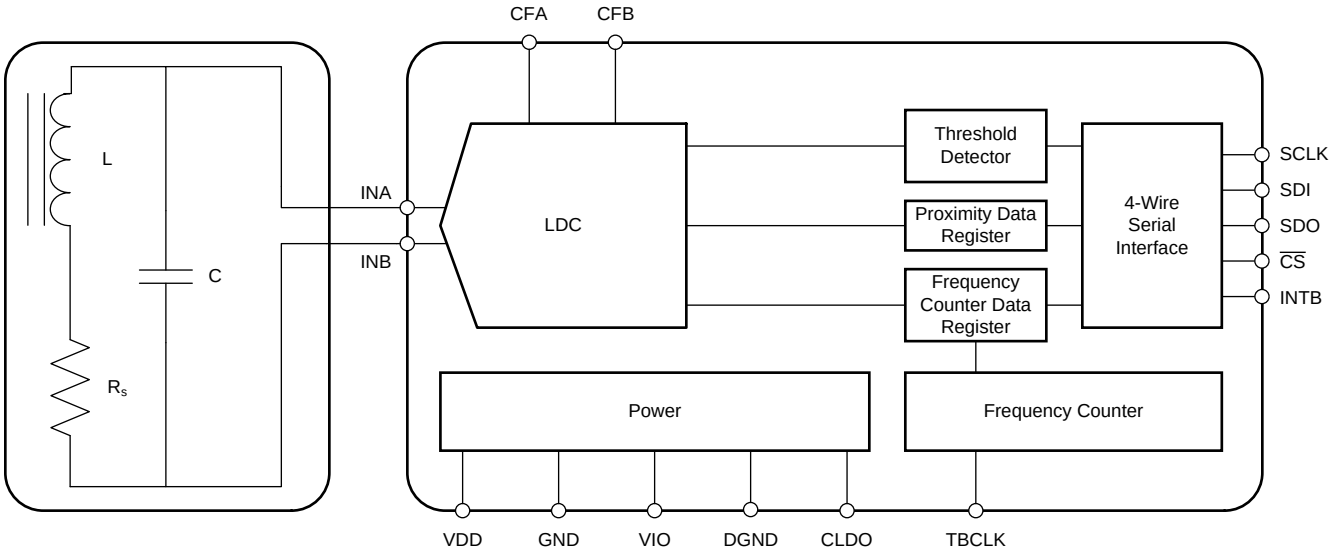
The LDC1041 is an Inductance-to-Digital Converter that simultaneously measures the impedance and resonant frequency of an LC resonator. It accomplishes this task by regulating the oscillation amplitude in a closed loop configuration to a constant level, while monitoring the energy dissipated by the resonator. By monitoring the amount of power injected into the resonator, the LDC1041 can determine the value of Rp; it returns this as a digital value which is inversely proportional to Rp. In addition, the LDC1041 also measure the oscillation frequency of the LC circuit; this frequency is used to determine the inductance of the LC circuit. The device outputs a digital value that is inversely proportional to frequency.

The threshold detector block provides a comparator with hysteresis, with the threshold registers programed and comparator enabled, proximity data register is compared with threshold registers and INTB pin indicates the output.

The device has a simple 4-wire SPI interface. The INTB pin provides multiple functions which are programmable with SPI.

The device has separate supplies for Analog and I/O, with analog operating at 5V and I/O at 1.8-5V. The integrated LDO needs a 56nF capacitor connected from CLDO pin to GND.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inductive Sensing

An AC current flowing through a coil will generate an AC magnetic field. If a conductive material, such as a metal target, is brought into the vicinity of the coil, this magnetic field will induce circulating currents (eddy currents) on the surface of the target. These eddy currents are a function of the distance, size, and composition of the target. The eddy currents then generate their own magnetic field, which opposes the original field generated by the coil. This mechanism is best compared to a transformer, where the coil is the primary core and the eddy current is the secondary core. The inductive coupling between both cores depends on distance and shape. Hence the resistance and inductance of the secondary core (eddy current), shows up as a distant dependent resistive and inductive component on the primary side (coil). Figure 5 to Figure 8 show a simplified circuit model.

Feature Description (continued)

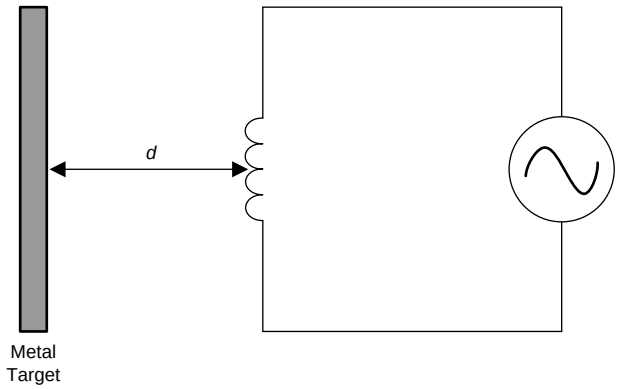


Figure 5. Inductor With A Metal Target

Eddy currents generated on the surface of the target can be modeled as a transformer as shown in Figure 6. The coupling between the primary and secondary coils is a function of the distance and the conductor's characteristics. In Figure 6, the inductance Ls is the coil's inductance, and Rs is the coil's parasitic series resistance. The inductance L(d), which is a function of distance d, is the coupled inductance of the metal target. Likewise, R(d) is the parasitic resistance of the eddy currents and is also a function of distance.

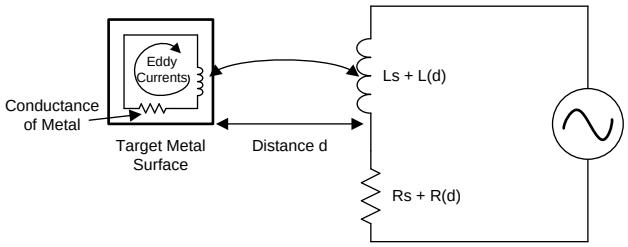


Figure 6. Metal Target Modeled As L And R With Circulating Eddy Currents

Generating an alternating magnetic field with just an inductor will consume a large amount of power. This power consumption can be reduced by adding a parallel capacitor, turning it into a resonator as shown in Figure 7 . In this manner the power consumption is reduced to the eddy and inductor losses Rs+R(d) only.

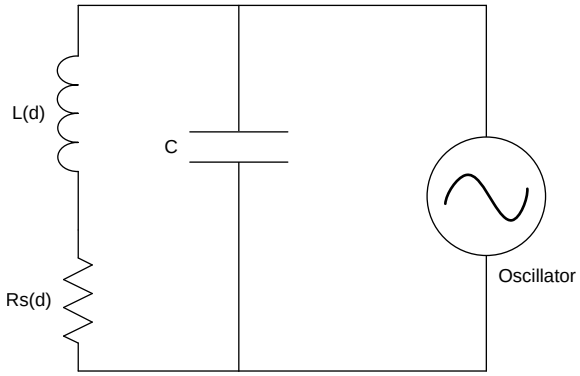


Figure 7. LC Tank Connected To Oscillator

The LDC1041 doesn't measure the series resistance directly; instead it measures the equivalent parallel resonance impedance Rp (see Figure 8). This representation is equivalent to the one shown in Figure 8 , where the parallel resonance impedance Rp(d) is given by:

Feature Description (continued)

$$Rp(d) = \frac{Ls + L(d)}{[Rs + R(d)] \times C} \quad (1)$$

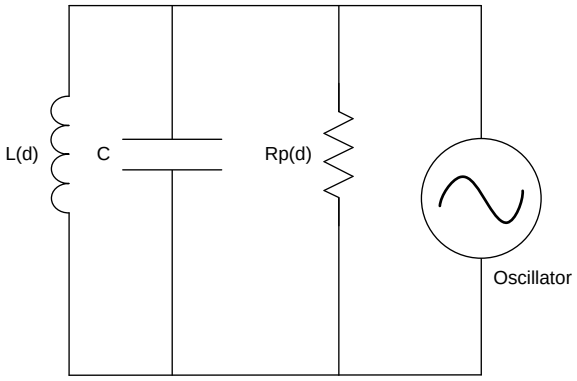


Figure 8. Equivalent Resistance Of Rs in Parallel With LC Tank

Figure 9 below shows the variation in Rp as a function of distance for a 14mm diameter PCB coil (Sensor Details:Table 19). The target in this example is a section of a 2mm thick stainless steel disk.

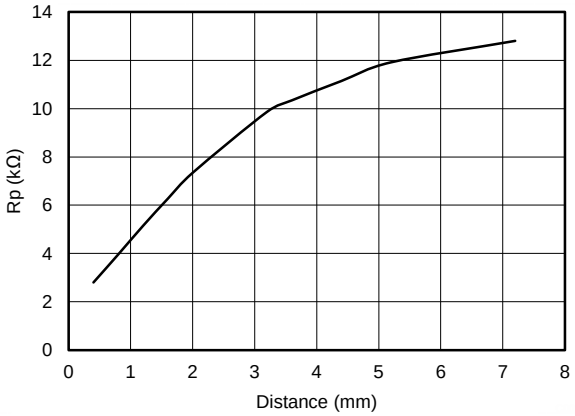


Figure 9. Typical Rp vs Distance With 14mm PCB Coil

Feature Description (continued)

7.3.2 Measuring Rp with LDC1041

The LDC1041 supports a wide range of LC combinations, with oscillation frequencies ranging from 5kHz to 5MHz and Rp ranging from 798Ω to 3.93MΩ. This range of Rp can be viewed as the maximum input range of an ADC. As illustrated in Figure 9, the range of Rp is typically much smaller than the maximum input range supported by the LDC1041. To get better resolution in the desired sensing range, the LDC1041 offers a programmable input range through the Rp_MIN and Rp_MAX registers. Refer to Calculation of Rp_MIN and Rp_MAX below for how to set these registers.

When the sensor's resonance impedance Rp drops below the programed Rp_MIN, the LDC's Rp output will clip at its full scale output. This situation could, for example, happen when a target comes too close to the coil.

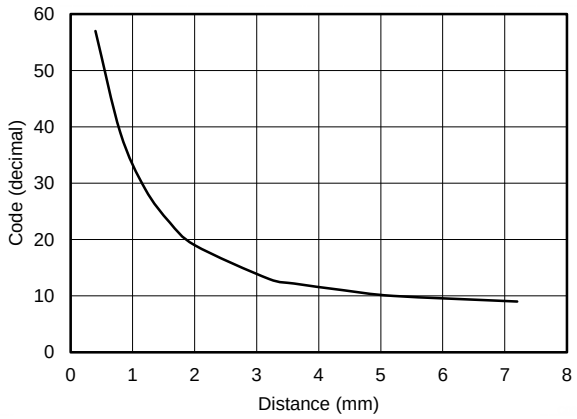


Figure 10. Transfer Characteristics Of LDC1041 With Rp_MIN= 1.347 kΩ And Rp_MAX= 38.785 kΩ

The resonance impedance can be calculated from the digital output code as follows:

$$Rp = \frac{Rp\_MAX \times Rp\_MIN}{Rp\_MIN \times (1 - Y) + Rp\_MAX \times Y}$$

Where:

- Y=Proximity Data/2^7
- Rp_MAX and Rp_MIN are the maximum and minimum Rp values selected in the respective registers
- Proximity data is the LDC output, register address 0x22. (2)

Example: If Proximity data (address 0x22) is 50, Rp_MIN is 2.394 kΩ, and Rp_MAX is 38.785 kΩ, the resonance impedance is given by:

Y=50/2^7 = 0.3906

Rp=(38785*2394)/(2394×(1-0.3906) + 38785×0.3906) =(92851290)/(15149.421 + 1458.9036)

Rp = 5.59 kΩ

7.3.3 Measuring Inductance with LDC1041

LDC1041 measures the sensor's frequency of oscillation using a frequency counter. The frequency counter timing is set by an external clock applied on TBCLK terminal. The sensor frequency can be calculated from the frequency counter register value (see registers 0x23 through 0x25) as follows:

$$\text{Sensor frequency, } f_{sensor} = \frac{1}{3} \times \frac{Fext}{Fcount} \times \text{Response time}$$

where

- Fext is the frequency of the external clock
- Fcount is the value obtained from the Frequency Counter Data register(address 0x23,0x24,0x25)
- Response Time is the programmed response time (see LDC configuration register, address 0x04) (3)

Feature Description (continued)

The sensor inductance can be determined by:

$$L = \frac{1}{C \times (2\pi \times f_{sensor})^2}$$

where

- C is the parallel capacitance of the resonator (4)

Example: If Fext=6MHz, Response time=6144, C=100pF and measured Fcount= 3000 (dec) (address 0x23 through 0x25)

f_{sensor}=(1/3)*(6000000/3000)*(6144)= 4.096MHz

Now using, $L = \frac{1}{C \times (2\pi \times f_{sensor})^2}$

Inductance, L = 15.098 µH

The accuracy of measurement largely depends upon the choice of the external time-base clock (TBCLK). A higher frequency will provide better measurement accuracy.

7.4 Device Functional Modes

7.4.1 Power Modes

The LDC1041 has two power modes:

1. Active Mode : In this mode the Proximity data and frequency data conversion is enabled.
2. Stand-by Mode: This is the default mode on device power-up. In this mode conversion is disabled.

7.4.2 INTB Pin Modes

The INTB terminal is a configurable output terminal which can be used to drive an interrupt on an MCU. The LDC1041 provides three different modes on INTB terminal:

1. Comparator Mode
2. Wake-Up Mode
3. DRDY Mode

LDC1041 has built-in High and Low trigger threshold registers which can be used as a comparator with programmable hysteresis or in a special mode which can be used to wake-up an MCU. These modes are explained in detail below.

7.4.2.1 Comparator Mode

In the Comparator mode, the INTB terminal is asserted or deasserted when the proximity register value increases above Threshold High or decreases below Threshold Low registers respectively. In this mode, the LDC1041 essentially behaves as a proximity switch with programmable hysteresis.

Device Functional Modes (continued)

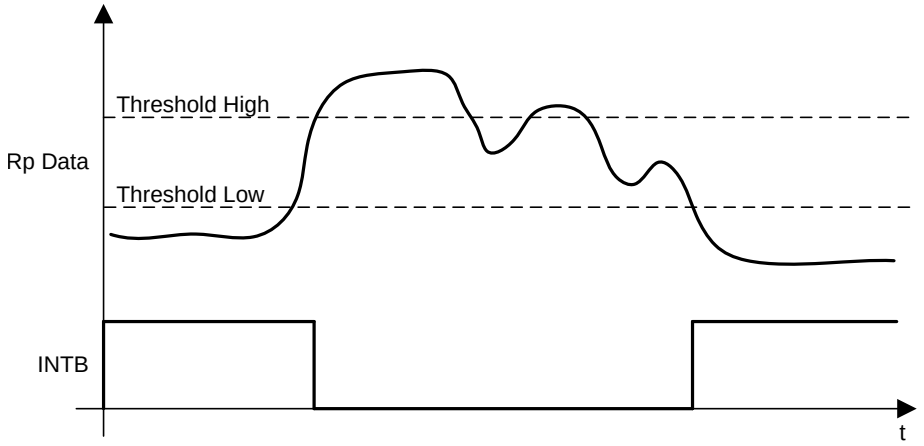


Figure 11. Behavior Of INTB Terminal In Comparator Mode

7.4.2.2 Wake-Up Mode

In Wake-Up mode, the INTB terminal is asserted when proximity register value increases above Threshold High and de-asserted when wake-up mode is disabled in INTB terminal mode register.

This mode can be used to wake-up an MCU from sleep, to conserve power.

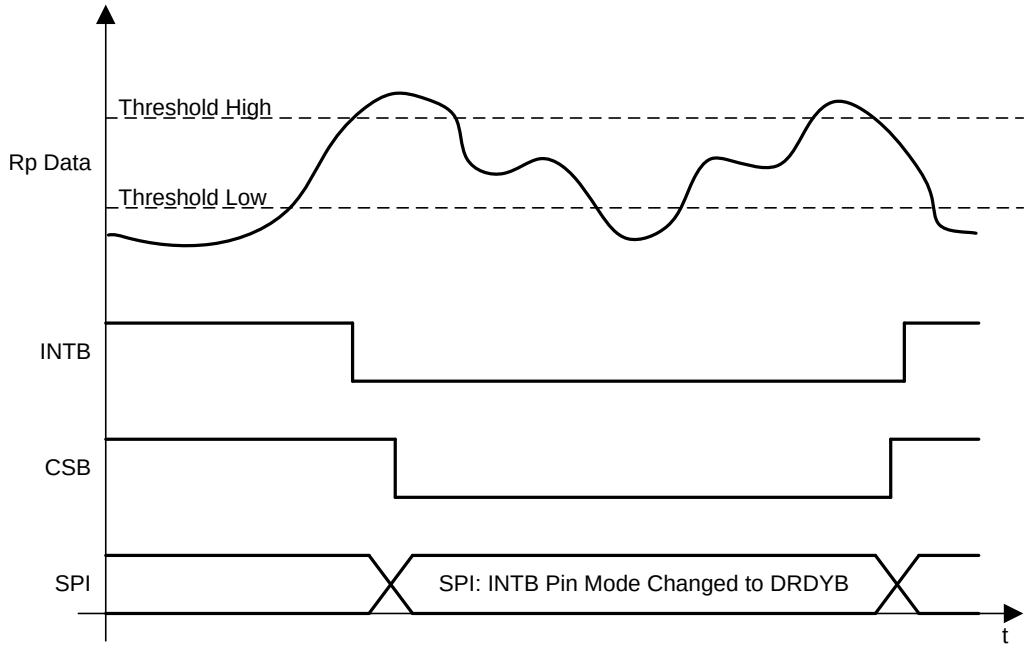


Figure 12. Behavior Of INTB Terminal In Wake-Up Mode

7.4.2.3 DRDYB Mode

In DRDY(Data Ready) mode, the INTB terminal is asserted every time the conversion data is available and de-asserted once the read command on register 0x22 is registered internally; if the read is in progress, the terminal is pulsed instead. The valid condition for new data availability is CSB high and DRDYB falling edge.

Device Functional Modes (continued)

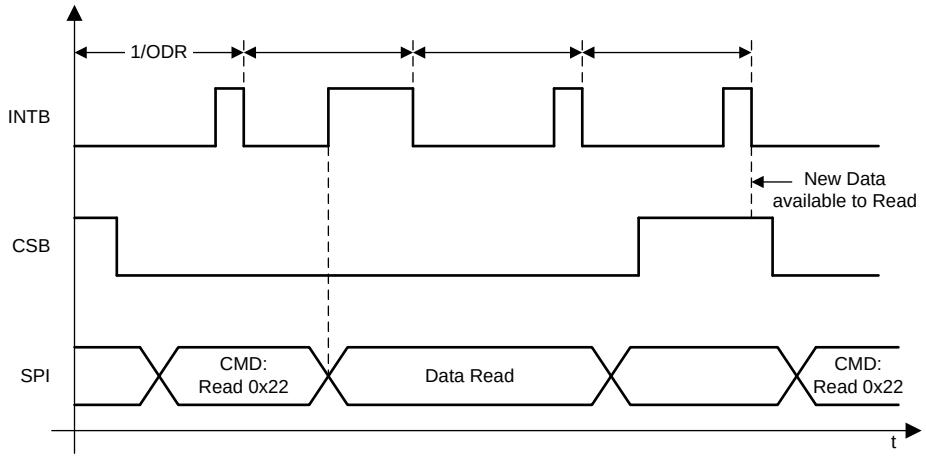


Figure 13. Behavior of INTB Terminal in DRDYB Mode with SPI Extending Beyond Subsequent Conversions

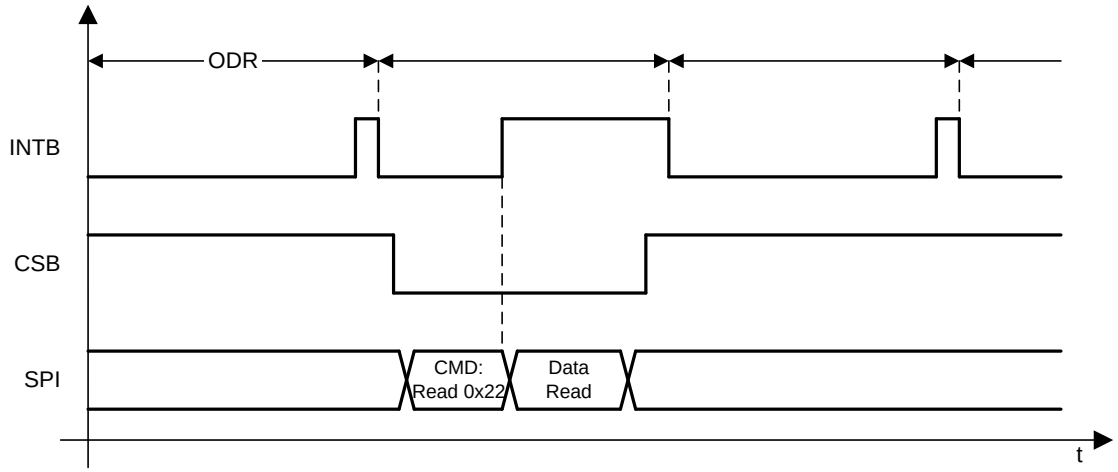


Figure 14. Behavior Of INTB Terminal In DRDYB Mode with SPI Reading The Data Within Subsequent Conversion

7.5 Programming

The LDC1041 utilizes a 4-wire SPI to access control and data registers. The LDC1041 is an SPI slave device and does not initiate any transactions.

7.5.1 SPI Description

A typical serial interface transaction begins with an 8-bit instruction, which is comprised of a read/write bit (MSB, R=1) and a 7 bit address of the register, followed by a data field which is typically 8 bits. However, the data field can be extended to a multiple of 8 bits by providing sufficient SPI clocks. Refer to the Extended SPI Transactions section below.

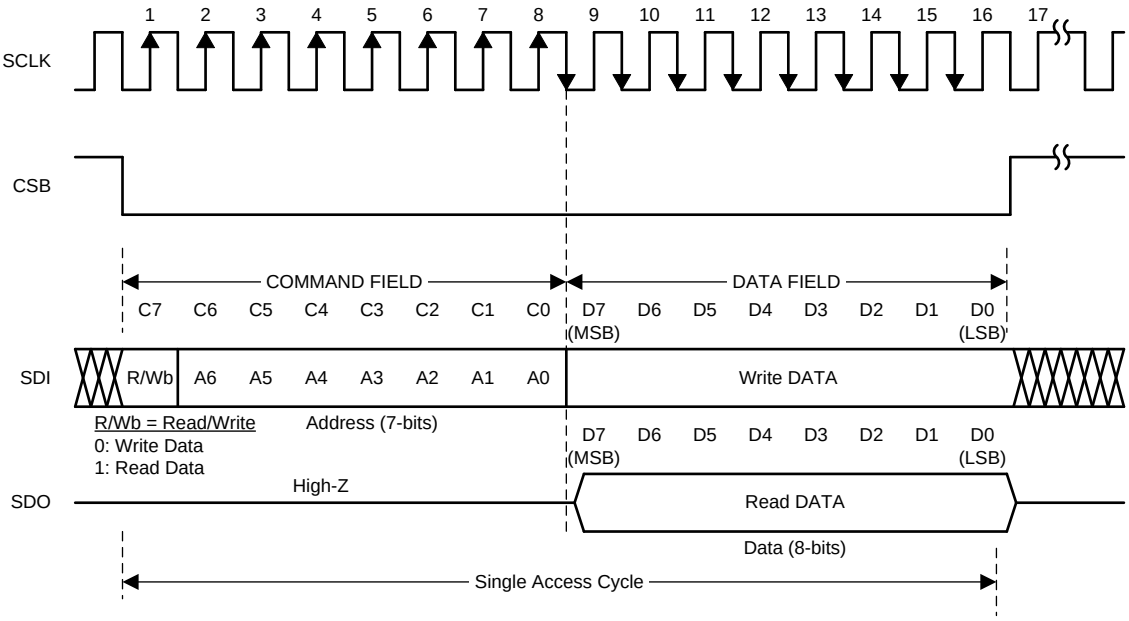


Figure 15. Serial Interface Protocol

Each assertion of CSB starts a new register access. The R/Wb bit in the command field configures the direction of the access; a value of 0 indicates a write operation and a value of 1 indicates a read operation. All output data is driven on the falling edge of the serial clock (SCLK), and all input data is sampled on the rising edge of the serial clock (SCLK). Data is written into the register on the rising edge of the 16th clock. It is required to deassert CSB after the 16th clock; if CSB is deasserted before the 16th clock, no data write will occur.

7.5.1.1 Extended SPI Transactions

A transaction may be extended to multiple registers by keeping the CSB asserted beyond the initial 16 clocks. In this mode, the register addresses increment automatically. CSB must be asserted during 8*(1+N) clock cycles of SCLK, where N is the amount of bytes to write or read during the transaction.

During an extended read access, SDO outputs the register contents every 8 clock cycles after the initial 8 clocks of the command field. During an extended write access, the data is written to the registers every 8 clock cycles after the initial 8 clocks of the command field.

Extended transactions can be used to read 8-bits of Proximity data and 24-bits of frequency data in a single SPI transaction by initiating a read from the register 0x22.

7.6 Register Map and Description

Table 1. Register Map(1)(2)(3)

Register Name	Address	Direction	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device ID	0x00	RO	0x84	Device ID							
Rp_MAX	0x01	R/W	0x0E	Rp Maximum							
Rp_MIN	0x02	R/W	0x14	Rp Minimum							
Watchdog Timer Frequency	0x03	R/W	0x45	Min Sensor Frequency							
LDC Configuration	0x04	R/W	0x1B	Reserved(000)			Amplitude		Response Time		
Reserved	0x05	RO	0x01	Reserved(00000001)							
Reserved	0x06	R/W	0xFF	Reserved							
Comparator Threshold High MSB	0x07	R/W	0xFF	Threshold High MSB							
Reserved	0x08	R/W	0x00	Reserved							
Comparator Threshold Low MSB	0x09	R/W	0x00	Threshold Low MSB							
INTB Terminal Configuration	0x0A	R/W	0x00	Reserved(00000)					INTB_MODE		
Power Configuration	0x0B	R/W	0x00	Reserved(0000000)							PWR_MODE
Status	0x20	RO		OSC Dead	DRDYB	Wake-up	Comparator	Do Not Care			
Reserved	0x21	RO		Reserved(00000000)							
Proximity Data	0x22	RO		Proximity Data							
Frequency Counter Data LSB	0x23	RO		FCOUNT LSB							
Frequency Counter Data Mid-Byte	0x24	RO		FCOUNT Mid Byte							
Frequency Counter Data MSB	0x25	RO		FCOUNT MSB							

(1) Values of register fields which are unused should be set to default values only.
(2) Registers 0x01 through 0x05 are Read Only when the part is awake (PWR_MODE bit is SET)
(3) R/W: Read/Write. RO: Read Only. WO: Write Only.

Table 2. Revision ID

Address = 0x00, Default=0x84, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	Revision ID	Revision ID of Silicon.

Table 3. Rp_MAX

Address = 0x01, Default=0x0E, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Rp Maximum	Maximum Rp that LDC1041 needs to measure. Configures the input dynamic range of LDC1041. See Table 4 for register settings.

Table 4. Register Settings for Rp_MAX

Register setting	Rp (kΩ)
0x00	3926.991
0x01	3141.593
0x02	2243.995
0x03	1745.329
0x04	1308.997
0x05	981.748
0x06	747.998
0x07	581.776
0x08	436.332
0x09	349.066
0x0A	249.333
0x0B	193.926
0x0C	145.444
0x0D	109.083
0x0E	83.111
0x0F	64.642
0x10	48.481
0x11	38.785
0x12	27.704
0x13	21.547
0x14	16.160
0x15	12.120
0x16	9.235
0x17	7.182
0x18	5.387
0x19	4.309
0x1A	3.078
0x1B	2.394
0x1C	1.796
0x1D	1.347
0x1E	1.026
0x1F	0.798

Table 5. Rp_MIN

Address = 0x02, Default=0x14, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Rp Minimum	Minimum Rp that LDC1041 needs to measure. Configures the input dynamic range of LDC1041. See Table 6 for register settings.(1)

(1) This Register needs a mandatory write as it defaults to 0x14.

Table 6. Register Settings for Rp_MIN

Register setting	Rp (kΩ)
0x20	3926.991
0x21	3141.593
0x22	2243.995
0x23	1745.329
0x24	1308.997
0x25	981.748
0x26	747.998
0x27	581.776
0x28	436.332
0x29	349.066
0x2A	249.333
0x2B	193.926
0x2C	145.444
0x2D	109.083
0x2E	83.111
0x2F	64.642
0x30	48.481
0x31	38.785
0x32	27.704
0x33	21.547
0x34	16.160
0x35	12.120
0x36	9.235
0x37	7.182
0x38	5.387
0x39	4.309
0x3A	3.078
0x3B	2.394
0x3C	1.796
0x3D	1.347
0x3E	1.026
0x3F	0.798

Table 7. Watchdog Timer Frequency

Address = 0x03, Default=0x45, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Min Sensor Frequency	Sets the watchdog timer. The Watchdog timer is set based on the lowest sensor frequency. $N = 68.94 \times \log_{10}\left(\frac{F}{2500}\right)$ where • F is the sensor frequency (5) Example: If Sensor frequency is 1Mhz Min Sensor Frequency=68.94*log10(1M/2500)=Round to nearest integer(179.38)=179

Table 8. LDC Configuration

Address = 0x04, Default=0x1B, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:5	Reserved	Reserved to 0
4:3	Amplitude	Sets the oscillation amplitude 00:1V 01:2V 10:4V **11:Reserved**
2:0	Response Time	000: Reserved 001: Reserved 010: 192 **011: 384** 100: 768 101: 1536 110: 3072 111: 6144

Table 9. Comparator Threshold High MSB

Address = 0x07, Default=0xFF, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Threshold High	Threshold High Register.

Table 10. Comparator Threshold Low MSB

Address = 0x09, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Threshold Low	Threshold Low Register.

Table 11. INTB Terminal Configuration

Address = 0x0A, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:3	Reserved	Reserved to 0
2:0	Mode	**000: All modes disabled** 001: Wake-up Enabled on INTB terminal 010: INTB terminal indicates the status of Comparator output 100: DRDYB Enabled on INTB terminal All other combinations are Reserved

Table 12. Power Configuration

Address = 0x0B, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:1	Reserved	Reserved to 0
0	PWR_MODE	**0:Stand-By mode** 1:Active Mode. Conversion is Enabled Refer to Power Modes for more details.

Table 13. Status

Address = 0x20, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7	OSC status	1:Indicates oscillator overloaded and stopped 0:Oscillator working
6	Data Ready	1:No new data available 0:Data is ready to be read
5	Wake-up	1:Wake-up disabled 0:Wake-up triggered. Proximity data is more than Threshold High value.
4	Comparator	1:Proximity data is less than Threshold Low value 0:Proximity data is more than Threshold High value
3:0	Do not Care	

Table 14. Proximity Data

Address = 0x22, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	Proximity data	Proximity data

Table 15. Frequency Counter LSB

Address = 0x23, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	FCOUNT LSB (FCOUNT[7:0])	LSB of Frequency Counter. Sensor frequency can be calculated using the output data rate. Please refer to the Measuring Inductance with LDC1041.

Table 16. Frequency Counter Mid-Byte

Address = 0x24, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	FCOUNT Mid byte (FCOUNT[15:8])	Middle Byte of Output data rate

Table 17. Frequency Counter MSB

Address = 0x25, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	FCOUNT MSB (FCOUNT[23:16])	MSB of Output data rate

Conversion data is updated to these registers only when a read is initiated on 0x22 register. If the read is delayed between subsequent conversions, these registers are not updated until another read is initiated on 0x22.

8 Applications and Implementation

8.1 Application Information

8.1.1 Calculation of Rp_MIN and Rp_MAX

Different sensing applications may have a different range of the resonance impedance Rp to measure. The LDC1041 measurement range of Rp is controlled by setting 2 registers – Rp_MIN and Rp_MAX. For a given application, Rp must never be outside the range set by these register values, otherwise the measured value will be clipped. For optimal sensor resolution, the range of Rp_MIN to Rp_MAX should not be unnecessarily large. The following procedure is recommended to determine the Rp_MIN and Rp_MAX register values.

8.1.1.1 Setting Rp_MAX

Rp_MAX sets the upper limit of the LDC1041 resonant impedance input range.

- Configure the sensor such that the eddy current losses are minimized. As an example, for a proximity sensing application, set the distance between the sensor and the target to the maximum sensing distance.
- Measure the resonant impedance Rp using an impedance analyzer.
- Multiply Rp by 2 and use the next higher value from Table 4.

Note that setting Rp_MAX to a value not listed in Table 4 can result in indeterminate behavior.

8.1.1.2 Setting Rp_MIN

Rp_MIN sets the lower limit of the LDC1041 resonant impedance input range.

- Configure the sensor such that the eddy current losses are maximized. As an example, for a proximity sensing application, set the distance between the sensor and the metal target to the minimum sensing distance.
- Measure the resonant impedance Rp using an impedance analyzer.
- Divide the Rp value by 2 and then select the next lower Rp value from Table 6.

Note that setting Rp_MIN to a value not listed on Table 6 can result in indeterminate behavior. In addition, Rp_MIN powers on with a default value of 0x14 which must be set to a value from Table 6 prior to powering on the LDC.

8.1.2 Output Data Rate

Output data rate of LDC1041 depends on the sensor frequency, f_{sensor} and 'Response Time' field in LDC Configuration register(Address:0x04).

$$\text{Output Data Rate} = \frac{f_{sensor}}{\left(\frac{\text{Response time}}{3}\right)} \tag{6}$$

8.1.3 Choosing Filter Capacitor (CFA and CFB Terminals)

The Filter capacitor is critical to the operation of the LDC1041. The capacitor should be low leakage, temperature stable, and it must not generate any piezoelectric noise (the dielectrics of many capacitors exhibit piezoelectric characteristics and any such noise is coupled directly through Rp into the converter). The optimal capacitance values range from 20pF to 100nF. The value of the capacitor is based on the time constant and resonating frequency of the LC tank.

If a ceramic capacitor is used, then a C0G (or NP0) grade dielectric is recommended; the voltage rating should be ≥10V. The traces connecting CFA and CFB to the capacitor should be as short as possible to minimize any parasitics.

For optimal performance, the chosen filter capacitor, connected between terminals CFA and CFB, needs to be as small as possible, but large enough such that the active filter does not saturate. The size of this capacitor depends on the time constant of the sense coil, which is given by L/Rs, (L=inductance, Rs=series resistance of the inductor at oscillation frequency). The larger this time constant, the larger filter capacitor is required. Hence, this time constant reaches its maximum when there is no target present in front of the sensing coil.

Application Information (continued)

The following procedure can be used to find the optimal filter capacitance:

1. Start with a large filter capacitor. For a ferrite core coil, 10nF is usually large enough. For an air coil or PCB coil, 100pF is usually large enough.
2. Power on the LDC and set the desired register values. Minimize the eddy currents losses. This is done by minimizing the amount of conductive target covering the sensor. For an axial sensing application, the target should be at farthest distance from coil. For a lateral or angular position application, the target coverage of the coil should be minimized.
3. Observe the signal on the CFB terminal using a scope. Since this node is very sensitive to capacitive loading, it is recommended to use an active probe. As an alternative, a passive probe with a 1kΩ series resistance between the tip and the CFB terminal can be used.
4. Vary the values of the filter capacitor until that the signal observed on the CFB terminal has an amplitude of approximate 1V peak-to-peak. This signal scales linearly with the reciprocal of the filter capacitance. For example, if a 100pF filter capacitor is applied and the signal observed on the CFB terminal has a peak-to-peak value of 200mV, the desired 1V peak-to-peak value is obtained using a 200mV / 1V * 100pF = 20pF filter capacitor.

8.2 Typical Applications

8.2.1 Axial Distance Sensing Using a PCB Sensor with LDC1041

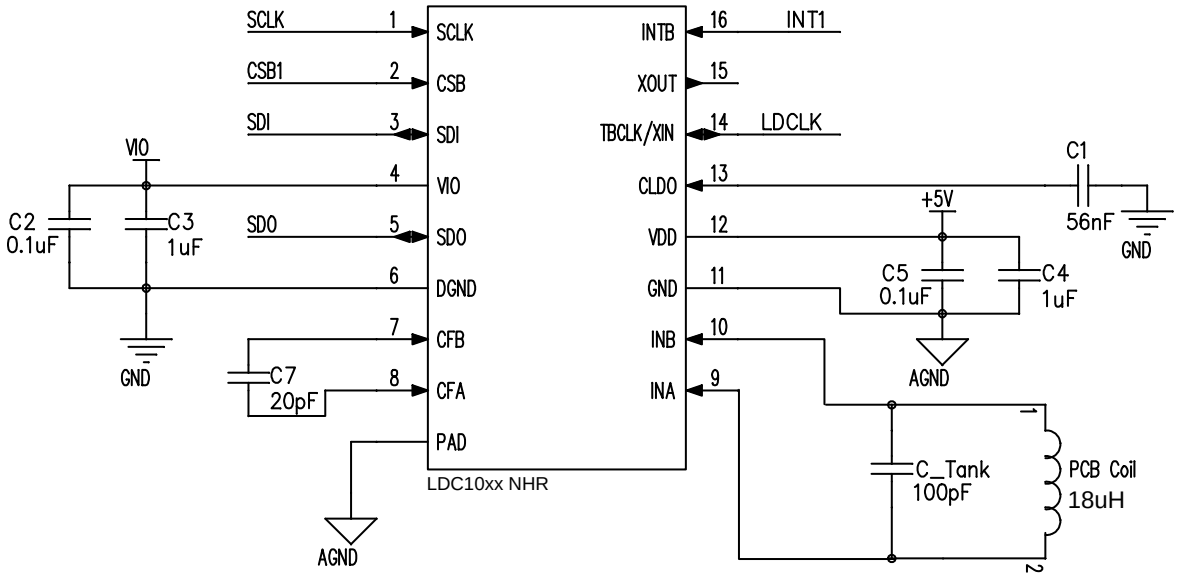


Figure 16. Typical Application Schematic, LDC10xx

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

Table 18. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum sensing distance	1 mm
Maximum sensing distance	8 mm
Output data rate	78 KSPS (Max data rate with LDC10xx series)
Number of PCB layers for sensor	2 layers

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Sensor and Target

In this example, consider a sensor with the below characteristics.

Table 19. Sensor Characteristics

PARAMETER	VALUE
Layers	2
Thickness of copper	1 Oz
Coil shape	Circular
Number of turns	23
Trace thickness	4 mil
Trace spacing	4 mil
PCB core material	FR4
Rp @ 1 mm	5 kΩ
Rp @ 8 mm	12.5 kΩ
Nominal Inductance	18 µH

Target material used is stainless steel

8.2.1.2.2 Calculating Sensor Capacitor

Sensor frequency depends on various factors in the application. In this example since one of the design parameter is to achieve output data rate of 78 KSPS, sensor frequency can be calculated as below.

$$\text{Output Data Rate} = \frac{f_{sensor}}{\left(\frac{\text{Response time}}{3}\right)} \tag{7}$$

With the lowest Response time of 192 and output data rate of 78 KSPS, sensor frequency calculated using the above formula is 4.99 MHz.

Now, using the below formula sensor capacitor is calculated to be 55 pF with a sensor inductance of 18 µH

$$L = \frac{1}{C \times (2\pi \times f_{sensor})^2} \tag{8}$$

8.2.1.2.3 Choosing Filter Capacitor

Using the steps given in Choosing Filter Capacitor (CFA and CFB Terminals) filter capacitor for the example sensor is 20 pF. Below waveform shows the pattern on CFB pin with 100 pF and 20 pF filter capacitor.

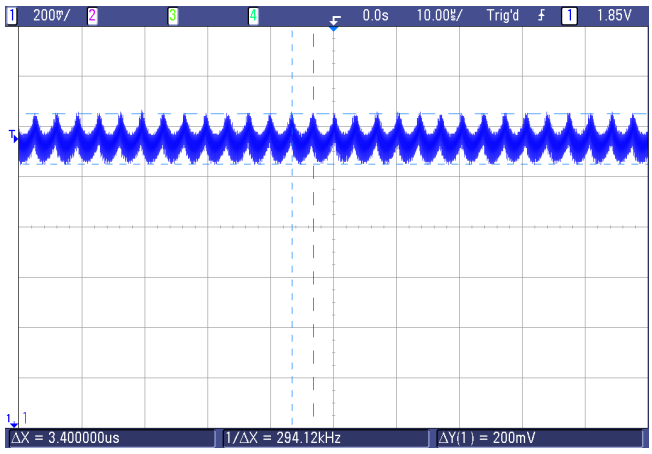


Figure 17. Waveform On CFB With 100pf

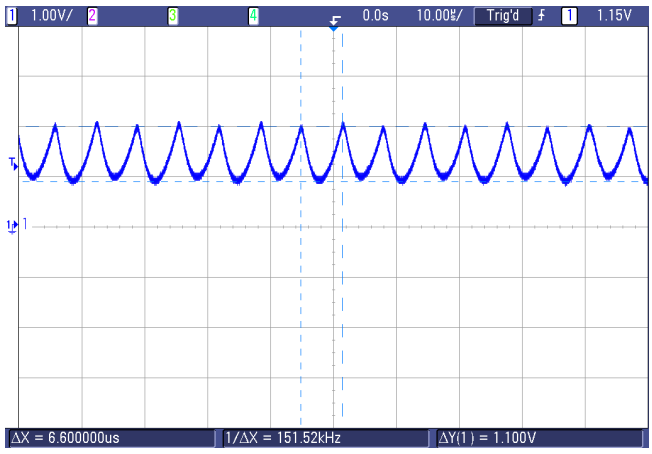


Figure 18. Waveform On CFB With 20pf

8.2.1.2.4 Setting Rp_MIN and Rp_MAX

Calculating value for Rp_MAX Register : Rp at 8mm is 12.5kΩ, 12500×2 = 25000. In Table 4, then 27.704 kΩ is the nearest value larger than 25kΩ; this corresponds to Rp_MAX value of 0x12

Calculating value for Rp_MIN Register : Rp at 1mm is 5kΩ, 5000/2 = 2500. In Table 6 , 2.394kΩ is the nearest value lower than 2.5kΩ; this corresponds to Rp_MIN value of 0x3B

8.2.1.2.5 Calculating Minimum Sensor Frequency

Using,

$$N = 68.94 \times \log_{10}\left(\frac{F}{2500}\right) \quad (9)$$

N is 227.51, round off to 228 decimal. This value has to be written into Watchdog Timer Register, which is used to wake up the internal circuit when the sensor is saturated.

8.2.1.3 Application Curves

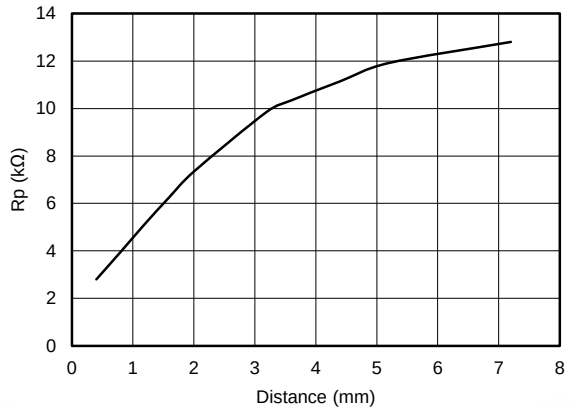


Figure 19. Rp vs Distance

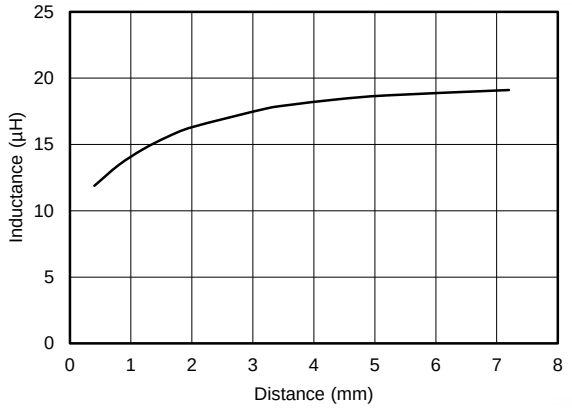


Figure 20. Inductance vs Distance

8.2.2 Linear Position Sensing Application Diagram

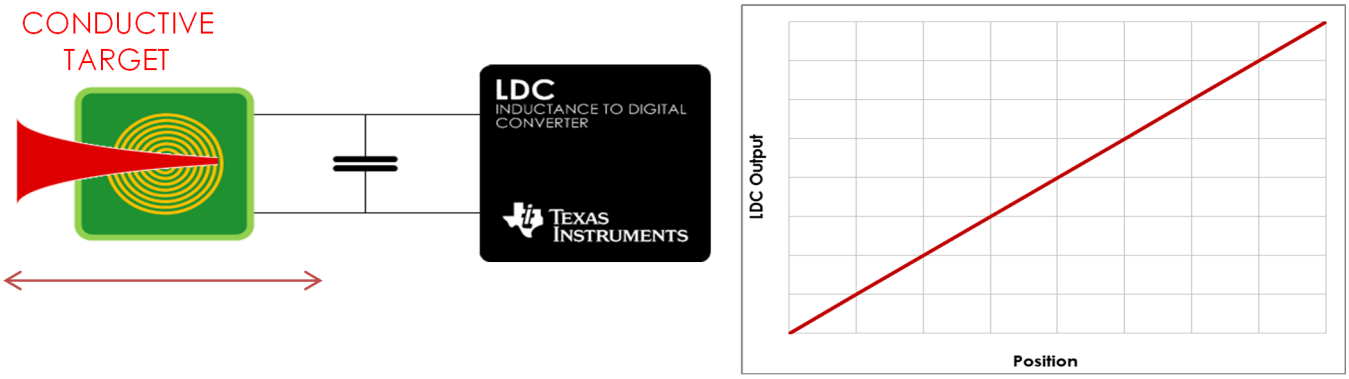


Figure 21. Linear Position Sensing

8.2.3 Angular Position Sensing Application Diagram

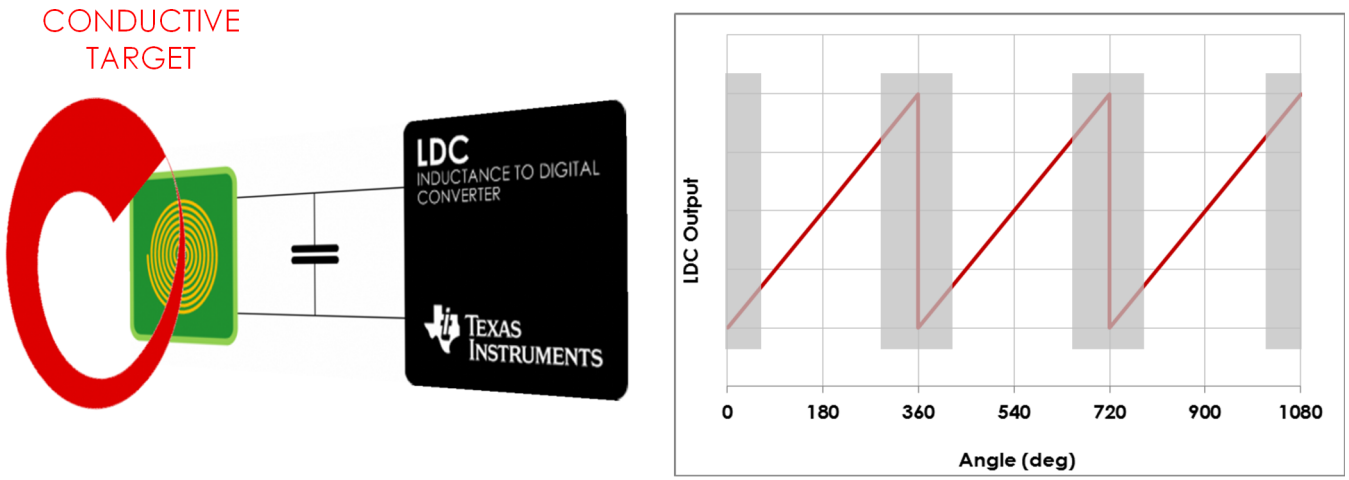


Figure 22. Angular Position Sensing

9 Power Supply Recommendations

The LDC1041 is designed to operate from an analog supply range of 4.75 V to 5.25 V and digital I/O supply range of 1.8V to 5.25V. The analog supply voltage should be greater than or equal to the digital supply voltage for proper operation of the device. The supply voltage should be well regulated. If the supply is located more than a few inches from the LDC1041 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10uF is a typical choice.

10 Layout

10.1 Layout Guidelines

● The VDD and VIO terminal should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1uF ceramic with a X5R or X7R dielectric.

● The optimum placement is closest to the VDD/VIO and GND/DGND terminals of the device. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the VDD/VIO terminal, and the GND/DGND terminal of the IC. See Figure 23 for a PCB layout example.

● The CLDO terminal should be bypassed to digital ground (DGND) with a 56nF ceramic bypass capacitor.

● The filter capacitor selected for the application using the procedure described in section Choosing Filter Capacitor (CFA and CFB Terminals) is connected between CFA and CFB terminals. Place the filter capacitor close to the CFA and CFB terminals. Do not use any ground/power plane below the capacitor and the trace connecting the capacitor and the CFA /CFB terminals.

● Use of two separate ground plane for GND and DGND is recommended with a start connection. See Figure 23 for a PCB layout example.

10.2 Layout Example

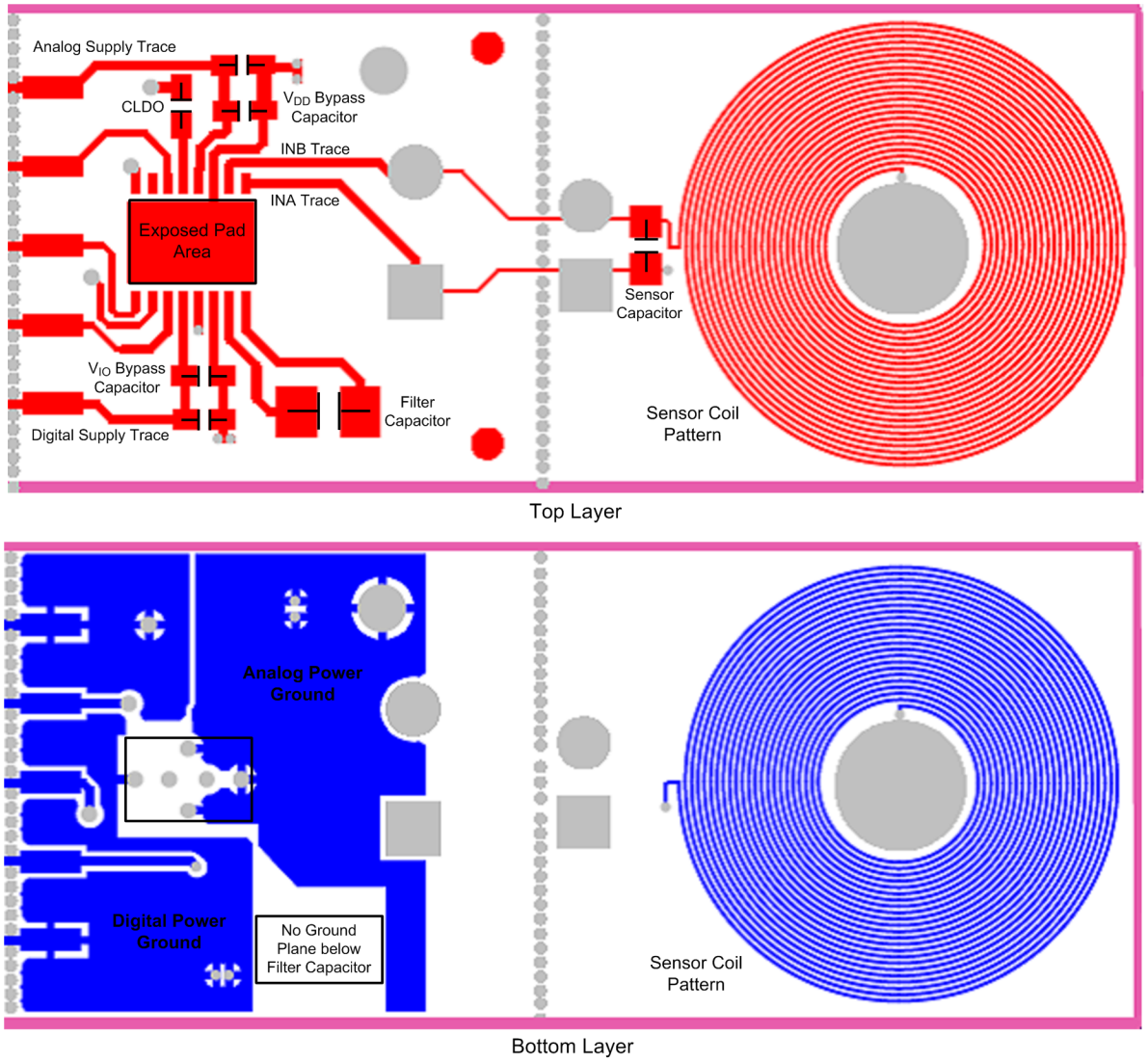


Figure 23. LDC10xx Board Layout

11 器件和文档支持

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LDC1041NHRJ	Active	Production	WSON (NHR) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1041
LDC1041NHRJ.A	Active	Production	WSON (NHR) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1041
LDC1041NHRJ.B	Active	Production	WSON (NHR) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1041
LDC1041NHRR	Active	Production	WSON (NHR) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1041
LDC1041NHRR.A	Active	Production	WSON (NHR) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1041
LDC1041NHRR.B	Active	Production	WSON (NHR) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LDC1041

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

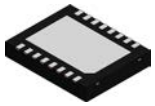
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

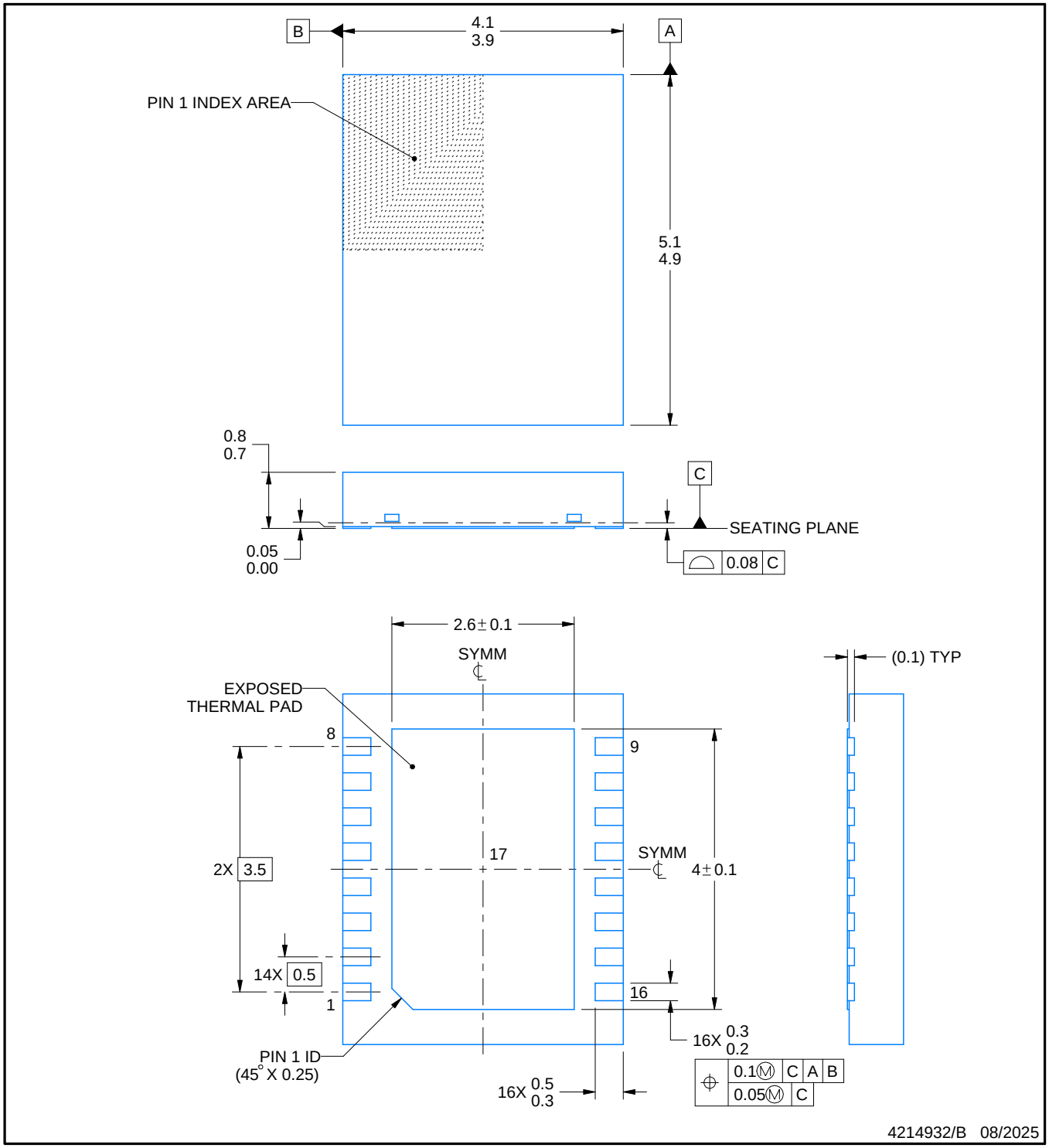
PACKAGE OUTLINE

NHR0016B



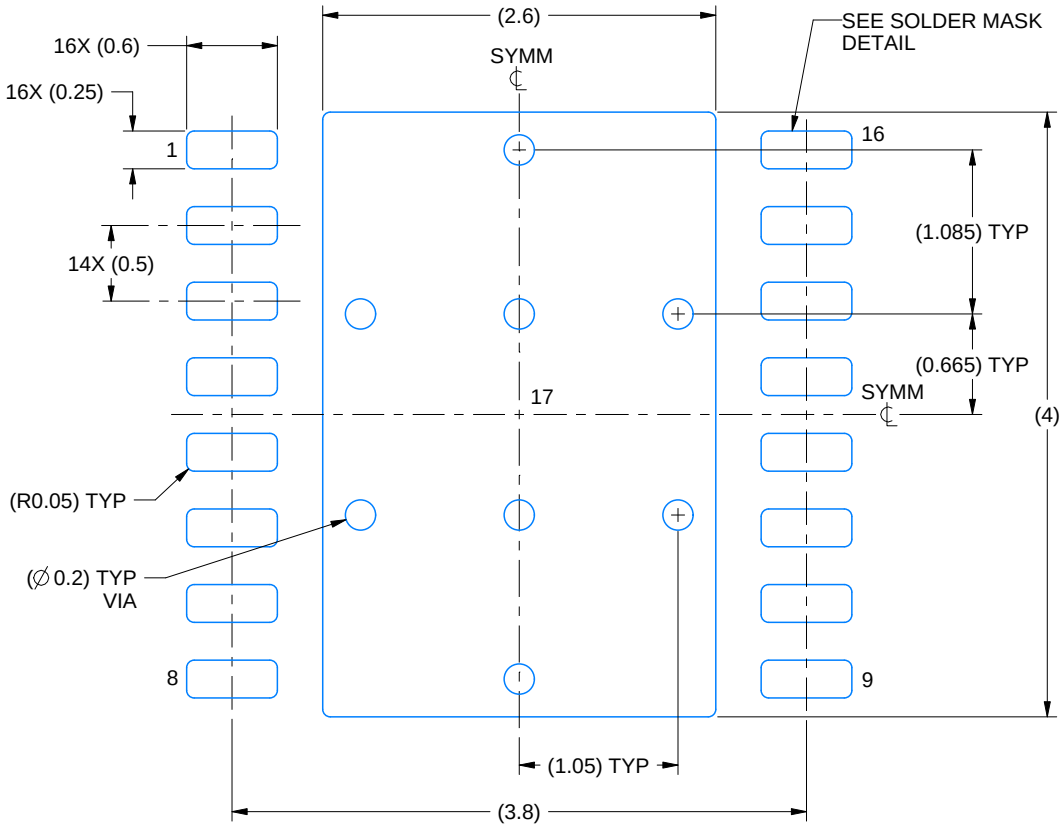
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

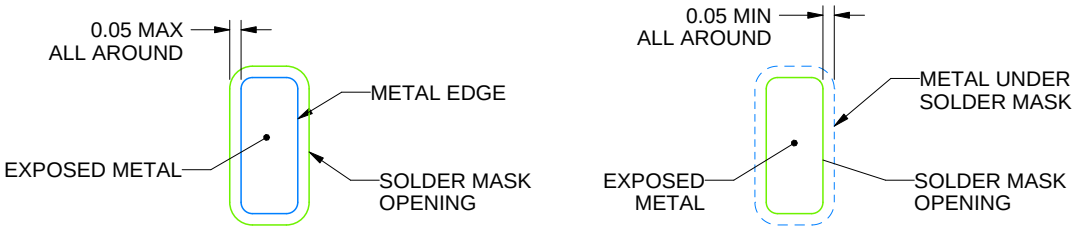


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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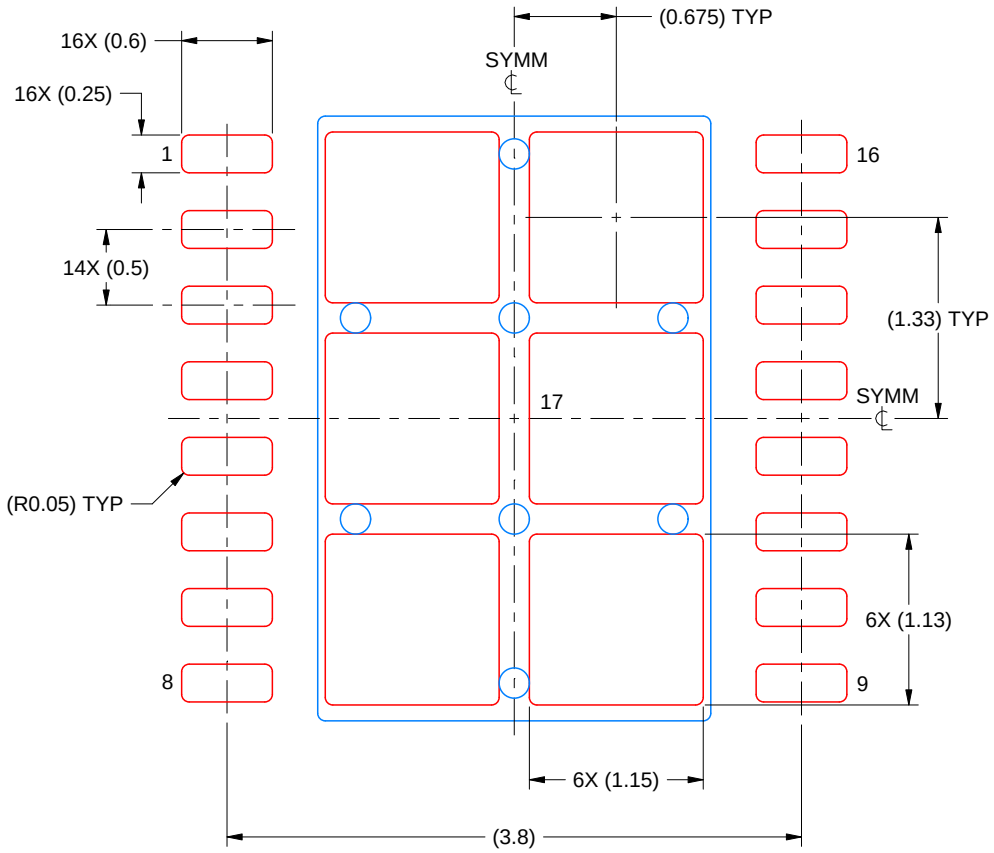
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月