具有集成式高效低辐射直流/直流转换器的 ISOW7821 高性能 5000V_{RMS} 增强型双通道数字隔离器

1 特性

- 集成高效直流/直流转换器与片上变压器
- 100Mbps 数据速率
- 稳健可靠的隔离栅：
  - 在 1kV_{RMS} 工作电压下，预计寿命超过 100 年
  - 高达 5000V 的 $_{RMS}$ 隔离额定值
  - 高达 10kV_{PK} 的浪涌保护能力
  - ±100kV/µs 最低 CMTI
- 3V 至 5.5V 宽输入电源电压范围
- 5V 或 3.3V 稳压输出
- 高达 0.65W 的输出功率
- 5V 至 5V；5V 至 3.3V：提供的负载电流 ≥ 130mA
- 3.3V 至 3.3V：提供的负载电流 ≥ 75mA
- 限制浪涌电流的软启动
- 过载保护和短路保护
- 热关断
- 默认输出：高电平和低电平选项
- 低传播延迟：典型值为 13ns（由 5V 电源供电）
- 优异的电磁兼容性 (EMC)
  - 系统级 ESD、EFT 和浪涌抗扰性
  - ±8kV IEC 61000-4-2 跨隔离栅接触放电保护
  - 低辐射
- 16 引脚宽体小外形尺寸集成电路 (SOIC) 封装
- 扩展温度范围：-40°C 至 +125°C
- 安全相关认证：
  - 符合 DIN VDE V 0884-11:2017-01 标准的 7071V_{PK} 增强型隔离
  - 符合 UL 1577 标准且长达 1 分钟的 5000V_{RMS} 隔离
  - 获得 CSA 认证，符合 IEC 60950-1、IEC 62368-1 和 IEC 60601-1 终端设备标准
  - 符合 GB4943.1-2011 的 CQC 认证
  - 符合 EN 60950-1、EN62368-1 和 EN 61010-1 的 TUV 认证

2 应用

- 工业自动化
- 电机控制
- 电网基础设施
- 医疗设备
- 测试和测量

3 说明

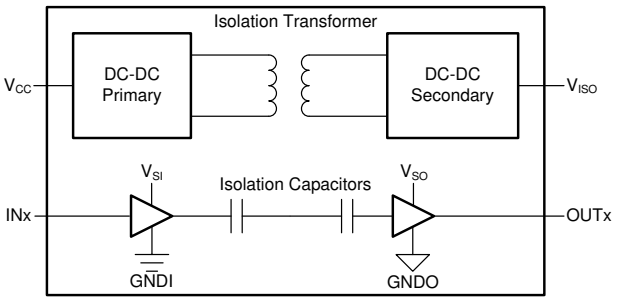
ISOW7821 器件是具有集成式高效电源转换器的高性能、双通道增强型数字隔离器。集成式直流/直流转换器高效运行，提供高达 650mW 的隔离式电源，可配置为各种输入和输出电压。因此，空间受限的隔离设计凭借该器件无需单独使用隔离式电源。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISOW7821	SOIC (16)	10.30mm x 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



V_{CC} 是以 GND1 为基准的主电源电压。V_{ISO} 是以 GND2 为基准的隔离电源电压。

V_{SI} 和 V_{SO} 可为 V_{CC} 或 V_{ISO}，具体取决于通道方向。

V_{SI} 是以 GNDI 为基准的输入侧电源电压，而 V_{SO} 是以 GNDO 为基准的输出侧电源电压。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (March 2018) to Revision B **Page**

- 通篇进行了编辑性和修饰性更改 ... 1
- 在 特性中添加了“稳健可靠的隔离栅”项目符号 ... 1
- 在 特性中添加了“在 1kV$_{RMS}$ 工作电压下，预计寿命超过 100 年”项目符号 ... 1
- 在 特性中添加了“高达 5000V 的 $_{RMS}$ 隔离额定值”项目符号 ... 1
- 在 特性中添加了“高达 10kV$_{PK}$ 的浪涌保护能力”项目符号 ... 1
- 在 特性中添加了“±8kV IEC 61000-4-2 跨隔离栅接触放电保护”项目符号 ... 1
- 在 特性和Insulation Specifications表中将 VDE 标准名称从“DIN V VDE V 0884-11:2017-01”更改为“DIN VDE V 0884-11:2017-01” ... 1
- 向 “特性”中的信息的 TUV 认证项目符号中添加了“EN 62368-1”标准 ... 1
- 删除了 “为选定的器件提供了汽车级版本”中的“已计划进行所有机构认证”项目符号 ... 1
- 更新了 简化原理图，以显示信号隔离通道的两个串联隔离电容器，而不是单个电容器 ... 1
- Added "Contact discharge per IEC 61000-4-2; Isolation barrier withstand test" specification of ±8000 in ESD Ratings table ... 6
- Added table note "IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device" to ESD Ratings table ... 6
- Deleted "TJ or Junction temperature" parameter from Recommended Operating Conditions table as it is already specified in Absolute Maximum Ratings table ... 6
- Added "See 图 34" to TEST CONDITIONS of V_{IOWM} specification ... 8

修订历史记录 **(**接下页**)**

- Updated Safety-Related Certifications table 9
- Added the following note to 图 25: "Optional 100 µF capacitor can be added between V_{CC} and GND1; refer to Power Supply Recommendations" 22
- Added the following note to 图 30: "Optional 100 µF capacitor can be added between V_{CC} and GND1; refer to Power Supply Recommendations" 28
- Added the following text to Design Requirements: "Optional 100 µF decoupling capacitor can be added between V_{CC} and GND1 pins; refer to *Power Supply Recommendations* for more details" 29
- Added text to Power Supply Recommendations section to emphasise that input decoupling capacitor should be larger than output capacitor by at least 100 µF 31
- Added the following note to 图 35: "Optional 100 µF capacitor can be added between V_{CC} and GND1; refer to Power Supply Recommendations" 33

Changes from Original (November 2017) to Revision A **Page**

- Changed OUTB to pin 4 and INB to pin 13 in the *Pin Functions* table 5

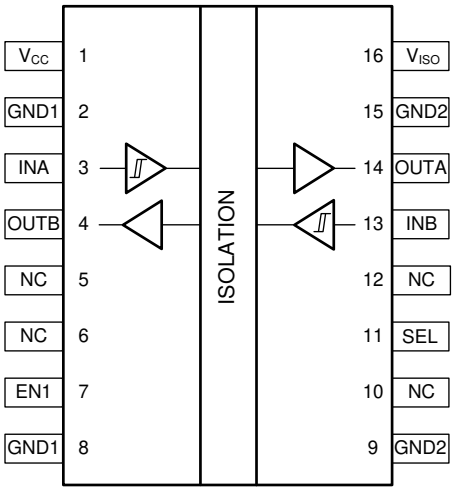
5 说明（续）

ISOW7821 器件可提供高电磁抗扰度和低辐射，同时能够隔离 CMOS 或 LVCMOS 数字 I/O。信号隔离通道具有由二氧化硅 (SiO_2) 绝缘栅相隔离的逻辑输入和输出缓冲器，而电源隔离使用片上变压器，以薄膜聚合物作为绝缘材料。提供各种正向和反向通道配置。如果输入信号丢失，则默认输出对于 ISOW7821 器件为高电平，对于具有 F 后缀的器件为低电平（请参阅*器件 具有*）。

这些器件有助于防止数据总线或者其他电路上的噪声电流进入本地接地并干扰或损坏敏感电路。凭借创新型芯片设计和布局技术，ISOW7821 器件的电磁兼容性得到了显著增强，可缓解系统级 ESD、EFT 和浪涌问题并符合辐射标准。电源转换器效率较高，允许在较高的环境温度下工作。ISOW7821 器件采用 16 引脚 SOIC 宽体 (SOIC-WB) DWE 封装。

6 Pin Configuration and Functions

DWE Package
16-Pin SOIC-WB
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	7	—	Output enable for side 1. Output pins on side 1 are enabled when EN1 is high or open. Output pins on side 1 are high impedance when EN1 is low.
GND1	2, 8	—	Ground connection for V_{CC}
GND2	9, 15	—	Ground connection for V_{ISO}
INA	3	I	Input channel A
OUTB	4	I	Output channel B
NC	5	—	Not connected
NC	6	—	Not connected
NC	10	—	Not connected
NC	12	—	Not connected
OUTA	14	O	Output channel A
INB	13	O	Input channel B
SEL	11	I	V_{ISO} selection pin. V_{ISO} = 5 V when SEL is connected to V_{ISO}. V_{ISO} = 3.3 V, when SEL is connected to GND2 or left floating. For more information see the *Device Functional Modes*.
V_{CC}	1	—	Supply voltage
V_{ISO}	16	—	Isolated supply voltage determined by SEL pin

7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	6	V
V_{ISO}	Isolated supply voltage	–0.5	6	V
V_{IO}	Voltage at INx, OUTx, SEL pins	–0.5	V_{CC} + 0.5, V_{ISO} + 0.5 (3)	V
I_O	Maximum output current through data channels	–15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.
(3) This value depends on whether the pin is located on the V_{CC} or V_{ISO} side. The maximum voltage at the I/O pins should not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test (3)	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
I_{OH}	High level output current (2)	V_{SO} (1) = 5 V	–4			mA
		V_{SO} = 3.3 V	–2			
I_{OL}	Low level output current (2)	V_{SO} = 5 V			4	mA
		V_{SO} = 3.3 V			2	
V_{IH}	High-level input voltage		0.7 × V_{SI}		V_{SI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{SI}	V
DR	Data rate				100	Mbps
T_A	Ambient temperature		–40		125	°C

(1) V_{SI} is the input side supply, V_{SO} is the output side supply
(2) This current is for data output channel.

7.4 Thermal Information

THERMAL METRIC(1)		ISOW7821 DWE (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

V_{CC} = 5.5 V, I_{ISO} = 110 mA, T_J = 150°C, T_A ≤ 80°C, C_L = 15 pF, input a 50-MHz 50% duty-cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)				1.16	W
P_{D1}	Maximum power dissipation (side-1)				0.58	W
P_{D2}	Maximum power dissipation (side-2)				0.58	W

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – capacitive signal isolation)	> 21	µm
		Minimum internal gap (internal clearance – transformer power isolation)	>120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test; See 图 34	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)	6250	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 1697\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2263\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 2652\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~3.5	pF
R_{IO}	Insulation resistance(5)	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V, T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
$V_{ISO(UL)}$	Withstand isolation voltage	$V_{TEST} = V_{ISO(UL)}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO(UL)} = 6000\ V_{RMS}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1, and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010/A1:2019, EN 60950-1:2006/A2:2013 and EN 62368-1:2014
Reinforced insulation; Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1414 V_{PK}; Maximum surge isolation voltage, 6250 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14 and IEC 62368-1 2nd Ed., 800 V_{RMS} maximum working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3+A1, 250 V_{RMS} maximum working voltage; Temperature rating is 90°C for reinforced insulation and 125°C for basic insulation; see certificate for details.	Single protection, 5000 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage;	5000 V_{RMS} Reinforced insulation per EN 61010-1:2010/A1:2019 up to working voltage of 600 V_{RMS}; 5000 V_{RMS} Reinforced insulation per EN 60950-1:2006/A2:2013 and EN 62368-1:2014 up to working voltage of 800 V_{RMS}
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 56.8°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 图 1			400	mA
		$R_{\theta JA}$ = 56.8°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 图 1			611	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 56.8°C/W, T_J = 150°C, T_A = 25°C, see 图 2			2200	mW
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

7.9 Electrical Characteristics—5-V Input, 5-V Output

V_{CC} = 5 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 50 mA	4.75	5.07	5.43	V
		External I_{ISO} = 0 to 130 mA	4.5	5.07	5.43	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 50 mA, V_{CC} = 4.5 V to 5.5 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 130 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 130 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{SI} (ISOW7821); V_I = 0 V (ISOW7821 with F suffix)		53%		
$V_{CC+(UVLO)}$	Positive-going UVLO threshold on V_{CC}, V_{ISO}				2.7	V
$V_{CC–(UVLO)}$	Negative-going UVLO threshold on V_{CC}, V_{ISO}		2.1			V
$V_{HYS\ (UVLO)}$	UVLO threshold hysteresis on V_{CC}, V_{ISO}			0.2		V
V_{ITH}	Input pin rising threshold				0.7	V_{SI}
V_{ITL}	Input pin falling threshold		0.3			V_{SI}
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1			V_{SI}
I_{IL}	Low level input current	V_{IL} = 0 at INx or SEL	–10			µA
I_{IH}	High level input current	V_{IH} = V_{SI}(1) at INx or SEL			10	µA
V_{OH}	High level output voltage	I_O = –4 mA, see 图 24	V_{SO}(1) – 0.4	V_{SO} – 0.2		V
V_{OL}	Low level output voltage	I_O = 4 mA, see 图 24		0.2	0.4	V
$\|CM_H\|$	High-level common-mode transient immunity	V_I = V_{SI}, V_{CM} = 1000 V; see 图 25	100			kV/µs
$\|CM_L\|$	Low-level common-mode transient immunity	V_I = 0 V, V_{CM} = 1000 V; see 图 25	100			kV/µs
I_{CC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		137		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 130 mA		100		mV

(1) V_{SI}= input side supply; V_{SO}= output side supply

7.10 Supply Current Characteristics—5-V Input, 5-V Output

V_{CC} = 5 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (ISOW7821); $V_I = V_{SI}$ (1) (ISOW7821 with F suffix)		21		mA
		No external I_{LOAD}; $V_I = V_{SI}$ (ISOW7821); V_I = 0 V (ISOW7821 with F suffix)		17		
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF, No external I_{LOAD}		19		
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF, No external I_{LOAD}		20		
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF, No external I_{LOAD}		33		
$I_{ISO(OUT)}$ (2)	Current available on isolated supply	V_I = 0 V (ISOW7821); $V_I = V_{SI}$ (ISOW7821 with F suffix)	127			mA
		$V_I = V_{SI}$ (ISOW7821); V_I = 0 V (ISOW7821 with F suffix)	130			
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF	128			
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF	128			
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF	125			

(1) V_{SI}= input side supply; V_{SO}= output side supply
(2) Current available to load should be derated by 2 mA/°C for T_A > 80°C.

7.11 Electrical Characteristics—5-V Input, 3.3-V Output

V_{CC} = 5 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 50 mA	3.13	3.34	3.56	V
		External I_{ISO} = 0 to 130 mA	3	3.34	3.56	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 50 mA, V_{CC} = 4.5 V to 5.5 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 10 to 130 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 130 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{SI} (ISOW7821); V_I = 0 V (ISOW7821 with F suffix)		48%		
$V_{CC+(UVLO)}$	Positive-going UVLO threshold on V_{CC}, V_{ISO}				2.7	V
$V_{CC–(UVLO)}$	Negative-going UVLO threshold on V_{CC}, V_{ISO}		2.1			V
$V_{HYS\ (UVLO)}$	UVLO threshold hysteresis on V_{CC}, V_{ISO}			0.2		V
V_{ITH}	Input pin rising threshold				0.7	V_{SI}
V_{ITL}	Input pin falling threshold		0.3			V_{SI}
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1			V_{SI}
I_{IL}	Low level input current	V_{IL} = 0 at INx or SEL	–10			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx or SEL			10	µA
V_{OH}	High level output voltage	I_O = –2 mA, see 图 24	V_{SO} (1) – 0.3	V_{SO} – 0.1		V
V_{OL}	Low level output voltage	I_O = 2 mA, see 图 24		0.1	0.3	V
$\|CM_H\|$	High-level common-mode transient immunity	V_I = V_{SI}, V_{CM} = 1000 V; see 图 25	100			kV/µs
$\|CM_L\|$	Low-level common-mode transient immunity	V_I = 0 V, V_{CM} = 1000 V; see 图 25	100			kV/µs
I_{CC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		137		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 130 mA		100		mV

(1) V_{SI}= input side supply; V_{SO}= output side supply

7.12 Supply Current Characteristics—5-V Input, 3.3-V Output

V_{CC} = 5 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (ISOW7821); $V_I = V_S$ (1) (ISOW7821 with F suffix)		17		mA
		No external I_{LOAD}; $V_I = V_{SI}$ (ISOW7821); V_I = 0 V (ISOW7821 with F suffix)		14		
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF, No external I_{LOAD}		16		
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF, No external I_{LOAD}		17		
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF, No external I_{LOAD}		27		
$I_{ISO(OUT)}$ (2)	Current available on isolated supply	V_I = 0 V (ISOW7821); $V_I = V_{SI}$ (ISOW7821 with F suffix)	127			mA
		$V_I = V_{SI}$ (ISOW7821); V_I = 0 V (ISOW7821 with F suffix)	130			
		All channels switching with square wave clock input of 1 Mbps; C_L= 15 pF	128			
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF	128			
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF	126			

(1) V_{SI}= input side supply; V_{SO}= output side supply
(2) Current available to load should be derated by 2 mA/°C for T_A > 105°C.

7.13 Electrical Characteristics—3.3-V Input, 3.3-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 30 mA	3.13	3.34	3.58	V
		External I_{ISO} = 0 to 75 mA	3	3.34	3.58	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 30 mA, V_{CC} = 3 V to 3.6 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 75 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 75 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{SI} (ISOW7821); V_I = 0 V (ISOW7821 with F suffix)		47%		
$V_{CC+(UVLO)}$	Positive-going UVLO threshold on V_{CC}, V_{ISO}				2.7	V
$V_{CC–(UVLO)}$	Negative-going UVLO threshold on V_{CC}, V_{ISO}		2.1			V
$V_{HYS\ (UVLO)}$	UVLO threshold hysteresis on V_{CC}, V_{ISO}			0.2		V
V_{ITH}	Input pin rising threshold				0.7	V_{SI}
V_{ITL}	Input pin falling threshold		0.3			V_{SI}
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1			V_{SI}
I_{IL}	Low level input current	V_{IL} = 0 at INx or SEL	–10			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx or SEL			10	µA
V_{OH}	High level output voltage	I_O = –2 mA, see 图 24	V_{SO} (1) – 0.3	V_{SO} – 0.1		V
V_{OL}	Low level output voltage	I_O = 2 mA, see 图 24		0.1	0.3	V
$\|CM_H\|$	High-level common-mode transient immunity	V_I = V_{SI}, V_{CM} = 1000 V; see 图 25	100			kV/µs
$\|CM_L\|$	Low-level common-mode transient immunity	V_I = 0 V, V_{CM} = 1000 V; see 图 25	100			kV/µs
I_{CC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		143		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 75 mA		90		mV

(1) V_{SI}= input side supply; V_{SO}= output side supply

7.14 Supply Current Characteristics—3.3-V Input, 3.3-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (ISOW7821); $V_I = V_S$ (1) (ISOW7821 with F suffix)		24		mA
		No external I_{LOAD}; $V_I = V_{SI}$ (ISOW7821); V_I = 0 V (ISOW7821 with F suffix)		19		
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF, No external I_{LOAD}		22		
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF, No external I_{LOAD}		22		
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF, No external I_{LOAD}		32		
$I_{ISO(OUT)}$ (2)	Current available on isolated supply	V_I = 0 V (ISOW7821); $V_I = V_{SI}$ (ISOW7821 with F suffix)	72			mA
		$V_I = V_{SI}$(ISOW7821); V_I = 0 V (ISOW7821 with F suffix)	75			
		All channels switching with square wave clock input of 1 Mbps; C_L= 15 pF	75			
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF	73			
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF	71			

(1) V_{SI}= input side supply; V_{SO}= output side supply
(2) Current available to load should be derated by 2 mA/°C for T_A > 115°C.

7.15 Switching Characteristics—5-V Input, 5-V Output

V_{CC} = 5 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 24		13	17.6	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.7	ns
$t_{SK(o)}$	Channel-channel output skew time(2)	Same-direction channels			4	ns
$t_{SK(p-p)}$	Part-part skew time(3)				4.5	ns
t_r, t_f	Output signal rise and fall times			2	4	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.16 Switching Characteristics—5-V Input, 3.3-V Output

V_{CC} = 5 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 24		14	19.7	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.4	ns
$t_{SK(o)}$	Channel-channel output skew time(2)	Same-direction channels			4	ns
$t_{SK(p-p)}$	Part-part skew time(3)				4.5	ns
t_r, t_f	Output signal rise and fall times			1	4	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.17 Switching Characteristics—3.3-V Input, 3.3-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 24		14.5	20.2	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.4	ns
$t_{SK(o)}$	Channel-channel output skew time(2)	Same-direction channels			4	ns
$t_{SK(p-p)}$	Part-part skew time(3)				4.5	ns
t_r, t_f	Output signal rise and fall times			1	3	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.18 Insulation Characteristics Curves

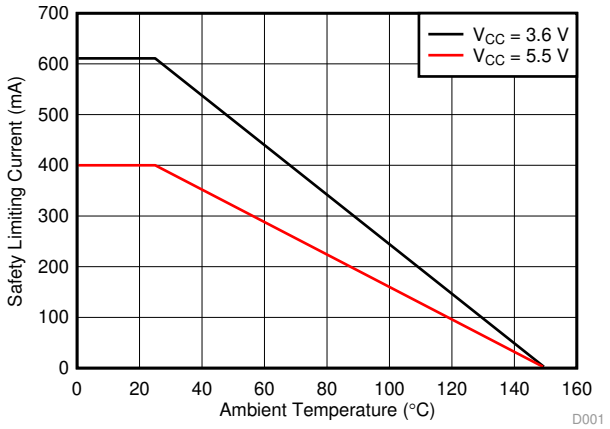


图 1. Thermal Derating Curve for Safety Limiting Current per VDE

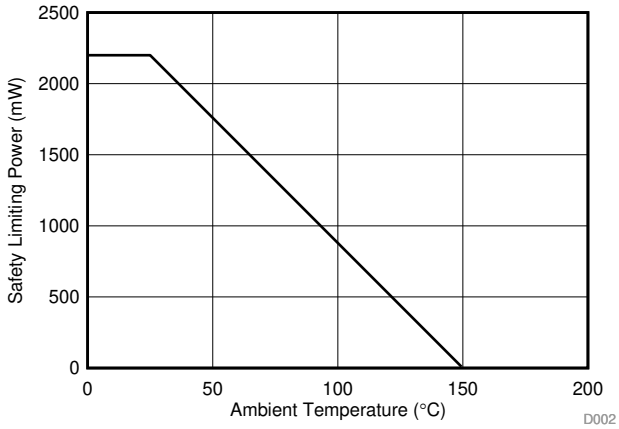
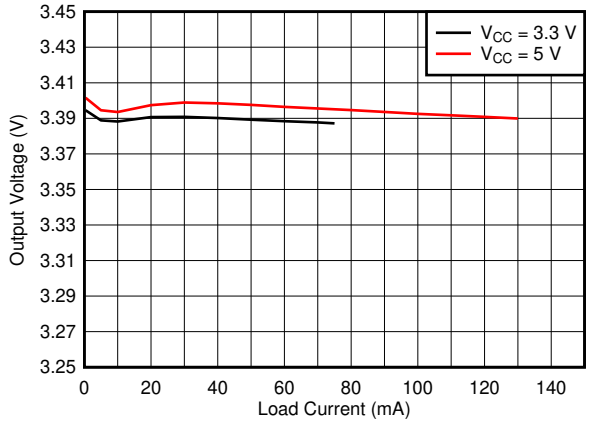


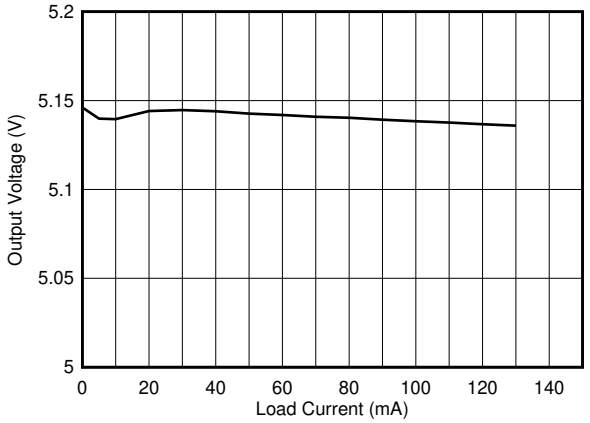
图 2. Thermal Derating Curve for Safety Limiting Power per VDE

7.19 Typical Characteristics



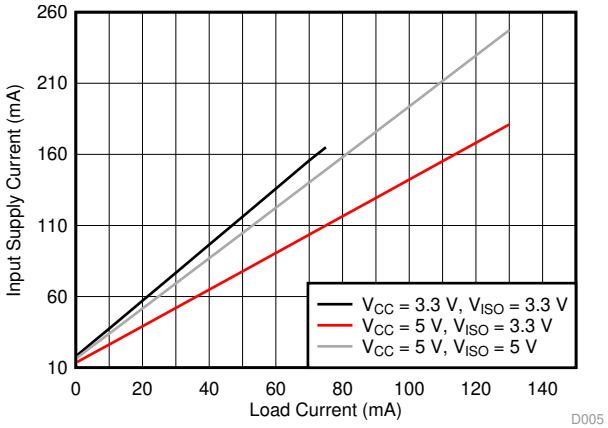
V_{ISO} = 3.3 V T_A = 25°C

图 3. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



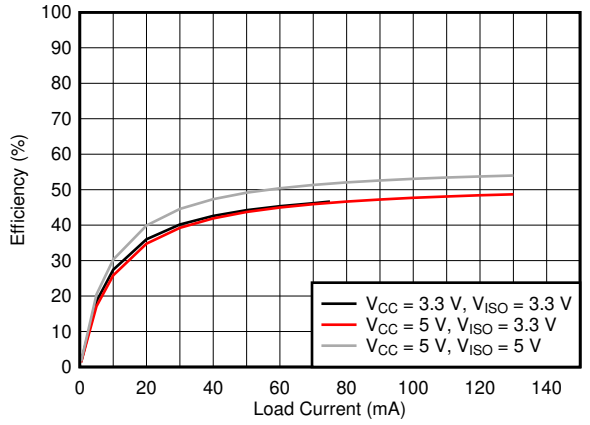
V_{ISO} = 5 V T_A = 25°C

图 4. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



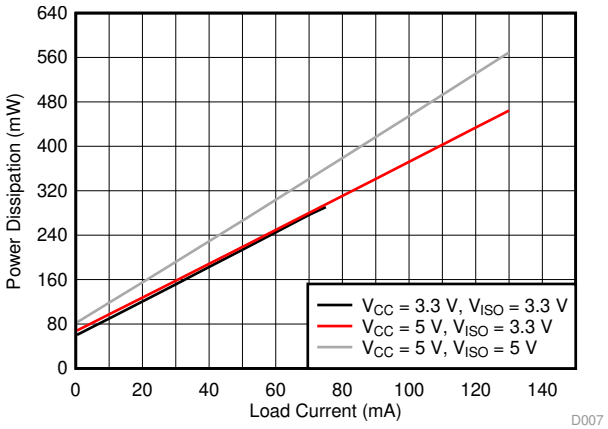
T_A = 25°C

图 5. ISOW7821 Supply Current (I_{CC}) vs Load Current (I_{ISO})



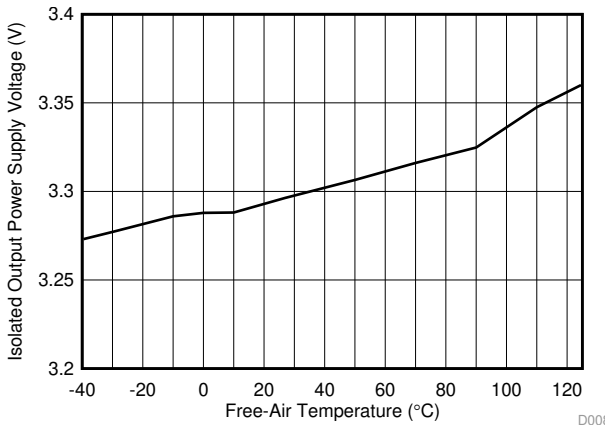
T_A = 25°C

图 6. Efficiency vs Load Current (I_{ISO})



T_A = 25°C

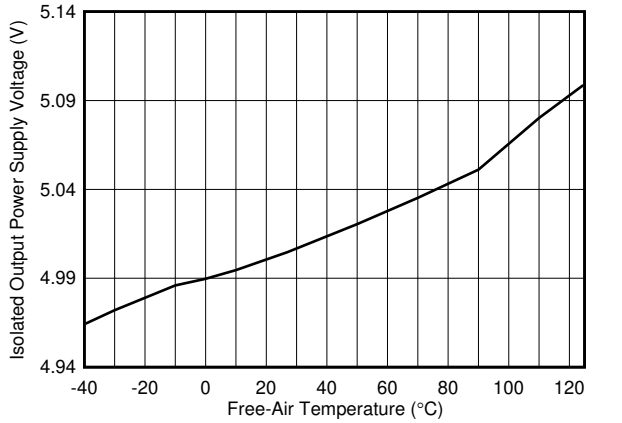
图 7. Power Dissipation vs Load Current (I_{ISO})



No I_{ISO} load V_{CC} = 5 V V_{ISO} = 3.3 V

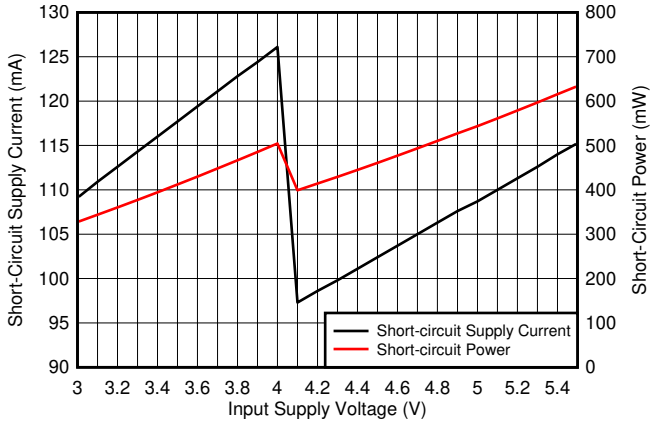
图 8. 3.3-V Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature

Typical Characteristics (接下页)



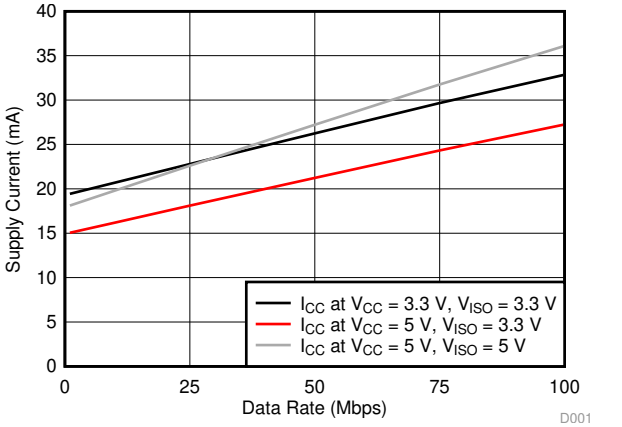
No I_{ISO} load V_{CC} = 5 V V_{ISO} = 5 V

图 9. 5-V Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



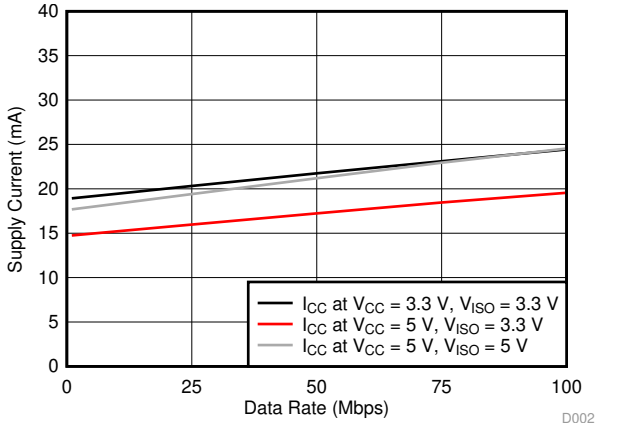
V_{ISO} shorted to GND2 T_A = 25°C

图 10. Short-Circuit Supply Current (I_{CC}) and Power (P) vs Supply Voltage (V_{CC})



C_L = 15 pF T_A = 25°C No I_{ISO} load

图 11. Supply Current vs Data Rate



C_L = no load T_A = 25°C No I_{ISO} load

图 12. Supply Current vs Data Rate

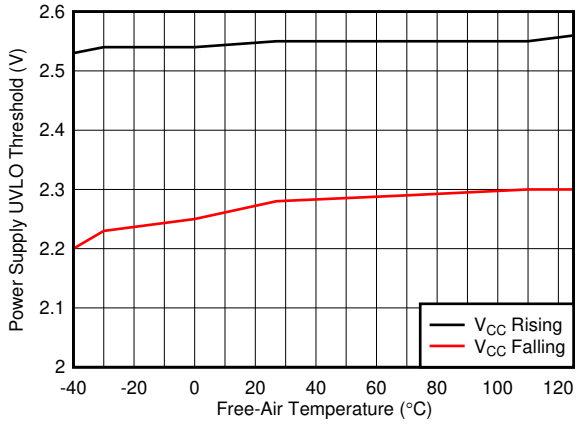


图 13. Power-Supply Undervoltage Threshold vs Free Air Temperature

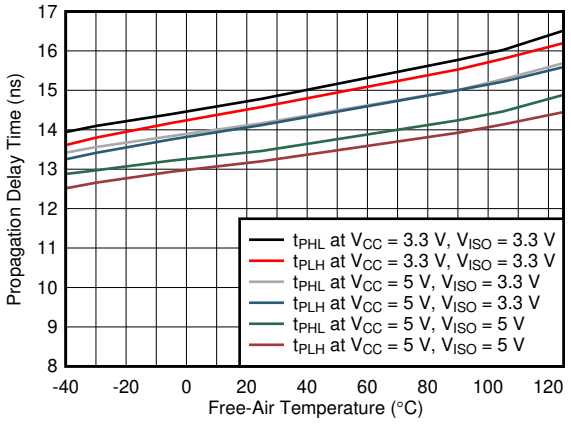
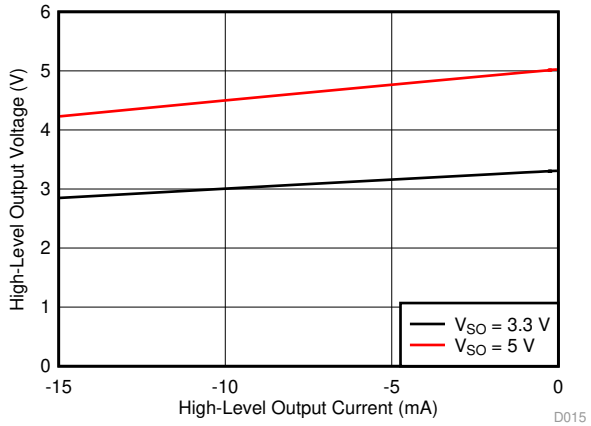


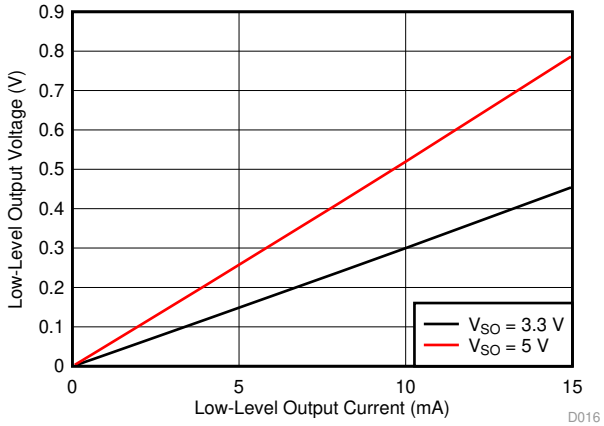
图 14. Propagation Delay Time vs Free-Air Temperature

Typical Characteristics (接下页)



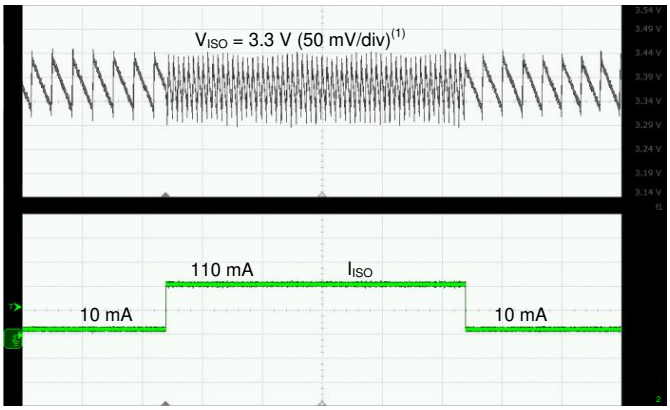
T_A = 25°C

图 15. High-Level Output Voltage vs High-Level Output Current



T_A = 25°C

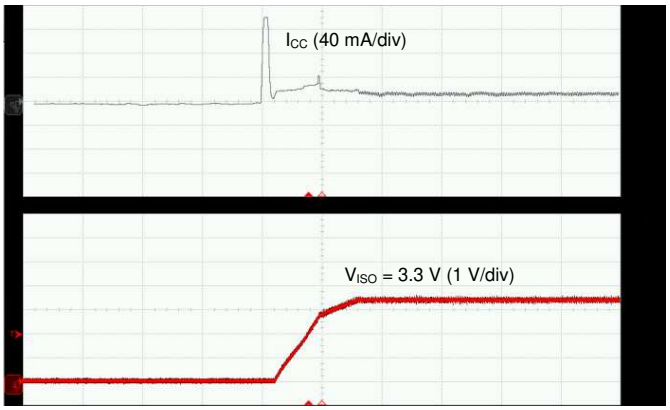
图 16. Low-Level Output Voltage vs Low-Level Output Current



V_{CC} = 5 V V_{ISO} = 3.3 V

1. Negligible undershoot and overshoot because of load transient

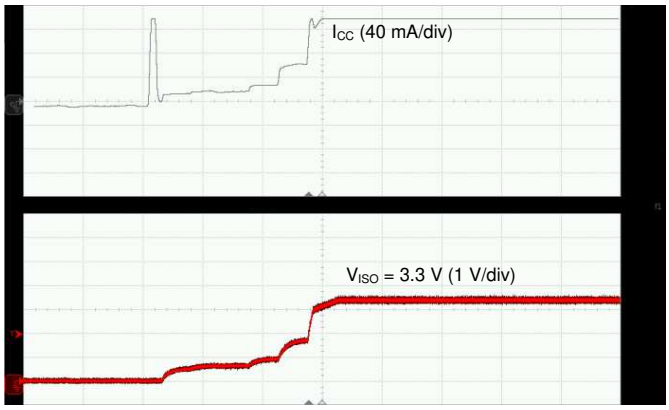
图 17. 10-mA to 110-mA Load Transient Response



V_{CC} = 5 V V_{ISO} = 3.3 V

Current spike is because of charging the input supply capacitor

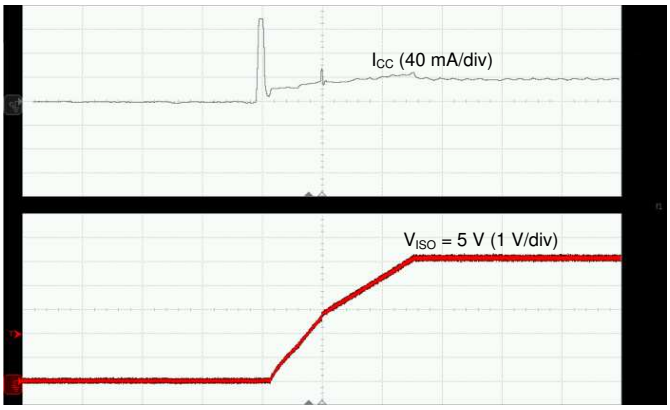
图 18. Soft Start at 10-mA Load



V_{CC} = 5 V V_{ISO} = 3.3 V

Input current spike is because of charging the input supply decoupling capacitor

图 19. Soft Start at 120-mA Load

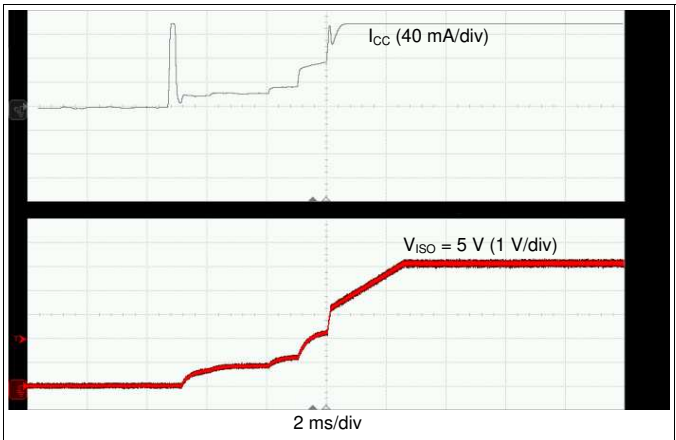


V_{CC} = 5 V V_{ISO} = 5 V

Input current spike is because of charging the input supply decoupling capacitor

图 20. Soft Start at 10-mA Load

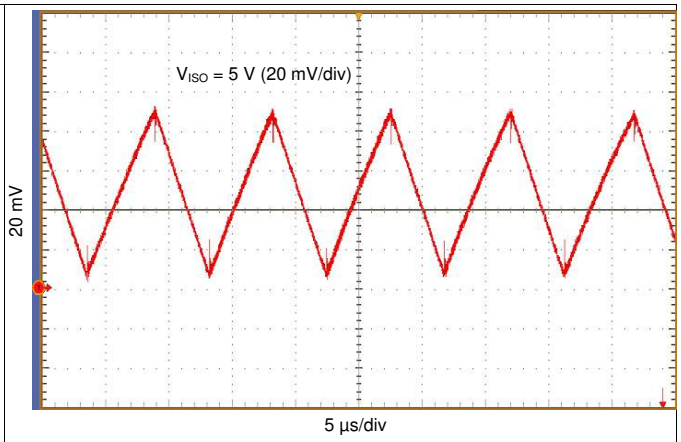
Typical Characteristics (接下页)



V_{CC} = 5 V V_{ISO} = 5 V

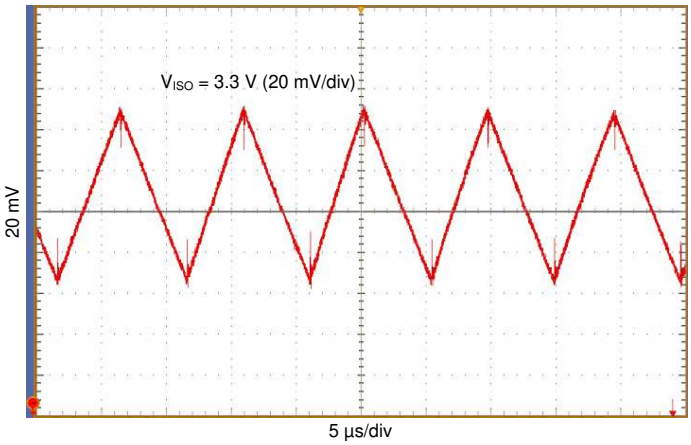
Input current spike is because of charging the input supply decoupling capacitor

图 21. Soft Start at 130-mA Load



V_{CC} = 5 V V_{ISO} = 5 V

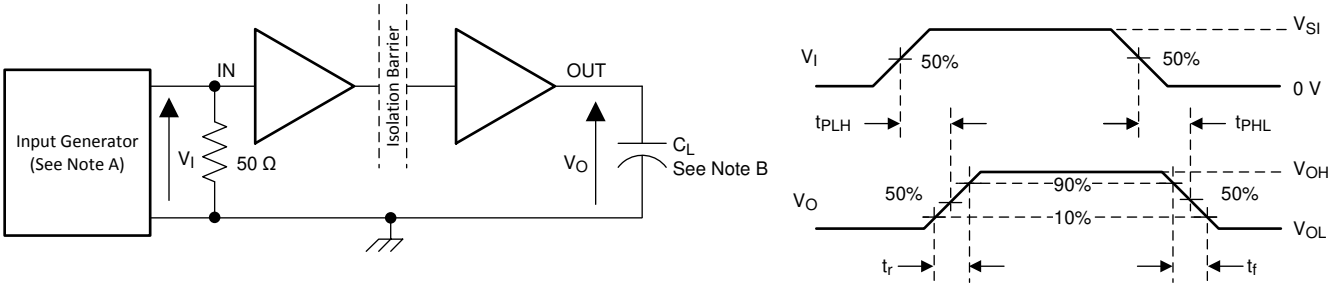
图 22. V_{ISO} Ripple Voltage at 130 mA



V_{CC} = 5 V V_{ISO} = 3.3 V

图 23. V_{ISO} Ripple Voltage at 130 mA

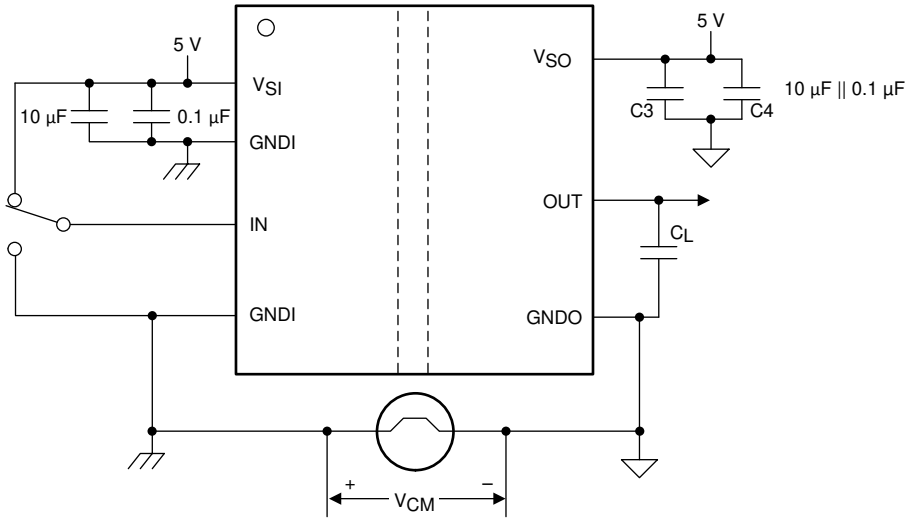
8 Parameter Measurement Information



The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50-Ω resistor is required to terminate the input generator signal. The resistor is not required in the actual application.

C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 24. Switching Characteristics Test Circuit and Voltage Waveforms



C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Optional 100 µF capacitor can be added between V_{CC} and GND1; refer to *Power Supply Recommendations*.

Pass-fail criteria: Outputs must remain stable.

图 25. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ISOW7821 device comprises a high-efficiency, low-emissions isolated DC-DC converter and two high-speed isolated data channels. 图 26 shows the functional block diagram of the ISOW7821 device.

The integrated DC-DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of a high-Q on-chip transformer provide high efficiency and low radiated emissions. The integrated transformer uses thin film polymer as the insulation barrier.

The V_{CC} supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified and regulated to either 3.3 V or 5 V, depending on the SEL pin. The output voltage, V_{ISO}, is monitored and feedback information is conveyed to the primary side through a dedicated isolation channel. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{CC} and V_{ISO} supplies which ensures robust system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

The integrated signal-isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. 图 27 shows a functional block diagram of a typical signal isolation channel.

The ISOW7821 device is suitable for applications that have limited board space and require more integration. These devices are also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

9.2 Functional Block Diagram

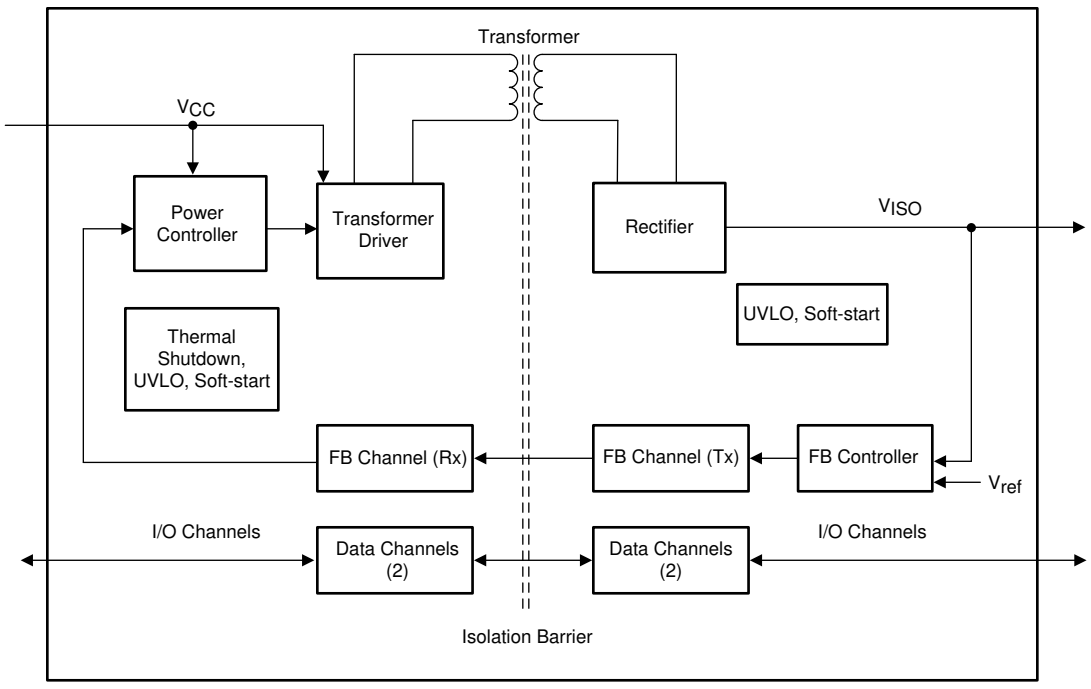


图 26. ISOW7821 Block Diagram

Functional Block Diagram (接下页)

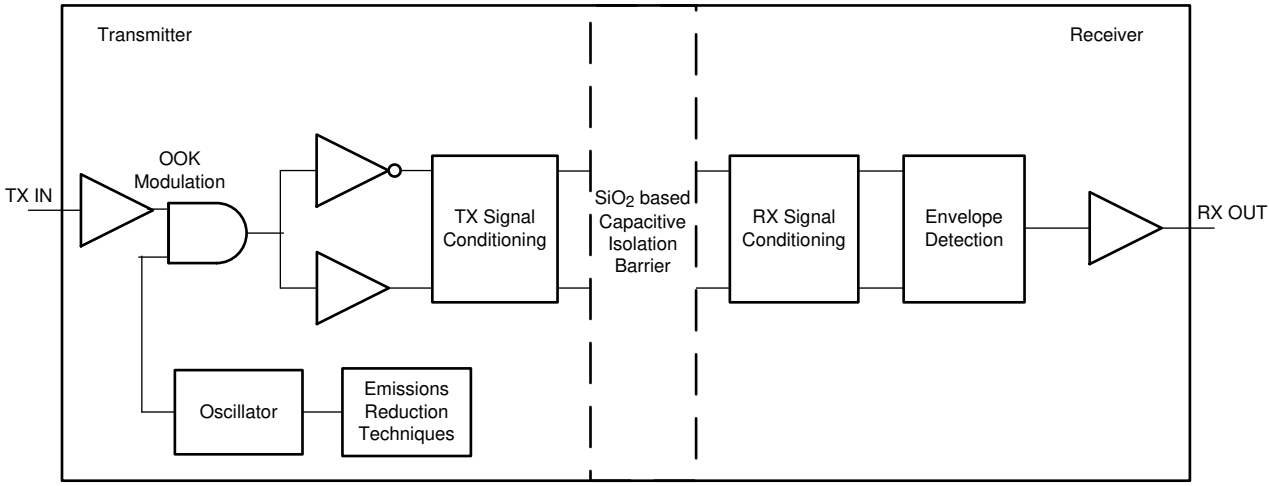


图 27. Conceptual Block Diagram of a Capacitive Data Channel

图 28 shows a conceptual detail of how the OOK scheme works.

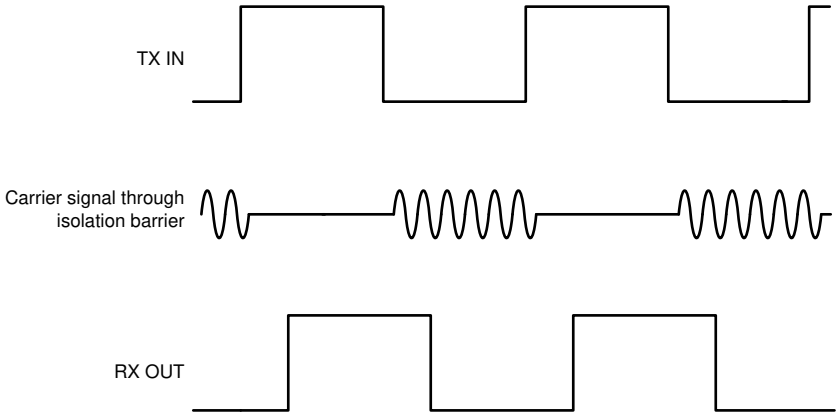


图 28. On-Off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

表 1 provides an overview of the device features.

表 1. Device Features

PART NUMBER(1)	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT STATE	RATED ISOLATION(2)
ISOW7821	1 forward, 1 reverse	100 Mbps	High	5000 V_{RMS} / 7071 V_{PK}
ISOW7821F			Low	

(1) The F suffix is part of the orderable part number. See the *机械、封装和可订购信息* section for the full orderable part number.
(2) For detailed isolation ratings, see the *Safety-Related Certifications* table.

9.3.1 Electromagnetic Compatibility (EMC) Considerations

The ISOW7821 device uses emissions reduction schemes for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISOW7821 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.3.2 Power-Up and Power-Down Behavior

The ISOW7821 device has built-in UVLO on the V_{CC} and V_{ISO} supplies with positive-going and negative-going thresholds and hysteresis. When the V_{CC} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{CC} supply and charges the V_{ISO} output in a controlled manner, avoiding overshoots. Outputs of the isolated data channels are in an indeterminate state until the V_{CC} or V_{ISO} voltage crosses the positive-going UVLO threshold. When the UVLO positive-going threshold is crossed on the secondary side V_{ISO} pin, the feedback data channel starts providing feedback to the primary controller. The regulation loop takes over and the isolated data channels go to the normal state defined by the respective input channels or their default states. Design should consider a sufficient time margin (typically 10 ms with 10-µF load capacitance) to allow this power up sequence before valid data channels are accounted for system functionality.

When V_{CC} power is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISO} capacitor then discharges depending on the external load. The isolated data outputs on the V_{ISO} side are returned to the default state for the brief time that the V_{ISO} voltage takes to discharge to zero.

9.3.3 Current Limit, Thermal Overload Protection

The ISOW7821 device is protected against output overload and short circuit. Output voltage starts dropping when the power converter is not able to deliver the current demanded during overload conditions. For a V_{ISO} short-circuit to ground, the duty cycle of the converter is limited to help protect against any damage.

Thermal protection is also integrated to help prevent the device from getting damaged during overload and short-circuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the temperature goes above 180°C, thermal shutdown activates and the primary controller turns off which removes the energy supplied to the V_{ISO} load, which causes the device to cool off. When the junction temperature goes below 150°C, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care should be taken in the design to prevent the device junction temperatures from reaching such high values.

9.4 Device Functional Modes

表 2 lists the supply configurations for these devices.

表 2. Supply Configurations

SEL INPUT	V_{CC}	V_{ISO}
Shorted to V_{ISO}	5 V	5 V
Shorted to GND2 or floating	5 V	3.3 V
Shorted to GND2 or floating	3.3 V (1)	3.3 V (2)

(1) V_{CC} = 3.3 V, SEL shorted to V_{ISO} (essentially V_{ISO} = 5 V) is not recommended mode of configuration.
(2) The SEL pin has a weak pulldown internally. Therefore for V_{ISO} = 3.3 V, the SEL pin should be strongly connected to the GND2 pin in noisy system scenarios.

表 3 lists the functional modes for ISOW7821 device.

表 3. Function Table (1)

INPUT SUPPLY (V_{CC})	INPUT (INx)	OUTPUT (OUTx)	COMMENTS
PU	H	H	Output channel assumes the logic state of its input
	L	L	
	Open	Default	Default mode (2): When INx is open, the corresponding output channel assumes logic based on default output mode of selected version
PD	x	Undetermined (3)	

(1) PU = Powered up (V_{CC} ≥ 2.7 V); PD = Powered down (V_{CC} < 2.1 V); X = Irrelevant; H = High level; L = Low level, V_{CC} = Input-side supply
(2) In the default condition, the output is high for ISOW7821 and low for ISOW7821 with the F suffix.
(3) The outputs are in an undetermined state when V_{CC} < 2.1 V.

9.4.1 Device I/O Schematics

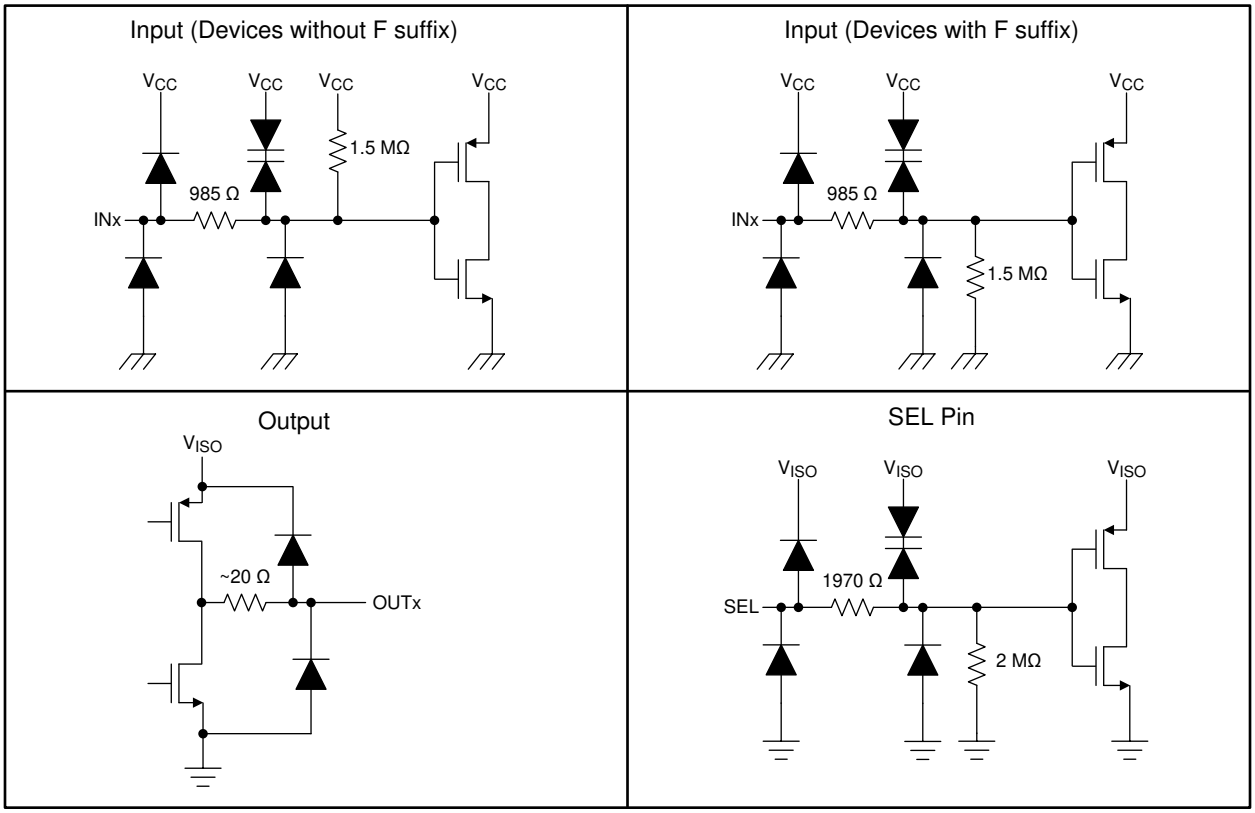


图 29. Device I/O Schematics

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

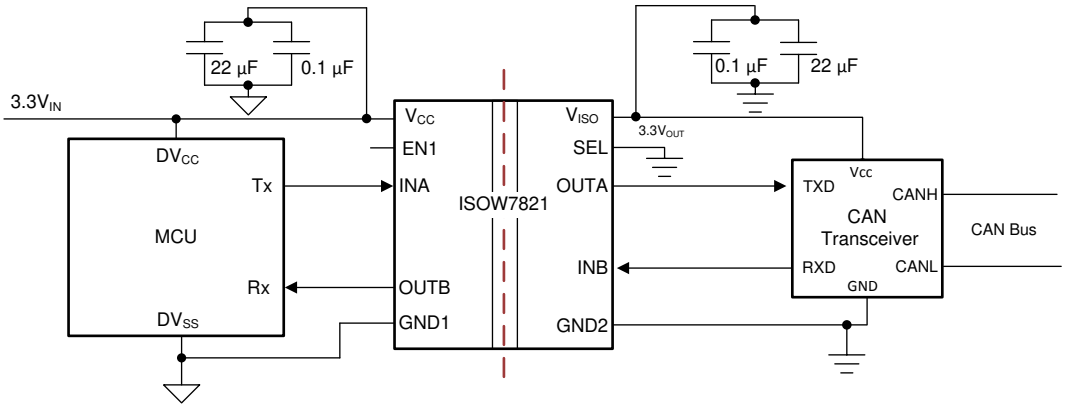
10.1 Application Information

The ISOW7821 high-performance, dual channel digital isolator with integrated DC-DC converter. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to the integrated DC-DC converter in the ISOW7821 device, the isolated supply is generated inside the device that can be used to power isolated side of the device and peripherals on isolated side, thus saving board space. The ISOW7821 device uses single-ended CMOS-logic switching technology. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is a microcontroller or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

The ISOW7821 device is suitable for applications that have limited board space and desire more integration. These devices are also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

10.2 Typical Application

图 30 shows the typical schematic for CAN isolation.



Optional 100 µF capacitor can be added between V_{CC} and GND1; refer to *Power Supply Recommendations*.

图 30. Isolating CAN Bus and Generating Isolated Power for CAN Transceiver

10.2.1 Design Requirements

To design with this device, use the parameters listed in 表 4.

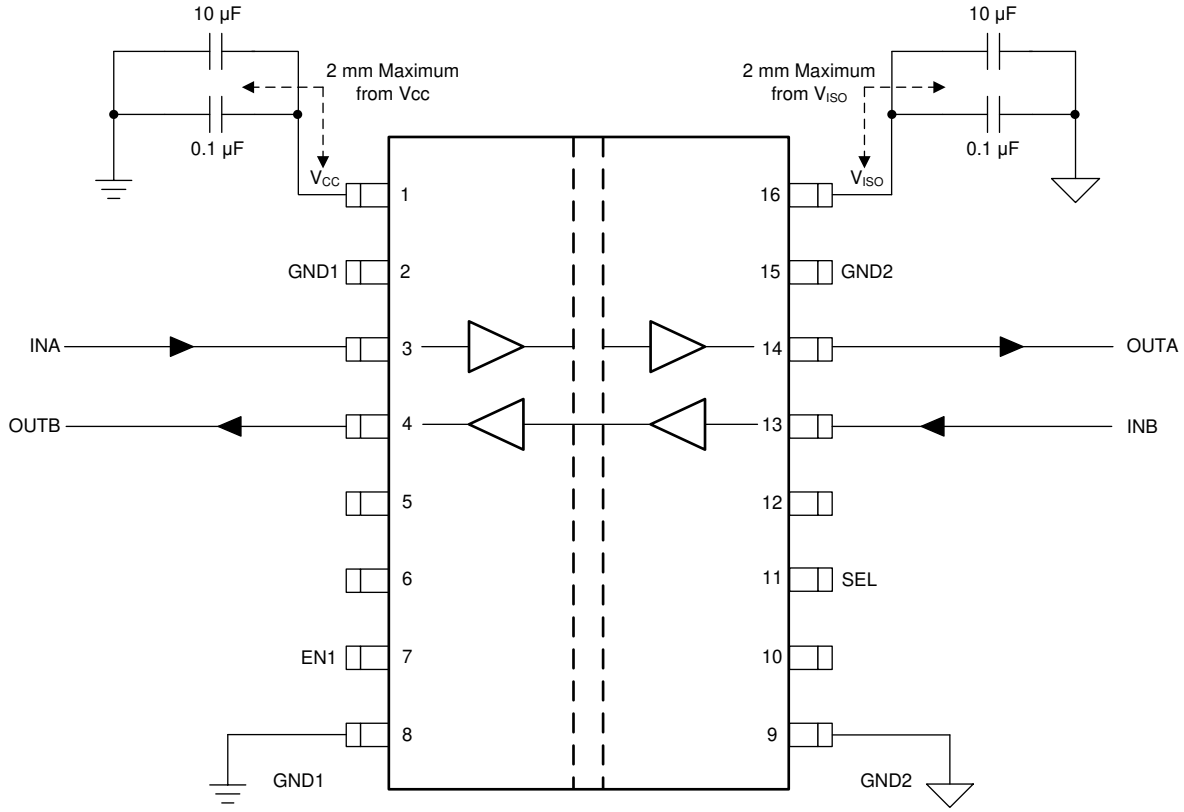
表 4. Design Parameters

PARAMETER	VALUE
Input voltage	3 V to 5.5 V
Decoupling capacitor between V_{CC} and GND1	0.1 µF to 10 µF
Decoupling capacitor between V_{ISO} and GND2	0.1 µF to 10 µF

Because of very-high current flowing through the ISOW7821 V_{CC} and V_{ISO} supplies, higher decoupling capacitors typically provide better noise and ripple performance. Although a 10-µF capacitor is adequate, higher decoupling capacitors (such as 47 µF) on both the V_{CC} and V_{ISO} pins to the respective grounds are strongly recommended to achieve the best performance. Optional 100 µF decoupling capacitor can be added between V_{CC} and GND1 pins; refer to *Power Supply Recommendations* for more details.

10.2.2 Detailed Design Procedure

The ISOW7821 device only requires external bypass capacitors to operate. These low-ESR ceramic bypass capacitors must be placed as close to the chip pads as possible.



Optional 100 µF capacitor can be added between V_{CC} and GND1; refer to *Power Supply Recommendations*.

图 31. Typical Circuit Hook-Up

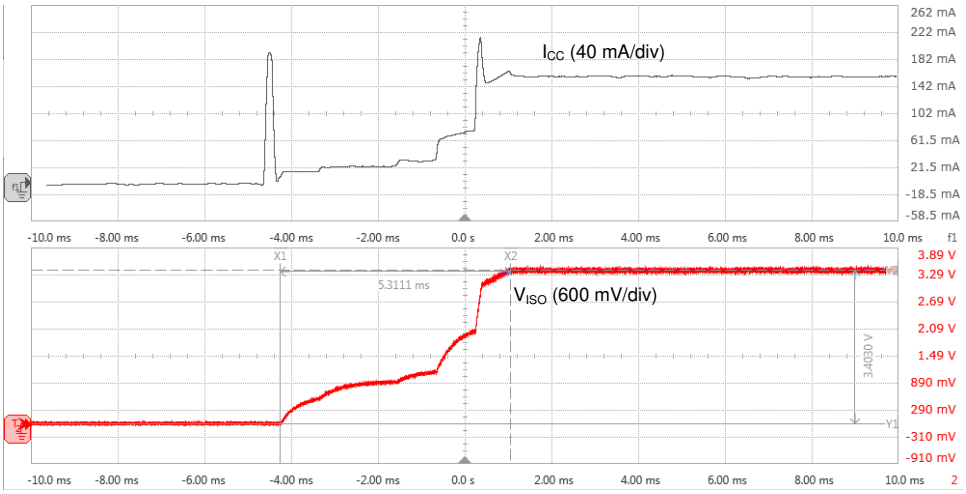
The V_{CC} power-supply input provides power to isolated data channels and to the isolated DC-DC converter. Use 公式 1 to calculate the total power budget on the primary side.

$$I_{CC} = (V_{ISO} \times I_{ISO}) / (\eta \times V_{CC}) + I_{inpx} \quad (1)$$

where

- I_{CC} is the total current required by the primary supply.
- V_{ISO} is the isolated supply voltage.
- I_{ISO} is the external load on the isolated supply voltage.
- η is the efficiency.
- V_{CC} is the supply voltage.
- I_{inpx} is the total current drawn for the isolated data channels and power converter when data channels are toggling at a specific data rate. This data is shown in the *Electrical Characteristics—5-V Input, 5-V Output* table.

10.2.3 Application Curve



V_{CC} = 3.3 V I_{ISO} = 70 mA

Input current spike is because of charging the input supply decoupling capacitor

图 32. Soft-Start Waveform

10.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 图 33 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

图 34 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1000 V_{RMS} with a lifetime of 1184 years.

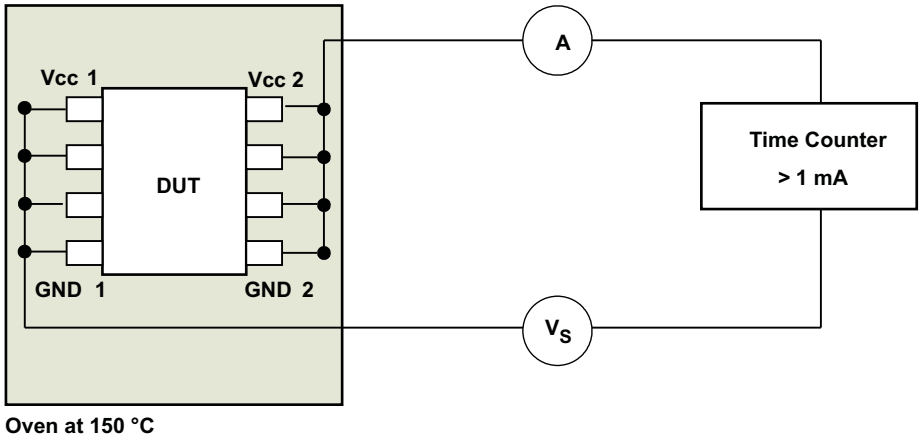


图 33. Test Setup for Insulation Lifetime Measurement

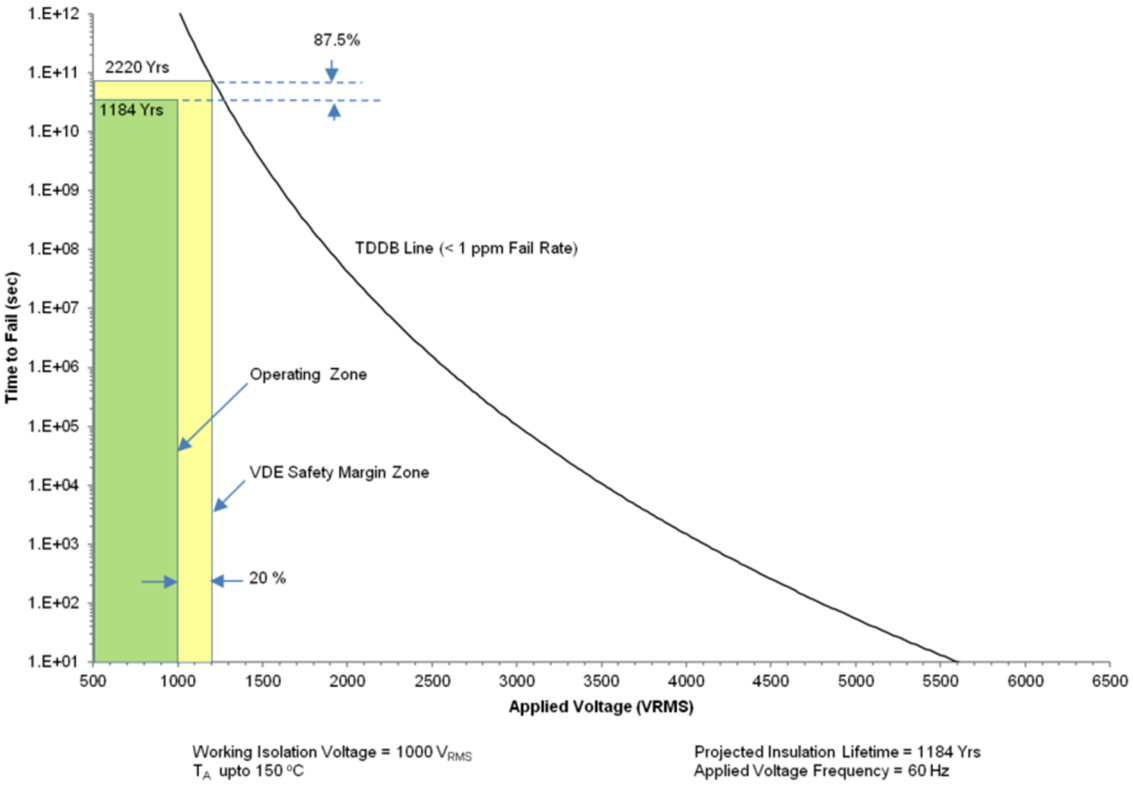


图 34. Insulation Lifetime Projection Data

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. The input supply must have an appropriate current rating to support output load and switching at the maximum data rate required by the end application. For more information, refer to the *Detailed Design Procedure* section.

ISOW7821 integrates a synchronous, isolated DC/DC converter along with isolated data channels. Due to finite efficiency of the integrated micro-transformer, for any given output load current, the input current will be proportionally higher. Thus, the input supply (V_{CC}) decoupling capacitor also needs to be sufficiently larger than the output supply (V_{ISO}) decoupling capacitor. It is recommended to have an input capacitor that is larger than the output capacitor by at least 100 µF. It is also recommended to have an input power supply to ISOW7821 with sufficient current limit to support output load current requirements. For an output load current of 130 mA, it is recommended to have >600 mA of input current limit and for lower output load currents, the input current limit can be proportionally lower. When the input supply is lower than 2.7 V, the device can go into a protected under-voltage lock out (UVLO) state per the UVLO thresholds specified in datasheet. Under UVLO state, it is recommended that the output voltage also be discharged to less than 2.1 V. This can be accomplished by having an input capacitor that is 100 µF larger compared to the output capacitor. It also helps to have a small load (~10 mA) at the output capacitor to bleed off any unwanted, residual charge. To make sure ISOW7821 quickly transitions from UVLO state to powered state, it is recommended to have an input supply rise time of less than 10 ms.

If it is not possible to follow the aforementioned recommendations and frequent brownouts are expected on the input supply, then simple secondary side monitoring, protection and reset components can help improve the robustness of overall system and power-up or reset mechanisms. More details on output monitoring, protection and an example of reset mechanism can be found in *Overvoltage protection for isolated DC/DC converter*.

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low-EMI PCB design (see 图 35). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Keep decoupling capacitors as close as possible to the V_{CC} and V_{ISO} pins.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

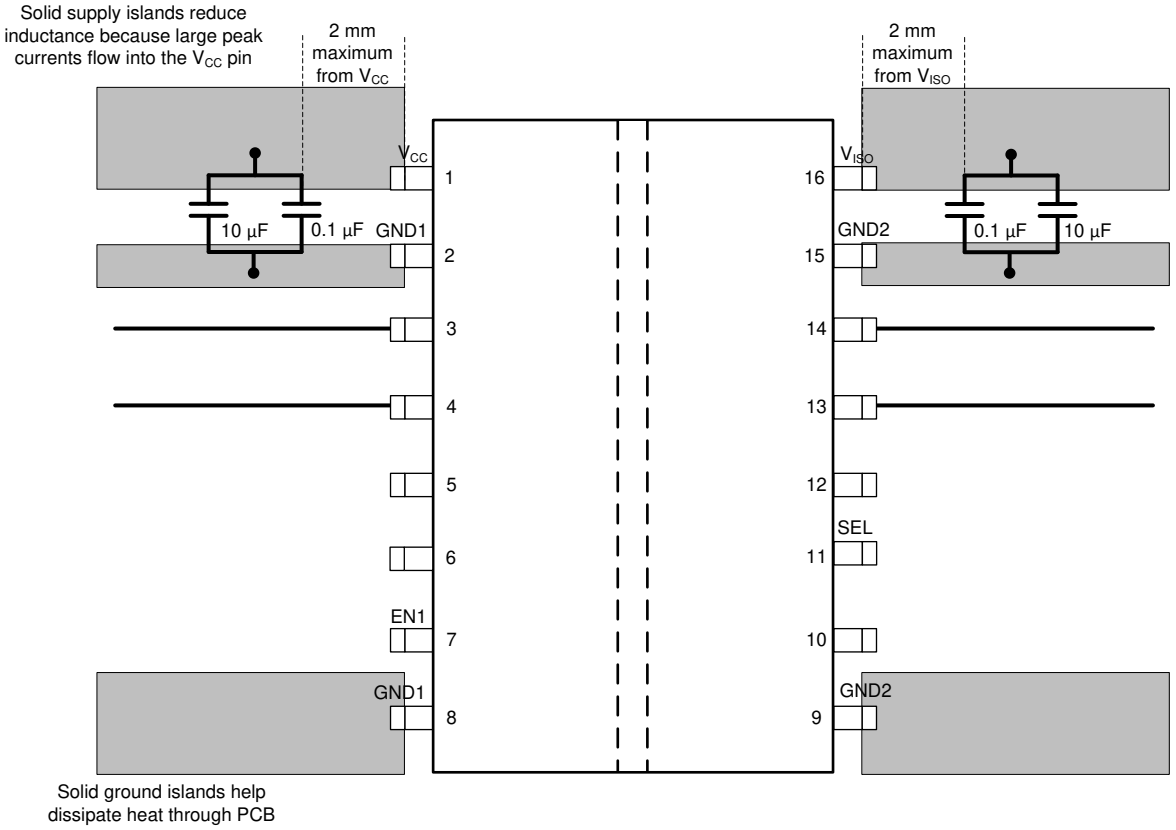
Because the device has no thermal pad to dissipate heat, the device dissipates heat through the respective GND pins. Ensure that enough copper is present on both GND pins to prevent the internal junction temperature of the device from rising to unacceptable levels.

The ISOW7821 integrated signal and power isolation device simplifies system design and reduces board area. The use of low-inductance micro-transformers in the ISOW7821 device necessitates the use of high frequency switching, resulting in higher radiated emissions compared to discrete solutions. The ISOW7821 device uses on-chip circuit techniques to reduce emissions compared to competing solutions. For further reduction in radiated emissions at system level, refer to the *Low-Emission Designs With ISOW7841 Integrated Signal and Power Isolator* application report.

12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.2 Layout Example



Optional 100 µF capacitor can be added between V_{CC} and GND1; refer to *Power Supply Recommendations*.

图 35. Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 开发支持

如需开发支持，请参阅*使用数字隔离器并集成电源的尺寸和成本优化型二进制模块参考设计* TI 设计

13.2 文档支持

13.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《数字隔离器设计指南》*
- 德州仪器 (TI)，*《隔离相关术语》*
- 德州仪器 (TI)，*《具有集成直流/直流转换器的 ISOW784x 四通道数字隔离器评估模块》*用户指南

13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 商标

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13.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOW7821DWE	Active	Production	SOIC (DWE) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW7821
ISOW7821DWE.A	Active	Production	SOIC (DWE) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW7821
ISOW7821DWE.B	Active	Production	SOIC (DWE) | 16	40 | TUBE	-	Call TI	Call TI	-40 to 125	
ISOW7821DWER	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW7821
ISOW7821DWER.A	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW7821
ISOW7821DWER.B	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOW7821FDWE	Active	Production	SOIC (DWE) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW7821F
ISOW7821FDWE.A	Active	Production	SOIC (DWE) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW7821F
ISOW7821FDWE.B	Active	Production	SOIC (DWE) | 16	40 | TUBE	-	Call TI	Call TI	-40 to 125	
ISOW7821FDWER	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW7821F
ISOW7821FDWER.A	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW7821F
ISOW7821FDWER.B	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

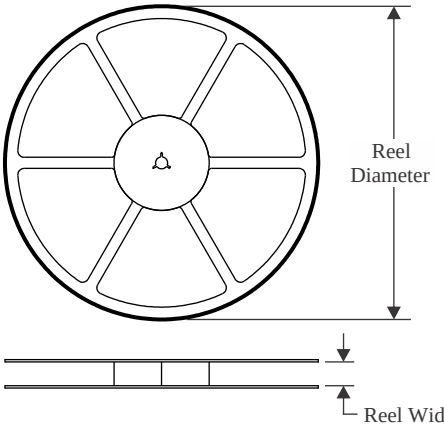
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

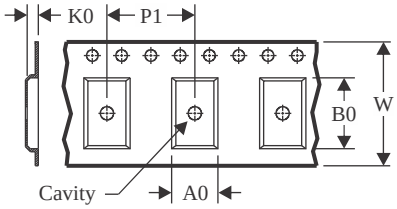
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

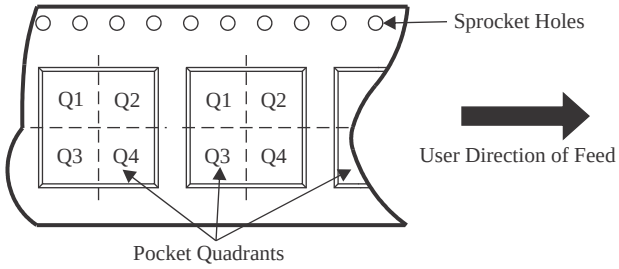


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

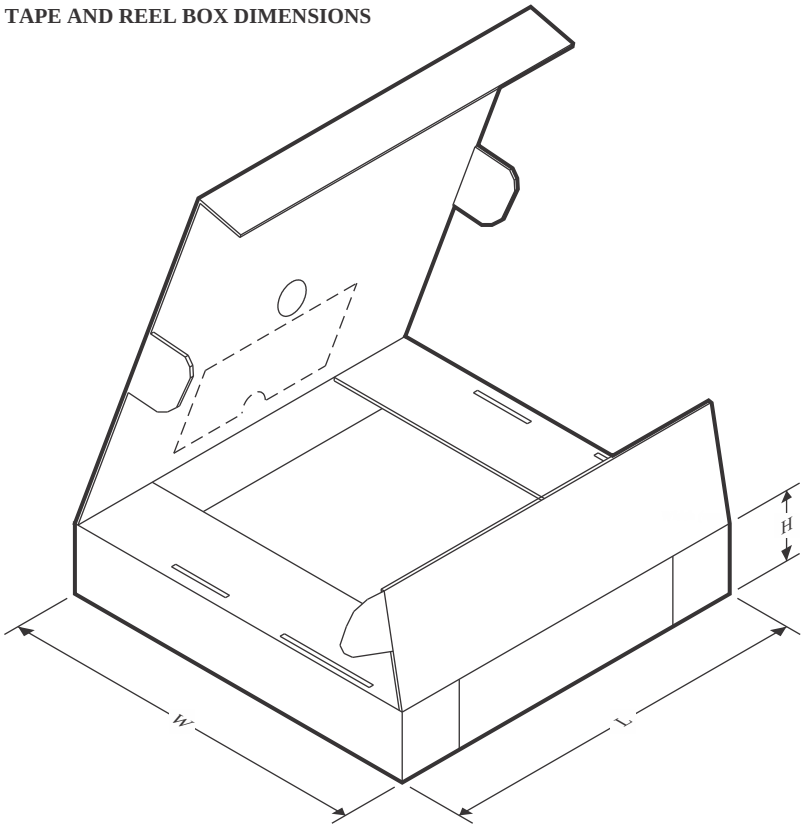
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOW7821DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISOW7821FDWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

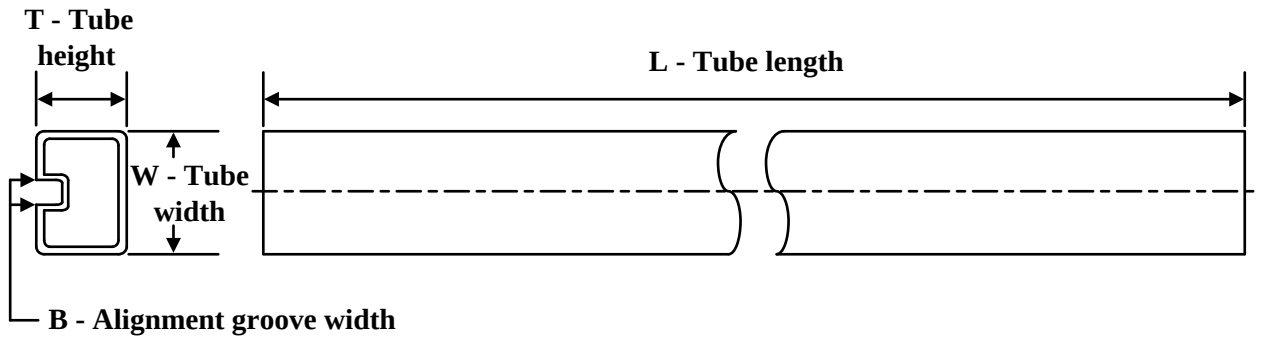
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

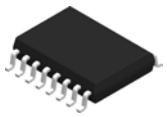
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOW7821DWER	SOIC	DWE	16	2000	350.0	350.0	43.0
ISOW7821FDWER	SOIC	DWE	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISOW7821DWE	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6
ISOW7821DWE.A	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6
ISOW7821FDWE	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6
ISOW7821FDWE.A	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6

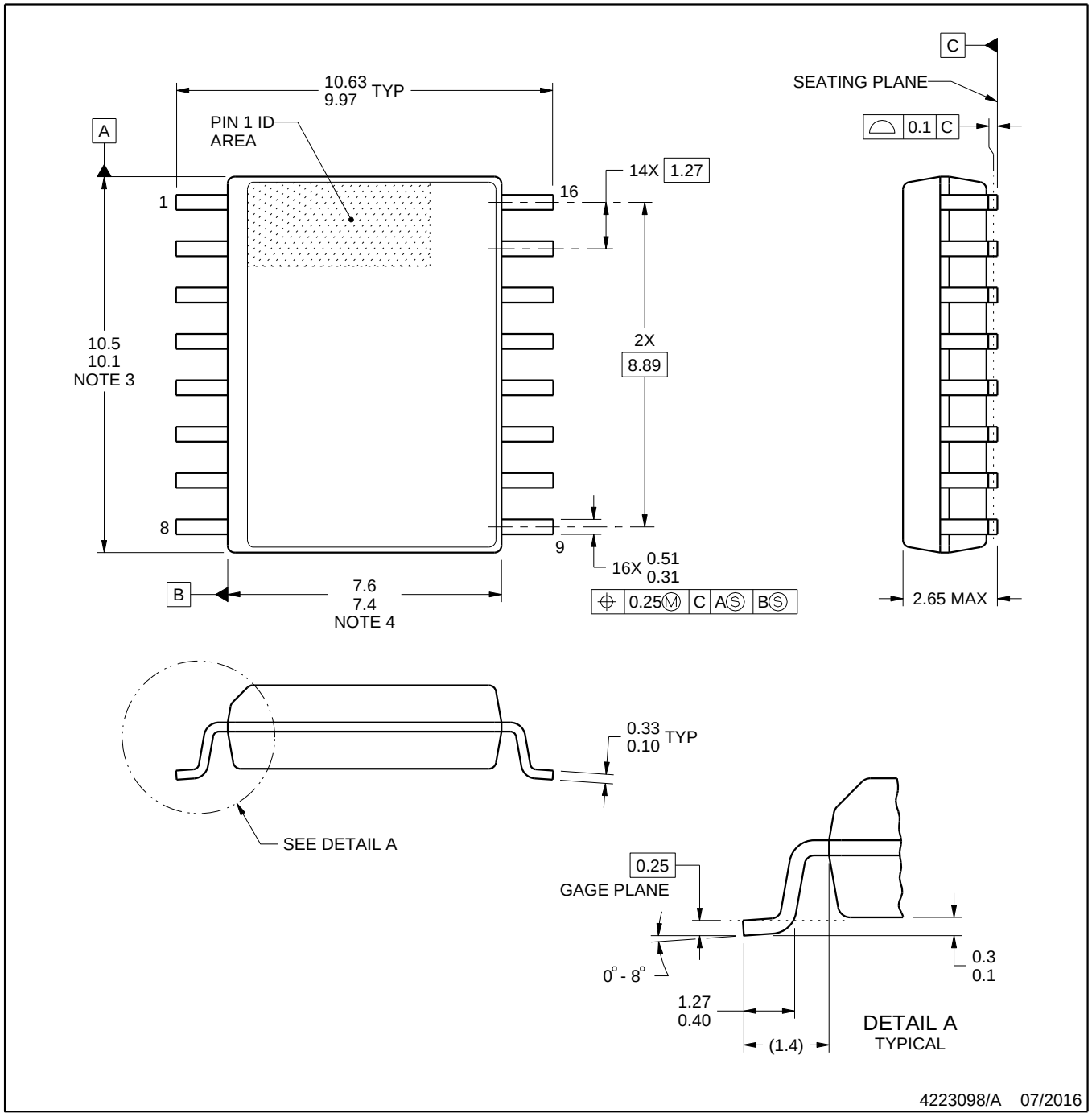


PACKAGE OUTLINE

DWE0016A

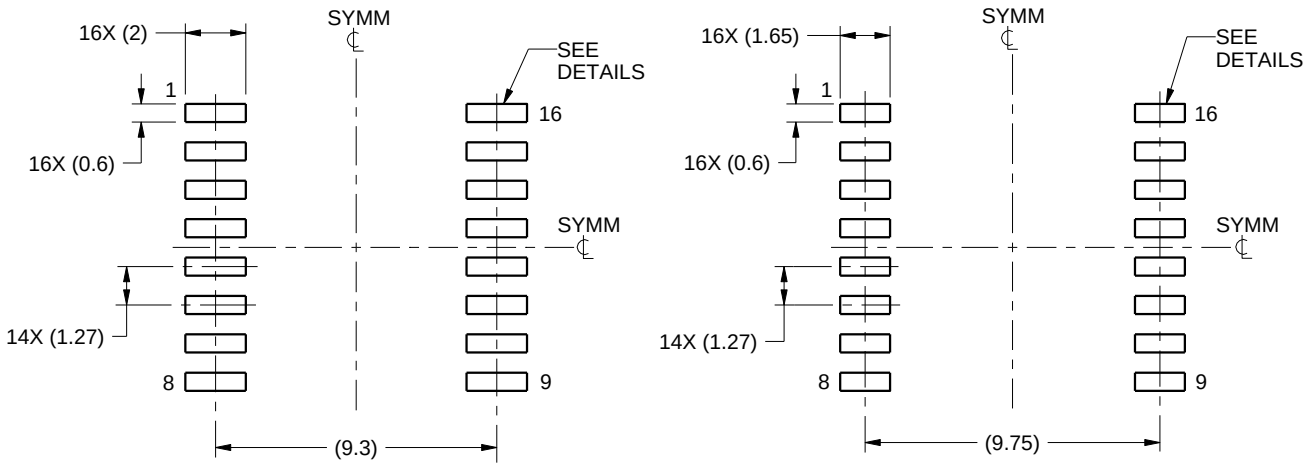
SOIC - 2.65 mm max height

SOIC



NOTES:

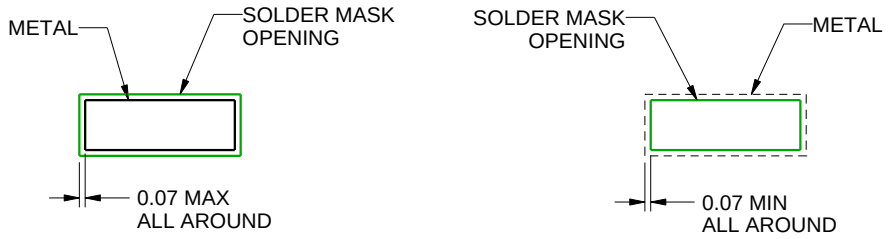
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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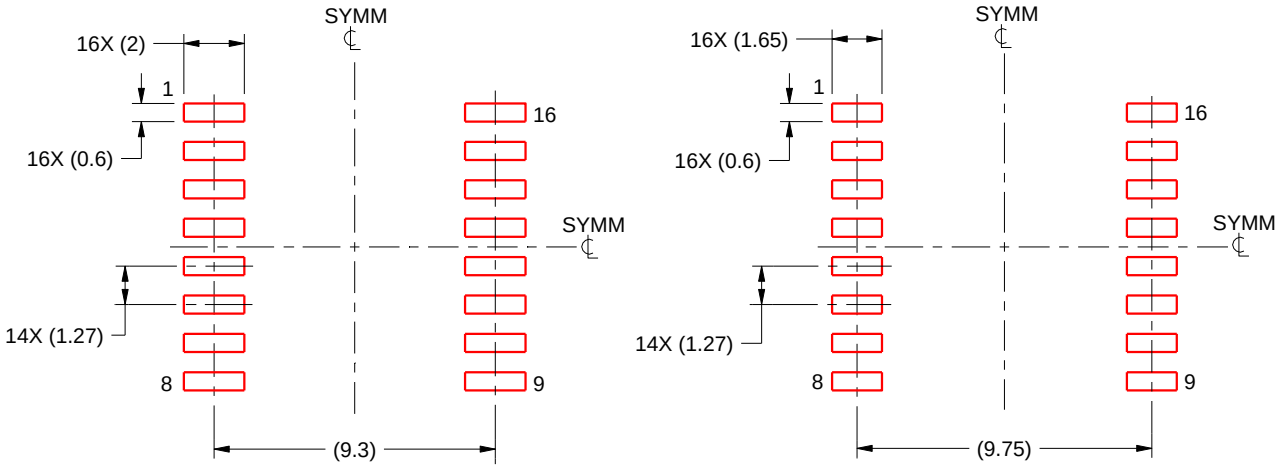
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月