ISO764xFM 低功耗四通道数字隔离器

1 特性

- 信号传输速率：150Mbps
- 低功耗，每通道 I_{CC} 典型值（3.3V 电源）：
  - ISO7640FM：在 25Mbps 时为 2mA
  - ISO7641FM: 在 25 Mbps 时为 2.4mA
- 低传播延迟：7ns（典型值）
- 故障安全模式下的输出默认为低电平状态
- 宽温度范围：-40°C 至 125°C
- 50kV/μs 瞬态抗扰度，典型值
- 采用 SiO_2 隔离格栅，使用寿命长
- 可由 2.7V、3.3V 和 5V 电源及逻辑电平供电
- 宽体小外形尺寸集成电路 (SOIC)-16 封装
- 安全及管理批准
  - 符合 UL 1577 且长达 1 分钟的 6000 V_{PK}/4243 V_{RMS}
  - VDE 6000 V_{PK} 瞬态过压，符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准的 1414 V_{PK} 工作电压
  - CSA 组件接受通知 5A、IEC 60950-1、IEC 61010-1 和 IEC 60601-1 终端设备标准
  - 符合 EN/UL/CSA 60950-1 和 EN/UL/CSA 61010-1 标准的 TUV 5 KV_{RMS} 强化绝缘
  - 符合 GB4943.1-2011 标准的 CQC 强化绝缘

2 应用

- 是下列应用中光耦合器的替代产品：
  - 工业现场总线 (Fieldbus)
    - Profibus 现场总线
    - Modbus
    - DeviceNet™ 数据总线
  - 伺服控制接口
  - 电机控制
  - 电源
  - 电池组

3 说明

ISO7640FM 和 ISO7641FM 可提供符合 UL 和 VDE 标准且长达 1 分钟的 6 KV_{PK} 电流隔离。 经实践证明，这些器件在 400 V_{RMS} 工作电压下可提供符合终端设备标准 EN/UL/CSA 60950-1 和 61010-1 且高达 5 KV_{RMS} 的强化绝缘。 ISO7640F 和 ISO7641F 均为四通道隔离器；ISO7640F 有四个正向通道，而 ISO7641F 有三个正向通道和一个反向通道。 后缀 F 表示故障安全情况下输出默认为低电平状态（请参见 表 4）。 M 级器件为高速隔离器，具有 150Mbps 的数据传输速率和短暂传播延迟。

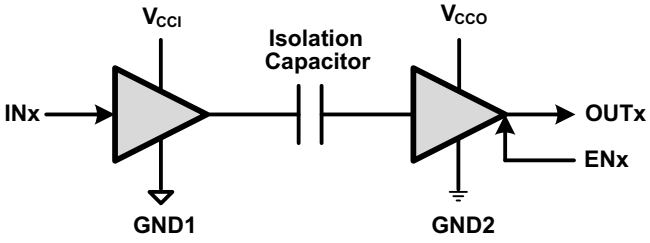
每个隔离通道都有一个由二氧化硅 (SiO_2) 绝缘隔栅分开的逻辑输入和输出缓冲器。 与隔离电源配合使用，这些器件可防止数据总线或者其它电路上的噪声电流进入本地接地或者干扰或损坏敏感电路。 这些器件具有晶体管晶体管逻辑电路 (TTL) 输入阈值，并且可由 2.7V、3.3V 和 5V 电压供电运行。 通过 3.3V 或 2.7V 电源供电时，所有输入均可耐受 5V 电压。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO7640FM	SOIC (16)	10.30mm x 7.50mm
ISO7641FM		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (September 2013) to Revision G — **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 已将 VDE 标准更改为 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12。 ... 1

Changes from Revision E (January 2013) to Revision F — **Page**

- 已更改 the REGULATORY INFORMATION table, TUV column From: Certificate Number: U8V 13 07 77311 009 To: Certificate Number: U8V 13 09 77311 010 ... 22

Changes from Revision D (July 2012) to Revision E — **Page**

- Changed Z to Undetermined in the OUTPUT (OUTx) column of the FUNCTION TABLE ... 24

Changes from Revision C (January 2012) to Revision D — **Page**

- 已从数据表中删除器件：ISO7631FM、ISO7631FC、ISO7640FC 和 ISO7641FC ... 1
- 已将标题从：低功耗三通道和四通道数字隔离器更改为：低功耗四通道数字隔离器 ... 1
- 已从特性列表删除器件 ... 1

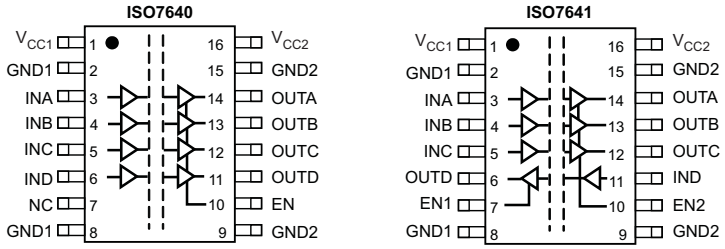
Changes from Revision B (December 2011) to Revision C **Page**

Changes from Revision A (October 2011) to Revision B **Page**

Changes from Original (September 2011) to Revision A **Page**

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO7640	ISO7641		
EN	10	-	I	Enables (when High or Open) or Disables (when Low) OUTA, OUTB, OUTC and OUTD of ISO7640
EN1	-	7	I	Enables (whenHigh or Open) or Disables (when Low) OUTD of ISO7641
EN2	-	10	I	Enables (when High or Open) or Disables (when Low) OUTA, OUTB, and OUTC of ISO7641
GND1	2	2	–	Ground connection for V_{CC1}
	8	8		
GND2	9	9	–	Ground connection for V_{CC2}
	15	15		
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	5	I	Input, channel C
IND	6	11	I	Input, channel D
NC	7	-	-	No Connect pins are floating with no internal connection
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	12	O	Output, channel C
OUTD	11	6	O	Output, channel D
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	–	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage(2)	V_{CC1}, V_{CC2}	–0.5	6	V
Voltage	INx, OUTx, ENx	–0.5	V_{CC} + 0.5(3)	V
Output Current, I_O		–15	15	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	
		Machine model, per JEDEC JESD22-A115-A	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.7		5.5	V
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage		0		0.8	V
t_{ui}	Input pulse duration	≥3-V Operation	6.67			ns
		<3-V Operation	10			
1 / t_{ui}	Signaling rate	≥3-V Operation	0		150	Mbps
		<3-V Operation	0		100	
T_J	Junction temperature		–40		136	°C
T_A	Ambient temperature		–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)			ISO76xx DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		72	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance		38	
$R_{\theta JB}$	Junction-to-board thermal resistance		39	
ψ_{JT}	Junction-to-top characterization parameter		9.4	
P_D	Maximum Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15 pF Input a 75-MHz 50% duty cycle square wave	399	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 图 9	V_{CCO} (1) –0.8	4.8		V
		I_{OH} = –20 μA; see 图 9	V_{CCO} (1) –0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 9		0.2	0.4	V
		I_{OL} = 20 μA; see 图 9		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see 图 12	25	75		kV/μs

(1) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

6.6 Electrical Characteristics: V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10%

V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 图 9	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.8	4.8		V
			OUTx on V_{CC2} (3.3V) side	V_{CC2} – 0.4	3		
		I_{OH} = –20 μA; see 图 9	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.1	5		
			OUTx on V_{CC2} (3.3V) side	V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 9			0.2	0.4	V
		I_{OL} = 20 μA; see 图 9			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see 图 12		25	50		kV/μs

6.7 Electrical Characteristics: V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10%

V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 图 9	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.4	3		V
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.8	4.8		
		I_{OH} = –20 μA; see 图 9	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.1	3.3		
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 9			0.2	0.4	V
		I_{OL} = 20 μA; see 图 9			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see 图 12		25	50		kV/μs

6.8 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 图 9	V_{CCO}(1) – 0.4	3		V
		I_{OH} = –20 µA; see 图 9	V_{CCO}(1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 9		0.2	0.4	V
		I_{OL} = 20 µA; see 图 9		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			425		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see 图 12	25	50		kV/µs

(1) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

6.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V(1) (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 图 9	V_{CCO}(2) – 0.5	2.4		V
		I_{OH} = –20 µA; see 图 9	V_{CCO}(2) – 0.1	2.7		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 9		0.2	0.4	V
		I_{OL} = 20 µA; see 图 9		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			350		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see 图 12	25	50		kV/µs

(1) For 2.7-V operation, max data rate is 100 Mbps.
(2) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

6.10 Supply Current: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.6	1.2	mA
I_{CC2}				4.5	6.6	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.7	1.3	
I_{CC2}				4.6	6.7	
I_{CC1}	10 Mbps			1.1	2	
I_{CC2}				6.6	10.5	
I_{CC1}	25 Mbps			1.9	3	
I_{CC2}				9.7	14.7	
I_{CC1}	150 Mbps			8.2	14.5	
I_{CC2}				35	58	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.6	4.2	mA
I_{CC2}				4.2	6.8	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.7	4.3	
I_{CC2}				4.3	6.9	
I_{CC1}	10 Mbps			3.6	4.9	
I_{CC2}				6	8.2	
I_{CC1}	25 Mbps			5.1	6.6	
I_{CC2}				8.8	11.4	
I_{CC1}	150 Mbps			17	22	
I_{CC2}				31	42	

6.11 Supply Current: V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10%

V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.6	1.2	mA
I_{CC2}				3.6	5.1	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.7	1.3	
I_{CC2}				3.7	5.2	
I_{CC1}	10 Mbps			1.1	2	
I_{CC2}				5	7.1	
I_{CC1}	25 Mbps			1.9	3	
I_{CC2}				6.9	11	
I_{CC1}	150 Mbps			8.2	14.5	
I_{CC2}				24	40	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.6	4.2	mA
I_{CC2}				3.2	4.9	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.7	4.3	
I_{CC2}				3.3	5	
I_{CC1}	10 Mbps			3.6	4.9	
I_{CC2}				4.4	5.8	
I_{CC1}	25 Mbps			5.1	6.6	
I_{CC2}				6.1	7.6	
I_{CC1}	150 Mbps			17	22	
I_{CC2}				20.6	26.5	

6.12 Supply Current: V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10%

V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.35	0.7	mA
I_{CC2}				4.5	6.6	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.4	0.8	
I_{CC2}				4.6	6.7	
I_{CC1}	10 Mbps			0.7	1.2	
I_{CC2}				6.6	10.5	
I_{CC1}	25 Mbps			1.1	2	
I_{CC2}				9.7	14.7	
I_{CC1}	150 Mbps			5	8.5	
I_{CC2}				35	58	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.9	2.9	mA
I_{CC2}				4.2	6.8	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2	3	
I_{CC2}				4.3	6.9	
I_{CC1}	10 Mbps			2.5	3.5	
I_{CC2}				6	8.2	
I_{CC1}	25 Mbps			3.4	4.5	
I_{CC2}				8.8	11.4	
I_{CC1}	150 Mbps			10.5	14.5	
I_{CC2}				31	42	

6.13 Supply Current: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.35	0.7	mA
I_{CC2}				3.6	5.1	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.4	0.8	
I_{CC2}				3.7	5.2	
I_{CC1}	10 Mbps			0.7	1.2	
I_{CC2}				5	7.1	
I_{CC1}	25 Mbps			1.1	2	
I_{CC2}				6.9	11	
I_{CC1}	150 Mbps			5	8.5	
I_{CC2}				24	40	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.9	2.9	mA
I_{CC2}				3.2	4.9	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2	3	
I_{CC2}				3.3	5	
I_{CC1}	10 Mbps			2.5	3.5	
I_{CC2}				4.4	5.8	
I_{CC1}	25 Mbps			3.4	4.5	
I_{CC2}				6.1	7.6	
I_{CC1}	150 Mbps			10.5	14.5	
I_{CC2}				20.6	26.5	

6.14 Supply Current: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.2	0.6	mA
I_{CC2}				3.3	5	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.2	0.7	
I_{CC2}				3.4	5.1	
I_{CC1}	10 Mbps			0.4	1.1	
I_{CC2}				4.4	6.8	
I_{CC1}	25 Mbps			0.8	1.8	
I_{CC2}				6	9.5	
I_{CC1}	100 Mbps			2.7	5	
I_{CC2}				14.2	21	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.6	2.4	mA
I_{CC2}				2.8	4.1	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.7	2.5	
I_{CC2}				2.9	4.2	
I_{CC1}	10 Mbps			2.1	3	
I_{CC2}				3.8	5	
I_{CC1}	25 Mbps			2.8	3.8	
I_{CC2}				5.2	6.7	
I_{CC1}	100 Mbps			6.4	7.5	
I_{CC2}				11.8	15.5	

6.15 Switching Characteristics: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 9	3.5	7	10.5	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$	See 图 9			2	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2	ns
		Opposite-direction Channels			3	ns
$t_{sk(pp)}$(3)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See 图 9		1.6		ns
t_f	Output signal fall time	See 图 9		1		ns
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See 图 10		5	16	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output	See 图 10		5	16	ns
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	See 图 10		4	16	ns
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	See 图 10		4	16	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See 图 11		9.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics: V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10%

V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 9	4	8	13	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$	See 图 9			2	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2.5	ns
		Opposite-direction Channels			3.5	ns
$t_{sk(pp)}$(3)	Part-to-part skew time				6	ns
t_r	Output signal rise time	See 图 9		2		ns
t_f	Output signal fall time	See 图 9		1.2		ns
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See 图 10		6.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output	See 图 10		6.5	17	ns
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	See 图 10		5.5	17	ns
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	See 图 10		5.5	17	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See 图 11		9.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics: V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10%

V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 9	4	7.5	12.5	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$	See 图 9			2	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2.5	ns
		Opposite-direction Channels			3.5	ns
$t_{sk(pp)}$(3)	Part-to-part skew time				6	ns
t_r	Output signal rise time	See 图 9		1.7		ns
t_f	Output signal fall time	See 图 9		1.1		ns
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See 图 10		5.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output	See 图 10		5.5	17	ns
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	See 图 10		4.5	17	ns
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	See 图 10		4.5	17	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See 图 11		9.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 9	4	8.5	14	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$	See 图 9			2	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			3	ns
		Opposite-direction Channels			4	ns
$t_{sk(pp)}$(3)	Part-to-part skew time				6.5	ns
t_r	Output signal rise time	See 图 9		2		ns
t_f	Output signal fall time	See 图 9		1.3		ns
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See 图 10		6.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output	See 图 10		6.5	17	ns
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	See 图 10		5.5	17	ns
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	See 图 10		5.5	17	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See 图 11		9.2		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.19 Switching Characteristics: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 9	5	8	16	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	See 图 9			2.5	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			4	ns
		Opposite-direction Channels			5	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				8	ns
t_r	Output signal rise time	See 图 9		2.3		ns
t_f	Output signal fall time	See 图 9		1.8		ns
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See 图 10		8	18	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output	See 图 10		8	18	ns
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	See 图 10		7	18	ns
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	See 图 10		7	18	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See 图 11		8.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.20 Typical Characteristics

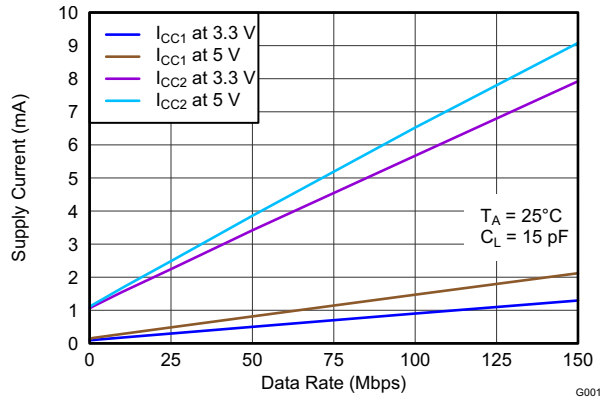


图 1. ISO7640FM Supply Current per Channel vs Data Rate

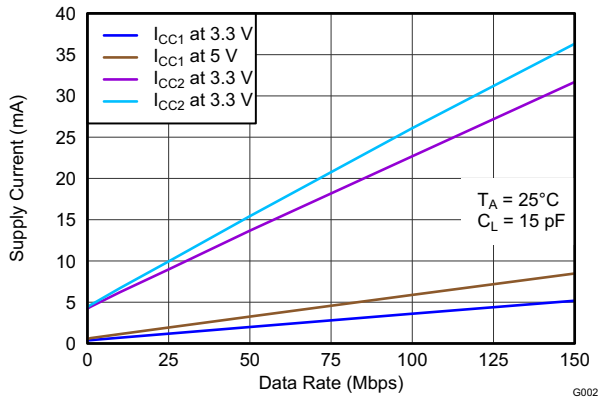


图 2. ISO7640FM Supply Current for All Channels vs Data Rate

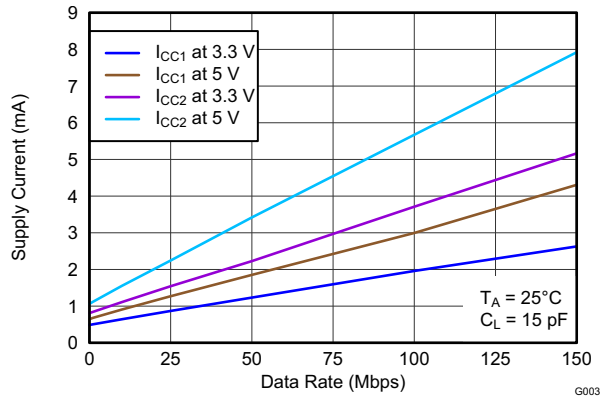


图 3. ISO7641FM Supply Current per Channel vs Data Rate

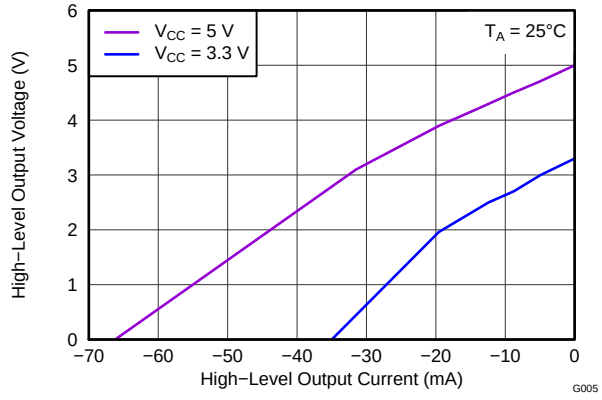


图 4. High-Level Output Voltage vs High-Level Output Current

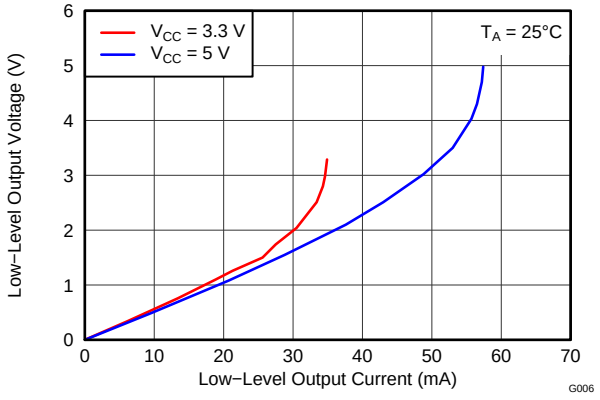


图 5. Low-Level Output Voltage vs Low-Level Output Current

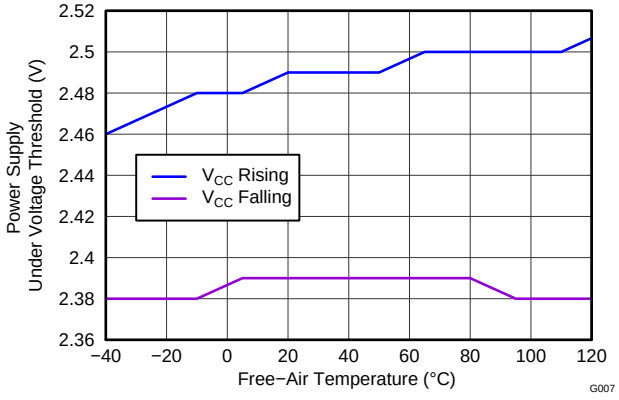


图 6. V_{CC} Undervoltage Threshold vs Free Air Temperature

Typical Characteristics (接下页)

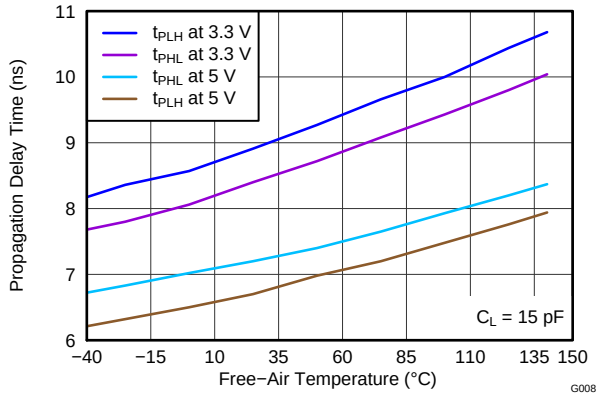


图 7. Propagation Delay Time vs Free Air Temperature

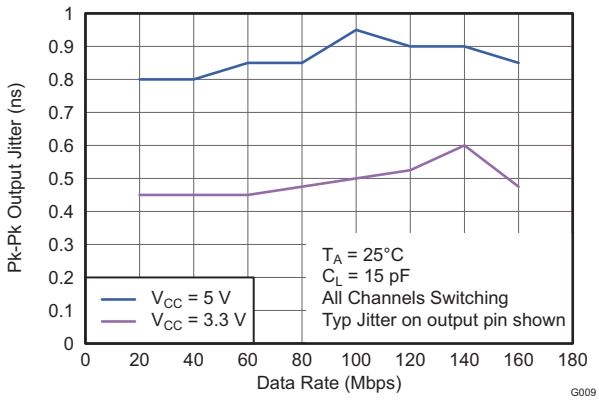
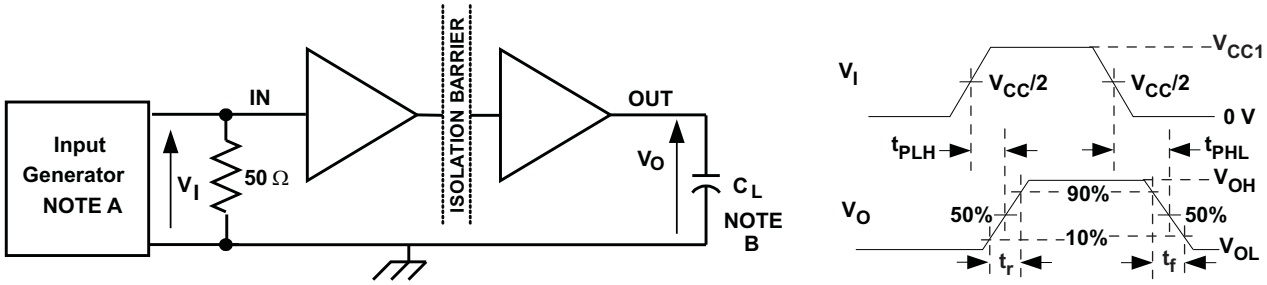


图 8. Output Jitter vs Data Rate

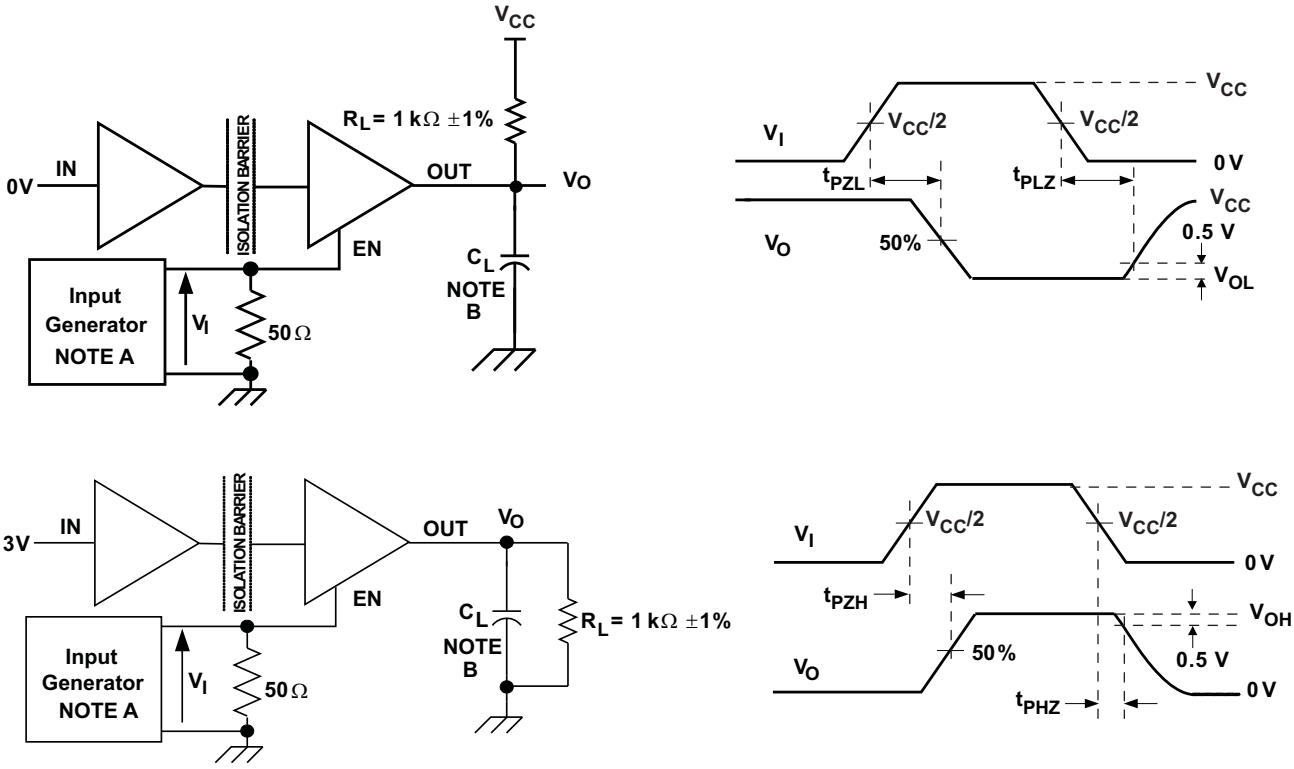
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50-Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 9. Switching Characteristics Test Circuit and Voltage Waveforms

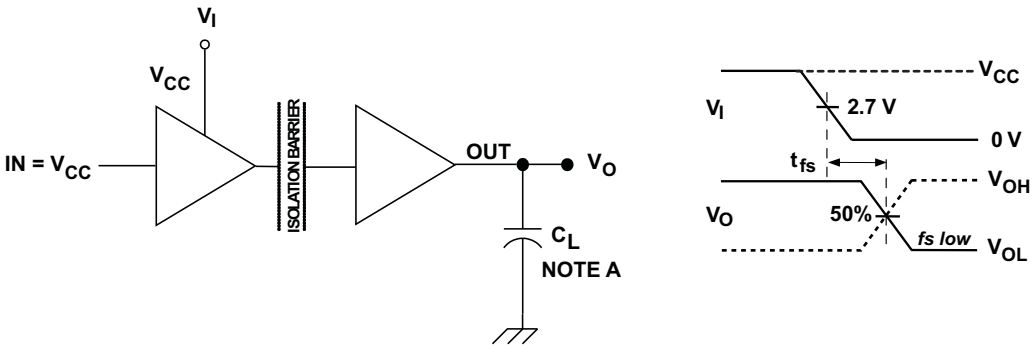


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

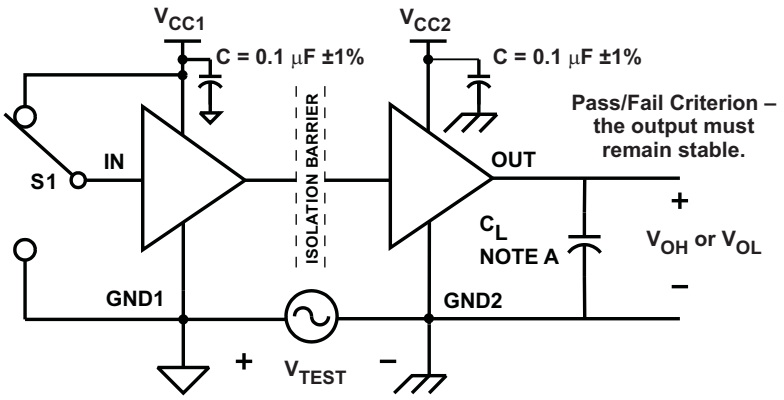
图 10. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (接下页)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 11. Fail-Safe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 12. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in 图 13 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single- ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

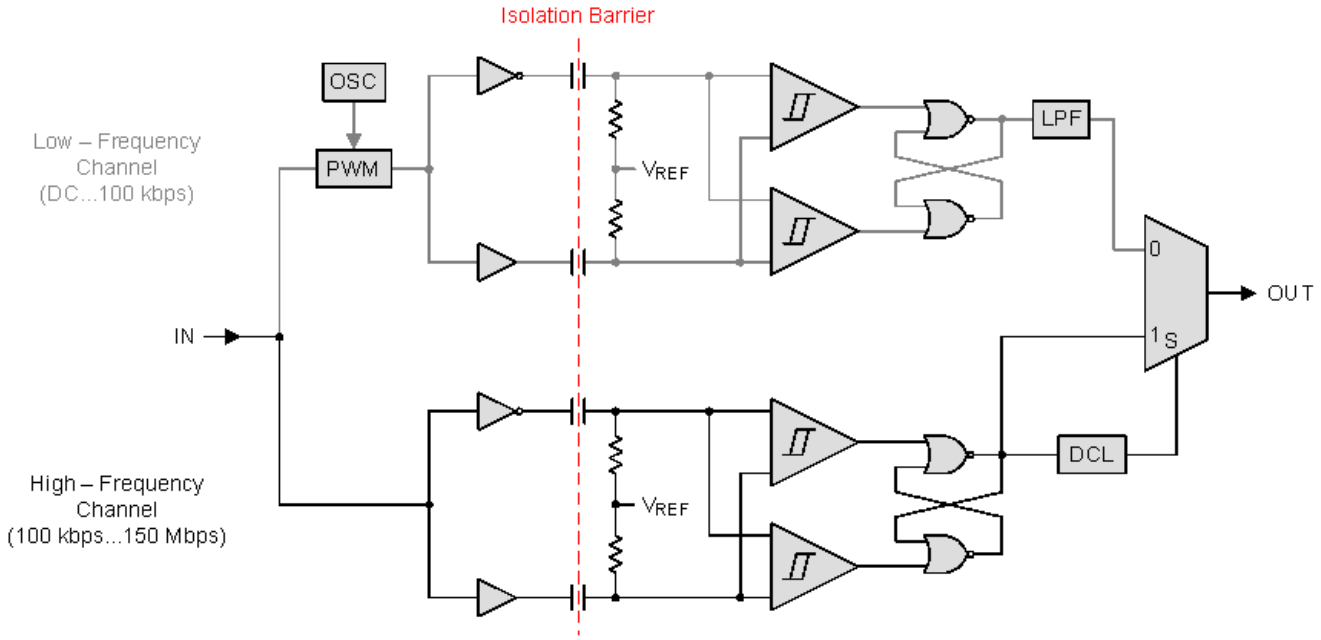


图 13. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

PRODUCT	RATED ISOLATION	PACKAGE	INPUT THRESHOLD	DATA RATE, INPUT FILTER	CHANNEL DIRECTION
ISO7640FM	6 KV_{PK} / 5 KV_{RMS} (1)	DW-16	1.5 V TTL	150 Mbps, No Noise Filter	4 Forward, 0 Reverse
ISO7641FM					3 Forward, 1 Reverse

(1) See the *表 2* table for detailed isolation ratings.

8.3.1 IEC Insulation and Safety-Related Specifications for DW-16 Package

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.3			mm
L(I02) (1)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.014			mm
R_{IO} (2)	Isolation resistance, Input to Output	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		$>10^{11}$		
C_{IO} (2)	Barrier capacitance, Input to Output	V_I = 0.4 sin (2πft), f = 1MHz		2		pF
C_I (3)	Input capacitance	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1MHz, V_{CC} = 5 V		2		pF

(1) Per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.
(3) Measured from input pin to ground.

注

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit-board (PCB) do not reduce this distance.

Creepage and clearance on a PCB become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a PCB are used to help increase these specifications.

8.3.2 DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics

over recommended operating conditions (unless otherwise noted) (4)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		1414	V_{PEAK}
V_{PR}	Input-to-output test voltage	After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	1697	V_{PEAK}
		Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, 100% Production test V_{PR} = V_{IORM} x 1.875, t = 1 s Partial discharge < 5 pC	2652	
V_{IOTM}	Maximum transient overvoltage	V_{TEST} = V_{IOTM} t = 60 sec (Qualification) t = 1 sec (100% Production)	6000	V_{PEAK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(4) Climatic Classification 40/125/21

表 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation classification	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–III
	Rated mains voltage ≤ 1000 V_{RMS}	I–II

表 2. Regulatory Information

VDE	TUV	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0084-10):2006-12	Certified according to EN/UL/CSA 60950-1 and EN/UL/CSA 61010-1	Approved under CSA Component Acceptance Notice 5A, IEC 61010-1, IEC 60950-1, IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation, Maximum Transient Overvoltage, 6000 V_{PK} , Maximum Working Voltage, 1414 V_{PK}	5000 V_{RMS} Isolation Rating, Reinforced Insulation, 400 V_{RMS} maximum working voltage, Basic Insulation, 600 V_{RMS} maximum working voltage	5000 V_{RMS} Isolation Rating, 380 V_{RMS} Reinforced and 760 V_{RMS} Basic working voltage per CSA 60950-1-07 and IEC 60950-1 (2nd Ed.), 300 V_{RMS} Reinforced and 600 V_{RMS} Basic working voltage per CSA 61010-1-04 and IEC 61010-1 (2nd Ed.), 2 Means of Patient Protection at 125 V_{RMS} per CSA 60601-1:08 and IEC 60601-1 (3rd Ed.)	Single Protection, 4243 V_{RMS} (1)	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Certificate number: U8V 13 09 77311 010	Master contract number: 220991	File Number: E181974	Certificate number: CQC14001109542

(1) Production tested ≥ 5092 VRMS for 1 second in accordance with UL 1577.

8.3.3 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

表 3. Safety Limiting Values

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 72°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			316	mA
			θ_{JA} = 72°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			482	
			θ_{JA} = 72°C/W, V_I = 2.7 V, T_J = 150°C, T_A = 25°C			643	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

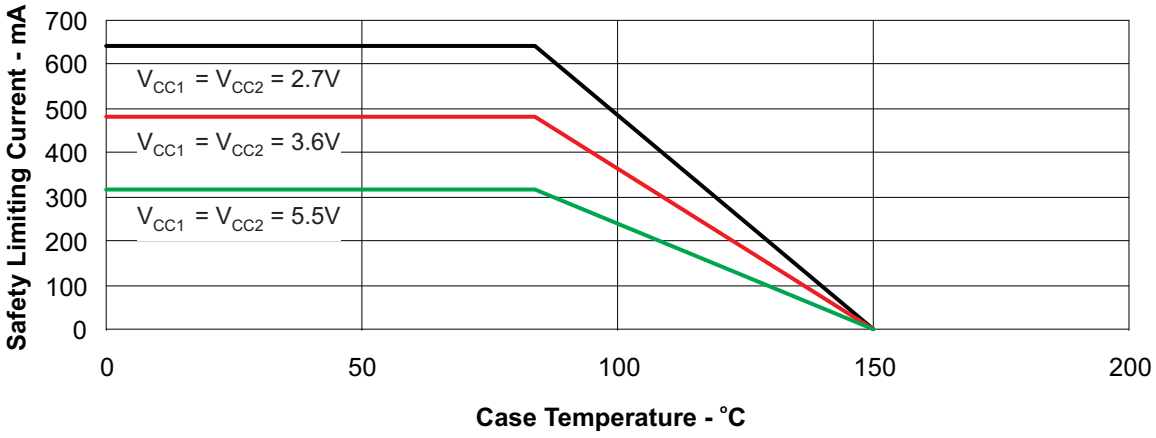


图 14. DW-16 θ_{JC} Thermal Derating Curve per DIN V VDE V 0884-10

8.4 Device Functional Modes

表 4. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	L
PD	PU	X	H or Open	L
PD	PU	X	L	Z
X	PD	X	X	Undetermined

(1) V_{CCI} = Input-side VCC; V_{CCO} = Output-side V_{CC}; PU = Powered Up (V_{CC} ≥ 2.7 V); PD = Powered Down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

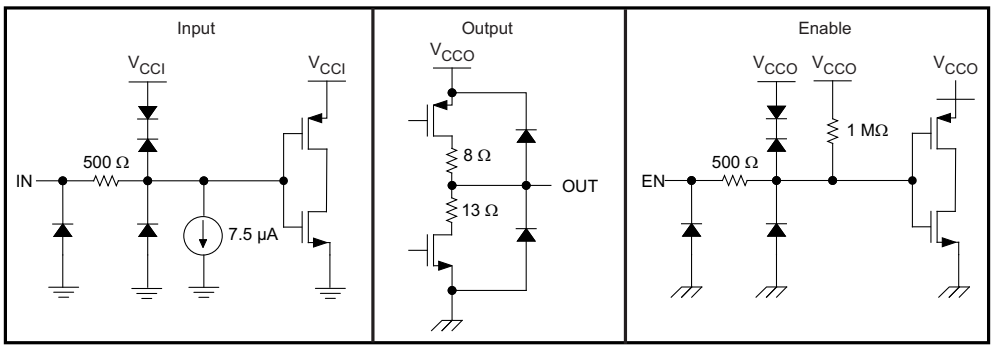


图 15. Device I/O Schematics

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO764x use single-ended TTL-logic switching technology. Its supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to note that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

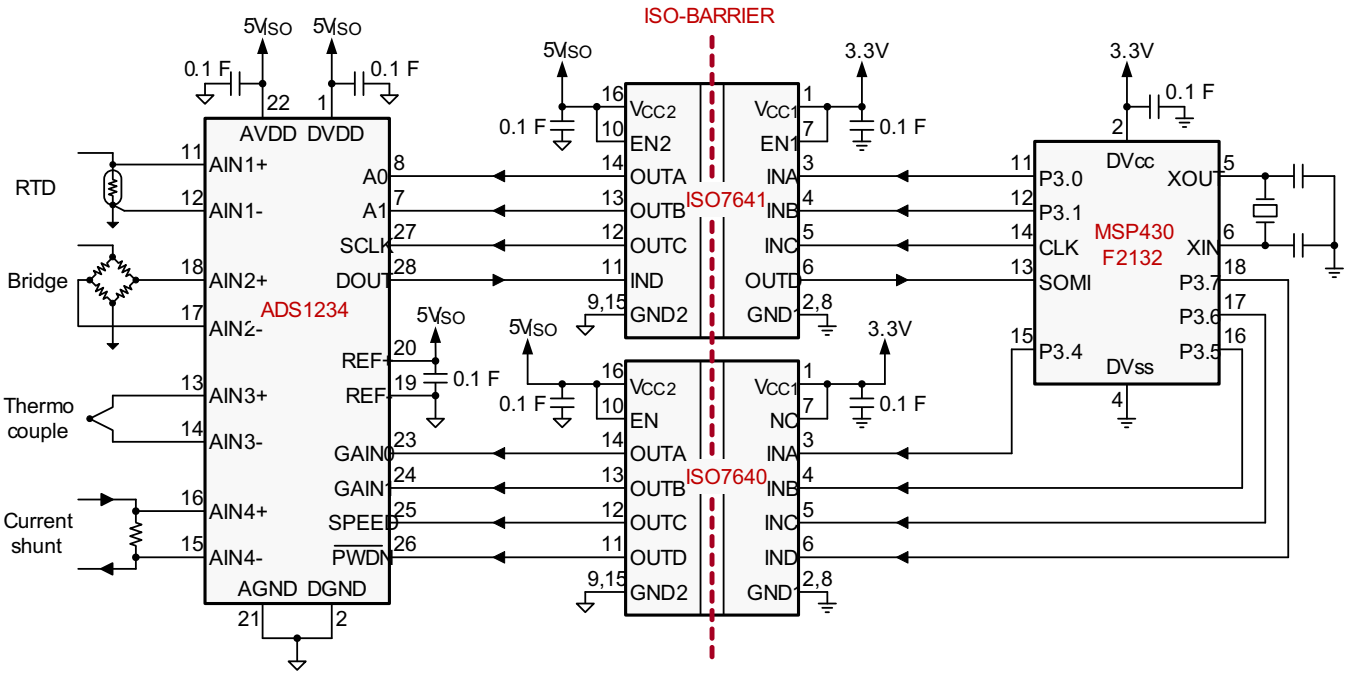


图 16. Isolated Data Acquisition System for Process Control

9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO764x device only requires two external bypass capacitors to operate.

Typical Application (接下页)

9.2.2 Detailed Design Procedure

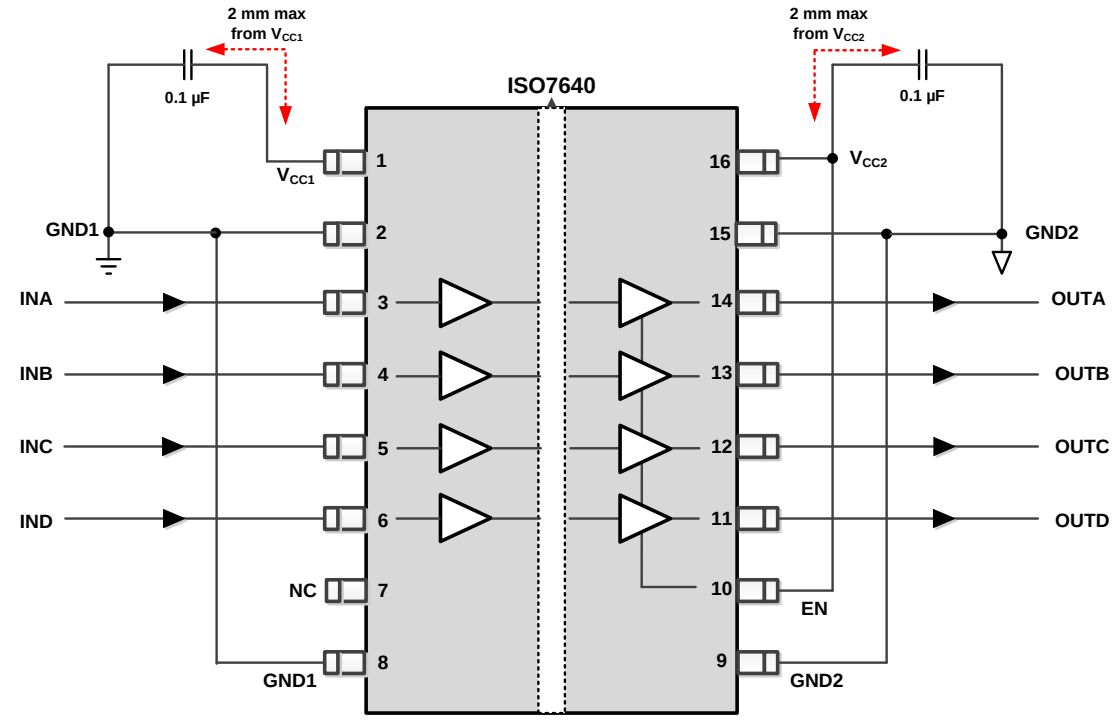


图 17. Typical ISO7640FM Circuit Hookup

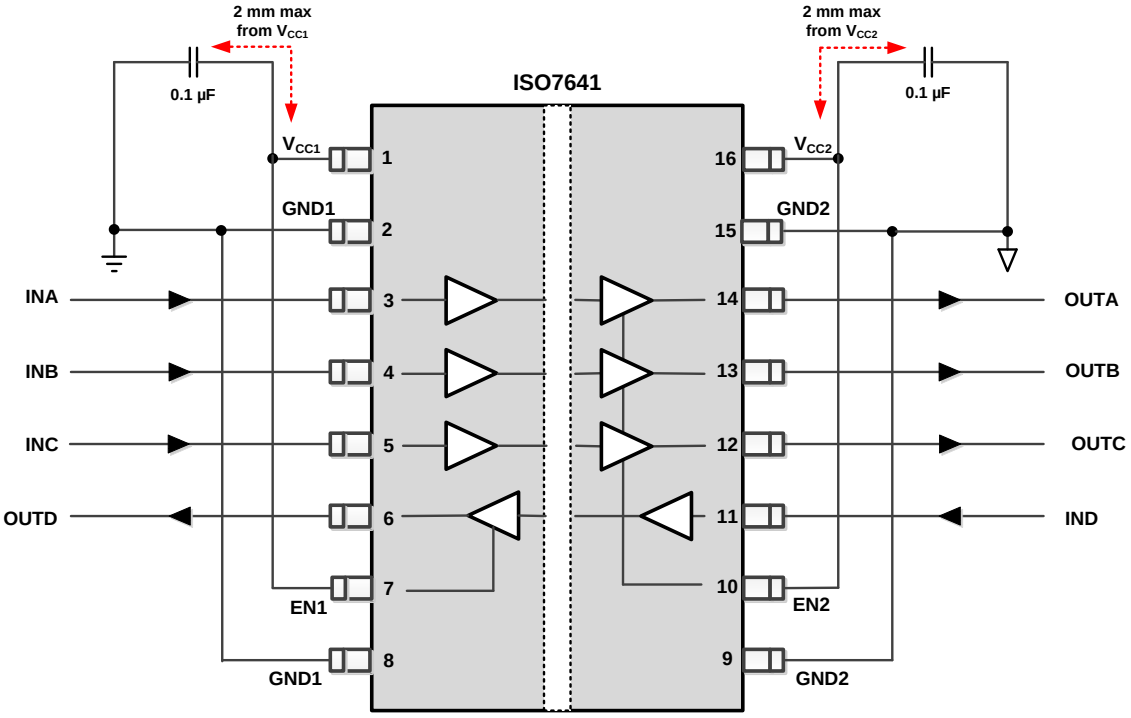


图 18. Typical ISO7641FM Circuit Hookup

Typical Application (接下页)

9.2.2.1 Typical Supply Current Equations

(Calculated based on room temperature and typical Silicon process)

ISO7640FM:

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 0.388 + 0.0312 \times f \quad (1)$$

$$I_{CC2} = 3.39 + 0.03561 \times f + 0.006588 \times f \times C_L \quad (2)$$

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 0.584 + 0.05349 \times f \quad (3)$$

$$I_{CC2} = 4.184 + 0.05597 \times f + 0.009771 \times f \times C_L \quad (4)$$

ISO7641FM:

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 1.848 + 0.03233 \times f + 0.001645 \times f \times C_L \quad (5)$$

$$I_{CC2} = 3.005 + 0.03459 \times f + 0.0049395 \times f \times C_L \quad (6)$$

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 2.369 + 0.05385 \times f + 0.002448 \times f \times C_L \quad (7)$$

$$I_{CC2} = 3.857 + 0.05506 \times f + 0.007348 \times f \times C_L \quad (8)$$

I_{CC1} and I_{CC2} are typical supply currents measured in mA; f is data rate measured in Mbps; C_L is the capacitive load on each channel measured in pF.

9.2.3 Application Curves

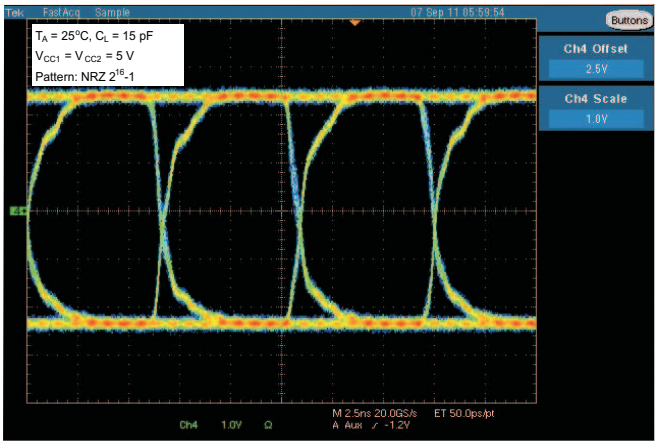


图 19. Typical Eye Diagram at 150 Mbps, 5-V Operation

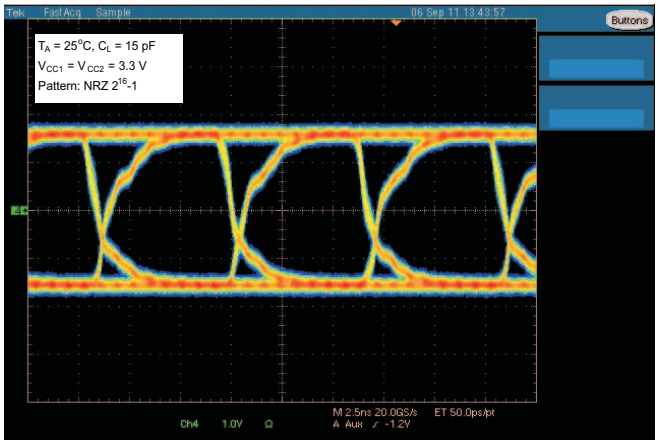


图 20. Typical Eye Diagram at 150 Mbps, 3.3-V Operation

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 图 21). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

注

For detailed layout recommendations, see *Digital Isolator Design Guide*, SLLA284.

11.2 Layout Example

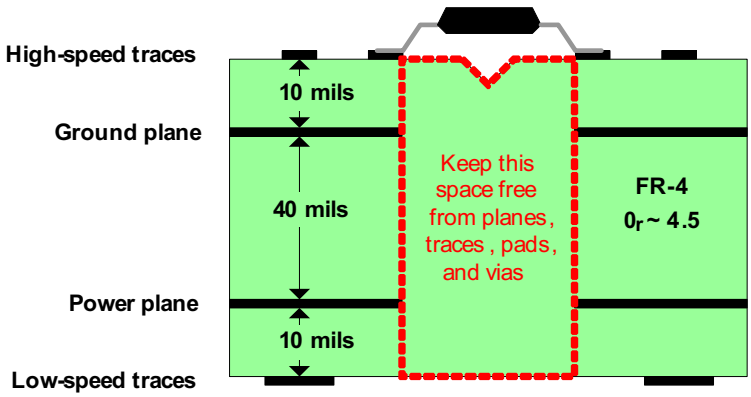


图 21. Recommended Layer Stack

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *《数字隔离器设计指南》*，SLLA284
- *《用于隔离电源的变压器驱动器》*（文献编号：SLLSEA0）

12.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **5.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ISO7640FM	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7641FM	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 商标

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12.4 静电放电警告

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12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

SLLA353 -- *《隔离相关术语》*。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7640FMDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM
ISO7640FMDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM
ISO7640FMDW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	-	Call TI	Call TI	-40 to 125	
ISO7640FMDWG4	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM
ISO7640FMDWG4.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM
ISO7640FMDWG4.B	Active	Production	SOIC (DW) | 16	40 | TUBE	-	Call TI	Call TI	-40 to 125	
ISO7640FMDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM
ISO7640FMDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM
ISO7640FMDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO7641FMDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM
ISO7641FMDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM
ISO7641FMDW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	-	Call TI	Call TI	-40 to 125	
ISO7641FMDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM
ISO7641FMDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM
ISO7641FMDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO7641FMDWRG4	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM
ISO7641FMDWRG4.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM
ISO7641FMDWRG4.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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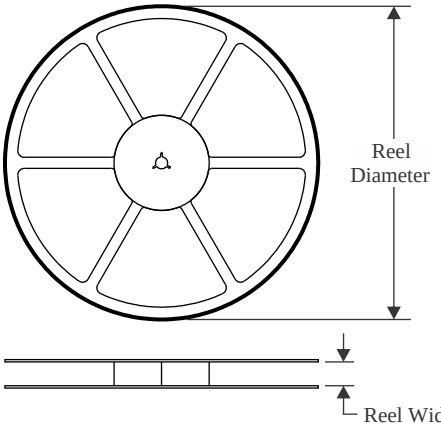
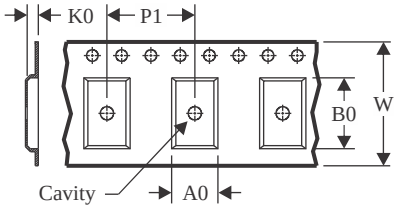
TAPE AND REEL INFORMATION

REEL DIMENSIONS

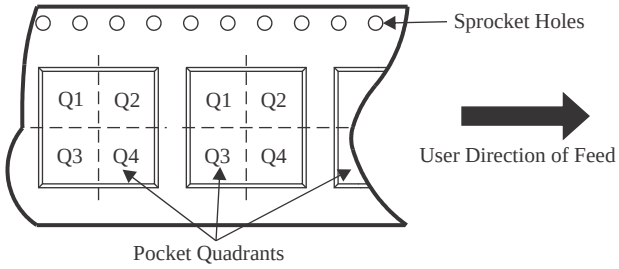


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

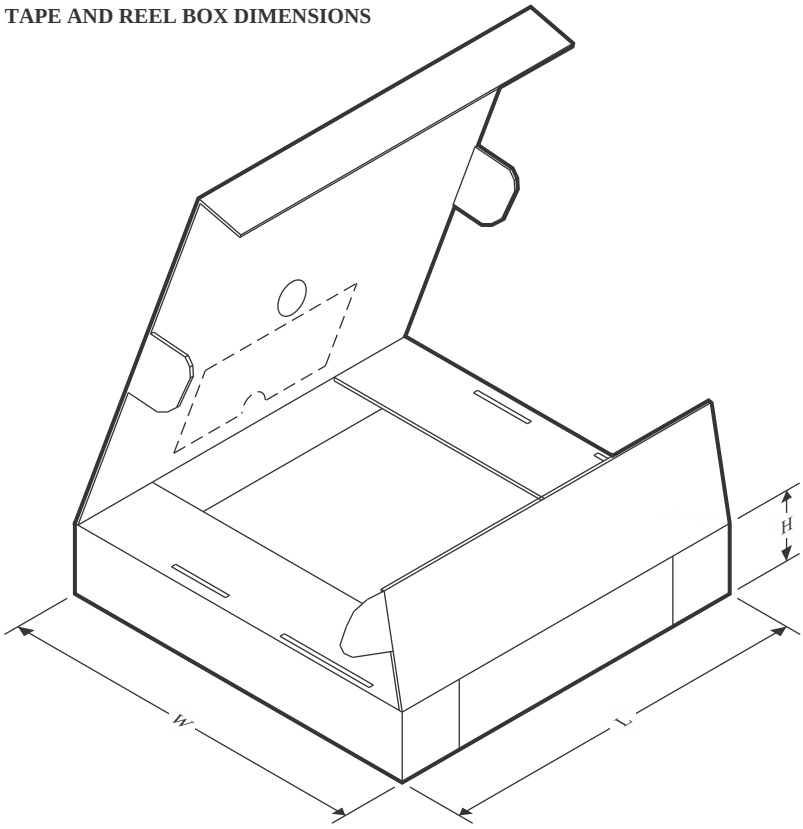
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7640FMDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7641FMDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7641FMDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

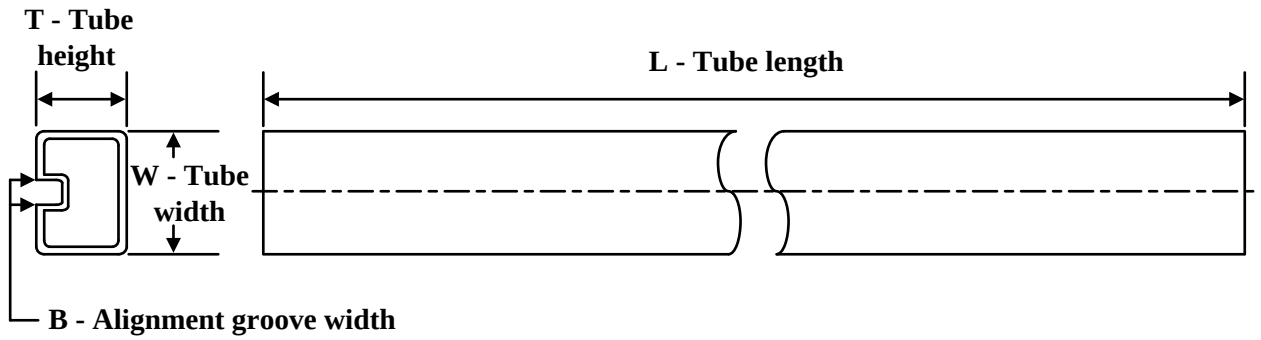
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7640FMDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7641FMDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7641FMDWRG4	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7640FMDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7640FMDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7640FMDWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7640FMDWG4.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7641FMDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7641FMDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

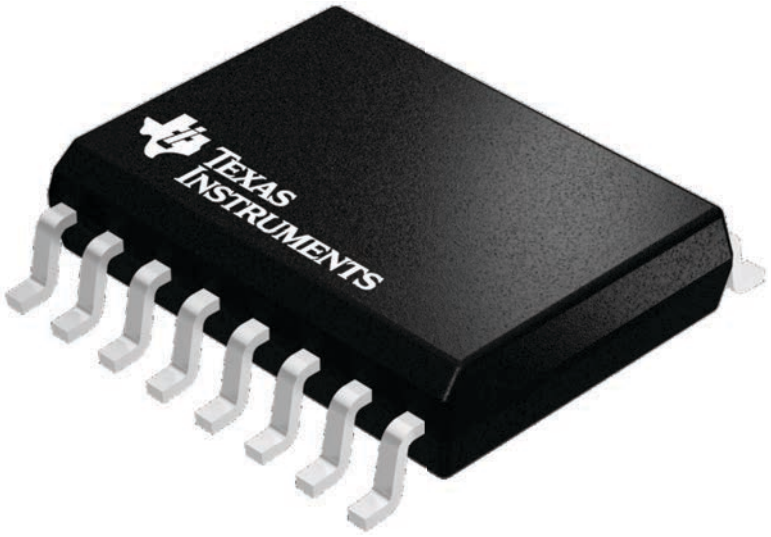
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

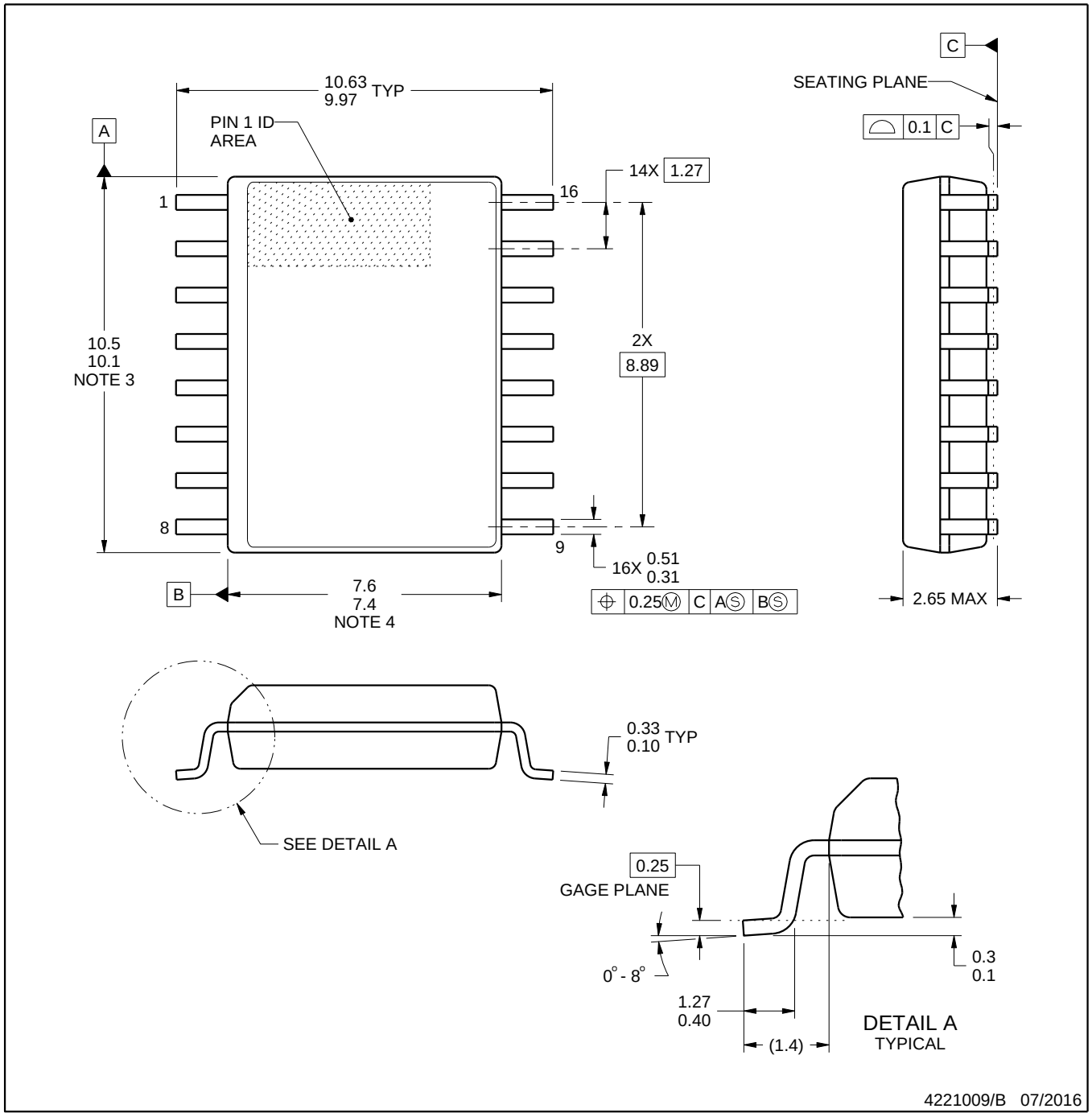
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



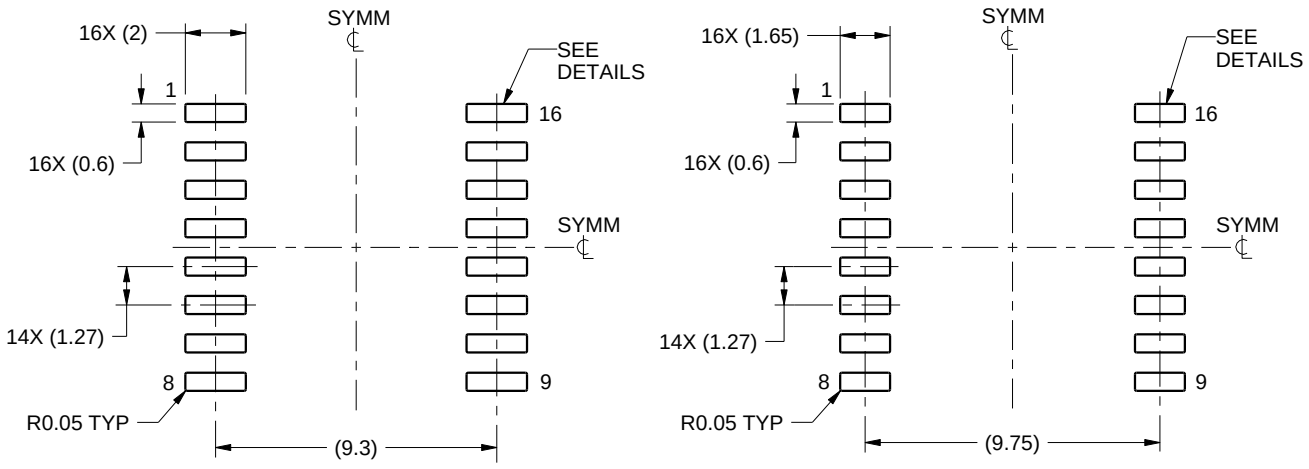
4224780/A

SOIC



NOTES:

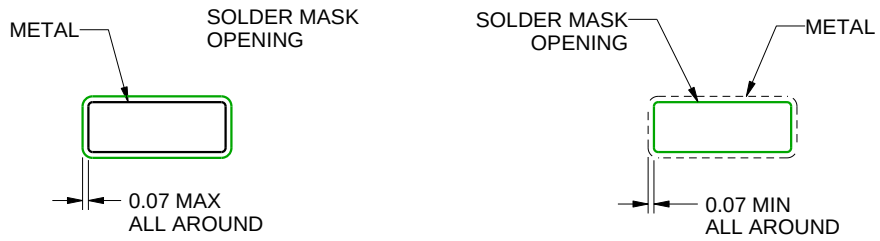
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

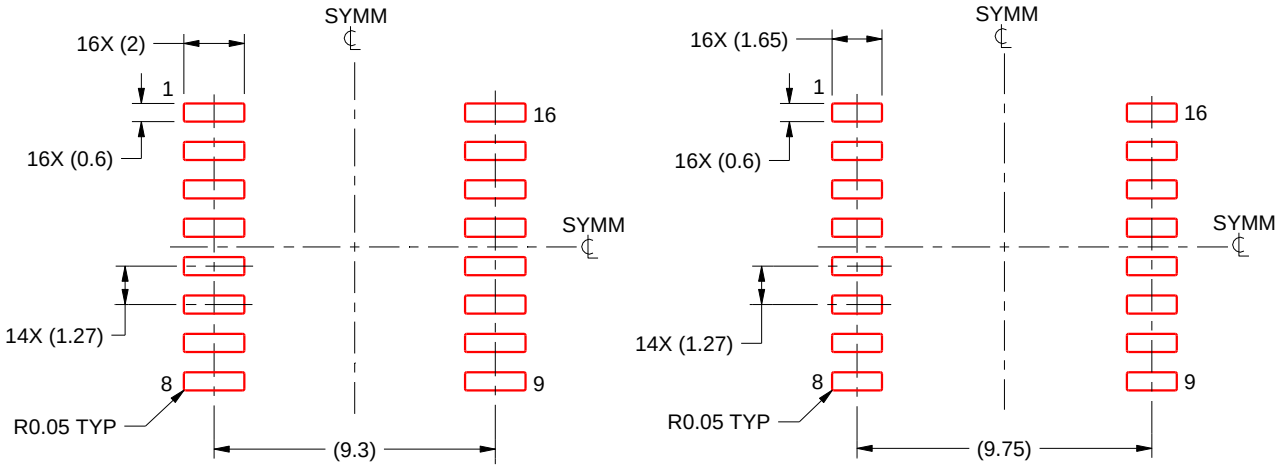
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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