

ISO722x-Q1 双通道数字隔离器

1 特性

- 1Mbps 和 25Mbps 信号传输速率选项
 - 低通道输出偏斜；最大值为 1ns
 - 低脉宽失真度 (PWD)；最大值为 1ns
 - 低抖动内容；速率为 25Mbps 时的典型值为 1ns
- 50kV/ μ s 典型瞬态抗扰度
- 由 2.8V (C 级)、3.3V 或 5V 电源供电
- 4kV ESD 保护
- 工作温度范围 -40°C 至 +125°C
- 额定电压下的使用寿命典型值为 28 年 (请参阅隔离寿命预测)
- 安全相关认证
 - DIN EN IEC 60747-17 (VDE 0884-17)
 - UL 1577 组件认证计划
 - IEC 61010-1、IEC 62368-1 认证

2 应用

- 工厂自动化
 - Modbus
 - Profibus™
 - DeviceNet™ 数据总线
- 计算机外设接口
- 伺服器控制接口
- 数据采集

3 说明

ISO7220x-Q1 和 ISO7221x-Q1 系列器件是双通道数字隔离器。为了方便 PCB 布局，ISO7220x-Q1 中的通道方向相同，ISO7221x-Q1 中的通道方向相反。这些器件具有逻辑输入和输出缓冲器，该缓冲器由 TI 的二氧化硅 (SiO₂) 隔离栅进行隔离，提供符合 VDE 标准、高达 4000V_{PK} 的电隔离。当与隔离电源配合使用时，这些器件可阻止高电压和隔离接地，并可防止数据总线或其他电路上的噪声电流进入本地接地或对敏感电路造成干扰或损坏。

对二进制输入信号进行调理并转换为平衡的信号，然后由隔离层进行差分。跨越该隔离层，差分比较器可接收逻辑转换信息，然后相应地设置或重置触发器和输出电路。电路将跨越隔离层发送定期更新脉冲，以验证直流输出电平是否正常。如果每 4 μ s 没有收到此直流刷新脉冲，则输入被视为未通电或未被主动驱动，失效防护电路会将输出驱动至逻辑高电平状态。

生成的时间常数提供快速运行，其信号传输速率范围为 0Mbps (直流) 到 25Mbps (线路上的信号传输速率是

每秒进行的电压转换次数，以单位 bps 来表示)。A 选项和 C 选项器件具有 TTL 输入阈值，并且在输入上具有噪声滤波器，可防止将瞬态脉冲传递到器件的输出。M 选项器件具有 CMOS $V_{CC}/2$ 输入阈值，没有输入噪声滤波器和额外的传播延迟。

ISO7220x-Q1 和 ISO7221x-Q1 系列器件需要两个电源电压 (2.8V (C 级)、3.3V、5V 或任意组合)。通过 2.8V 或 3.3V 电源供电时，所有输入均可耐受 5V 电压，所有输出均为 4mA CMOS。

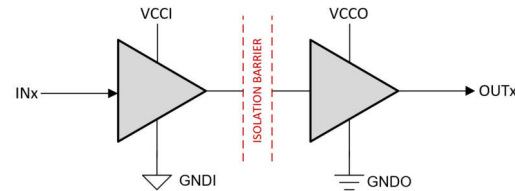
ISO7220x-Q1 和 ISO7221x-Q1 系列器件在 -40°C 至 +125°C 的环境温度范围内运行。

封装信息

器件型号	封装 ⁽¹⁾	本体尺寸 (标称值)	封装尺寸 ⁽²⁾
ISO7220x-Q1	D (SOIC, 8)	4.90mm × 3.91mm	4.9mm × 6mm
ISO7221x-Q1			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



V_{CCI} 和 $GNDI$ 分别是输入通道的电源和接地连接引脚。

V_{CCO} 和 $GNDO$ 分别是输出通道的电源和接地连接引脚。

简化版原理图



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4 Pin Configuration and Functions

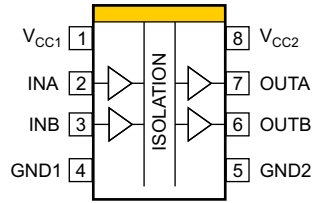


图 4-1. ISO7220x-Q1 D Package 8-Pin SOIC Top View

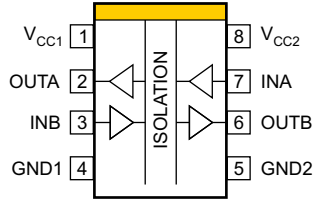


图 4-2. ISO7221x-Q1 D Package 8-Pin SOIC Top View

表 4-1. Pin Functions

NAME	PIN		Type ⁽¹⁾	DESCRIPTION
	ISO7220x-Q1	ISO7221x-Q1		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	8	8	—	Power supply, V_{CC2}

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

Parameter		Value
V _{CC}	Supply voltage ⁽¹⁾ , V _{CC1} , V _{CC2}	- 0.5 V to 6 V
V _I	Voltage at IN, OUT	- 0.5 V to V _{CC} + 0.5 V ⁽²⁾
I _O	Output current	±15 mA
T _J	Maximum junction temperature	150°C
T _{stg}	Storage temperature	- 65°C to 150°C

- (1) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
 (2) Maximum voltage must not exceed 6 V.

5.2 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage ⁽¹⁾	V _{CC1} , V _{CC2}	3		5.5	V
I _{OH}	High-level output current				4	mA
I _{OL}	Low-level output current		- 4			mA
t _{ui}	Input pulse width	ISO722xA-Q1	1			μs
		ISO722xC-Q1	40			ns
1/t _{ui}	Signaling rate	ISO722xA-Q1	0		1000	kbps
		ISO722xC-Q1	0		25	Mbps
V _{IH}	High-level input voltage		2		V _{CC}	V
V _{IL}	Low-level input voltage		0		0.8	V
T _A	Ambient temperature		- 40		125	°C
T _J	Operating virtual-junction temperature		- 40		150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
 For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.3 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Basic certificate: 40047657	Master contract number: 220991	File number: E181974

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾			ISO7220x-Q1 ISO7221x-Q1	UNIT
			D (SOIC)	
			8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	Low-K Thermal Resistance ⁽¹⁾	212	°C/W
		High-K Thermal Resistance	122	
R _{θJC(top)}	Junction-to-case (top) thermal resistance		69.1	°C/W
R _{θJB}	Junction-to-board thermal resistance		47.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter		15.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter		47.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance		—	°C/W

- (1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

5.5 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety input, output, or supply current	R _{θJA} = 212°C/W, V _I = 5.5 V, T _J = 170°C, T _A = 25°C, see Thermal Information			124	mA
		R _{θJA} = 212°C/W, V _I = 3.6 V, T _J = 170°C, T _A = 25°C, see Thermal Information			190	
T _S	Safety temperature				150	°C

- (1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air [thermal impedance](#) of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤ 150 V _{RMS}	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-III	
		Rated mains voltage ≤ 400 V _{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17):⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V _{PK}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} t = 60 s (qualification), t = 1 s (100% production)	4000	V _{PK}
q _{pd}	Apparent charge ⁽³⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.3 × V _{IORM} , t _m = 10 s	≤ 5	
		Method b: At routine test (100% production); V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.5 × V _{IORM} , t _m = 1 s (method b1) or V _{pd(m)} = V _{ini} , t _m = t _{ini} (method b2)	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁴⁾	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	1	pF
R _{IO}	Isolation resistance, input to output ⁽⁴⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 2500 V _{RMS} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{ISO} = 3000 V _{RMS} , t = 1 s (100% production)	2500	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

- (3) Apparent charge is electrical discharge caused by a partial discharge (pd).
 (4) All pins on each side of the barrier tied together creating a two-terminal device

5.7 Electrical Characteristics

$V_{CC1} = 3.3\text{ V}$, $V_{CC2} = 5\text{ V}$ ⁽¹⁾, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT		
I_{CC1}	Supply current, V_{CC1}	ISO7220x-Q1	$V_I = V_{CC}$ or 0 V, no load				mA		
		Quiescent						0.6	1
		ISO7221x-Q1						4.3	9.5
		1 Mbps						1	2
		25 Mbps						5	11
I_{CC2}	Supply current, V_{CC2}	ISO7220x-Q1	$V_I = V_{CC}$ or 0 V, no load				mA		
		Quiescent						16	31
		ISO7221x-Q1						8.5	17
		1 Mbps						18	32
		25 Mbps						10	18
V_{OH}	High-level output voltage	ISO7220x-Q1	$I_{OH} = -4\text{ mA}$				V		
		ISO7221x-Q1 (3.3-V side)						$V_{CC} - 0.8$	
		$I_{OH} = -20\ \mu\text{A}$						$V_{CC} - 0.4$	
V_{OL}	Low-level output voltage		$I_{OL} = 4\text{ mA}$				V		
								$I_{OL} = 20\ \mu\text{A}$	0.4
$V_{I(HYS)}$	Input threshold voltage hysteresis				150		mV		
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	μA		
I_{IL}	Low-level input current		IN from 0 V or V_{CC}		-10		μA		
C_I	Input capacitance to ground		IN at V_{CC} , $V_I = 0.4\text{ sin}(2\pi\text{ ft})$, $f=2\text{MHz}$		1		pF		
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See 图 6-3		15	40	kV/ μs		

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
 For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.8 Electrical Characteristics

$V_{CC1} = V_{CC2} = 3.3\text{ V}^{(1)}$, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
I_{CC1}	Supply current, V_{CC1}	ISO7220x-Q1	Quiescent	$V_I = V_{CC}$ or 0 V, no load	0.6	1	mA	
		ISO7221x-Q1			4.3	9.5		
		ISO7220A-Q1	1 Mbps		1	2		
		ISO7221A-Q1			5	11		
		ISO7221C-Q1	25 Mbps		6	12		
I_{CC2}	Supply current, V_{CC2}	ISO7220x-Q1	Quiescent	$V_I = V_{CC}$ or 0 V, no load	8	18	mA	
		ISO7221x-Q1			4.3	9.5		
		ISO7220A-Q1	1 Mbps		9	19		
		ISO7221A-Q1			5	11		
		ISO7221C-Q1	25 Mbps		6	12		
V_{OH}	High-level output voltage			$I_{OH} = -4\text{ mA}$	$V_{CC} - 0.4$	3	V	
				$I_{OH} = -20\text{ }\mu\text{A}$	$V_{CC} - 0.1$	3.3		
V_{OL}	Low-level output voltage			$I_{OL} = 4\text{ mA}$		0.2	0.4	V
				$I_{OL} = 20\text{ }\mu\text{A}$		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150	mV	
I_{IH}	High-level input current			IN from 0 V or V_{CC}			10	μA
I_{IL}	Low-level input current			IN from 0 V or V_{CC}		-10		μA
C_I	Input capacitance to ground			IN at V_{CC} , $V_I = 0.4\text{ sin}(2\pi ft)$, $f=2\text{MHz}$		1	pF	
CMTI	Common-mode transient immunity			$V_I = V_{CC}$ or 0 V, See 图 6-3		15	40	kV/ μs

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.9 Electrical Characteristics

$V_{CC1} = 5\text{ V}$, $V_{CC2} = 3.3\text{ V}$ ⁽¹⁾, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x-Q1	Quiescent	$V_I = V_{CC}$ or 0 V, no load	1	2	mA
		ISO7221x-Q1			8.5	17	
		ISO7220A-Q1	1 Mbps	$V_I = V_{CC}$ or 0 V, no load	2	3	
		ISO7221A-Q1			10	18	
		ISO7221C-Q1	25 Mbps	$V_I = V_{CC}$ or 0 V, no load	12	22	
I_{CC2}	Supply current, V_{CC2}	ISO7220x-Q1	Quiescent	$V_I = V_{CC}$ or 0 V, no load	8	18	mA
		ISO7221x-Q1			4.3	9.5	
		ISO7220A-Q1	1 Mbps	$V_I = V_{CC}$ or 0 V, no load	9	19	
		ISO7221A-Q1			5	11	
		ISO7221C-Q1	25 Mbps	$V_I = V_{CC}$ or 0 V, no load	6	12	
V_{OH}	High-level output voltage	ISO7220x-Q1	$I_{OH} = -4\text{ mA}$	$V_{CC} - 0.4$			V
		ISO7221x-Q1 (5-V side)		$V_{CC} - 0.8$			
				$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4\text{ mA}$			0.4	V
			$I_{OL} = 20\text{ }\mu\text{A}$			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	μA
I_{IL}	Low-level input current		IN from 0 V to V_{CC}		-10		μA
C_I	Input capacitance to ground		IN at V_{CC} , $V_I = 0.4\text{ sin}(2\pi ft)$, $f=2\text{MHz}$		1		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See 图 6-3	15	40		kV/ μs

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.10 Electrical Characteristics

V_{CC1} and V_{CC2} at 5 V⁽¹⁾, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT			
I_{CC1}	Supply current, V_{CC1}	ISO7220x-Q1	$V_I = V_{CC}$ or 0 V, no load		1	2	mA			
		ISO7221x-Q1						Quiescent	8.5	17
		ISO7220A-Q1						1 Mbps	2	3
		ISO7221A-Q1							10	18
		ISO7221C-Q1						25 Mbps	12	22
I_{CC2}	Supply current, V_{CC2}	ISO7220x-Q1	$V_I = V_{CC}$ or 0 V, no load		16	31	mA			
		ISO7221x-Q1						Quiescent	8.5	17
		ISO7220A-Q1						1 Mbps	17	32
		ISO7221A-Q1							10	18
		ISO7221C-Q1						25 Mbps	12	22
V_{OH}	High-level output voltage			$I_{OH} = -4$ mA	$V_{CC} - 0.8$	4.6	V			
				$I_{OH} = -20$ μ A	$V_{CC} - 0.1$	5				
V_{OL}	Low-level output voltage			$I_{OL} = 4$ mA		0.2	V			
				$I_{OL} = 20$ μ A		0		0.1		
$V_{I(HYS)}$	Input voltage hysteresis					150	mV			
I_{IH}	High-level input current			IN from 0 V to V_{CC}			10 μ A			
I_{IL}	Low-level input current			IN from 0 V to V_{CC}		-10	μ A			
C_I	Input capacitance to ground			IN at V_{CC} , $V_I = 0.4 \sin(2\pi ft)$, $f=2$ MHz		1	pF			
CMTI	Common-mode transient immunity			$V_I = V_{CC}$ or 0 V, See 图 6-3		25	50 $kV/\mu s$			

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.11 Switching Characteristics

$V_{CC1} = 3.3$ V \pm 10%, $V_{CC2} = 5$ V \pm 10%, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH} , t_{pHL}	Propagation delay	ISO722xA-Q1	See 图 6-1	268	395	605	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} $ ⁽¹⁾						
t_{pLH} , t_{pHL}	Propagation delay	ISO722xC-Q1	See 图 6-1	21	36	48	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} $ ⁽¹⁾						
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	ISO722xA-Q1				190	ns
		ISO722xC-Q1				10	
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7220A-Q1			3	15	ns
t_r	Output signal rise time	See 图 6-1			2.3		ns
t_f	Output signal fall time	See 图 6-1			2.3		ns
t_{fs}	Failsafe output delay time from input power loss	See 图 6-2			3		μs

- (1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

- (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.12 Switching Characteristics

$V_{CC1} = 5\text{ V} \pm 10\%$, $V_{CC2} = 3.3\text{ V} \pm 10\%$, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH} , t_{pHL}	Propagation delay	ISO722xA-Q1	See 图 6-1	253	410	585	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} ^{(1)}$						
t_{pLH} , t_{pHL}	Propagation delay	ISO722xC-Q1	See 图 6-1	21	36	48	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} ^{(1)}$						
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	ISO722xA-Q1				180	ns
		ISO722xC-Q1					
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7220A-Q1			3	15	ns
t_r	Output signal rise time		See 图 6-1		2.3		ns
t_f	Output signal fall time		See 图 6-1		2.3		
t_{fs}	Failsafe output delay time from input power loss		See 图 6-2		3		$\mu\text{ s}$

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.13 Switching Characteristics

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH} , t_{pHL}	Propagation delay	ISO722xA-Q1	See 图 6-1	267	400	610	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} ^{(1)}$						
t_{pLH} , t_{pHL}	Propagation delay	ISO722xC-Q1	See 图 6-1	23	40	52	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} ^{(1)}$						
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	ISO722xA-Q1				190	ns
		ISO722xC-Q1					
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7220A-Q1			3	15	ns
t_r	Output signal rise time		See 图 6-1		2.3		ns
t_f	Output signal fall time		See 图 6-1		2.3		ns
t_{fs}	Failsafe output delay time from input power loss		See 图 6-2		3		$\mu\text{ s}$

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

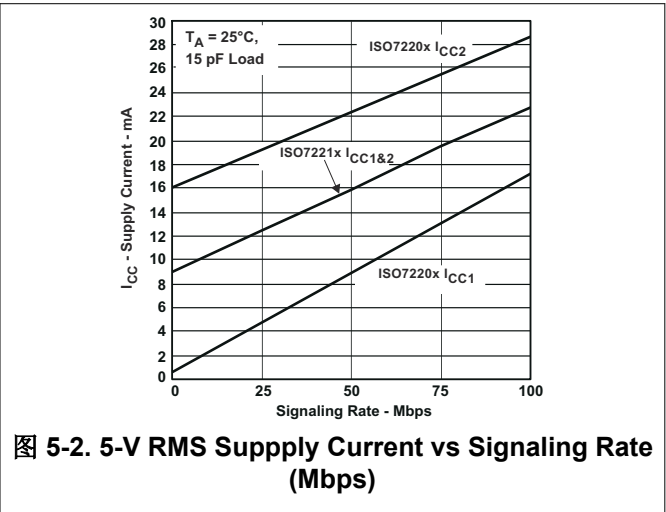
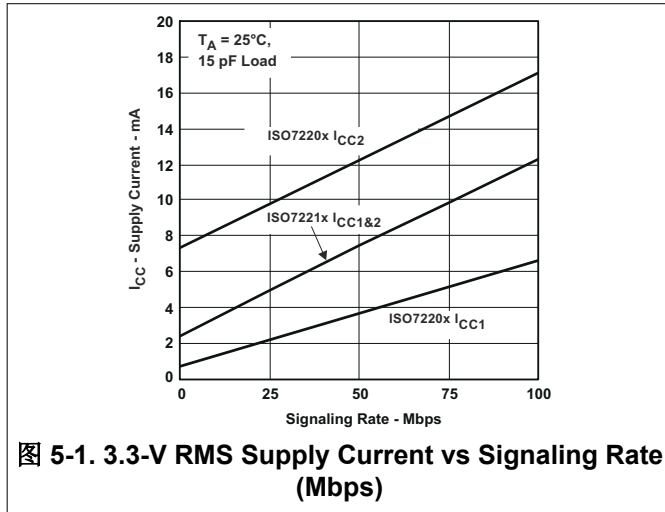
5.14 Switching Characteristics

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA-Q1	See 图 6-1	252	405	600	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} ^{(1)}$						
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC-Q1	See 图 6-1	21	32	42	ns
PWD	Pulse-width distortion $ t_{pHL} - t_{pLH} ^{(1)}$						
$t_{sk(pp)}$	Part-to-part skew ⁽²⁾	ISO722xA-Q1				180	ns
		ISO722xC-Q1				10	
$t_{sk(o)}$	Channel-to-channel output skew ⁽³⁾	ISO7220A-Q1			3	15	ns
t_r	Output signal rise time		See 图 6-1		2.3		ns
t_f	Output signal fall time		See 图 6-1		2.3		ns
t_{fs}	Failsafe output delay time from input power loss		See 图 6-2		3		$\mu\text{ s}$

- (1) Also referred to as pulse skew.
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.15 Typical Characteristics



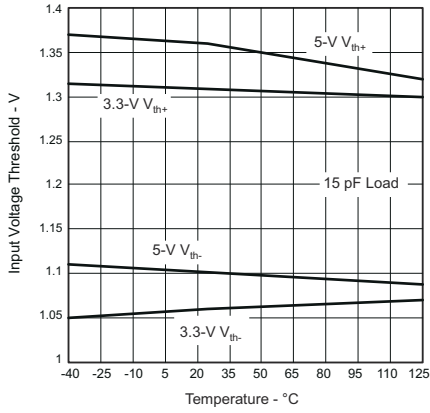


图 5-3. ISO722xA-Q1 and ISO722xC -Q1 Input Voltage Low-to-High Switching Threshold vs Free-Air Temperature

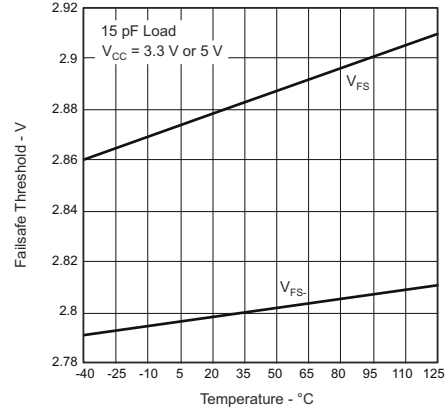


图 5-4. V_{CC} Failsafe Threshold vs Free-Air Temperature

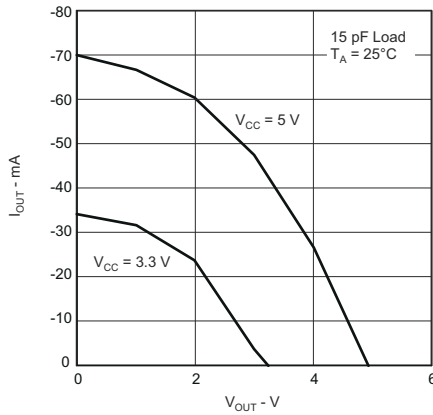


图 5-5. High-Level Output Current vs High-Level Output Voltage

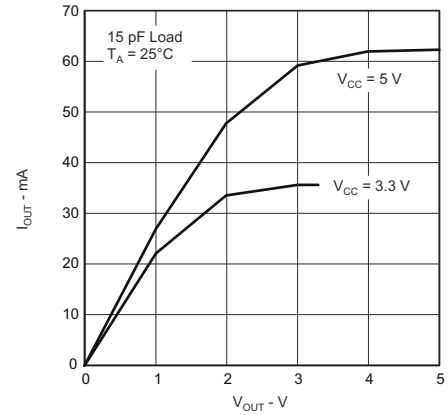
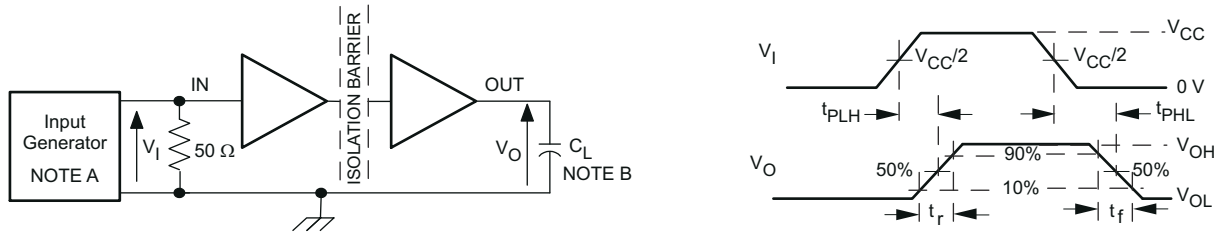


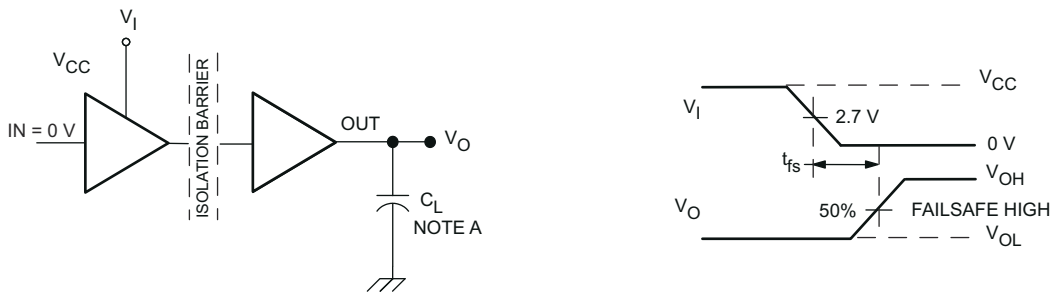
图 5-6. Low-Level Output Current vs Low-Level Output Voltage

6 Parameter Measurement Information



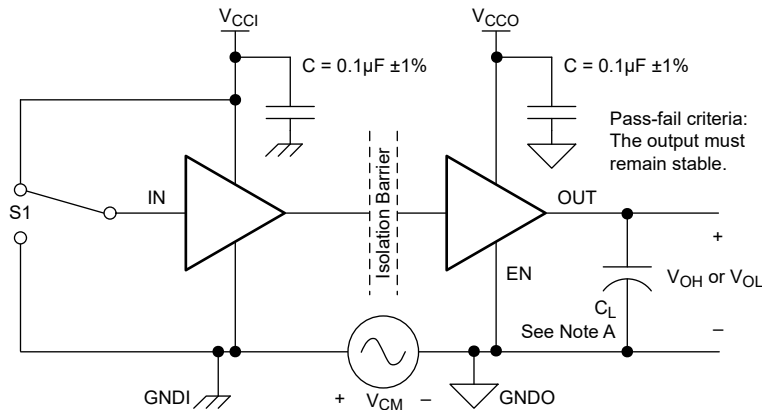
- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_0 = 50 \Omega$.
- B. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

图 6-1. Switching Characteristic Test Circuit and Voltage Waveforms



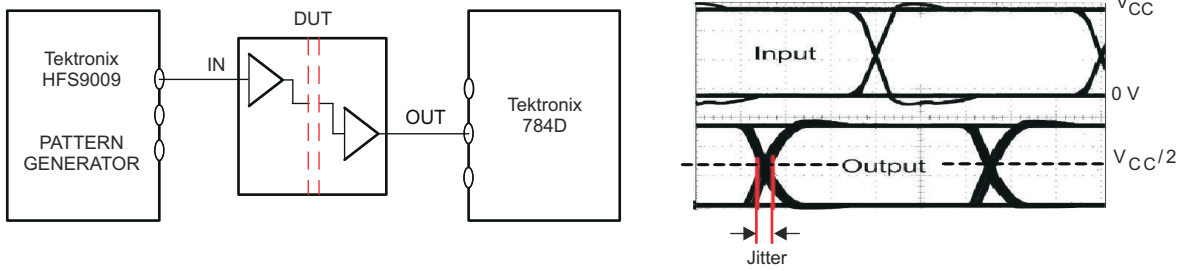
- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

图 6-2. Failsafe Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

图 6-3. Common-Mode Transient Immunity Test Circuit



PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps.

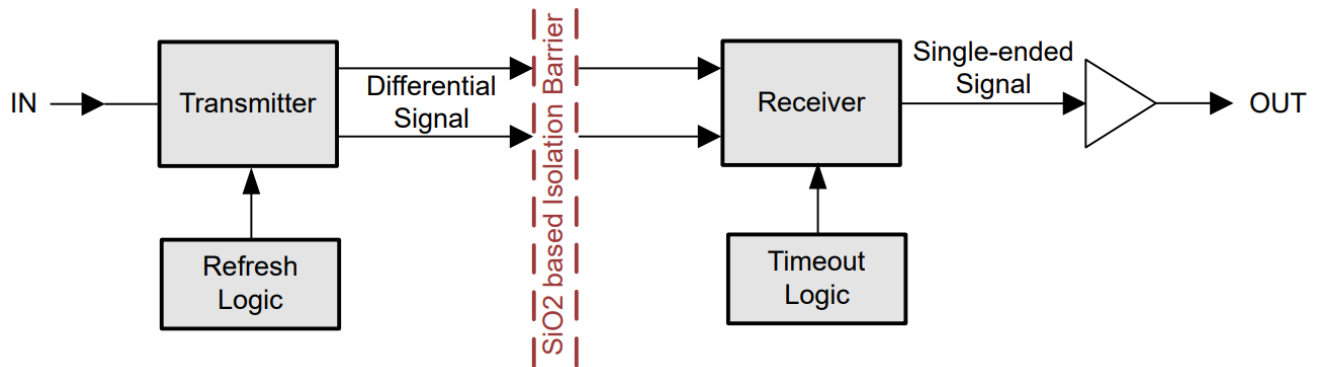
图 6-4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

7 Detailed Description

7.1 Overview

The ISO722xx-Q1 family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

7.2 Functional Block Diagram



7.3 Feature Description

表 7-1 provides an overview of the device features.

表 7-1. Device Features

PART NUMBER	MAXIMUM SIGNALING RATE	INPUT THRESHOLD	CHANNEL DIRECTION
ISO7220A-Q1	1 Mbps	$\cong 1.5\text{ V}$ (TTL) (CMOS compatible)	2/0
ISO7221A-Q1	1 Mbps	$\cong 1.5\text{ V}$ (TTL) (CMOS compatible)	1/1
ISO7221C-Q1	25 Mbps	$\cong 1.5\text{ V}$ (TTL) (CMOS compatible)	

7.4 Device Functional Modes

The ISO7220x-Q1 and ISO7221x-Q1 family of devices functional modes are listed in 表 7-2.

表 7-2. ISO7220x-Q1 or ISO7221x-Q1 Function Table

INPUT SIDE V_{CC} ⁽¹⁾	OUTPUT SIDE V_{CC}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

(1) PU = Powered Up ($V_{CC} \geq 3.0\text{ V}$), PD = Powered Down ($V_{CC} \leq 2.5\text{ V}$), X = Irrelevant, H = High Level, L = Low Level

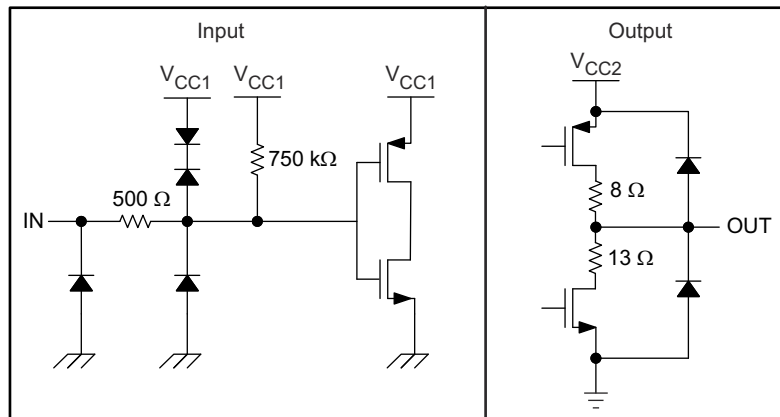


图 7-1. Device I/O Schematics

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO7220x and ISO7221x family devices use single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3 V (2.8 V for C-grade) to 5.5 V for both supplies, V_{CC1} and V_{CC2} . When designing with digital isolators, because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

The ISO7221x-Q1 family of devices can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4- to 20-mA current loop.

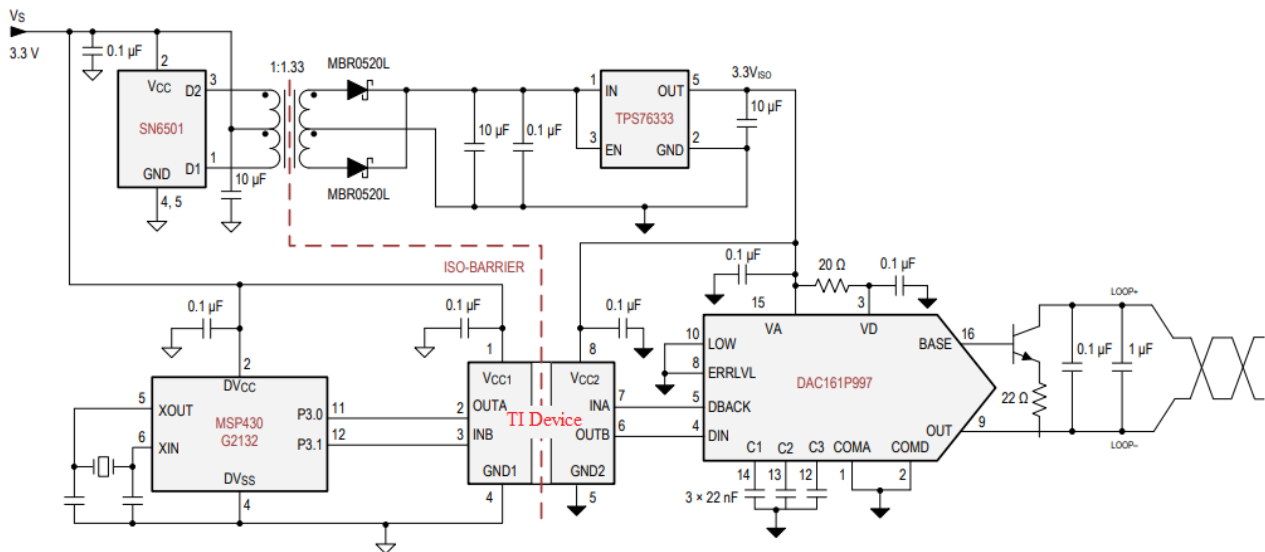


图 8-1. Isolated 4- to 20-mA Current Loop

8.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias (or limit current), the ISO7220x-Q1 and ISO7221x-Q1 devices require only two external bypass capacitors to operate.

8.2.2 Detailed Design Procedure

图 8-2 和 图 8-3 显示了一个典型的 ISO7220x-Q1 和 ISO7221x-Q1 电路的接线。唯一的外部元件是两个旁路电容器。

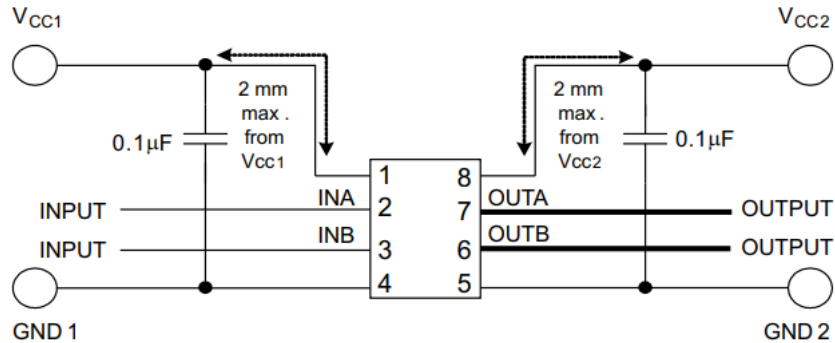


图 8-2. Typical ISO7220x-Q1 Circuit Hook-Up

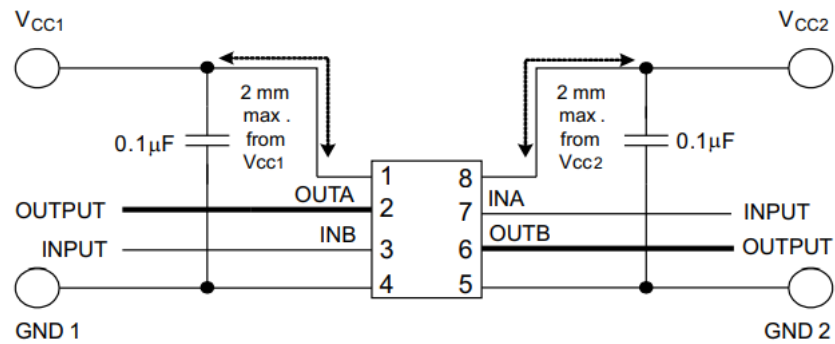


图 8-3. Typical ISO7221x-Q1 Circuit Hook-Up

8.2.3 Insulation Lifetime

At maximum working voltage, the isolation barrier of the ISO72x and ISO72xM family of devices has more than 28 years of life.

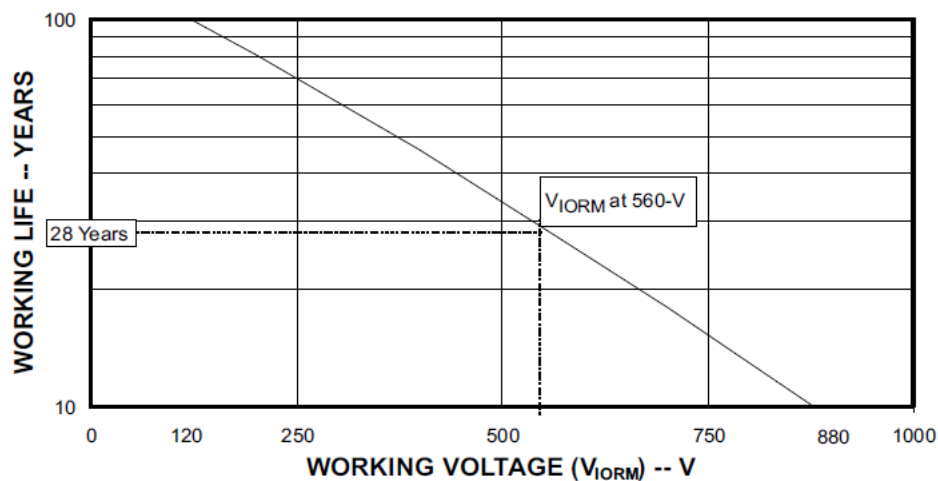


图 8-4. Insulation Lifetime Projection

8.3 Power Supply Recommendations

To help provide reliable operation at all data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies](#).

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers are required to accomplish a low EMI PCB design (see [图 8-5](#)). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Route the high-speed traces on the top layer to avoid the use of vias (and the introduction of the inductances) and allow for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Place a solid ground plane next to the high-speed signal layer to establish controlled impedance for transmission line interconnects and provide an excellent low-inductance path for the return current flow.
- Place the power plane next to the ground plane to create additional high-frequency bypass capacitance of approximately 100 pF/in².
- Route the slower speed control signals on the bottom layer to allow for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. Adding a second plane system to the stack makes the stack mechanically stable and prevents warping. The power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

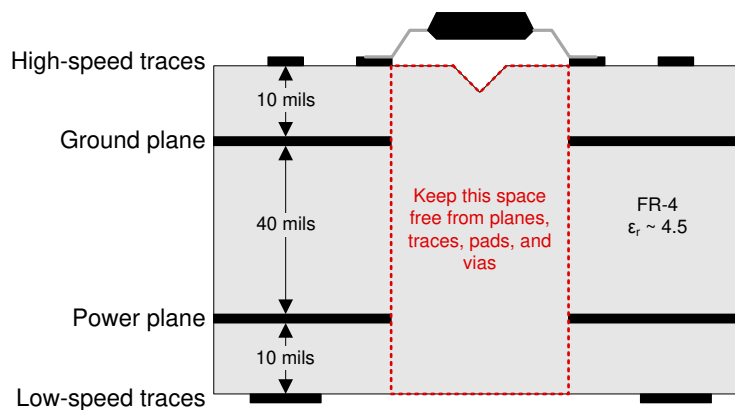


图 8-5. Recommended Layer Stack

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

For development support, refer to:

- [AC-mains LED Lighting with DALI DMX512 & Power Line Communications Reference Design](#)
- [Industrial Servo Drive and AC Inverter Drive Reference Design](#)
- [Low-Cost Single/Dual-Phase Isolated Electricity Measurement Reference Design](#)
- [Noise Tolerant Capacitive Touch HMI Reference Design](#)
- [Type 2 PoE PSE, 6kV Lightning Surge Reference Design](#)

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)

9.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.5 Trademarks

Profibus™ is a trademark of Profibus.

DeviceNet™ is a trademark of Open DeviceNet Vendors Association.

TI E2E™ is a trademark of Texas Instruments.

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9.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (November 2024) to Revision F (February 2025)

Page

- 更新了整个文档中的表格、图和交叉参考的编号格式..... 1

Changes from Revision D (April 2020) to Revision E (November 2024)	Page
• 更新了整个文档中的内容，以便更好地与器件的商用版本保持一致.....	1
• 通篇将引用内容从电容隔离更新为隔离栅.....	1
• 通篇将“VDE V 0884-11”更新为“DIN VDE 0884-17”.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....	4
• Updated electrical and switching characteristics to match device performance.....	6
• Added the <i>Detailed Description</i> , <i>Overview</i> , <i>Feature Description</i> , <i>Functional Block Diagram</i> , and <i>Device Functional Modes</i> sections.....	16
• Added the <i>Typical Application</i> , <i>Power Supply Recommendations</i> , and <i>Layout</i> sections.....	18

Changes from Revision C (May 2012) to Revision D (April 2020)	Page
• 将标准名称从“IEC 60747-5-2 (VDE 0884 , 修订版 2)、IEC 61010-1”更改为“DIN VDE V 0884-11:2017-01、DIN EN 61010-1”并添加了“IEC 62368-1” (在“特性”中).....	1
• 通篇进行了编辑性和修饰性更改.....	1
• Deleted typical values (TYP) for 'Input pulse width' and 'Signaling rate' specifications in Recommended Operating Conditions table.....	4
• Added 'Ambient temperature' specification in Recommended Operating Conditions table.....	4
• Changed 'Propagation delay' maximum (MAX) limit for ISO722xA From: 480 ns To: 605 ns in Switching Characteristics at $V_{CC1} = 3.3\text{ V} \pm 10\%$, $V_{CC2} = 5\text{ V} \pm 10\%$	9
• Changed 'Pulse-width distortion' maximum (MAX) limit for ISO722xA From: 18 ns To: 22 ns in Switching Characteristics at $V_{CC1} = 3.3\text{ V} \pm 10\%$, $V_{CC2} = 5\text{ V} \pm 10\%$	9
• Changed 'ISO722xA' to 'ISO7220A' and deleted 'ISO722xC' row from 'Channel-to-channel output skew' specification in Switching Characteristics at $V_{CC1} = 3.3\text{ V} \pm 10\%$, $V_{CC2} = 5\text{ V} \pm 10\%$	9
• Changed 'Propagation delay' maximum (MAX) limit for ISO722xA From: 480 ns To: 585 ns in Switching Characteristics at $V_{CC1} = 5\text{ V} \pm 10\%$, $V_{CC2} = 3.3\text{ V} \pm 10\%$	11
• Changed 'ISO722xA' to 'ISO7220A' and deleted 'ISO722xC' row from 'Channel-to-channel output skew' specification in Switching Characteristics at $V_{CC1} = 5\text{ V} \pm 10\%$, $V_{CC2} = 3.3\text{ V} \pm 10\%$	11
• Changed 'Pulse-width distortion' maximum (MAX) limit for ISO722xA From: 14 ns To: 18 ns in Switching Characteristics at $V_{CC1} = 5\text{ V} \pm 10\%$, $V_{CC2} = 3.3\text{ V} \pm 10\%$	11
• Changed 'Propagation delay' maximum (MAX) limit for ISO722xA From: 485 ns To: 610 ns in Switching Characteristics at $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$	11
• Changed 'ISO722xA' to 'ISO7220A' and deleted 'ISO722xC' row from 'Channel-to-channel output skew' specification in Switching Characteristics at $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$	11
• Changed 'Pulse-width distortion' maximum (MAX) limit for ISO722xA From: 18 ns To: 22 ns in Switching Characteristics at $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$	11
• Changed 'ISO722xA' to 'ISO7220A' and deleted 'ISO722xC' row from 'Channel-to-channel output skew' specification in Switching Characteristics at $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$	12
• Changed 'Pulse-width distortion' maximum (MAX) limit for ISO722xA From: 14 ns To: 18 ns in Switching Characteristics at $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$	12
• Changed 'Propagation delay' maximum (MAX) limit for ISO722xA From: 480 ns To: 600 ns in Switching Characteristics at $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$	12

11 Mechanical, Packaging, and Orderable Information

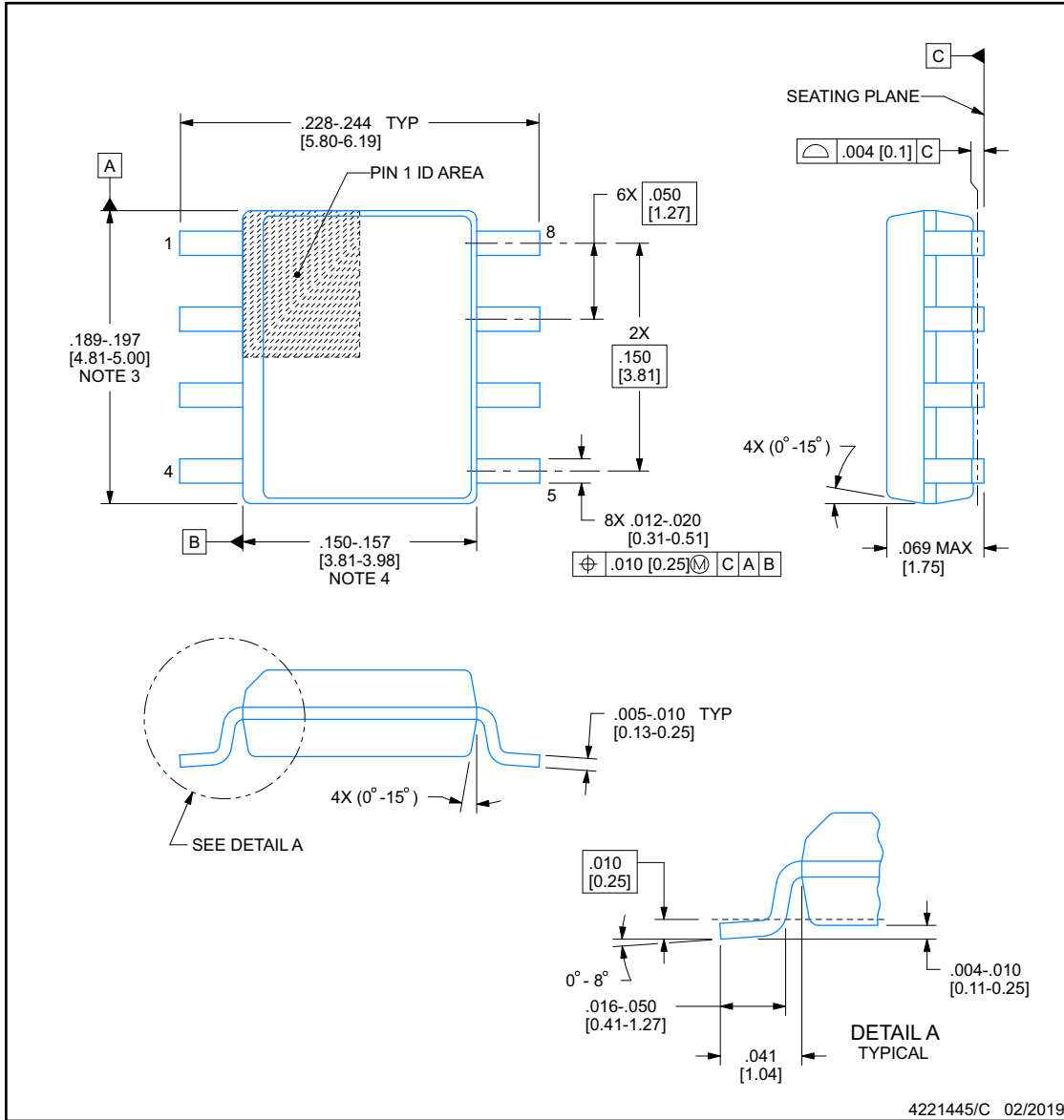
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



D0008B

PACKAGE OUTLINE
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

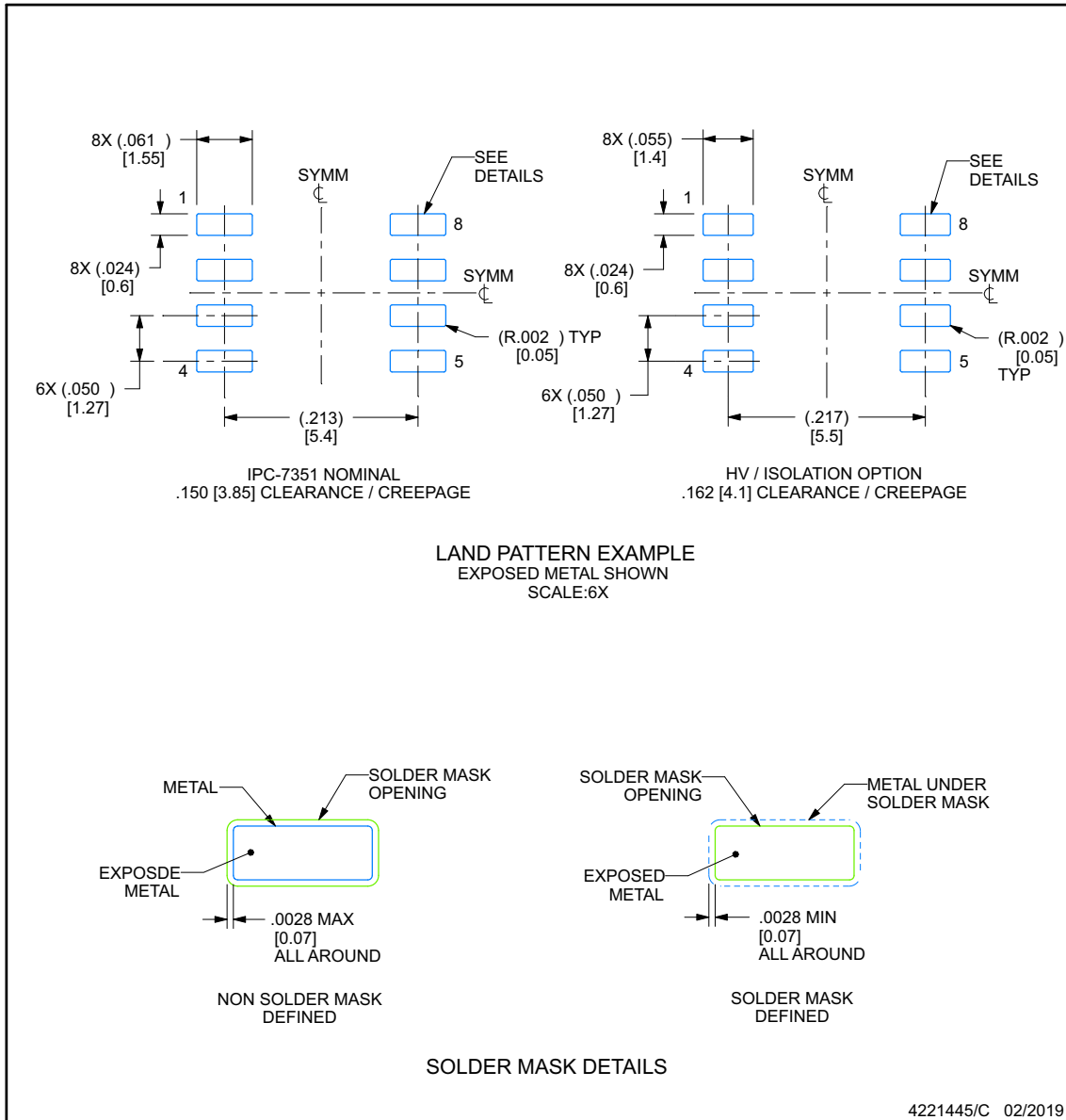
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

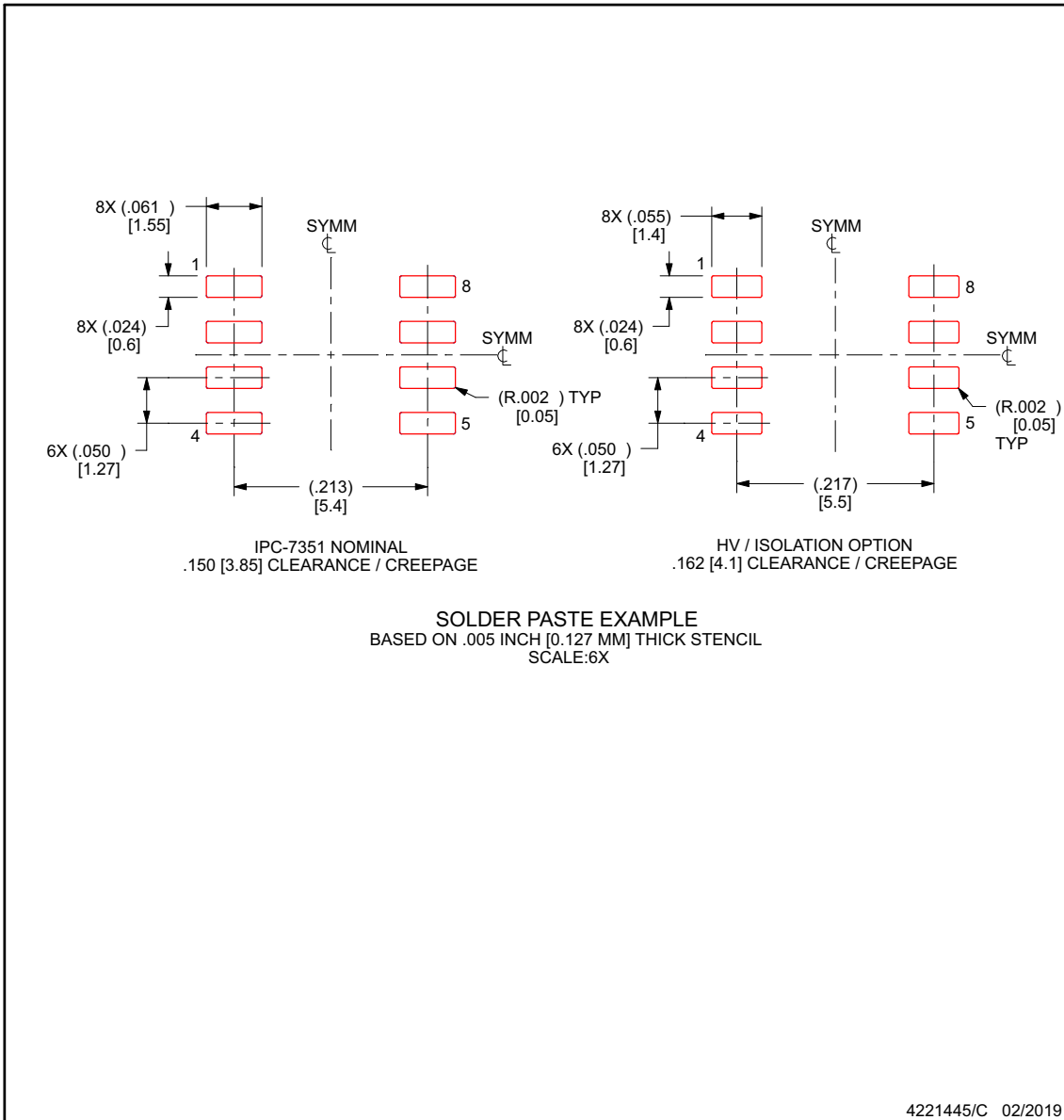
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7220AQDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7220AQ
ISO7220AQDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7220AQ
ISO7220AQDRQ1.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7220AQ
ISO7221AQDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7221AQ
ISO7221AQDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7221AQ
ISO7221AQDRQ1.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7221AQ
ISO7221CQDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7221CQ
ISO7221CQDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7221CQ
ISO7221CQDRQ1.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7221CQ

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO7220A-Q1, ISO7221A-Q1, ISO7221C-Q1 :

- Catalog : [ISO7220A](#), [ISO7221A](#), [ISO7221C](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7220AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7220AQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221AQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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