ISO721-Q1、ISO722-Q1 3.3V 和 5V 高速数字隔离器

1 特性

- 100Mbps 信号传输速率选项
- 传播延迟为 12ns（典型值）。
- 脉冲偏移为 0.5ns（典型值）。
- 低功耗睡眠模式
- 额定工作电压下的使用寿命通常为 28 年（请参阅绝缘特性曲线）
- 失效防护输出
- 大多数光隔离器和磁隔离器的直接替代产品
- 由 3.3V 和 5V 电源供电
- -40°C 至 +125°C 工作温度范围
- 安全相关认证：
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 组件认证计划
  - IEC 61010-1、IEC 62368-1 认证

2 应用

- 工厂自动化
  - Modbus
  - Profibus™
  - DeviceNet™ 数据总线
- 计算机外设接口
- 伺服器控制接口
- 数据采集

3 说明

ISO721-Q1 和 ISO722-Q1 器件是数字隔离器，其逻辑输入和输出缓冲器由二氧化硅 (SiO_2) 绝缘栅进行隔离。该隔离栅可提供符合 VDE 0884-17 标准、高达 $4000V_{PK}$ 的电隔离。与隔离式电源一起使用时，这些器件可防止数据总线或者其他电路上的噪声电流进入本地接地并且干扰或损坏敏感电路。

对二进制输入信号进行调理并转换为平衡的信号，然后由隔离层进行差分。跨越该隔离层，差分比较器可接收逻辑转换信息，然后相应地设置或重置触发器和输出电路。电路将跨越隔离层发送定期更新脉冲，以提供适当的直流输出电平。

如果没有接收到该直流刷新脉冲的时间超过 4 µs，则输入被视为未通电或未被主动驱动，失效防护电路会将输出驱动至逻辑高电平状态。

这些器件需要两个 3.3V 和 5V 电源电压或二者的任意组合。通过 3.3V 电源供电时，所有输入均可耐受 5V 电压，所有输出均为 4mA CMOS。

ISO722-Q1 器件包含一个低电平有效输出使能端，当被驱动至高逻辑电平时，该使能端会将输出置于高阻抗状态并关闭内部偏置电路以节省功耗。

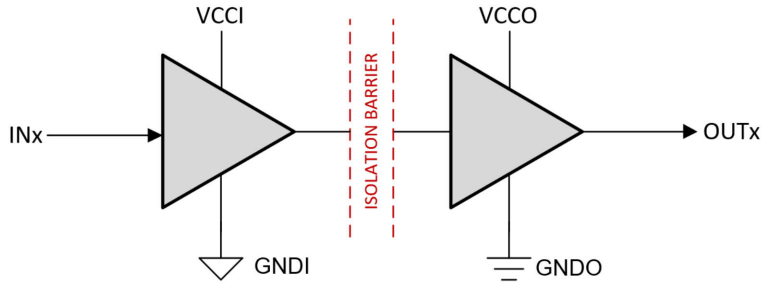
ISO721-Q1 和 ISO722-Q1 器件具有 TTL 输入阈值，并且在输入端具有噪声滤波器，可防止持续时间高达 2ns 的瞬态脉冲传递到器件的输出端。

ISO721-Q1 和 ISO722-Q1 器件在 –40°C 至 +125°C 的环境温度范围内运行。

封装信息

器件型号(1)	封装	本体尺寸（标称值）	封装尺寸(2)
ISO721-Q1	D（SOIC，8）	4.90mm × 3.91mm	4.9mm × 6mm
ISO722-Q1			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化版原理图

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4 Device Comparison Table

PART NUMBER	SIGNALING RATE	OUTPUT ENABLED	INPUT THRESHOLDS	NOISE FILTER
ISO721-Q1	100 Mbps	NO	TTL	YES
ISO722-Q1	100 Mbps	YES	TTL	YES

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5 Pin Configuration and Functions

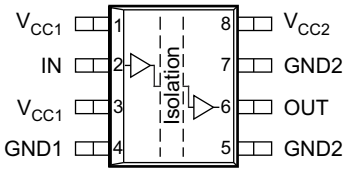

图 5-1. ISO721-Q1
D Package 8-Pin SOIC
Top View

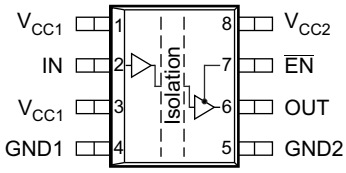

图 5-2. ISO722-Q1
D Package 8-Pin SOIC
Top View

表 5-1. Pin Functions

PIN			Type[1]	DESCRIPTION
NAME	NO.			
	ISO721x-Q1	ISO722x-Q1		
V_{CC1}	1	1	—	Power supply, V_{CC1}
	3	3		
V_{CC2}	8	8	—	Power supply, V_{CC2}
IN	2	2	I	Input
OUT	6	6	O	Output
$\overline{EN}$	—	7	I	Output enable. OUT is enabled when $\overline{EN}$ is low or disconnected and disabled when $\overline{EN}$ is high.
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
	7			

(1) I = Input; O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

See (1)

Parameter		Value
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5 V to 6 V
V_I	Voltage at IN or OUT terminal	–0.5 V to 6 V
I_O	Output current	±15 mA
T_J	Maximum virtual-junction temperature	170°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values. Vrms values are not listed in this publication.

6.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}		3	5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current		–4		mA
t_{ui}	Input pulse duration		10		ns
V_{IH}	High-level input voltage (IN)		2	V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0	0.8	V
T_A	Operating free-air temperature		–40	125	°C
T_J	Operating virtual-junction temperature	See the Thermal Information table		150	°C
H	External magnetic field intensity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

6.3 Thermal Information

THERMAL METRIC(1)			D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Thermal Resistance(2)	212	°C/W
		High-K Thermal Resistance	122	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		69.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		47.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter		15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter		47.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

6.4 Power Ratings

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150C, C_L = 15 pF, Input a 100 Mbps 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation				159	mW

6.5 Insulation Specifications

PARAMETER	TEST CONDITIONS	VALUE	UNIT
GENERAL			

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PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ⩽150 V_{RMS}	I-IV	
		Rated mains voltage ⩽300 V_{RMS}	I-III	
		Rated mains voltage ⩽400 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17):(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification), t = 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3. Vini = VIOTM, tini = 60 s; Vpd(m) = 1.2 × VIOR	⩽5	pC
		Method a: After environmental tests subgroup 1, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.3 × VIORM , tm = 10 s,	⩽5	
		Method b1: At routine test (100% production) Vini = VIOTM, tini = 1 s; Vpd(m) = 1.5 × VIORM , tm = 1 s,	⩽5	
C_{IO}	Barrier capacitance, input to output(4)	VI = 0.4 sin (2 π ft), f = 1 MHz	1	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ⩽ T_A ⩽ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 2500 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

6.6 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Certificate planned	Certificate planned	Certificate planned

6.7 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see Thermal Information			124	mA
		$R_{\theta JA}$ = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see Thermal Information			190	

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Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.8 Electrical Characteristics: V_{CC1} and V_{CC2} 5-V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load			0.5	1	mA
		25 Mbps				2	4	
I_{CC2}	V_{CC2} supply current	ISO722-Q1 Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			200	μA
		Quiescent		$\overline{EN}$ at 0 V or ISO721-Q1		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load			10	14	
V_{OH}	High-level output voltage		I_{OH} = -4 mA		V_{CC} – 0.8	4.6		V
			I_{OH} = – 20 μA		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.2	0.4	V
			I_{OL} = 20 μA			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at 2 V				10	μA
I_{IL}	Low-level input current		IN at 0.8 V		– 10			
I_{OZ}	High-impedance output current	ISO722-Q1	$\overline{EN}$, IN at V_{CC}				1	μA
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See 图 7-5		15	50		kV/μs

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

6.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load			0.3	0.6	mA
		25 Mbps				1	2	
I_{CC2}	V_{CC2} supply current	ISO722-Q1 Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			150	μA
		Quiescent		$\overline{EN}$ at 0 V or ISO721-Q1		4	6.5	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load			5	7.5	
V_{OH}	High-level output voltage		I_{OH} = – 4 mA		V_{CC} – 0.4	3		V
			I_{OH} = – 20 μA		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.2	0.4	V
			I_{OL} = 20 μA			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at 2 V				10	μA
I_{IL}	Low-level input current		IN at 0.8 V		– 10			μA
I_{OZ}	High-impedance output current	ISO722-Q1	$\overline{EN}$, IN at V_{CC}				1	μA

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over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2 π ft), f=2MHz		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See 图 7-5	15	40		kV/ μ s

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

6.10 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load			0.3	0.6	mA
		25 Mbps				1	2	
I_{CC2}	V_{CC2} supply current	ISO722-Q1 Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			200	μ A
		Quiescent		$\overline{EN}$ at 0 V or ISO721-Q1		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load			10	14	
V_{OH}	High-level output voltage		I_{OH} = – 4 mA		V_{CC} – 0.8	4.6		V
			I_{OH} = – 20 μ A		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.2	0.4	V
			I_{OL} = 20 μ A			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at 2 V				10	μ A
I_{IL}	Low-level input current		IN at 0.8 V		– 10			μ A
I_{OZ}	High-impedance output current	ISO722-Q1	$\overline{EN}$, IN at V_{CC}				1	μ A
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2 π ft), f=2MHz			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See 图 7-5		15	40		kV/ μ s

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

6.11 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load			0.5	1	mA
		25 Mbps				2	4	
I_{CC2}	V_{CC2} supply current	ISO722-Q1	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			150	μ A
		Quiescent		$\overline{EN}$ at 0 V or ISO721-Q1		4	6.5	mA
		25 Mbps				5	7.5	
V_{OH}	High-level output voltage		I_{OH} = – 4 mA		V_{CC} – 0.4	3		V
			I_{OH} = – 20 μ A		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.2	0.4	V
			I_{OL} = 20 μ A			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN at 2 V				10	μ A
I_{IL}	Low-level input current		IN at 0.8 V		– 10			μ A
I_{OZ}	High-impedance output current	ISO722-Q1	$\overline{EN}$, IN at V_{CC}				1	μ A
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2 π ft), f=2MHz			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See 图 7-5		15	40		kV/ μ s

(1) For 5-V operation, V_{CC1} or V_{CC2} specification is from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} or V_{CC2} specification is from 3 V to 3.6 V.

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6.12 Switching Characteristics: V_{CC1} and V_{CC2} 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output		See 图 7-1		17	24	ns
t_{PHL}	Propagation delay , high-to-low-level output		See 图 7-1		17	24	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$		See 图 7-1		0.5	2	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	3	ns
t_r	Output-signal rise time		See 图 7-1		2.3		ns
t_f	Output-signal fall time		See 图 7-1		2.3		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722-Q1	See 图 7-2	6	8	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output	ISO722-Q1	See 图 7-2	3.5	4	15	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output	ISO722-Q1	See 图 7-3	5.5	8	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output	ISO722-Q1	See 图 7-3	4	5	15	µs
t_{fs}	Failsafe output delay time from input power loss		See 图 7-4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter		See 图 7-6		2		ns
			See 图 7-6		3		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output		See 图 7-1		20	34	ns
t_{PHL}	Propagation delay , high-to-low-level output		See 图 7-1		20	34	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$		See 图 7-1		0.5	3	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		See 图 7-1		2.3		ns
t_f	Output signal fall time		See 图 7-1		2.3		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722-Q1	See 图 7-2	7	13	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output	ISO722-Q1	See 图 7-2	5	6	15	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output	ISO722-Q1	See 图 7-3	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output	ISO722-Q1	See 图 7-3	5	6	15	µs
t_{fs}	Failsafe output delay time from input power loss		See 图 7-4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter		See 图 7-6		2		ns
			See 图 7-6		3		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.14 Switching Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	See 图 7-1		17	30	ns
t_{PHL}	Propagation delay , high-to-low-level output	See 图 7-1		17	30	ns
$t_{sk(p)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$	See 图 7-1		0.5	3	ns
$t_{sk(pp)}$ (1)	Part-to-part skew			0	5	ns

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over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time		See 图 7-1		2.3		ns
t_f	Output signal fall time		See 图 7-1		2.3		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722-Q1	See 图 7-2	7	9	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			4.5	5	15	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See 图 7-3	7	9	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			4.5	5	15	µs
t_{fs}	Failsafe output delay time from input power loss		See 图 7-4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter		See 图 7-6		2		ns
			See 图 7-6		3		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

6.15 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output		See 图 7-1		19	30	ns
t_{PHL}	Propagation delay , high-to-low-level output		See 图 7-1		19	30	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$		See 图 7-1		0.5	3	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		See 图 7-1		2.3		ns
t_f	Output signal fall time		See 图 7-1		2.3		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-impedance output	ISO722-Q1	See 图 7-2	7	13	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output			5	6	15	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See 图 7-3	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output			5	6	15	µs
t_{fs}	Failsafe output delay time from input power loss		See 图 7-4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter		See 图 7-6		2		ns
			See 图 7-6		3		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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6.16 Typical Characteristics

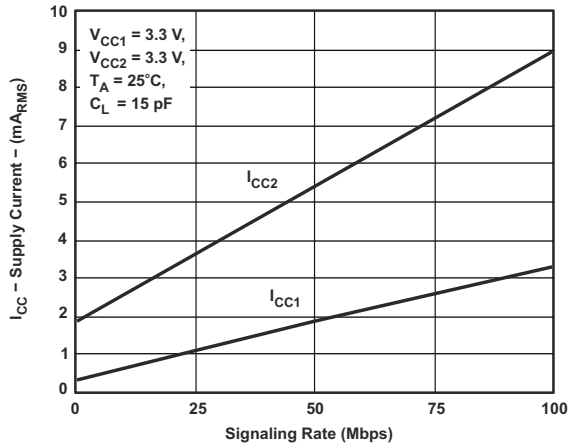

图 6-1. RMS Supply Current Versus Signaling Rate

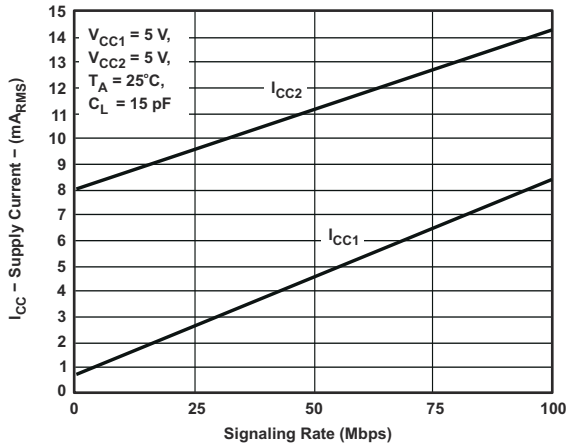

图 6-2. RMS Supply Current Versus Signaling Rate

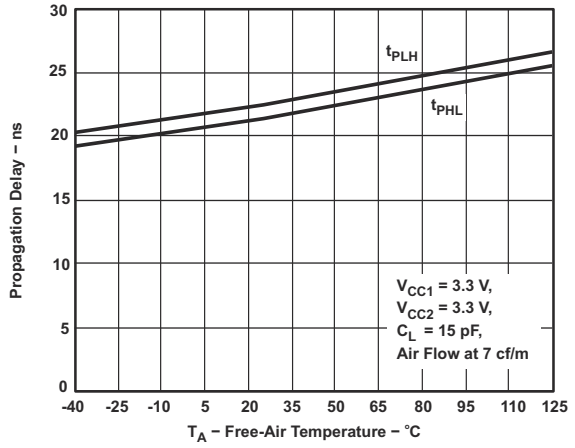

图 6-3. Propagation Delay Versus Free-Air Temperature

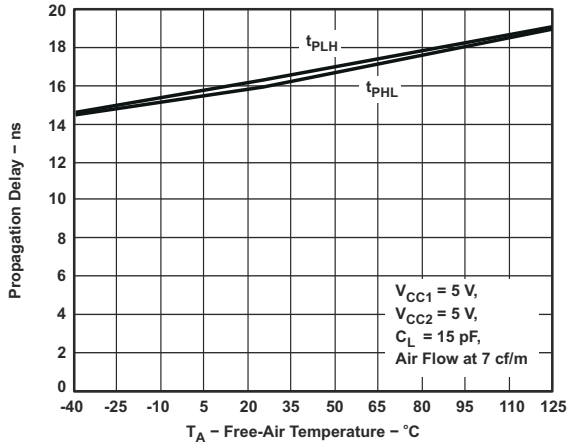

图 6-4. Propagation Delay Versus Free-Air Temperature

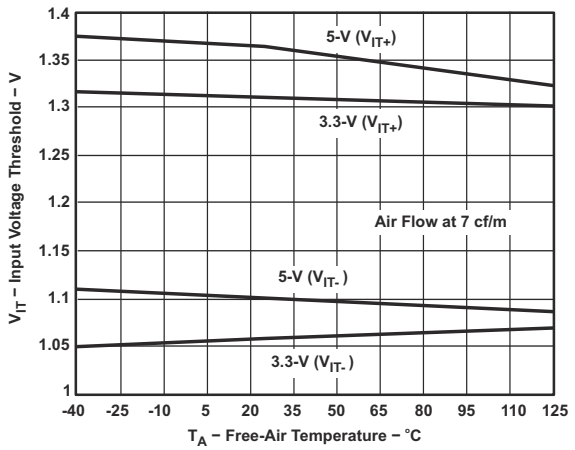

图 6-5. Input Threshold Voltage Versus Free-Air Temperature

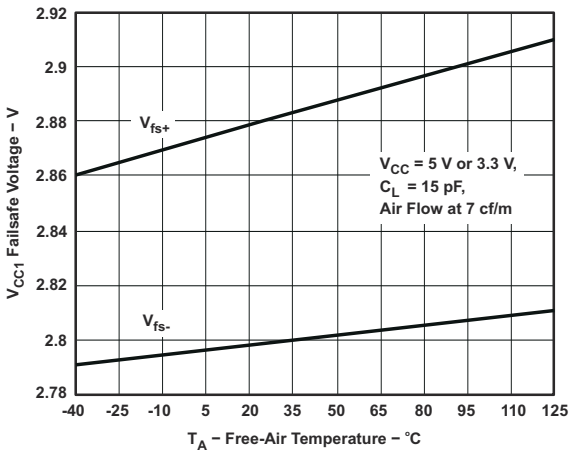

图 6-6. V_{CC1} Failsafe Threshold Voltage Versus Free-Air Temperature

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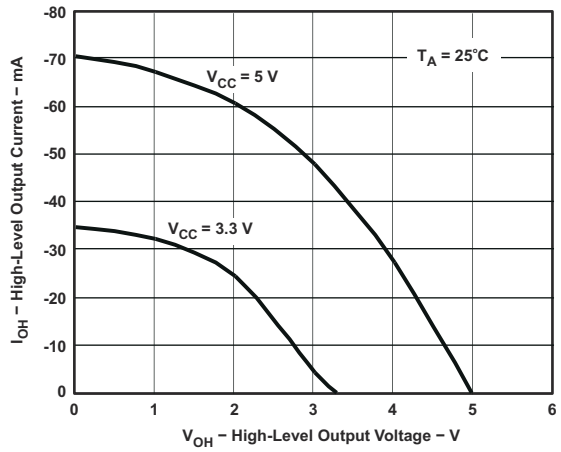

图 6-7. High-Level Output Current Versus High-Level Output Voltage

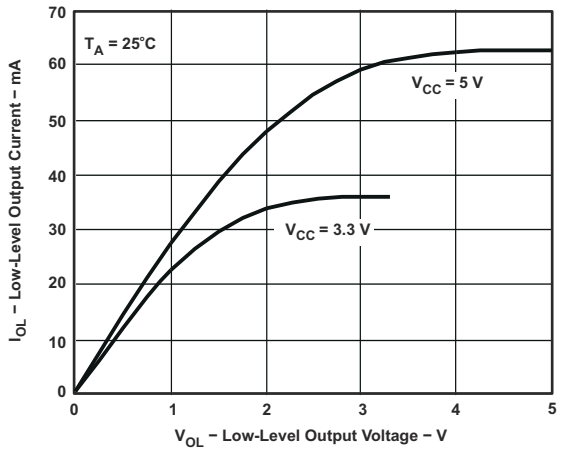

图 6-8. Low-Level Output Current Versus Low-Level Output Voltage

6.17 Insulation Characteristics Curves

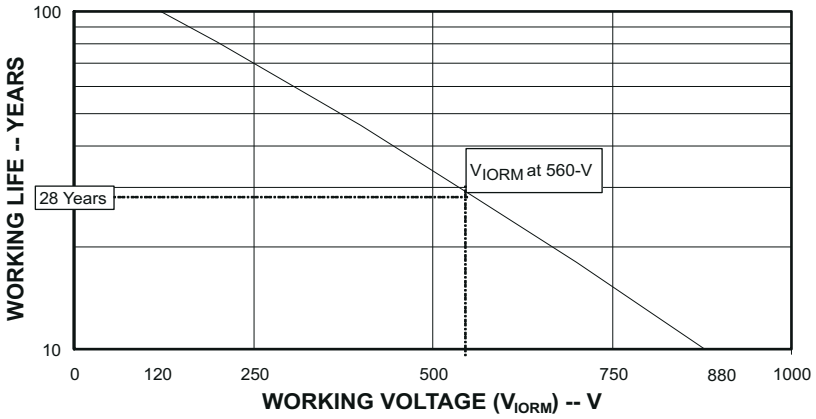

图 6-9. Time Dependent Dielectric Breakdown Testing Results

7 Parameter Measurement Information

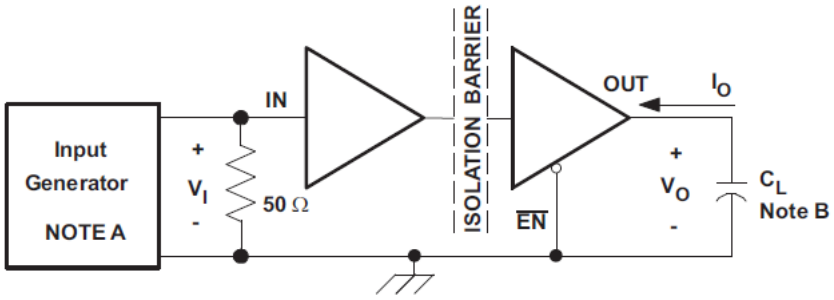

图 7-1. Switching Characteristic Test Circuit and Voltage Waveforms

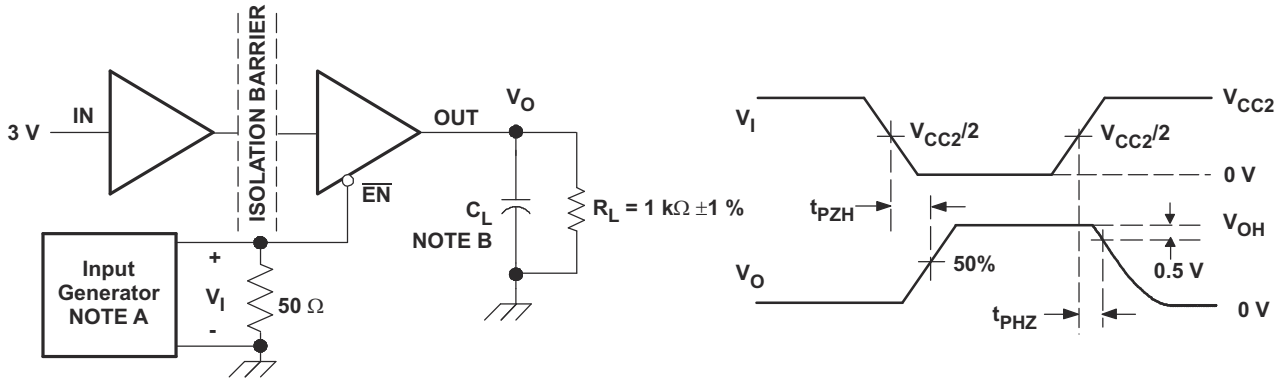

图 7-2. ISO722-Q1 Sleep-Mode High-Level Output Test Circuit and Voltage Waveforms

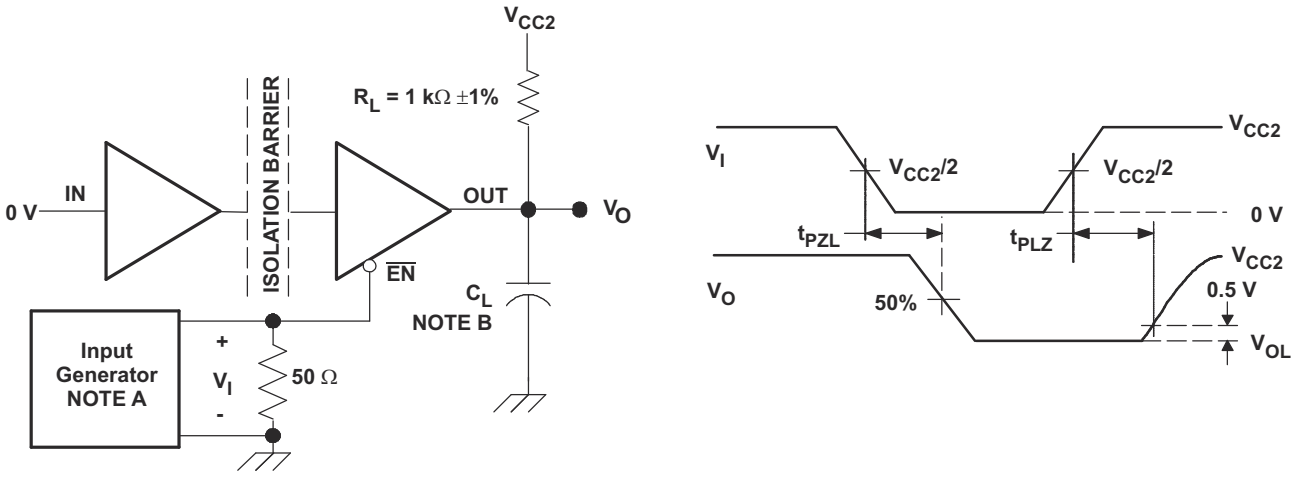

图 7-3. ISO722-Q1 Sleep-Mode Low-Level Output Test Circuit and Voltage Waveforms

备注

A: The input pulse is supplied by a generator having the following characteristics:

PRR ⩽ 50 kHz, 50% duty cycle, t_r ⩽ 3 ns, t_f ⩽ 3 ns, Z_O = 50 Ω.

B: C_L = 15 pF ± 20% and includes instrumentation and fixture capacitance.

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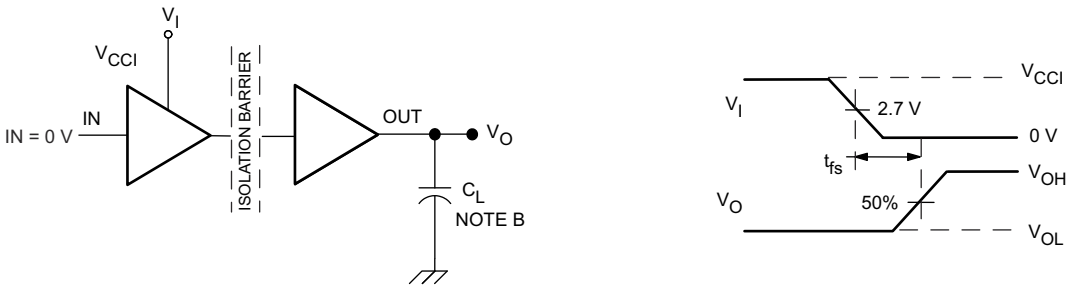
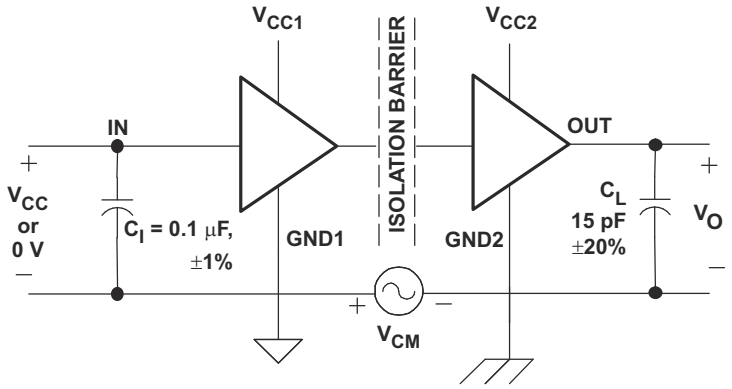


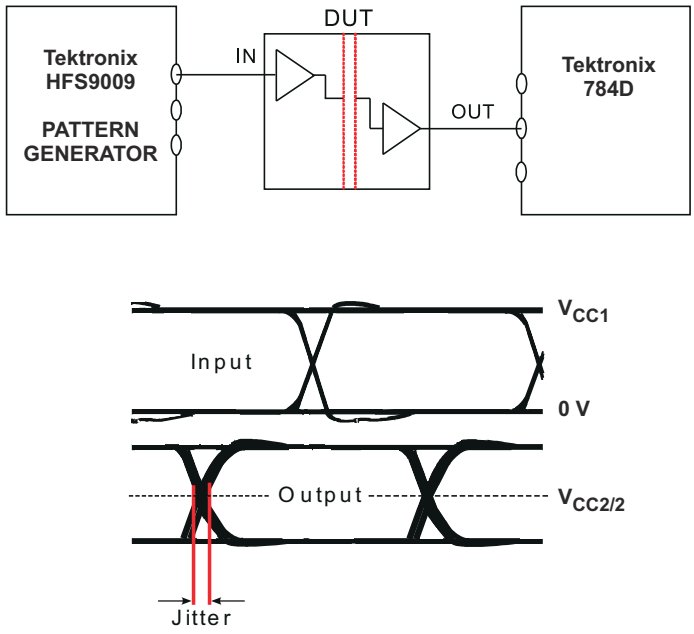
NOTE: V_I transition time is 100 ns.

图 7-4. Failsafe Delay Time Test Circuit and Voltage Waveforms



NOTE: Pass/fail criterion is no change in V_O.

图 7-5. Common-Mode Transient-Immunity Test Circuit and Voltage Waveform



NOTE: Bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

图 7-6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

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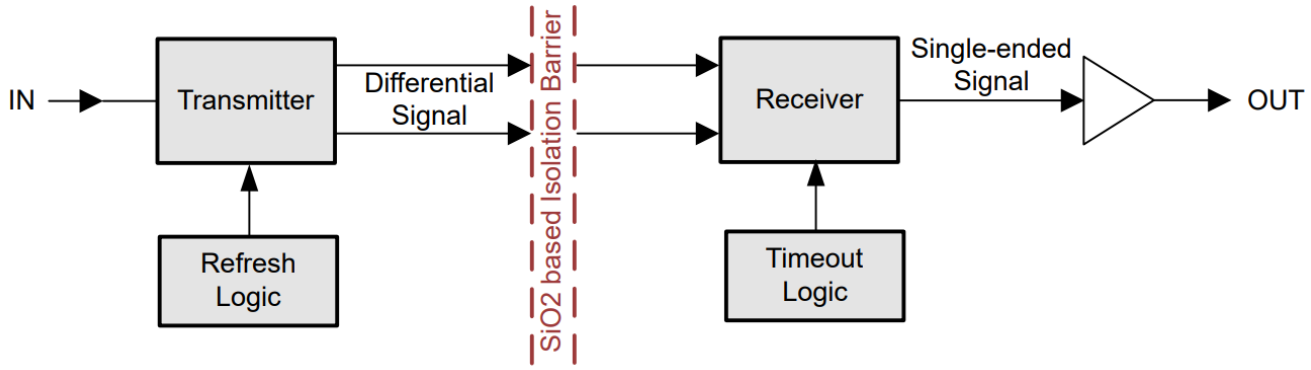
8 Detailed Description

8.1 Overview

The ISO72x-Q1 family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

8.2 Functional Block Diagram



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8.3 Device Functional Modes

表 8-1 and 表 8-2 list the functional modes for the ISO72x-Q1 family of devices.

表 8-1. ISO721-Q1 Functional Table

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

表 8-2. ISO722-Q1 Functional Table

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT ENABLE ($\overline{EN}$)	OUTPUT (OUT)
PU	PU	H	L or open	H
		L	L or open	L
		X	H	Z
		Open	L or open	H
PD	PU	X	L or open	H
PD	PU	X	H	Z
X	PD	X	X	Undetermined

8.3.1 Device I/O Schematic

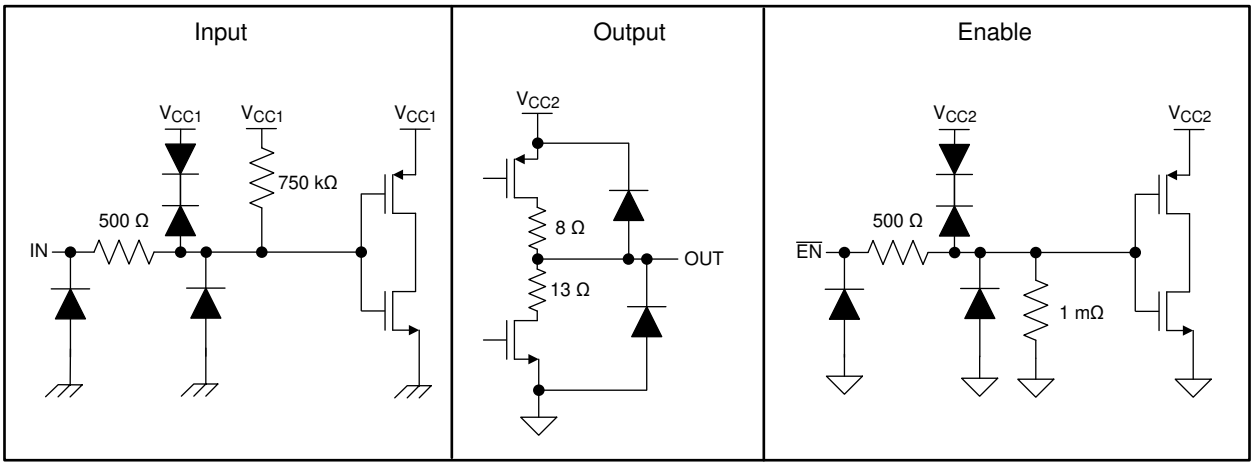


图 8-1. Equivalent Input and Output Schematic Diagrams

9 Application and Implementation

备注

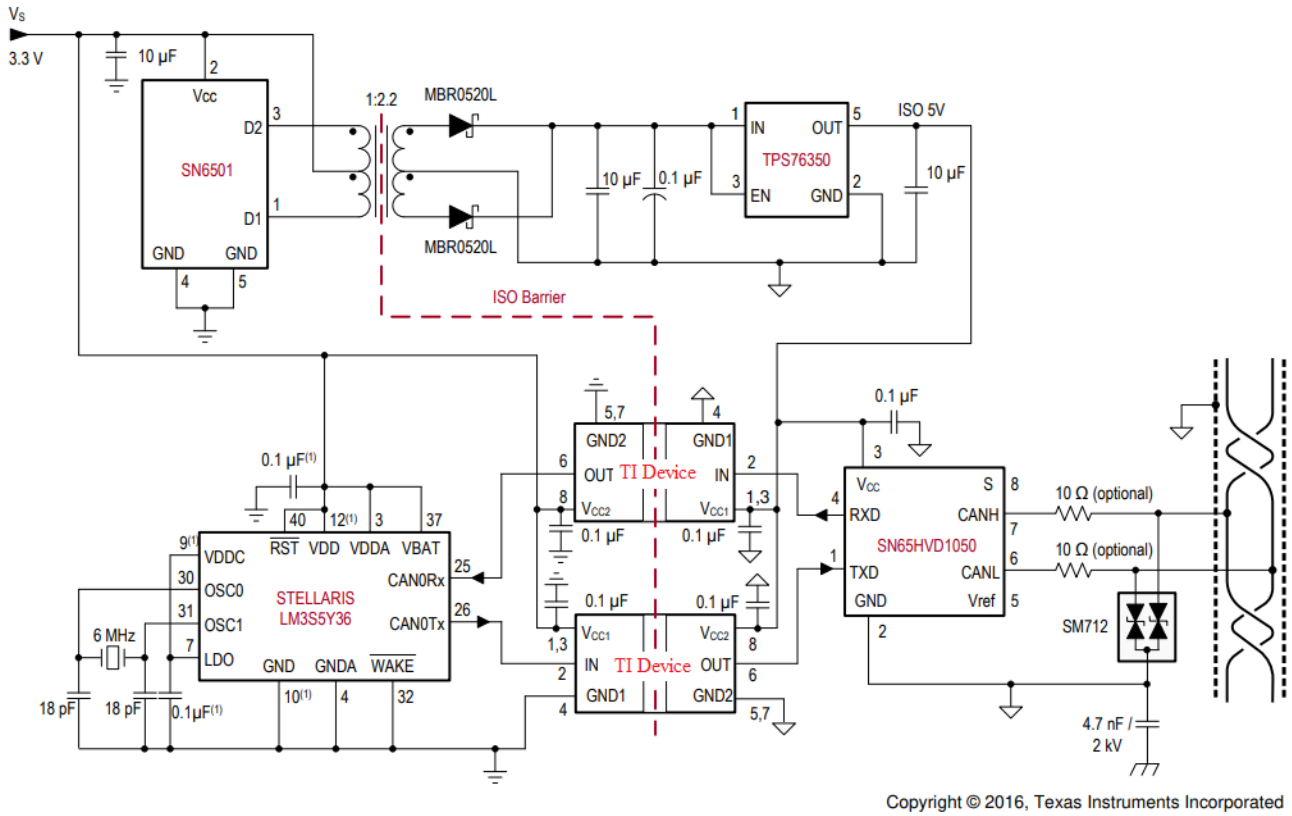
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ISO72x-Q1 devices use single-ended TTL or CMOS-logic-switching technology. The supply voltage range of the devices is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, because the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO721 device can be used with Texas Instruments’ microcontroller, CAN transceiver, transformer driver, and low-dropout voltage regulator to create an Isolated CAN Interface as shown in 图 9-1.



A. Multiple pins and capacitors omitted for clarity purpose.

图 9-1. Isolated CAN Interface

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9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO72x-Q1 devices only require two external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

图 9-2 shows a typical circuit hook-up for the ISO721-Q1 device.

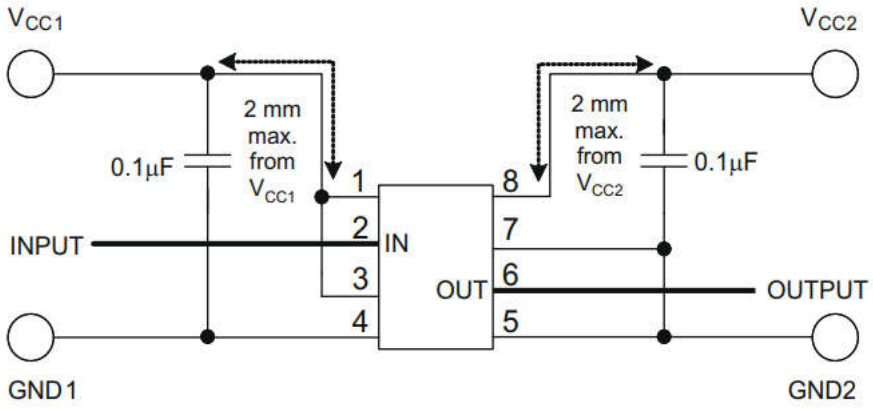

图 9-2. Typical ISO721-Q1 Circuit Hook-up

The ISO72x-Q1 isolators have the same functional pinout as those of most other vendors as shown in 图 9-3, and are often pin-for-pin drop-in replacements. The notable differences in the products are propagation delay, signaling rate, power consumption, and transient protection rating. 表 9-1 is used as a guide for replacing other isolators with the ISO72x-Q1 family of single-channel isolators.

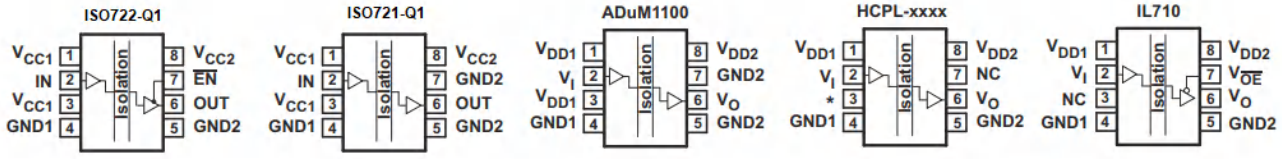

图 9-3. Pin Cross Reference

表 9-1. Cross Reference

ISOLATOR	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7		PIN 8
							ISO721-Q1 OR ISO721M-Q1	ISO722-Q1 OR ISO722M-Q1	
ISO721(1) (2)	V_{CC1}	IN	V_{CC1}	GND1	GND2	OUT	GND2	$\overline{EN}$	V_{CC2}
ADuM1100(1) (2)	V_{DD1}	V_I	V_{DD1}	GND1	GND2	V_O	GND2		V_{DD2}
HCPL-xxxx	V_{DD1}	V_I	*Leave Open(3)	GND1	GND2	V_O	NC(5)		V_{DD2}
IL710	V_{DD1}	V_I	NC(4)	GND1	GND2	V_O	$V_{\overline{OE}}$		V_{DD2}

(1) Pin 1 must be used as V_{CC1}. Pin 3 can also be used as V_{CC1} or left open, as long as pin 1 is connected to V_{CC1}.
(2) Pin 5 must be used as GND2. Pin 7 can also be used as GND2 or left open, as long as pin 5 is connected to GND2.
(3) Pin 3 of the HCPL devices must be left open. This is not a problem when substituting an ISO72x-Q1 device, because the extra V_{CC1} on pin 3 can be left an open circuit as well.
(4) Pin 3 of the IL710 must not be tied to ground on the circuit board because this shorts the ISO72x-Q1 V_{CC1} to ground. The IL710 pin 3 can only be tied to V_{CC} or left open to drop in an ISO72x-Q1 device.

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(5) An HCPL device pin 7 must be left floating (open) or grounded when an ISO722-Q1 or ISO722M-Q1 device is to be used as a drop-in replacement. If pin 7 of the ISO722-Q1 or ISO722M-Q1 device is placed in a high logic state, the output of the device is disabled.

9.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor must be placed at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet.

9.4 Layout

9.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 图 9-4). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

9.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

9.4.2 Layout Example

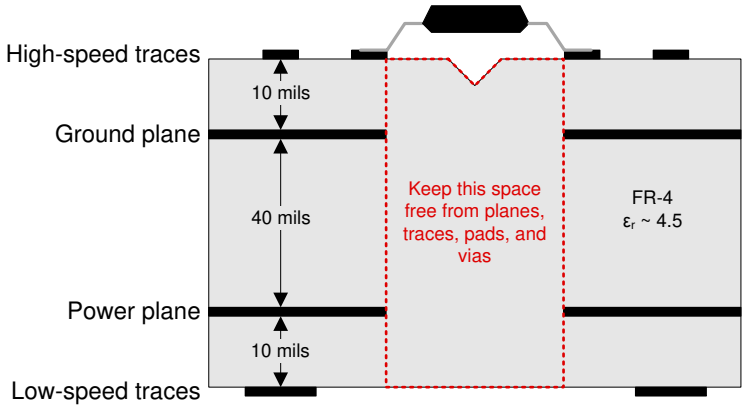

图 9-4. Recommended Layer Stack

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

For development support, see the following:

- Texas Instruments, *36Vdc-75Vdc Input, 20V @ 4A Output, Active Clamp Forward* TI Reference Design
- Texas Instruments, *18Vdc-54Vdc Input, 24V @ 5A Output, Active Clamp Forward* TI Reference Design
- Texas Instruments, *36Vdc-75Vdc Input, 6V @ 20A Output, Active Clamp Forward* TI Reference Design
- Texas Instruments, *ISO72x IBIS Model*

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *Isolated RS-485 Reference Design* application report
- Texas Instruments, *ISO721EVM* user's guide

10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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10.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (November 2024) to Revision E (February 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

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Changes from Revision C (July 2013) to Revision D (November 2024)	Page
• 通篇将“VDE V 0884-11”更新为“DIN VDE 0884-17”	1
• 通篇将引用内容从电容隔离更新为隔离栅	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations	4
• Updated electrical and switching characteristics to match device performance	6
• Added the *Detailed Description*, *Overview*, *Feature Description*, *Functional Block Diagram*, and *Device Functional Modes* sections	14
• Added the *Typical Application*, *Power Supply Recommendations*, and *Layout* sections	16

Changes from Revision B (June 2013) to Revision C (July 2013)	Page
• 将温度等级从 3 更改为 1	1
• Changed the IEC 60664-1 RATINGS TABLE - Specification I-III test conditions From: Rated mains voltage ≤150 VRMS To: Rated mains voltage ≤300 VRMS. Added a row for the I-II specifications	4

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO721QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	IS721Q
ISO721QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	IS721Q
ISO721QDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO722QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	IS722Q
ISO722QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	IS722Q
ISO722QDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO721-Q1, ISO722-Q1 :

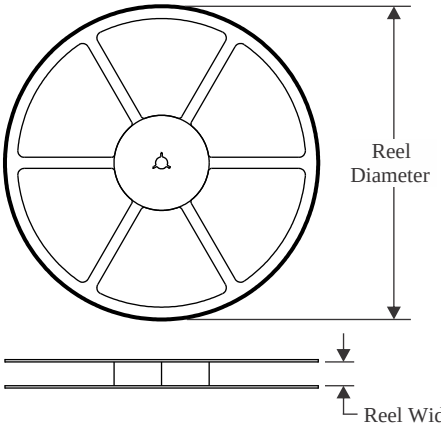
- Catalog : ISO721, ISO722
- Military : ISO721M

NOTE: Qualified Version Definitions:

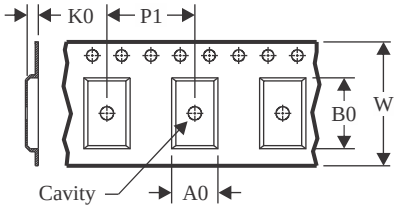
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

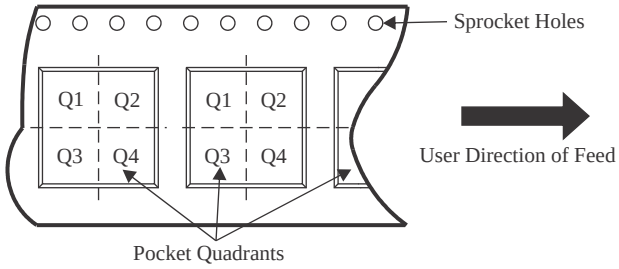


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

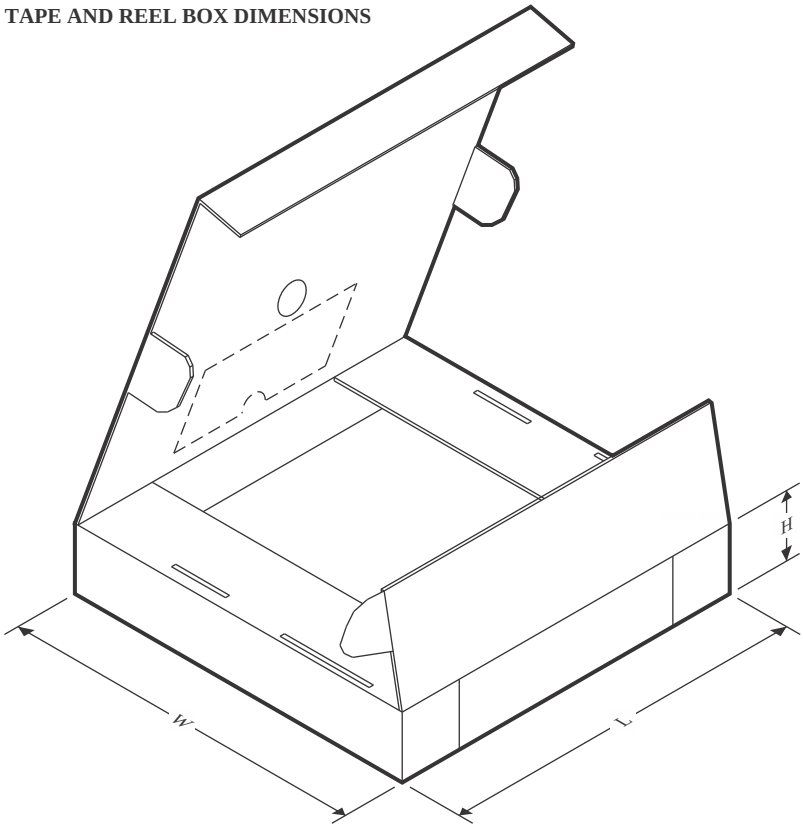
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

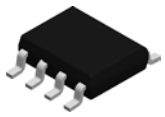
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO721QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO722QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO721QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO722QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0

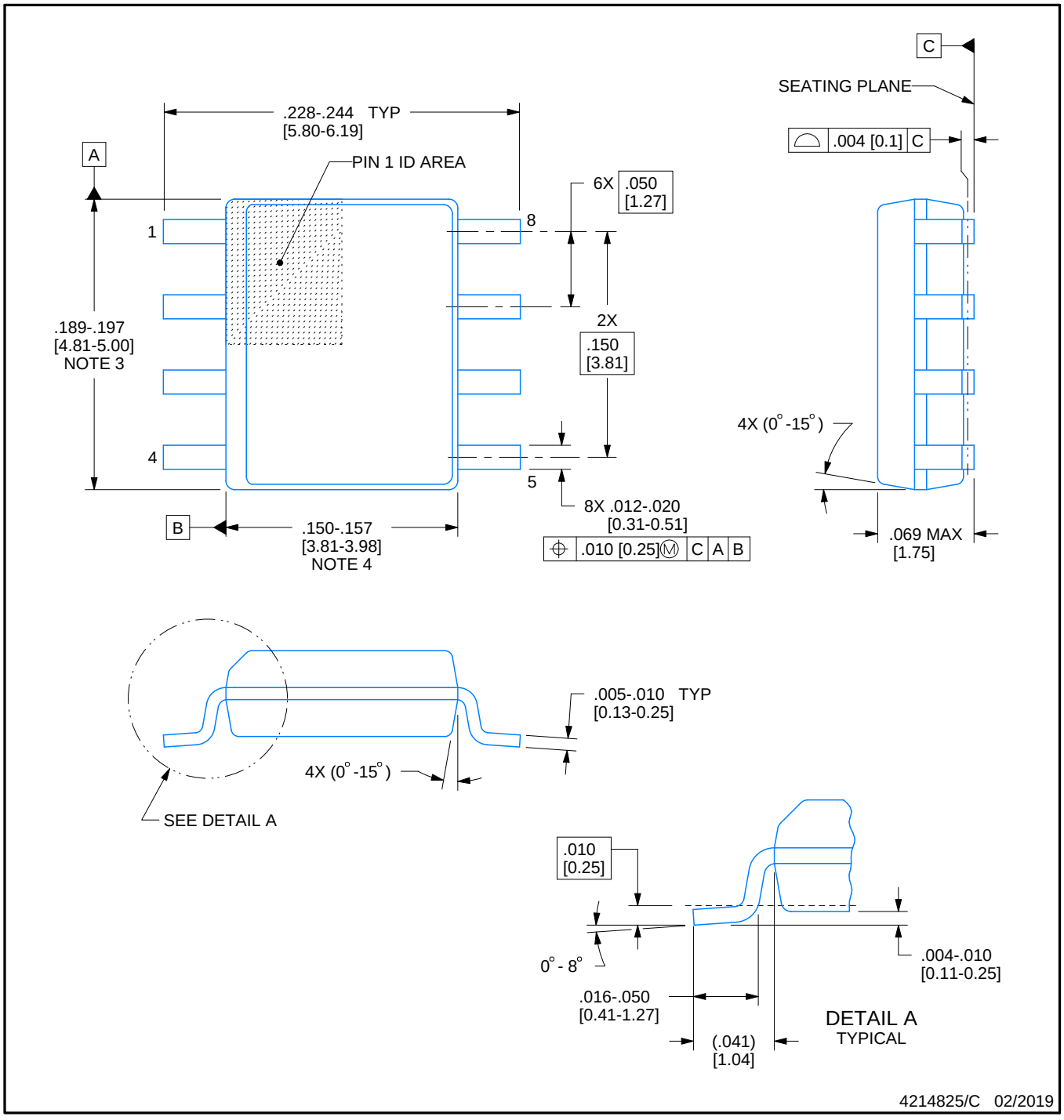


PACKAGE OUTLINE

D0008A

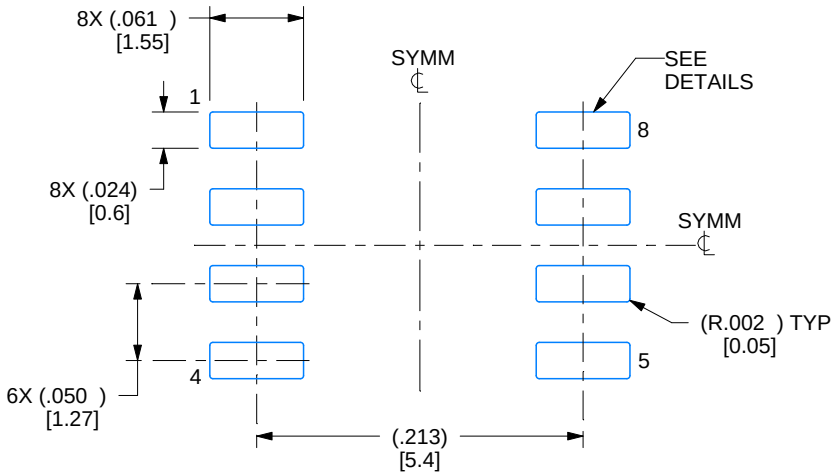
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

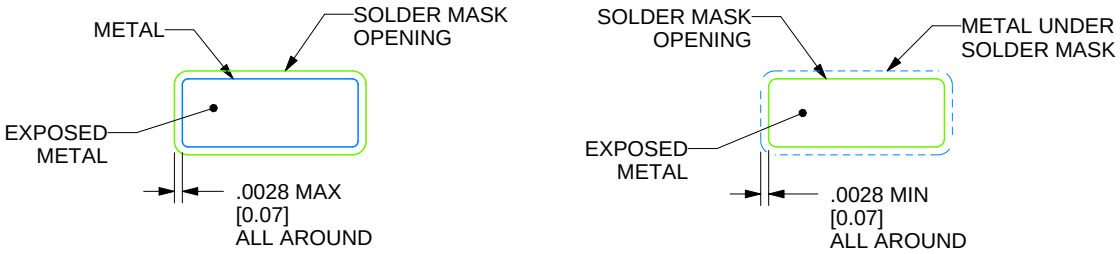


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

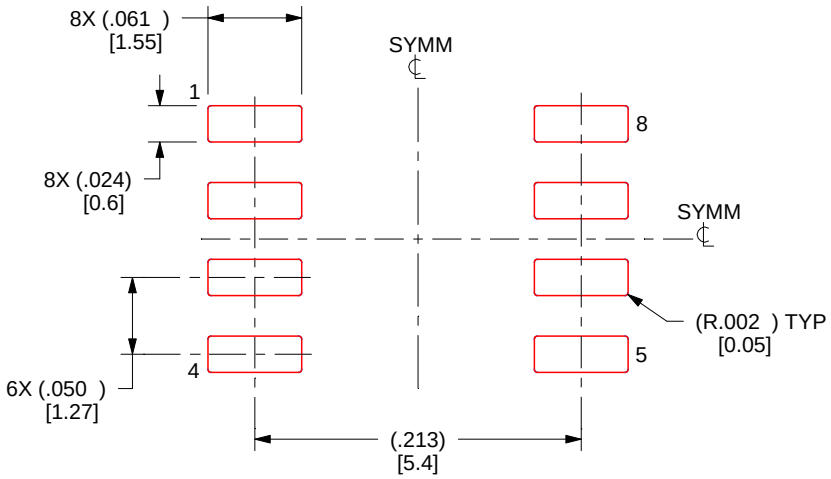
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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