ISO7041-Q1 汽车类超低功耗四通道数字隔离器

1 特性

- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
- 提供功能安全
  - 可提供用于功能安全系统设计的文档：ISO7041-Q1
- 满足 VDA320 隔离要求
- 超低功耗
  - 每通道静态电流为 3.5 µA (3.3V)
  - 100kbps 时的每通道电流为 15 µA (3.3V)
  - 1Mbps 时的每通道电流为 116 µA (3.3V)
- 稳健可靠的隔离栅
  - 预计寿命超过 100 年
  - 隔离额定值为 3000V_{RMS}
  - CMTI 典型值为 ±100kV/ µs
- 宽电源电压范围：3.0V 至 5.5V
- 宽温度范围：–40°C 至 125°C
- 小型 16-QSOP 封装 (16-DBQ)
- 信令速率：高达 4Mbps
- 默认输出*高电平* (ISO7041-Q1) 和*低电平* (ISO7041F-Q1) 选项
- 优异的电磁兼容性 (EMC)
  - 系统级 ESD、EFT 和浪涌抗扰性
  - 在整个隔离栅具有 ±8kV IEC 61000-4-2 接触放电保护
  - 超低干扰 (EMI)
- 安全相关认证（计划）：
  - DIN V VDE 0884-11:2017-01
  - UL 1577 组件认证计划
  - IEC 60950-1、IEC 62368-1、IEC 61010-1、IEC60601-1 和 GB 4943.1-2011 认证

2 应用

- 混合动力、电动和动力总成系统 (EV/HEV)
  - 电池管理系统 (BMS)
  - 车载充电器
  - 牵引逆变器
  - 直流/直流转换器
  - 逆变器和电机控制

3 说明

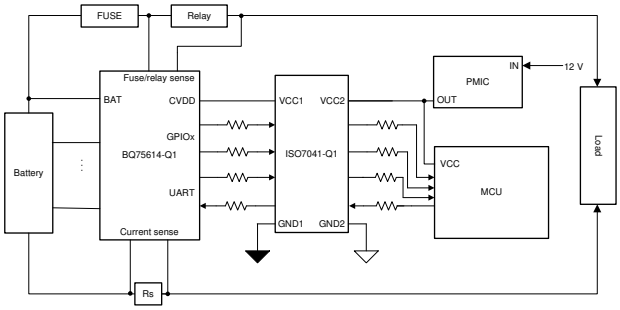
ISO7041-Q1 器件是一款可用于隔离 CMOS 或 LVCMOS 数字 I/O 的超低功耗多通道数字隔离器。每条隔离通道的逻辑输入和输出缓冲器均由双电容二氧化硅 (SiO_2) 绝缘栅相隔离。基于边缘的创新架构与开关键控调制方案相结合，使这些隔离器具有非常低的功耗，同时符合 UL1577 规定的 3000V_{RMS} 隔离额定值。ISO7041-Q1 器件在 3.3V 时的每通道动态电流消耗低于 120 µA/Mbps，每通道静态电流消耗为 3.5 µA，因此可用于对功耗和热性能有要求的系统设计中。

该器件可在低至 3.0V 和高达 5.5V 的电压下工作，并可在隔离层的每一侧采用不同电源电压的情况下完全正常运行。四通道隔离器采用 16-QSOP 封装，具有三个正向通道和一个反向通道。该器件具有默认输出高电平和低电平选项。如果输入功率或信号出现损失，则不具有 F 后缀的 ISO7041-Q1 器件默认输出*高电平*，具有 F 后缀的 ISO7041F-Q1 器件默认输出*低电平*。请参阅器件功能模式 部分以了解详情。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
ISO7041-Q1	QSOP (16)	4.90mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用原理图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
June 2022	*	Initial Release

Device Comparison Table

表 5-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION
ISO7041-Q1	3 Forward, 1 Reverse	4 Mbps	High	DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7041-Q1 with F suffix	3 Forward, 1 Reverse	4 Mbps	Low	DBQ-16	3000 V_{RMS} / 4242 V_{PK}

5 Pin Configuration and Functions

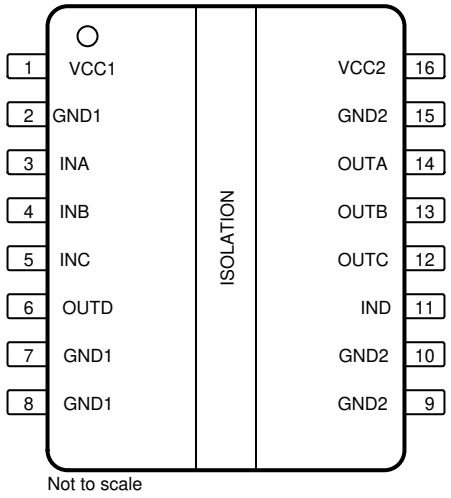


图 5-1. ISO7041-Q1 DBQ Package 16-Pin QSOP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	2	—	Ground connection for V_{CC1}
	7		
	8		
GND2	9	—	Ground connection for V_{CC2}
	10		
	15		
INA	3	I	Input, channel A. 300-Ω series resistor recommended
INB	4	I	Input, channel B. 300-Ω series resistor recommended
INC	5	I	Input, channel C. 300-Ω series resistor recommended
IND	11	I	Input, channel D. 300-Ω series resistor recommended
OUTA	14	O	Output, channel A. 300-Ω series resistor recommended
OUTB	13	O	Output, channel B. 300-Ω series resistor recommended
OUTC	12	O	Output, channel C. 300-Ω series resistor recommended
OUTD	6	O	Output, channel D. 300-Ω series resistor recommended
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

6 Specifications

6.1 绝对最大额定值

在自然通风条件下的工作温度范围内（除非另有说明）(1) (2) (3)

		最小值	最大值	单位
电源电压	V_{CC1} 至 GND1	-0.5	6	V
	V_{CC2} 至 GND2	-0.5	6	
输入/输出电压	INx 至 GNDx	-0.5	V_{CCX} + 0.5	V
	OUTx 至 GNDx	-0.5	V_{CCX} + 0.5	
	ENx 至 GNDx	-0.5	V_{CCX} + 0.5	
输入电流	输入通道，Ii	-15	15	mA
输出电流	Io	-15	15	mA
温度	运行结温，T_J		150	°C
	贮存温度，T_{stg}	-65	150	°C

(1) 超出这些列出的绝对最大额定值的压力可能会对器件造成永久损坏。这些仅仅是压力额定值，并不表示器件在这些条件下以及在“建议运行条件”以外的任何其他条件下能够正常运行。在绝对最大额定值条件下长时间运行可影响器件可靠性。
(2) 除差分 I/O 总线电压以外的所有电压值都是以本地接地端子（GND1 或 GND2）为基准的峰值电压值。
(3) 最大电压不得超过 6V。

6.2 ESD Ratings

(1) (2)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4)	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1} (1)	Supply Voltage Side 1		3.0		5.5	V
V_{CC2} (1)	Supply Voltage Side 2		3.0		5.5	V
V_{IH}	High level Input voltage		0.7 x V_{CCI}		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	High level output current	V_{CCO} (2) = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			mA
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	mA
DR	Data Rate		0		4	Mbps
T_A	Ambient temperature		-40		125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.4 Thermal Information

THERMAL METRIC(1)		ISO7041-Q1 DBQ (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 1-MHz 50% duty cycle square wave			7.82	mW
P_{D1}	Maximum power dissipation (side-1)				4.46	mW
P_{D2}	Maximum power dissipation (side-2)				3.36	mW

Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
			QSOP-16	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	>3.7	mm
CPG	External Creepage(1)	Side 1 to side 2 distance across package surface	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ⩽ 300 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; See TBD	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM} , t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 6400 V_{PK} (qualification)	4000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} , t_m = 10 s	⩽ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM} , t_m = 10 s	⩽ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} , t_m = 1 s	⩽ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2 π ft), f = 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ⩽ T_A ⩽ 150°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} , t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

6.6 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017- 01	Certified according to IEC 60950-1 and IEC 62368-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010/A1:2019, EN 60950- 1:2006/ A2:2013 and EN 62368-1:2014
Maximum transient isolation voltage, 4242 V_{PK}; Maximum repetitive peak isolation voltage, 566 V_{PK}; Maximum surge isolation voltage, 4000 V_{PK}	3000 V_{RMS} insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1- 14 and IEC 62368-1:2014 370 V_{RMS} (DBQ-16) maximum working voltage (pollution degree 2, material group I)	Single protection, 3000 V_{RMS}	Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage	EN 61010- 1:2010/ A1:2019, 300 V_{RMS} basic isolation EN 60950- 1:2006/ A2:2013 and EN 62368-1:2014, 400 V_{RMS} basic isolation
Certification Planned	Certification Planned	Certification Planned	Certification Planned	Certification Planned

6.7 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16-QSOP PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 87°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			261	mA
		$R_{\theta JA}$ = 87°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			399	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 87°C/W, T_J = 150°C, T_A = 25°C			1435	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.8 Electrical Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -4 mA	V_{CCO} - 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2 π ft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.9 Supply Current Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7041-Q1						
Supply current - DC signal	Refresh disable	I_{CC1}		6.2	14.3	µA
		I_{CC2}		10.1	18.5	µA
	Refresh enable V_I = V_{CCI} (1) (ISO7041-Q1); V_I = 0 V (ISO7041-Q1 with F suffix)	I_{CC1}		8.2	16.7	µA
		I_{CC2}		10.8	18.5	µA
	Refresh enable V_I = 0 V (ISO7041-Q1); V_I = V_{CCI} (ISO7041-Q1 with F suffix)	I_{CC1}		9.5	19.9	µA
		I_{CC2}		11.3	19.5	µA
Supply current - AC signal	Refresh disable 10 kbps, No Load	I_{CC1}		6.7	19.7	µA
		I_{CC2}		11.8	20.6	µA
	Refresh disable 100 kbps, No Load	I_{CC1}		37.1	57.4	µA
		I_{CC2}		25.8	37.7	µA
	Refresh disable 1 Mbps, No Load	I_{CC1}		340.5	436.1	µA
		I_{CC2}		167.0	211.1	µA
	Refresh enable 10 kbps, No Load	I_{CC1}		10.6	20.8	µA
		I_{CC2}		11.9	20.4	µA
	Refresh enable 100 kbps, No Load	I_{CC1}		37.1	57.4	µA
		I_{CC2}		25.8	37.7	µA
	Refresh enable 1 Mbps, No Load	I_{CC1}		338.3	436.1	µA
		I_{CC2}		166.0	211.1	µA
Total Supply Current Per Channel, Refresh Disabled	DC Signal	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.1	7.4	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.9	10.7	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		17.4	23.4	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		137.0	164.5	µA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Total Supply Current Per Channel, Refresh Enabled	V_I = V_{CCI} (ISO7041-Q1); V_I = 0 V (ISO7041-Q1 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.8	8.5	µA
	V_I = 0 V (ISO7041-Q1); V_I = V_{CCI} (ISO7041-Q1 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.3	9.6	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.7	10.4	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		16.4	22.3	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		125.9	154.0	µA

(1) V_{CCI} = Input-side V_{CC}

6.10 Electrical Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -2mA	V_{CCO} - 0.3			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA			0.3	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V	50	100		kV/us
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2 π ft), f = 1 MHz, V_{CC} = 3.6 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.11 Supply Current Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7041-Q1						
Supply current - DC signal	Refresh disable	I_{CC1}		5.1	8.8	µA
		I_{CC2}		8.9	14.0	µA
	Refresh enable V_I = V_{CCI} (1) (ISO7041-Q1); V_I = 0 V (ISO7041-Q1 with F suffix)	I_{CC1}		6.8	12.2	µA
		I_{CC2}		9.6	14.0	µA
	Refresh enable V_I = 0 V (ISO7041-Q1); V_I = V_{CCI} (ISO7041-Q1 with F suffix)	I_{CC1}		8.1	14.8	µA
		I_{CC2}		10.0	15.6	µA
Supply current - AC signal	Refresh disable 10 kbps, No Load	I_{CC1}		7.9	13.7	µA
		I_{CC2}		10.4	15.9	µA
	Refresh disable 100 kbps, No Load	I_{CC1}		35.9	48.3	µA
		I_{CC2}		22.7	31.4	µA
	Refresh disable 1 Mbps, No Load	I_{CC1}		316.4	395.7	µA
		I_{CC2}		147.2	188.2	µA
	Refresh enable 10 kbps, No Load	I_{CC1}		9.8	16.4	µA
		I_{CC2}		10.5	16.2	µA
	Refresh enable 100 kbps, No Load	I_{CC1}		35.9	48.3	µA
		I_{CC2}		22.7	31.4	µA
	Refresh enable 1 Mbps, No Load	I_{CC1}		315.3	395.7	µA
		I_{CC2}		146.2	188.2	µA
Total Supply Current Per Channel, Refresh Disabled	DC Signal	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.5	5.7	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.2	8.2	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		14.8	19.2	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		115.7	138.7	µA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Total Supply Current Per Channel, Refresh Enabled	V_I = V_{CCI} (ISO7041-Q1); V_I = 0 V (ISO7041-Q1 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.2	6.8	µA
	V_I = 0 V (ISO7041-Q1); V_I = V_{CCI} (ISO7041-Q1 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.6	7.7	µA
	10 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.2	8.2	µA
	100 kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		14.8	19.2	µA
	1 Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		115.7	138.7	µA

(1) V_{CCI} = Input-side V_{CC}

6.12 Switching Characteristics

V_{CC1}, V_{CC2} = 3.0 V to 5.5 V (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 7-1		148	165	ns
$t_{P(dft)}$	Propagation delay drift			15		ps/℃
t_{UI}	Minimum pulse width	See 图 7-1	250			ns
PWD	Pulse width distortion				10	ns
$t_{sk(o)}$	Channel to channel output skew time	Same-direction channels			10	ns
		Opposite-direction channels			10	ns
$t_{sk(p-p)}$	Part to part skew time				70	ns
t_r	Output signal rise time	See 图 7-1			16	ns
t_f	Output signal fall time	See 图 7-1			16	ns
t_{DO}	Default output delay time from input power loss	See 图 7-2		400	750	us
t_{PU}	Time from UVLO to valid output data		1		5	ms
F_R	Refresh rate		5	10		kbps

6.13 Insulation Characteristics Curves

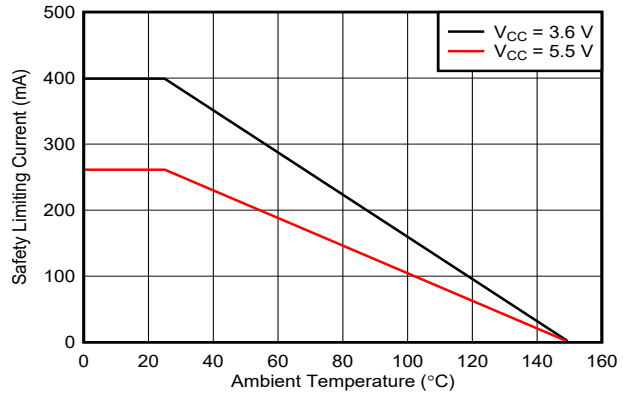


图 6-1. Thermal Derating Curve for Limiting Current per VDE

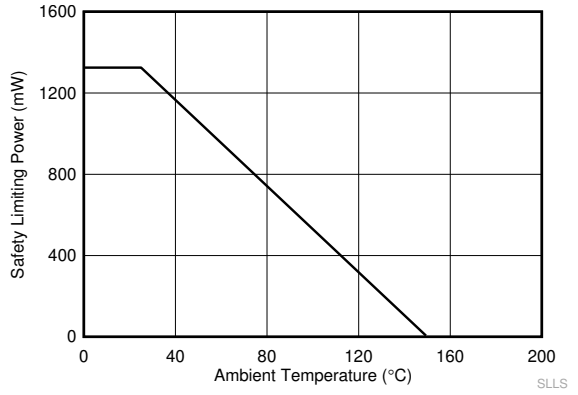


图 6-2. Thermal Derating Curve for Limiting Power per VDE

6.14 Typical Characteristics

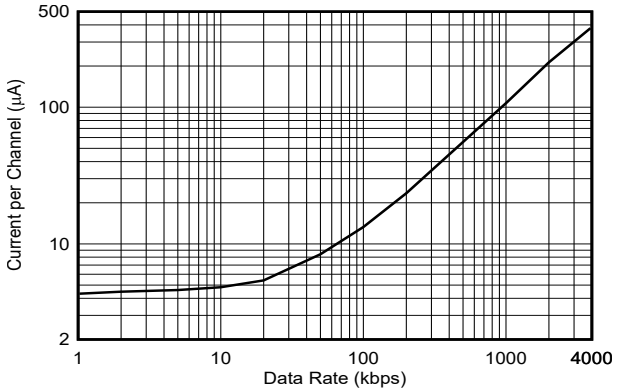


图 6-3. ISO7041-Q1 Supply Current vs Data Rate at 3.3 V (With No Load)

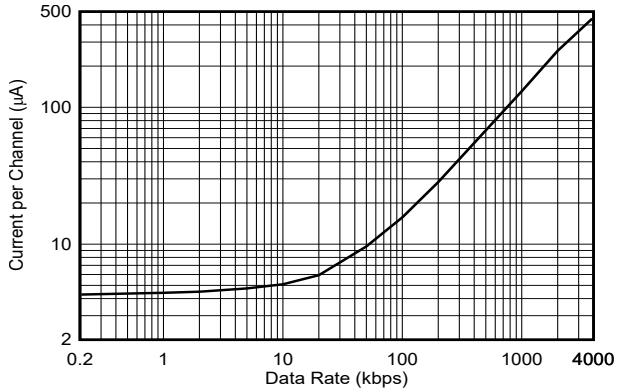


图 6-4. ISO7041-Q1 Supply Current vs Data Rate at 3.3 V (With 15-pF Load)

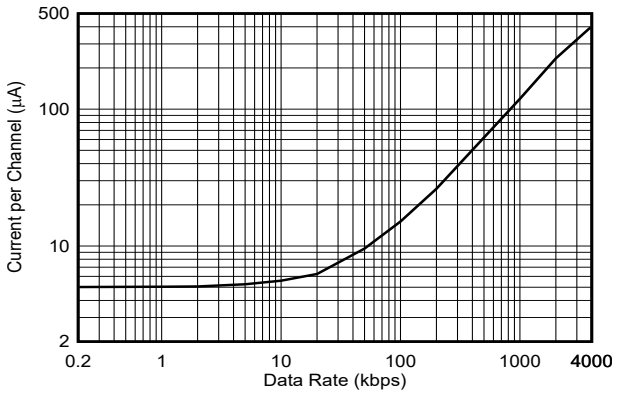


图 6-5. ISO7041-Q1 Supply Current vs Data Rate at 5 V (With No Load)

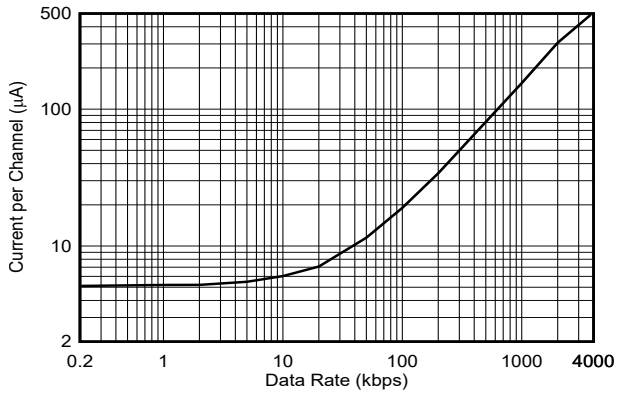
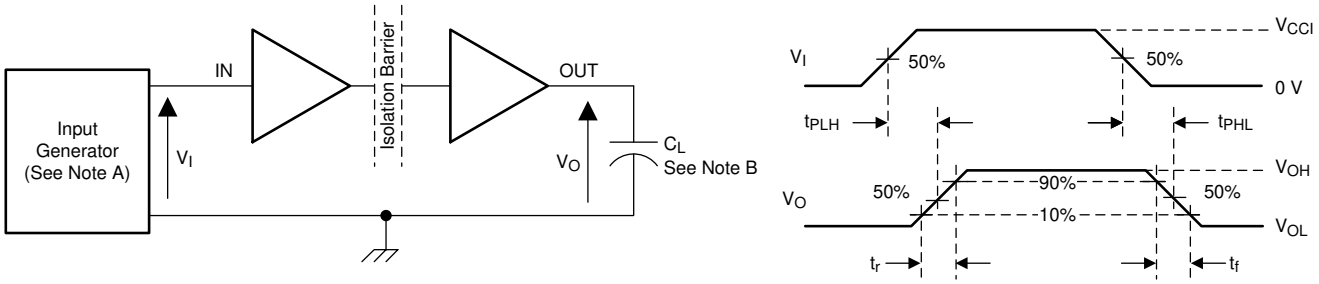


图 6-6. ISO7041-Q1 Supply Current vs Data Rate at 5 V (With 15-pF Load)

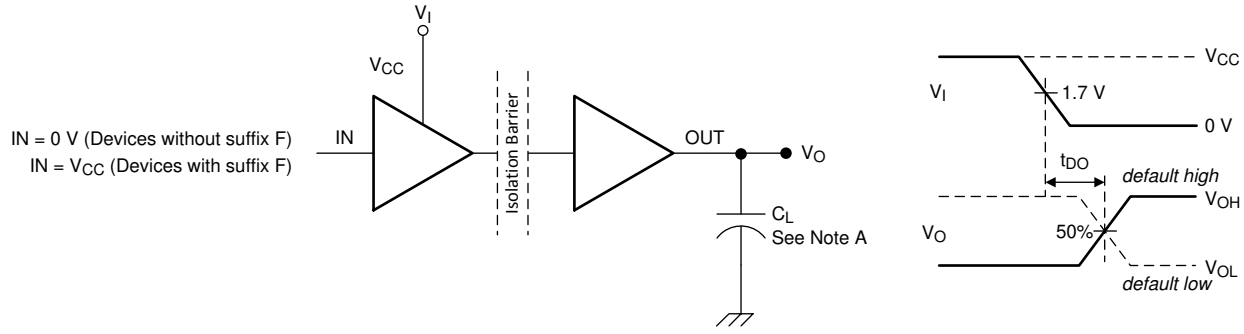
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 50 kHz, 50% duty cycle, t_r ⩽ 3 ns, t_f ⩽ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

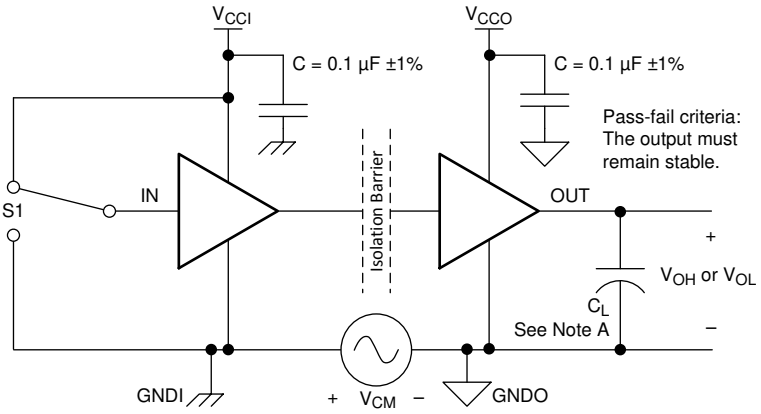
图 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

图 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 7-3. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO7041-Q1 device uses edge encoding of data with an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide isolation barrier. The transmitter uses a high frequency carrier signal to pass data across the barrier representing a signal edge transition. Using this method achieves very low power consumption and high immunity. The receiver demodulates the carrier signal after advanced signal conditioning and produces the output through a buffer stage. For low data rates, a refresh logic option is available to make sure the output state matches the input state. Advanced circuit techniques are used to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Conceptual Block Diagram of a Digital Capacitive Isolator, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

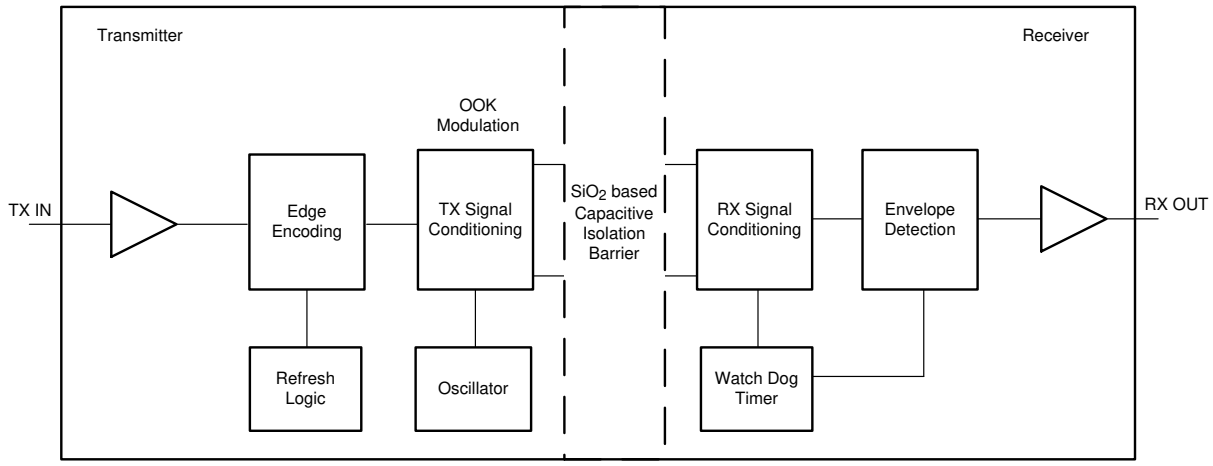


图 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

8.3.1 Refresh

The ISO7041 uses an edge based encoding scheme to transfer an input signal change across the isolation barrier versus sending across the DC state. The built in refresh function consistently validates that the DC output state of each isolator channel matches the DC input state. An internal watchdog timer monitors for activity on the individual inputs and transmits the logic state when there is no input signal transition for more than 100 µs. This ensures that the input and output state of the isolator always match.

8.3.2 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO70xx family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.

- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

The device has no issue being able to meet either CISPR 22 Class A and CISPR22 Class B standards in an unshielded environment.

8.4 Device Functional Modes

表 8-1 shows the functional modes for the device.

表 8-1. Function Table

V_{CCI} (1)	V_{CCO}	INPUT (INx)	REFRESH ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	L	H	Normal Operation: A channel output assumes the logic state of its input.
		L	L	L	
		X	H	Undetermined	The device needs an input signal transition to validate the output tracks the input state. Without a signal edge transition, the output will be in an undetermined state.
PD	PU	X	L	Default	When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for the device without the F suffix and *Low* for device with the F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
			H	Undetermined	When V_{CCI} is unpowered, a channel output assumes the logic state based on the previous state of the output before V_{CCI} powered down.
X	PD	X	L	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined.(2) When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.
			H	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined.(2) When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the selected default option.
X	X	X	Open	Undetermined	When ENx is unconnected or open, the device output will be in an undetermined and unknown state. ENx must be connected high or low for the device to behave correctly.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geqslant 1.54$ V); PD = Powered down ($V_{CC} \leqslant 1.54$); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance.

(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

8.4.1 Device I/O Schematics

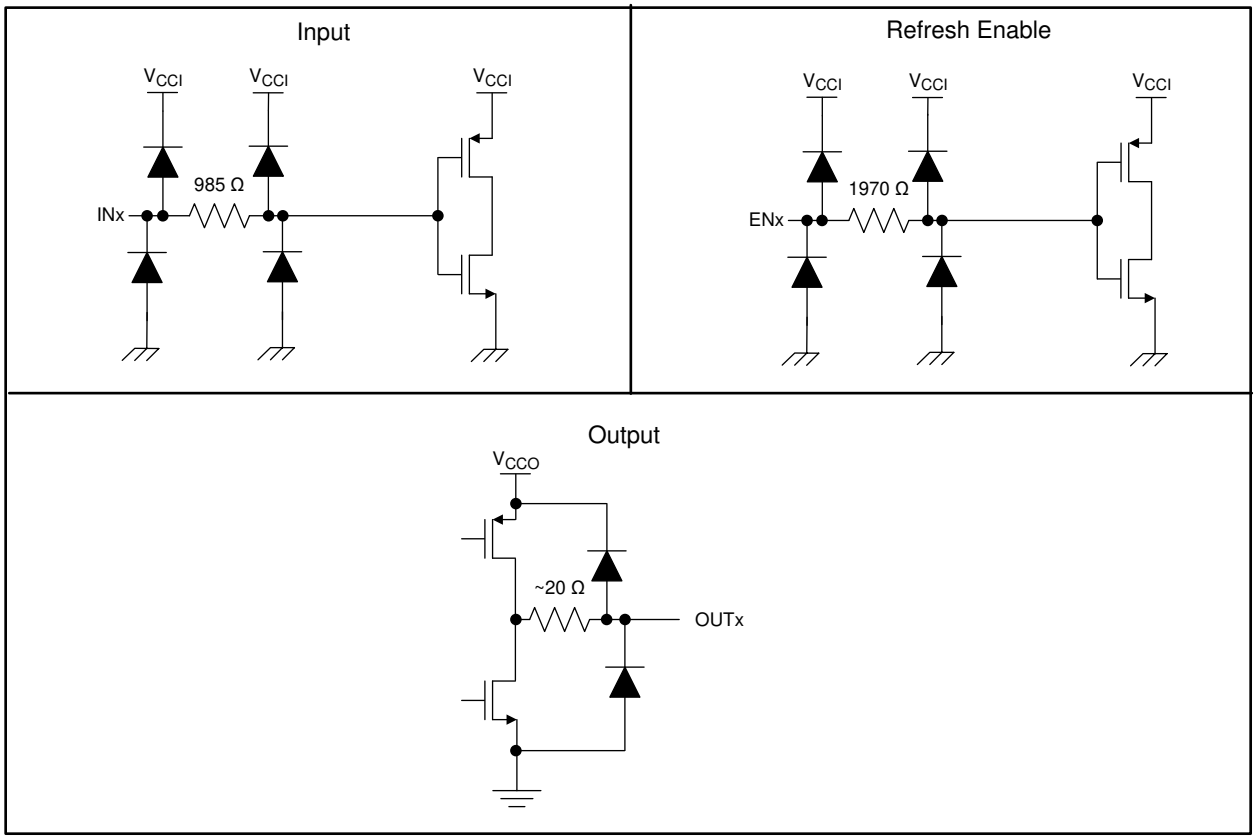


图 8-2. Device I/O Schematics

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7041-Q1 device is an ultra-low power digital isolator. The device uses single-ended CMOS-logic switching technology. The voltage range is from 3.0 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}, and can be set irrespective of one another. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard. See *Isolated power and data interface for low-power applications reference design* TI Design for detailed information on designing the ISO70xx in low-power applications.

9.1.1 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see 图 9-1 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm) and a minimum insulation lifetime of 20 years. VDE standard also requires additional safety margin of 20% for working voltage and 87.5% for insulation lifetime which translates into minimum required life time of 37.5 years.

图 9-2 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of these devices is 400 VRMS with a lifetime of >100 years. Other factors, such as package size, pollution degree, material group, and so forth can further limit the working voltage of the component. The working voltage of the DBQ-16 package specified up to 400 VRMS. At the lower working voltages, the corresponding insulation barrier life time is much longer.

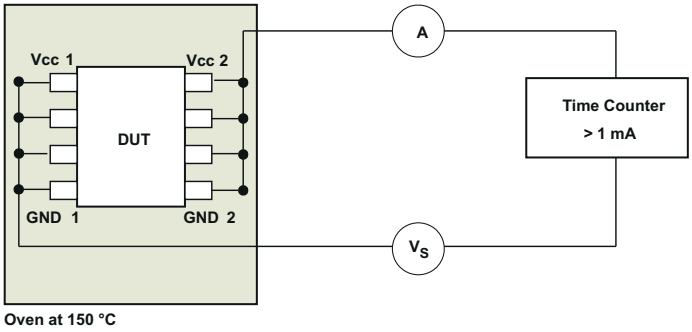


图 9-1. Test Setup for Insulation Lifetime Measurement

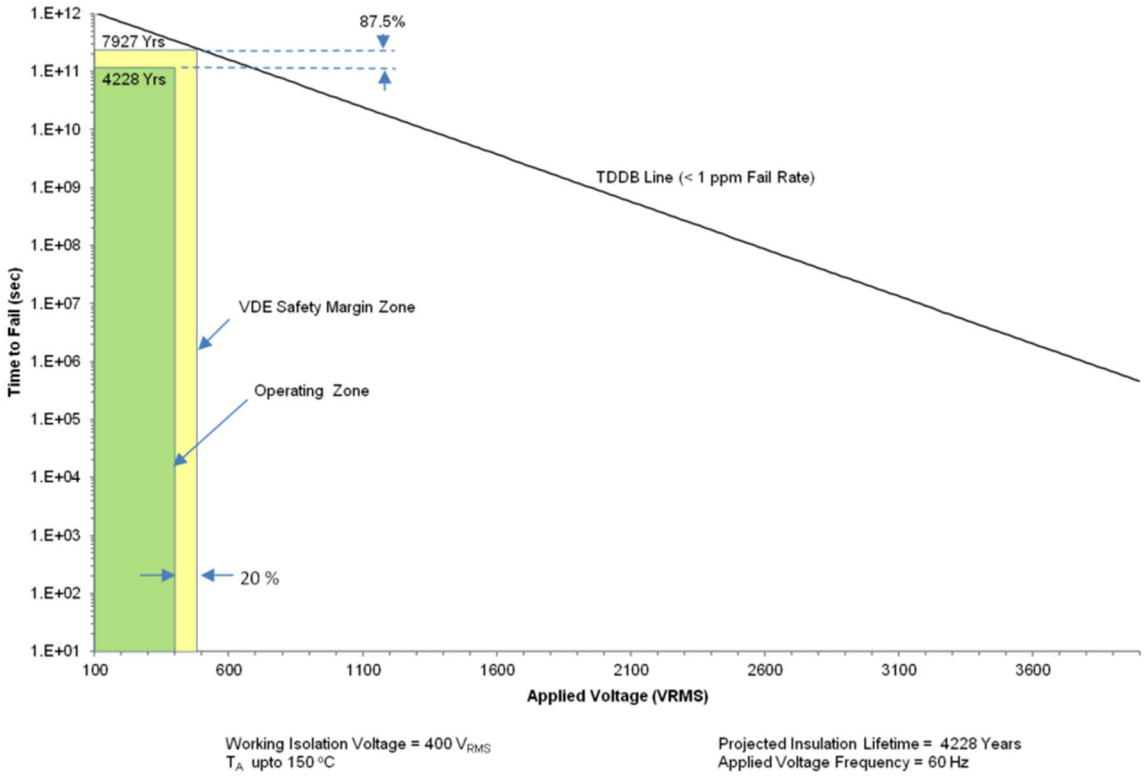


图 9-2. Insulation Lifetime Projection Data

9.2 Typical Application

Isolated UART for an Automotive Battery Management System shows the isolated UART and GPIO (NFAULT) interface.

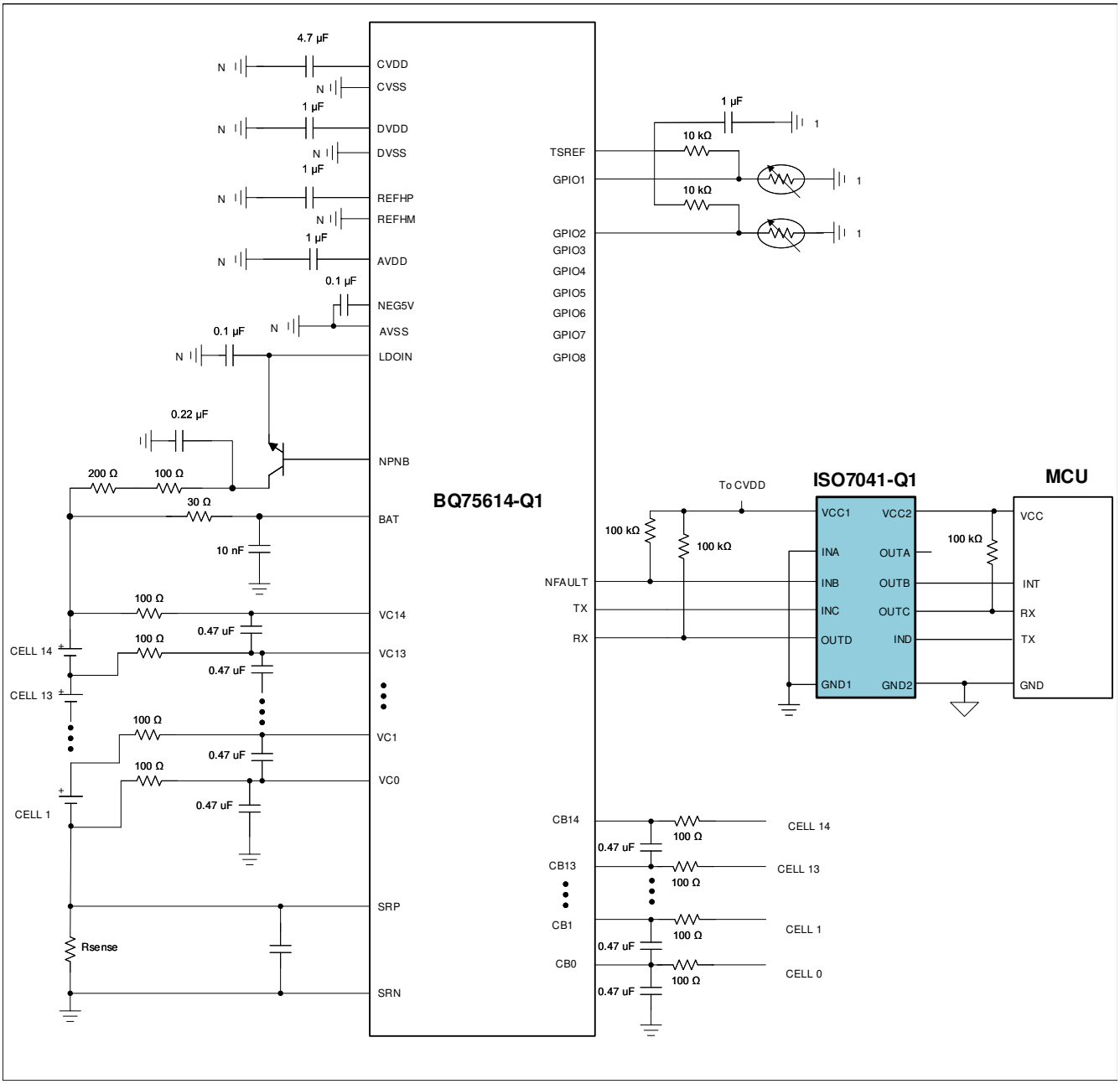


图 9-3. Isolated UART for an Automotive Battery Management System

9.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	3.0 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the device only require two external bypass capacitors to operate.

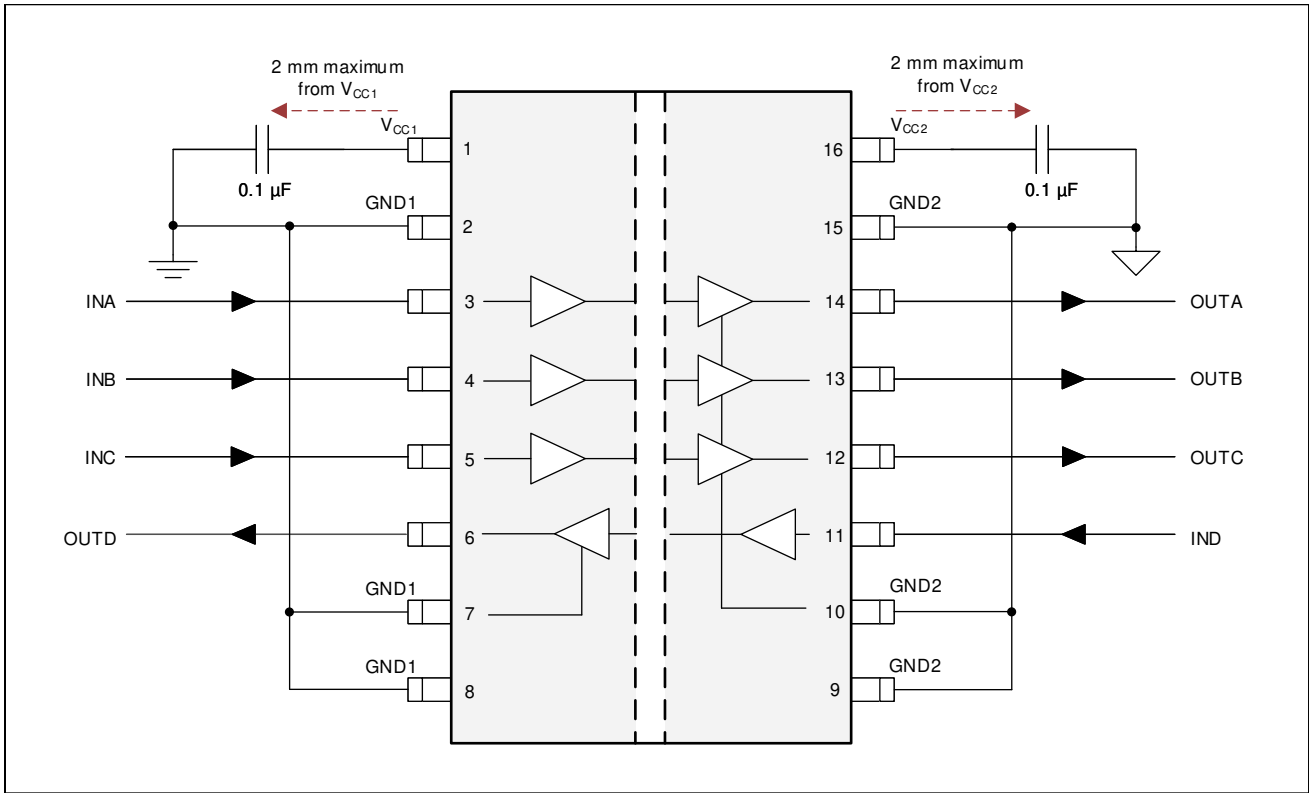


图 9-4. Typical ISO7041-Q1 Circuit Hook-up

9.2.3 Application Curves

The following typical eye diagrams of the device indicates wide open eye at the maximum data rate of 4 Mbps.

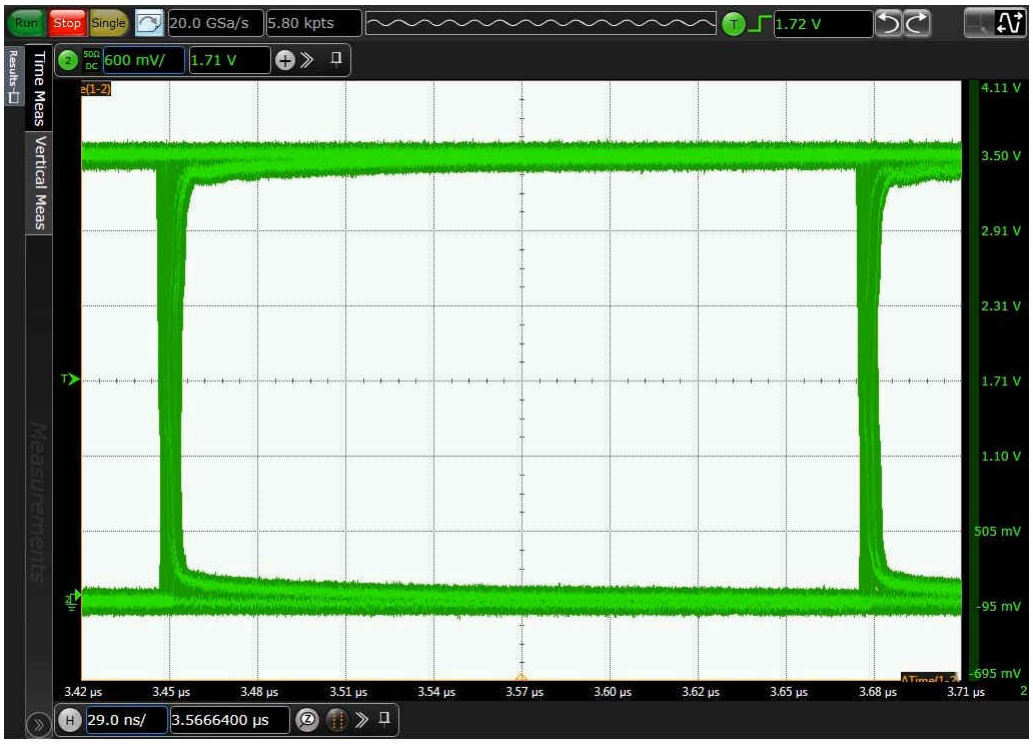


图 9-5. Eye Diagram at 4 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

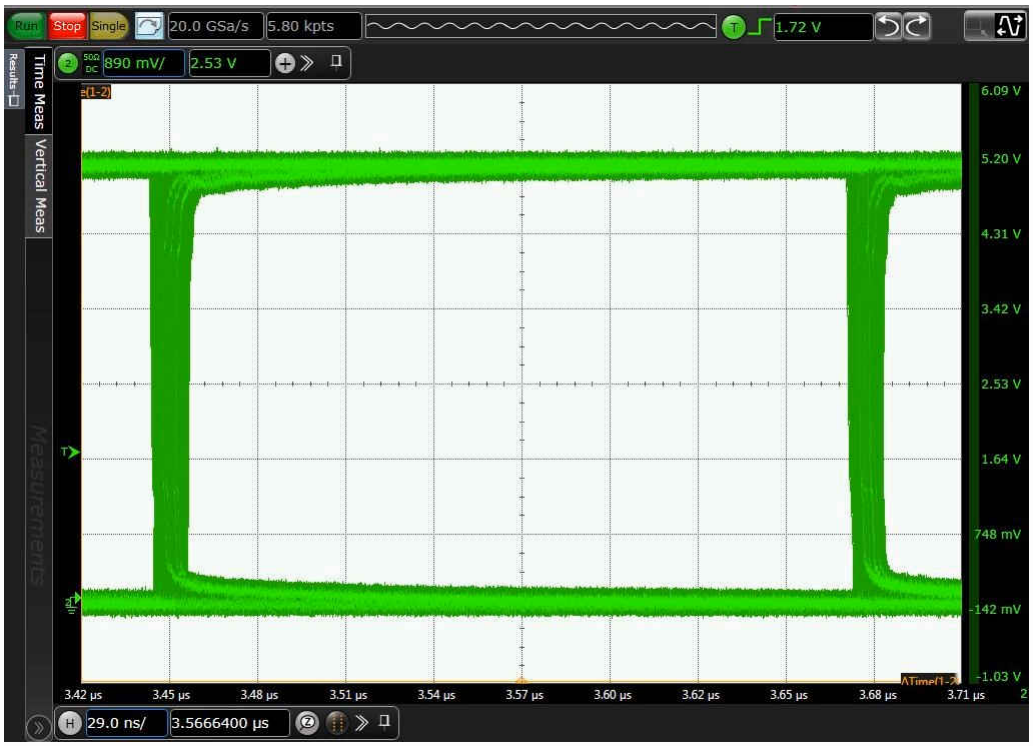


图 9-6. Eye Diagram at 4 Mbps PRBS 2^{16} – 1, 5 V and 25°C

10 Power Supply Recommendations

Put a 0.1-μF bypass capacitor at the input and output supply pins (V_{CC1} and V_{CC2}) to make sure that operation is reliable at data rates and supply voltage. Put the capacitors as near to the supply pins as possible. If only one primary-side power supply is available in an application, use a transformer driver to help generate the isolated power for the secondary-side. Texas Instruments recommends the SN6501 device or SN6505A device. Refer to the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet for detailed power supply design and transformer selection recommendations.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 图 11-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the *Digital Isolator Design Guide* for detailed layout recommendations,.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

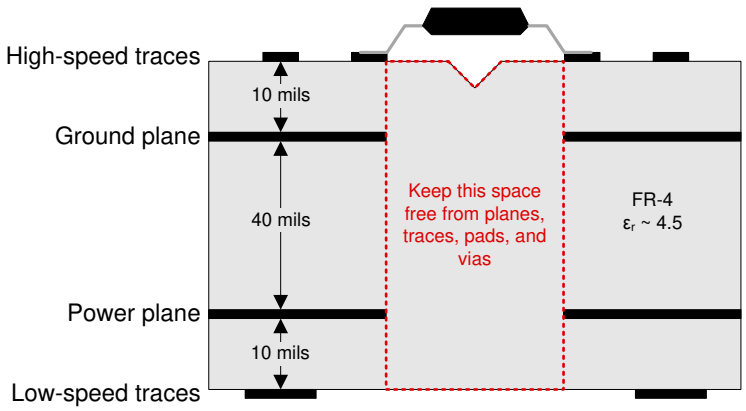


图 11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments,*BQ75614-Q1, 14-S automotive precision battery monitor, balancer and integrated protector with ASIL-D compliance*
- Texas Instruments, *Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications* TI Design
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet
- Texas Instruments, *Isolated power and data interface for low-power applications reference design* TI Design

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7041FQDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7041F
ISO7041FQDBQRQ1.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO7041QDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7041
ISO7041QDBQRQ1.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

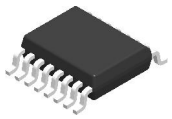
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ISO7041-Q1 :

- Catalog : ISO7041

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

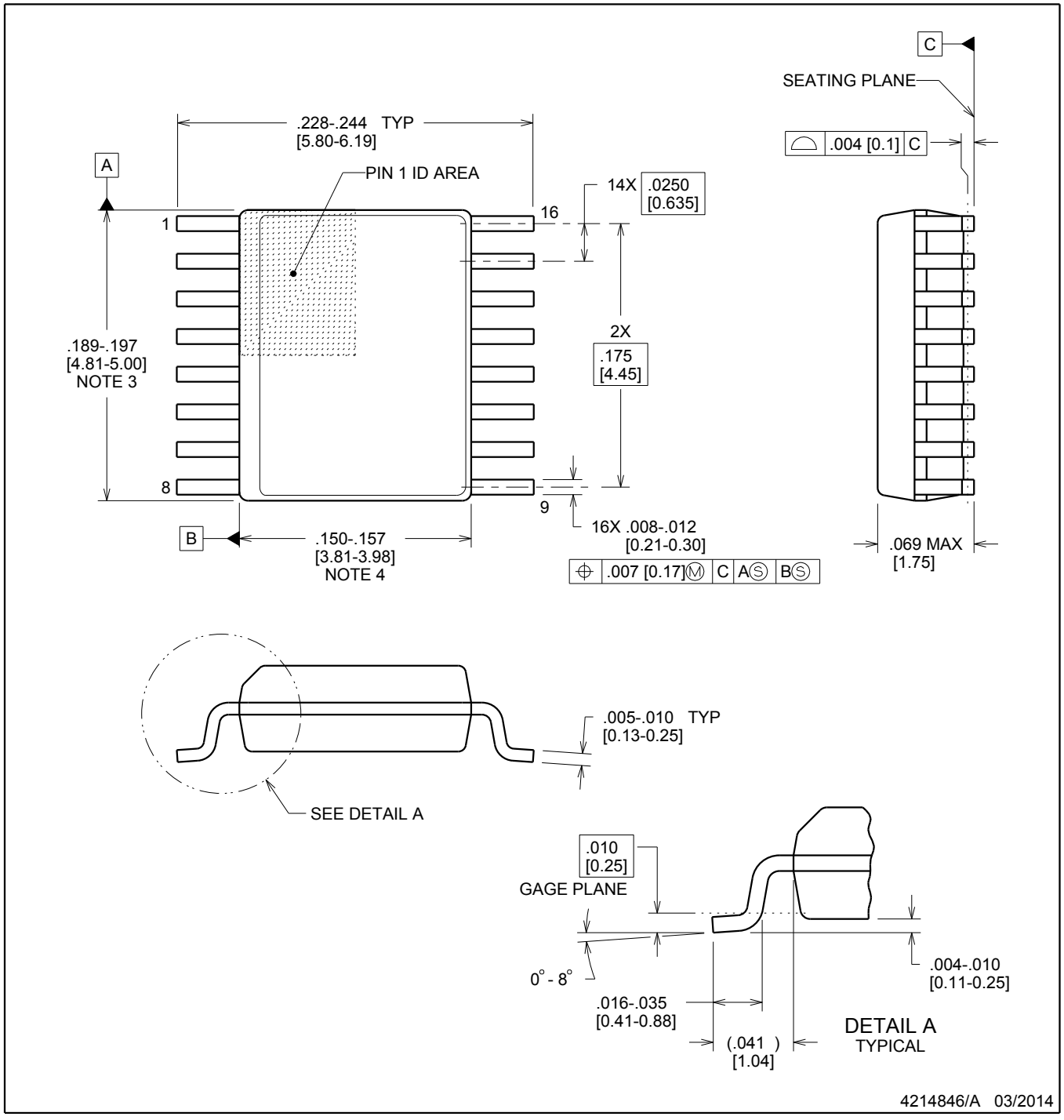


PACKAGE OUTLINE

DBQ0016A

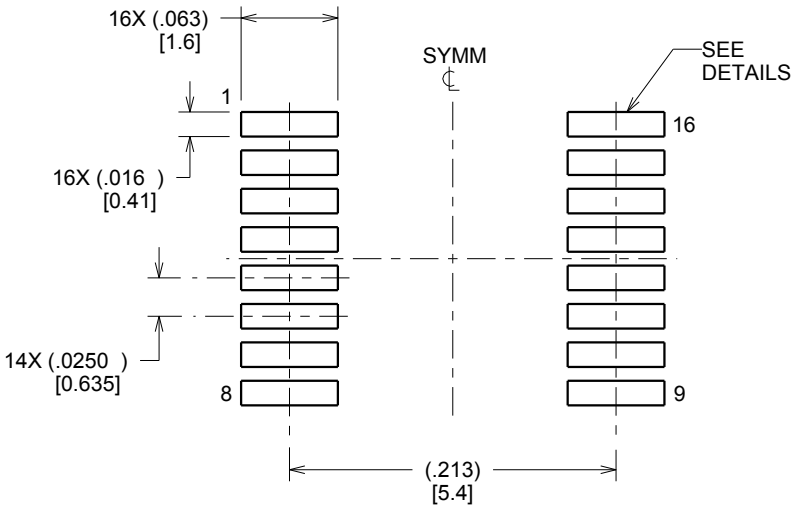
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

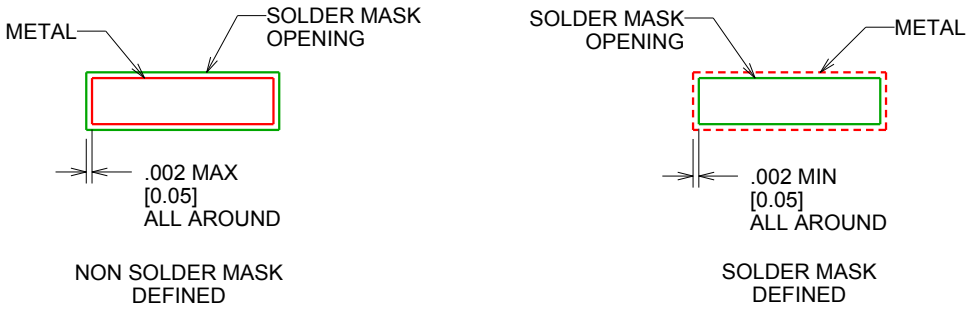


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

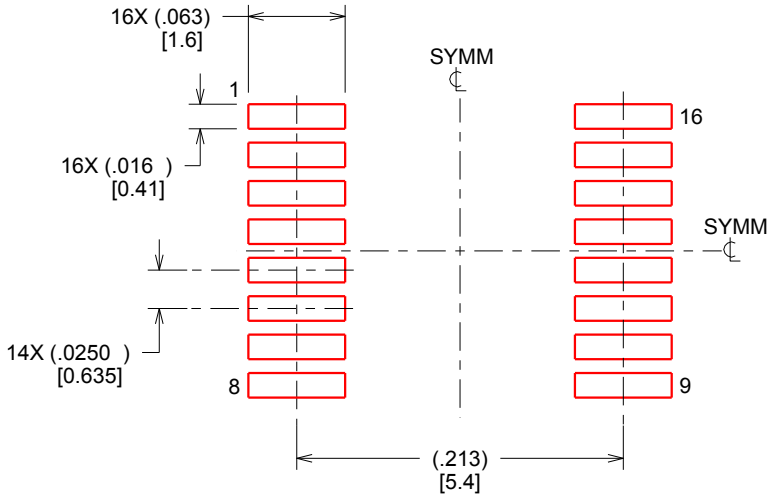
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265