

EMC 性能优异的 ISO676x-Q1 通用六通道自动增强型数字隔离器

1 特性

- 具有符合 AEC-Q100 标准的下列特性：
 - 器件温度等级 1：-40°C 至 +125°C 环境温度范围
- 满足 VDA320 隔离要求
- 50Mbps 数据速率
- 稳健可靠的隔离栅：
 - 在 1500 V_{RMS} 工作电压下具有超长的寿命
 - 隔离等级高达 5000 V_{RMS}
 - 浪涌能力高达 10kV
 - CMTI 典型值为 ±150 kV/μs
- 宽电源电压范围：1.71V 到 1.89V 和 2.25V 到 5.5V
- 1.71V 至 5.5V 电平转换
- 默认输出高电平 (ISO676x-Q1) 和低电平 (ISO676xF-Q1) 选项
- 1Mbps 时的每通道电流典型值为 1.6mA
- 低传播延迟：11ns (典型值)
- 优异的电磁兼容性 (EMC)
 - 系统级 ESD、EFT 和浪涌抗扰性
 - 低辐射
- 宽体 SOIC (DW-16) 封装
- 安全相关认证：
 - DIN EN IEC 60747-17 (VDE 0884-17)
 - UL 1577 组件认证计划
 - IEC 62368-1、IEC 61010-1、IEC 60601-1 和 GB 4943.1 认证

2 应用

- 混合动力、电动和动力总成系统 (EV/HEV)
 - 电池管理系统 (BMS)
 - 车载充电器
 - 直流/直流转换器
 - 逆变器和电机控制

3 说明

ISO676x-Q1 器件是高性能六通道数字隔离器，可提供符合 UL 1577 的 5000 V_{RMS} 隔离额定值，非常适合具有此类需求的成本敏感型应用。这些器件还通过了 VDE、TUV、CSA 和 CQC 认证。

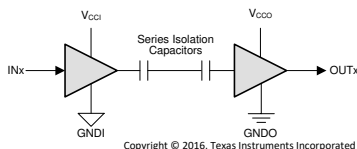
在隔离 CMOS 或者 LVCMOS 数字 I/O 的同时，ISO676x-Q1 器件可提供高电磁抗扰度和低辐射，同时具备低功耗特性。每条隔离通道的逻辑输入和输出缓冲器均由 TI 的双电容二氧化硅 (SiO₂) 绝缘栅相隔离。ISO676x 系列器件采用所有可能的引脚配置，因此所有六个通道都可以处于同一方向，或者一个、两个或三个通道处于反向，而其余通道处于正向。如果输入功率或信号出现损失，不带后缀 F 的器件默认输出高电平，带后缀 F 的器件默认输出低电平。更多详细信息，请参见器件功能模式部分。

这些器件与隔离式电源结合使用，有助于防止 CAN 和 LIN 等数据总线上的噪声电流损坏敏感电路。凭借创新型芯片设计和布线技术，ISO676x-Q1 器件的电磁兼容性得到了显著增强，可缓解系统级 ESD、EFT 和浪涌问题并符合辐射标准。ISO676x-Q1 系列器件采用 16 引脚 SOIC 宽体 (DW) 封装，是对前几代器件的引脚到引脚的升级。

器件描述

器件型号 (1)	封装	封装尺寸
ISO6760-Q1、ISO6760F-Q1、ISO6761-Q1、ISO6761F-Q1、ISO6762-Q1、ISO6762F-Q1、ISO6763-Q1、ISO6763F-Q1	SOIC (DW)	10.30mm x 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



V_{CCI} = 输入电源, V_{CCO} = 输出电源
GNDI = 输入接地, GNDO = 输出接地

简化版原理图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (May 2022) to Revision C (May 2023)	Page
• 将整个文档中的标准名称从“DIN VDE V 0884-11:2017-01”更改为“DIN EN IEC 60747-17 (VDE 0884-17)”.....	1
• 通篇更新了标记为“计划”的标准，以包含证书编号.....	1
• 通篇删除了所有标准名称中的标准版本和年份参考.....	1
• Added Maximum impulse voltage (V_{IMP}) specification per DIN EN IEC 60747-17 (VDE 0884-17).....	9
• Changed test conditions and values of Maximum surge isolation voltage (V_{IOSM}) specification per DIN EN IEC 60747-17 (VDE 0884-17).....	9
• Clarified method b test conditions of Apparent charge (q_{PD}).....	9
• Changed working voltage lifetime margin from: 87.5% to: 50%, minimum required insulation lifetime from: 37.5 years to: 30 years and insulation lifetime per TDDb from: 220 years to: 36 years per DIN EN IEC 60747-17 (VDE 0884-17).....	34
• Changed 图 9-8 per DIN EN IEC 60747-17 (VDE 0884-17).....	34
• Updated to DW0016B mechanical drawing.....	38
Changes from Revision A (November 2021) to Revision B (May 2022)	Page
• Updated CMTI spec for 5-V, 3.3-V and 2.5-V supply conditions.....	6

5 Pin Configuration and Functions

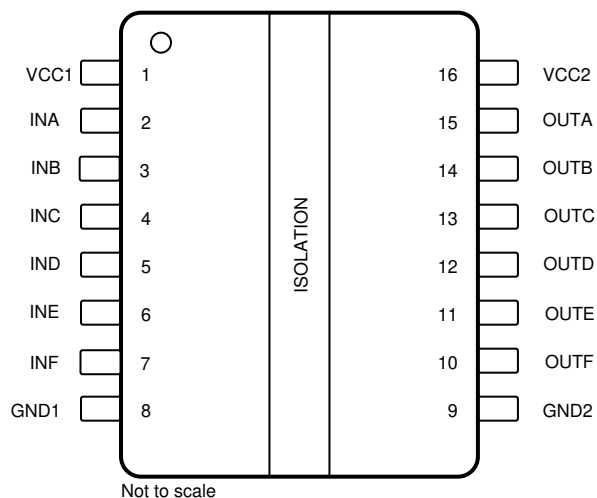


图 5-1. ISO6760-Q1 DW Package 16-Pin SOIC-WB Top View

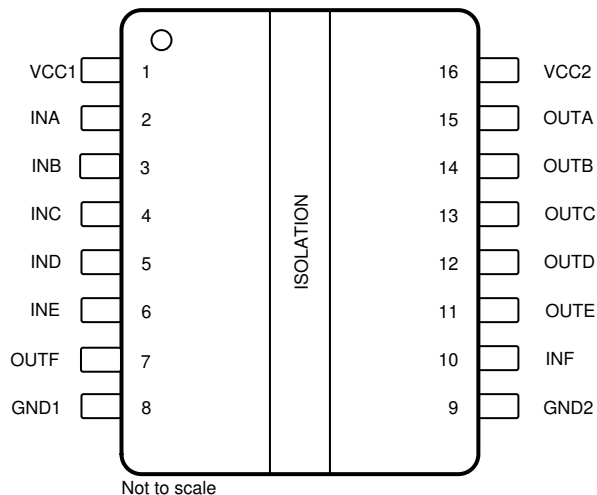


图 5-2. ISO6761-Q1 DW Package 16-Pin SOIC-WB Top View

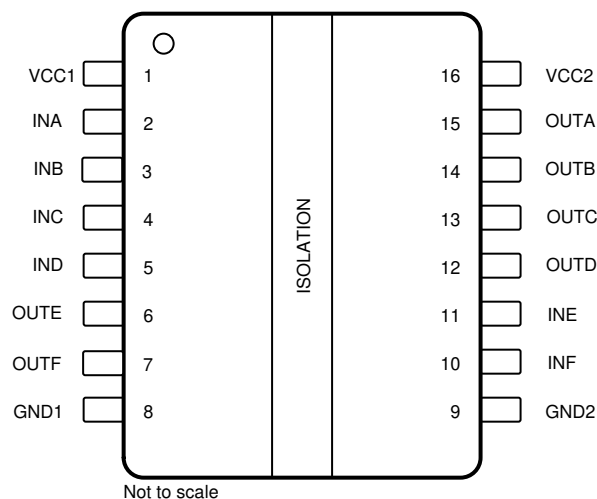


图 5-3. ISO6762-Q1 DW Package 16-Pin SOIC-WB Top View

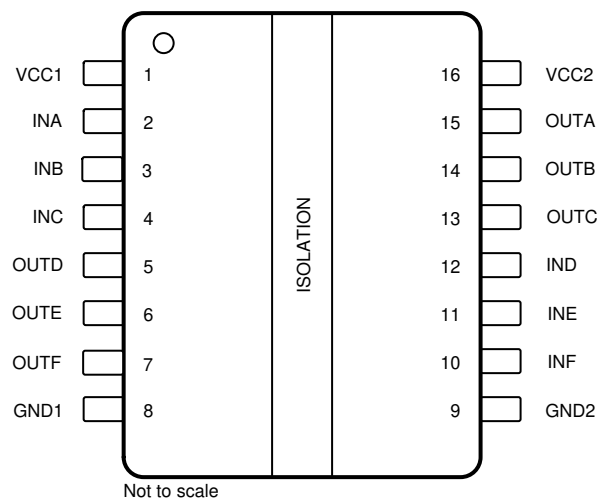


图 5-4. ISO6763-Q1 DW Package 16-Pin SOIC-WB Top View

表 5-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	NO.					
	ISO6760-Q1	ISO6761-Q1	ISO6762-Q1	ISO6763-Q1		
GND1	8	8	8	8	—	Ground connection for V _{CC1}
GND2	9	9	9	9	—	Ground connection for V _{CC2}
INA	2	2	2	2	I	Input, channel A
INB	3	3	3	3	I	Input, channel B
INC	4	4	4	4	I	Input, channel C
IND	5	5	5	12	I	Input, channel D
INE	6	6	11	11	I	Input, channel E
INF	7	10	10	10	I	Input, channel F
OUTA	15	15	15	15	O	Output, channel A
OUTB	14	14	14	14	O	Output, channel B
OUTC	13	13	13	13	O	Output, channel C
OUTD	12	12	12	5	O	Output, channel D

表 5-1. Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	NO.					
	ISO6760-Q1	ISO6761-Q1	ISO6762-Q1	ISO6763-Q1		
OUTE	11	11	6	6	O	Output, channel E
OUTF	10	7	7	7	O	Output, channel F
V _{CC1}	1	1	1	1	—	Power supply, side 1
V _{CC2}	16	16	16	16	—	Power supply, side 2

6 Specifications

6.1 Absolute Maximum Ratings

See⁽¹⁾

		MIN	MAX	UNIT
Supply Voltage ⁽²⁾	V _{CC1} to GND1	-0.5	6	V
	V _{CC2} to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	V _{CCX} + 0.5 ⁽³⁾	V
	OUTx to GNDx	-0.5	V _{CCX} + 0.5 ⁽³⁾	
Output Current	I _o	-15	15	mA
Temperature	Operating junction temperature, T _J		150	°C
	Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- (3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

(1) (2)

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$V_{CC1}^{(1)}$	Supply Voltage Side 1	$V_{CC} = 1.8V^{(3)}$	1.71		1.89	V
		$V_{CC} = 2.5V \text{ to } 5V^{(3)}$	2.25		5.5	V
$V_{CC2}^{(1)}$	Supply Voltage Side 2	$V_{CC} = 1.8V^{(3)}$	1.71		1.89	V
		$V_{CC} = 2.5V \text{ to } 5V^{(3)}$	2.25		5.5	V
$V_{cc(UVLO+)}$	UVLO threshold when supply voltage is rising			1.53	1.71	V
$V_{cc(UVLO-)}$	UVLO threshold when supply voltage is falling		1.1	1.41		V
$V_{hys(UVLO)}$	Supply voltage UVLO hysteresis		0.08	0.13		V
V_{IH}	High level Input voltage		$0.7 \times V_{CCI}^{(2)}$		V_{CCI}	V
V_{IL}	Low level Input voltage		0	$0.3 \times V_{CCI}$		V
I_{OH}	High level output current	$V_{CCO}^{(2)} = 5V$	-4			mA
		$V_{CCO} = 3.3V$	-2			mA
		$V_{CCO} = 2.5V$	-1			mA
		$V_{CCO} = 1.8V$	-1			mA
I_{OL}	Low level output current	$V_{CCO} = 5V$			4	mA
		$V_{CCO} = 3.3V$			2	mA
		$V_{CCO} = 2.5V$			1	mA
		$V_{CCO} = 1.8V$			1	mA
DR	Data Rate		0		50	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another

(2) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(3) The channel outputs are in undetermined state when $1.89V < V_{CC1}$, $V_{CC2} < 2.25V$ and $1.05V < V_{CC1}$, $V_{CC2} < 1.71V$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO676x	UNIT
		DW (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6760						
P _D	Maximum power dissipation (both sides)	V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 25-MHz 50% duty cycle square wave			192	mW
P _{D1}	Maximum power dissipation (side-1)				45	mW
P _{D2}	Maximum power dissipation (side-2)				147	mW
ISO6761						
P _D	Maximum power dissipation (both sides)	V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 25-MHz 50% duty cycle square wave			197	mW
P _{D1}	Maximum power dissipation (side-1)				63	mW
P _{D2}	Maximum power dissipation (side-2)				134	mW
ISO6762						
P _D	Maximum power dissipation (both sides)	V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 25-MHz 50% duty cycle square wave			197	mW
P _{D1}	Maximum power dissipation (side-1)				81	mW
P _{D2}	Maximum power dissipation (side-2)				116	mW
ISO6763						
P _D	Maximum power dissipation (both sides)	V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 25-MHz 50% duty cycle square wave			196	mW
P _{D1}	Maximum power dissipation (side-1)				98	mW
P _{D2}	Maximum power dissipation (side-2)				98	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDb) Test; See 图 9-8	1500	V _{RMS}
		DC voltage	2121	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 x V _{IOTM} , t= 1 s (100% production)	7071	V _{PK}
V _{IMP}	Maximum impulse voltage ⁽³⁾	Tested in air, 1.2/50-us waveform per IEC 62368-1	7692	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽⁴⁾	V _{IOSM} ≥ 1.3 x V _{IMP} ; Tested in oil (qualification test), 1.2/50- μ s waveform per IEC 62368-1	10000	V _{PK}
q _{pd}	Apparent charge ⁽⁵⁾	Method a, After Input-output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 x V _{IORM} , t _m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 x V _{IORM} , t _m = 10 s	≤5	
		Method b: At routine test (100% production) and preconditioning (type test); V _{ini} = 1.2 x V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 x V _{IORM} , t _m = 1 s (method b1) or V _{pd(m)} = V _{ini} , t _m = t _{ini} (method b2)	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁶⁾	V _{IO} = 0.4 x sin (2 π ft), f = 1 MHz	~1	pF
R _{IO}	Isolation resistance ⁽⁶⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 x V _{ISO} , t = 1 s (100% production)	5000	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).

- (6) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 7071 V _{PK} ; Maximum repetitive peak isolation voltage, 2121 V _{PK} ; Maximum surge isolation voltage, 10000 V _{PK}	600 V _{RMS} reinforced insulation per CSA 62368-1 and IEC 62368-1; 600 V _{RMS} reinforced insulation per CSA 61010-1 and IEC 61010-1 (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V _{RMS} max working voltage	Single protection, 5000 V _{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V _{RMS} maximum working voltage	5000 V _{RMS} reinforced insulation per EN 61010-1 and EN 62368-1 up to working voltage of 600 V _{RMS}
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC21001304083	Client ID number: 077311

6.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I _S	Safety input, output, or supply current ⁽¹⁾	R _{θJA} = 68.8°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C			330	mA
		R _{θJA} = 68.8°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C			504	mA
		R _{θJA} = 68.8°C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C			660	mA
		R _{θJA} = 68.8°C/W, V _I = 1.89 V, T _J = 150°C, T _A = 25°C			956	mA
P _S	Safety input, output, or total power ⁽¹⁾	R _{θJA} = 68.8°C/W, T _J = 150°C, T _A = 25°C			1820	mW
T _S	Maximum safety temperature ⁽¹⁾				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where T_{J(max)} is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics—5-V Supply

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4 \text{ mA}$; See 图 7-1	$V_{CCO} - 0.4$		V
V_{OL}	Low-level output voltage	$I_{OL} = 4 \text{ mA}$; See 图 7-1		0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		$0.7 \times V_{CCI}^{(1)}$		V
$V_{IT-(IN)}$	Falling input switching threshold	$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx		10	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at INx	-10		μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200 \text{ V}$; See 图 7-3	100	150	$\text{kV}/\mu\text{s}$
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2 \text{ MHz}$, $V_{CC} = 5 \text{ V}$	2.8		pF

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(2) Measured from input pin to same side ground.

6.10 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6760							
Supply current - DC signal	V _I = VCC1 (ISO6760); V _I = 0 V (ISO6760 with F suffix)		I _{CC1}		2.2	2.8	mA
			I _{CC2}		3.1	5.2	
	V _I = 0 V (ISO6760); V _I = VCC1 (ISO6760 with F suffix)		I _{CC1}		8.3	11.1	
			I _{CC2}		3.4	5.7	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		5.3	7.0	
			I _{CC2}		3.7	5.9	
		10 Mbps	I _{CC1}		5.4	7.2	
			I _{CC2}		7.0	9.7	
		50 Mbps	I _{CC1}		6.3	8.1	
			I _{CC2}		21.9	26.6	
ISO6761							
Supply current - DC signal	V _I = VCC1 (ISO6761); V _I = 0 V (ISO6761 with F suffix)		I _{CC1}		2.4	3.5	mA
			I _{CC2}		3.6	5.8	
	V _I = 0 V (ISO6761); V _I = VCC1 (ISO6761 with F suffix)		I _{CC1}		7.6	10.4	
			I _{CC2}		5.0	7.6	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		5.1	7.0	
			I _{CC2}		4.6	7.0	
		10 Mbps	I _{CC1}		5.8	7.8	
			I _{CC2}		7.4	10.2	
		50 Mbps	I _{CC1}		8.9	11.4	
			I _{CC2}		20.0	24.4	
ISO6762							

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	$V_I = V_{CC1}$ (ISO6762); $V_I = 0\text{ V}$ (ISO6762 with F suffix)		I_{CC1}		2.7	4.1	mA
			I_{CC2}		3.3	5.2	
	$V_I = 0\text{ V}$ (ISO6762); $V_I = V_{CC1}$ (ISO6762 with F suffix)		I_{CC1}		6.9	9.7	
			I_{CC2}		5.6	8.3	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		5	7	
			I_{CC2}		4.7	7	
		10 Mbps	I_{CC1}		6.2	8.4	
			I_{CC2}		7	9.6	
		50 Mbps	I_{CC1}		11.7	14.6	
			I_{CC2}		17.2	21.1	
ISO6763							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO6763); $V_I = 0\text{ V}$ (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		3	4.7	mA
	$V_I = 0\text{ V}$ (ISO6763); $V_I = V_{CCI}$ (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		6.3	9	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		4.8	7	
		10 Mbps	I_{CC1}, I_{CC2}		6.6	9	
		50 Mbps	I_{CC1}, I_{CC2}		14.4	17.8	

6.11 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC0} - 0.2$			V
V_{OL}	Low-level output voltage	0.2			V
$V_{IT+(IN)}$	Rising input switching threshold	$0.7 \times V_{CCI}^{(1)}$			V
$V_{IT-(IN)}$	Falling input switching threshold	$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10 μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at INx			-10 μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V, $V_{CM} = 1200 \text{ V}$; See 图 7-3			100 150 kV/ μs
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2 \text{ MHz}$, $V_{CC} = 3.3 \text{ V}$			2.8 pF

(1) $V_{CCI} = \text{Input-side } V_{CC}$; $V_{CC0} = \text{Output-side } V_{CC}$

(2) Measured from input pin to same side ground.

6.12 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6760							
Supply current - DC signal	V _I = VCC1 (ISO6760); V _I = 0 V (ISO6760 with F suffix)		I _{CC1}		2.2	2.8	mA
			I _{CC2}		3.1	5.1	
	V _I = 0 V (ISO6760); V _I = VCC1 (ISO6760 with F suffix)		I _{CC1}		8.3	10.9	
			I _{CC2}		3.4	5.6	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		5.3	6.9	
			I _{CC2}		3.5	5.7	
		10 Mbps	I _{CC1}		5.3	7	
			I _{CC2}		5.9	8.5	
		50 Mbps	I _{CC1}		5.9	7.6	
			I _{CC2}		16.6	20.9	
ISO6761							
Supply current - DC signal	V _I = VCC1 (ISO6761); V _I = 0 V (ISO6761 with F suffix)		I _{CC1}		2.4	3.5	mA
			I _{CC2}		3.6	5.8	
	V _I = 0 V (ISO6761); V _I = VCC1 (ISO6761 with F suffix)		I _{CC1}		7.5	10.3	
			I _{CC2}		4.9	7.5	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		5	7	
			I _{CC2}		4.5	6.9	
		10 Mbps	I _{CC1}		5.5	7.5	
			I _{CC2}		6.5	9.2	
		50 Mbps	I _{CC1}		7.7	10	
			I _{CC2}		15.5	19.6	
ISO6762							

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	$V_I = V_{CC1}$ (ISO6762); $V_I = 0\text{ V}$ (ISO6762 with F suffix)		I_{CC1}		2.7	4.1	mA
			I_{CC2}		3.3	5.2	
	$V_I = 0\text{ V}$ (ISO6762); $V_I = V_{CC1}$ (ISO6762 with F suffix)		I_{CC1}		6.9	9.6	
			I_{CC2}		5.6	8.2	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		4.9	6.9	
			I_{CC2}		4.6	6.9	
		10 Mbps	I_{CC1}		5.7	7.9	
			I_{CC2}		6.2	8.8	
		50 Mbps	I_{CC1}		9.6	12.4	
			I_{CC2}		13.5	17.1	
ISO6763							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO6763); $V_I = 0\text{ V}$ (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		3	4.6	mA
	$V_I = 0\text{ V}$ (ISO6763); $V_I = V_{CCI}$ (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		6.2	8.9	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		4.8	6.9	
		10 Mbps	I_{CC1}, I_{CC2}		6	8.4	
		50 Mbps	I_{CC1}, I_{CC2}		11.6	14.7	

6.13 Electrical Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1 \text{ mA}$; See 图 7-1		$V_{CCO} - 0.1$	V
V_{OL}	Low-level output voltage	$I_{OL} = 1 \text{ mA}$; See 图 7-1		0.1	V
$V_{IT+(IN)}$	Rising input switching threshold		$0.7 \times V_{CCI}$ (1)		V
$V_{IT-(IN)}$	Falling input switching threshold	$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ (1) at INx		10	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at INx	-10		μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200 \text{ V}$; See 图 7-3	100	150	kV/ μs
C_i	Input Capacitance (2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2 \text{ MHz}$, $V_{CC} = 2.5 \text{ V}$	2.8		pF

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(2) Measured from input pin to same side ground.

6.14 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6760							
Supply current - DC signal	$V_I = V_{CC1}$ (ISO6760); $V_I = 0\text{ V}$ (ISO6760 with F suffix)		I_{CC1}		2.2	2.8	mA
			I_{CC2}		3.1	5.1	
	$V_I = 0\text{ V}$ (ISO6760); $V_I = V_{CC1}$ (ISO6760 with F suffix)		I_{CC1}		8.3	10.8	
			I_{CC2}		3.4	5.6	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		5.2	6.8	
			I_{CC2}		3.5	5.6	
		10 Mbps	I_{CC1}		5.3	6.9	
			I_{CC2}		5.3	7.7	
		50 Mbps	I_{CC1}		5.7	7.5	
			I_{CC2}		13.2	16.9	
ISO6761							
Supply current - DC signal	$V_I = V_{CC1}$ (ISO6761); $V_I = 0\text{ V}$ (ISO6761 with F suffix)		I_{CC1}		2.4	3.5	mA
			I_{CC2}		3.6	5.7	
	$V_I = 0\text{ V}$ (ISO6761); $V_I = V_{CC1}$ (ISO6761 with F suffix)		I_{CC1}		7.5	10.3	
			I_{CC2}		4.9	7.5	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		5	6.9	
			I_{CC2}		4.4	6.8	
		10 Mbps	I_{CC1}		5.3	7.3	
			I_{CC2}		5.9	8.5	
		50 Mbps	I_{CC1}		7	9.3	
			I_{CC2}		12.7	16.3	
ISO6762							

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V _I = VCC1 (ISO6762); V _I = 0 V (ISO6762 with F suffix)		I _{CC1}		2.7	4	mA
			I _{CC2}		3.3	5.2	
	V _I = 0 V (ISO6762); V _I = VCC1 (ISO6762 with F suffix)		I _{CC1}		6.9	9.6	
			I _{CC2}		5.6	8.2	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		4.9	6.9	
			I _{CC2}		4.6	6.8	
		10 Mbps	I _{CC1}		5.5	7.6	
			I _{CC2}		5.8	8.2	
		50 Mbps	I _{CC1}		8.4	11	
			I _{CC2}		11.2	14.5	
ISO6763							
Supply current - DC signal	V _I = V _{CCI} (ISO6763); V _I = 0 V (ISO6763 with F suffix)		I _{CC1} , I _{CC2}		3	4.6	mA
	V _I = 0 V (ISO6763); V _I = V _{CCI} (ISO6763 with F suffix)		I _{CC1} , I _{CC2}		6.2	8.9	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1} , I _{CC2}		4.7	6.9	
		10 Mbps	I _{CC1} , I _{CC2}		5.6	7.9	
		50 Mbps	I _{CC1} , I _{CC2}		9.8	12.7	

6.15 Electrical Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1\text{mA}$; See 图 7-1	$V_{CCO} - 0.1$		V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{mA}$; See 图 7-1		0.1	V
$V_{IT+(IN)}$	Rising input switching threshold		$0.7 \times V_{CCI}^{(1)}$		V
$V_{IT-(IN)}$	Falling input switching threshold	$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx		10	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at INx	-10		μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200 \text{ V}$; See 图 7-3	50	75	$\text{kV}/\mu\text{s}$
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2 \text{ MHz}$, $V_{CC} = 1.8 \text{ V}$	2.8		pF

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(2) Measured from input pin to same side ground.

6.16 Supply Current Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6760							
Supply current - DC signal	V _I = VCC1 (ISO6760); V _I = 0 V (ISO6760 with F suffix)		I _{CC1}		1.5	2.1	mA
			I _{CC2}		3	5.1	
	V _I = 0 V (ISO6760); V _I = VCC1 (ISO6760 with F suffix)		I _{CC1}		7.3	10.3	
			I _{CC2}		3.3	5.6	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		4.4	6.2	
			I _{CC2}		3.3	5.5	
		10 Mbps	I _{CC1}		4.5	6.3	
			I _{CC2}		4.6	7	
		50 Mbps	I _{CC1}		4.8	6.7	
			I _{CC2}		10.1	13	
ISO6761							
Supply current - DC signal	V _I = VCC1 (ISO6761); V _I = 0 V (ISO6761 with F suffix)		I _{CC1}		1.8	2.9	mA
			I _{CC2}		3.4	5.7	
	V _I = 0 V (ISO6761); V _I = VCC1 (ISO6761 with F suffix)		I _{CC1}		6.7	9.8	
			I _{CC2}		4.6	7.4	
Supply current - AC signal	All channels switching with square wave clock input; C _L = 15 pF	1 Mbps	I _{CC1}		4.3	6.4	
			I _{CC2}		4.1	6.7	
		10 Mbps	I _{CC1}		4.6	6.7	
			I _{CC2}		5.2	7.9	
		50 Mbps	I _{CC1}		5.8	8.1	
			I _{CC2}		9.9	13	
ISO6762							

$V_{CC1} = V_{CC2} = 1.8 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	$V_I = V_{CC1}$ (ISO6762); $V_I = 0\text{ V}$ (ISO6762 with F suffix)		I_{CC1}		2.2	3.6	mA
			I_{CC2}		3	5	
	$V_I = 0\text{ V}$ (ISO6762); $V_I = V_{CC1}$ (ISO6762 with F suffix)		I_{CC1}		6.2	9.2	
			I_{CC2}		5.1	8	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		4.3	6.5	
			I_{CC2}		4.2	6.6	
		10 Mbps	I_{CC1}		4.7	7	
			I_{CC2}		5	7.6	
		50 Mbps	I_{CC1}		6.8	9.3	
			I_{CC2}		8.9	11.8	
ISO6763							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO6763); $V_I = 0\text{ V}$ (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		2.6	4.3	mA
	$V_I = 0\text{ V}$ (ISO6763); $V_I = V_{CCI}$ (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		5.7	8.6	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		4.2	6.5	
		10 Mbps	I_{CC1}, I_{CC2}		4.9	7.3	
		50 Mbps	I_{CC1}, I_{CC2}		7.9	10.5	

6.17 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO676x						
t_{PLH}, t_{PHL}	Propagation delay time	See 图 7-1		11	18	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				7	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				6	ns
t_r	Output signal rise time	See 图 7-1			4.5	ns
t_f	Output signal fall time				4.5	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See 图 7-2		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO676x						
t_{PLH}, t_{PHL}	Propagation delay time	See 图 7-1		11	18	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				7	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				7	ns
t_r	Output signal rise time	See 图 7-1			3.2	ns
t_f	Output signal fall time				3.2	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See 图 7-2		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.19 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO676x						
t_{PLH}, t_{PHL}	Propagation delay time	See 图 7-1		12	20.5	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				7.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				7	ns
t_r	Output signal rise time	See 图 7-1			4	ns
t_f	Output signal fall time				4	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See 图 7-2		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.20 Switching Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO676x						
t_{PLH}, t_{PHL}	Propagation delay time	See 图 7-1		15	24	ns
PWD	Pulse width distortion $ t_{PHL} - t_{PLH} $				8.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽¹⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽²⁾				8.8	ns
t_r	Output signal rise time	See 图 7-1			4.7	ns
t_f	Output signal fall time				4.7	ns
t_{PU}	Time from UVLO to valid output data				300	μs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See 图 7-2		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

- (1) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.21 绝缘特性曲线

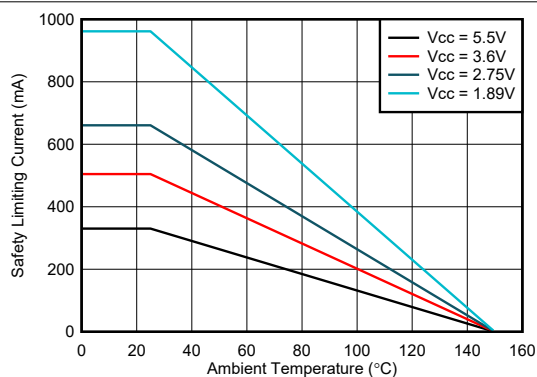


图 6-1. DW-16 封装安全限制电流的热降额曲线

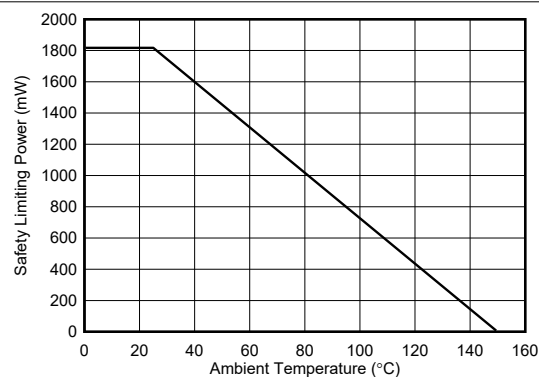


图 6-2. DW-16 封装安全限制功率的热降额曲线

6.22 Typical Characteristics

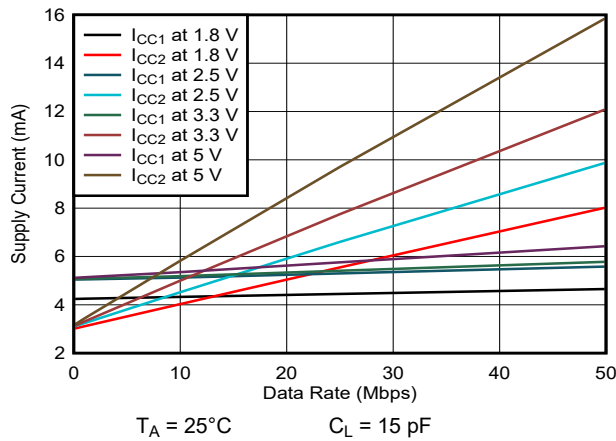


图 6-3. ISO6760-Q1 Supply Current vs Data Rate (With 15-pF Load)

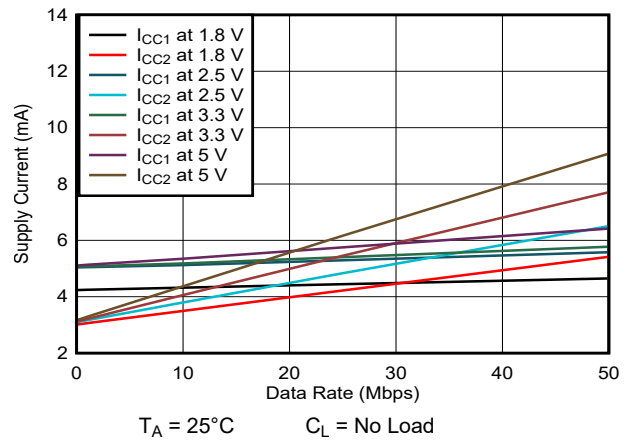


图 6-4. ISO6760-Q1 Supply Current vs Data Rate (With No Load)

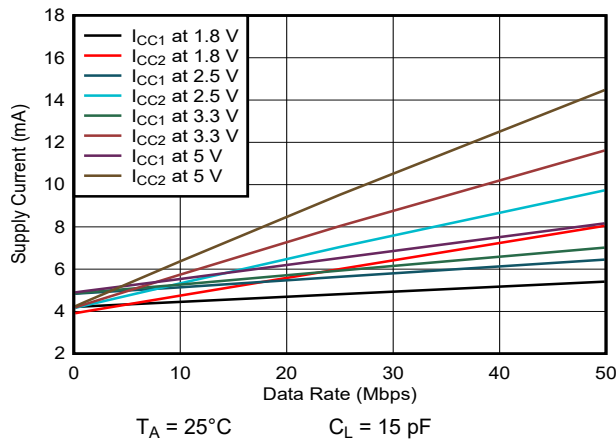


图 6-5. ISO6761-Q1 Supply Current vs Data Rate (With 15-pF Load)

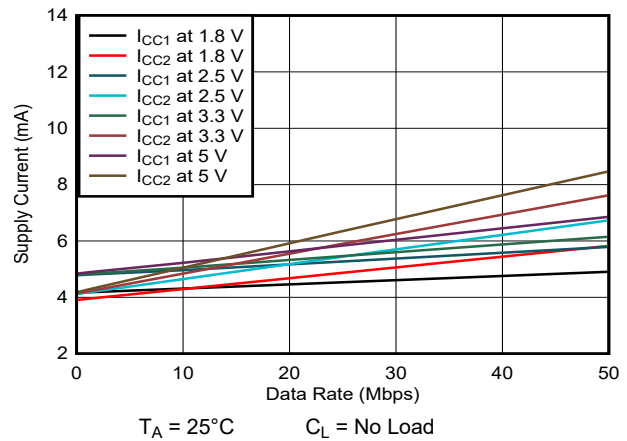


图 6-6. ISO6761-Q1 Supply Current vs Data Rate (With No Load)

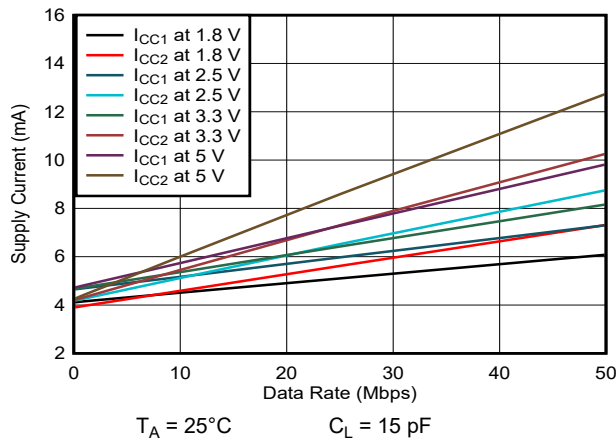


图 6-7. ISO6762-Q1 Supply Current vs Data Rate (With 15-pF Load)

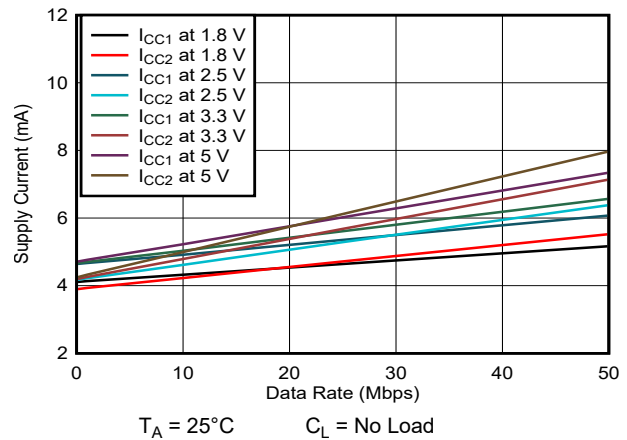


图 6-8. ISO6762-Q1 Supply Current vs Data Rate (With No Load)

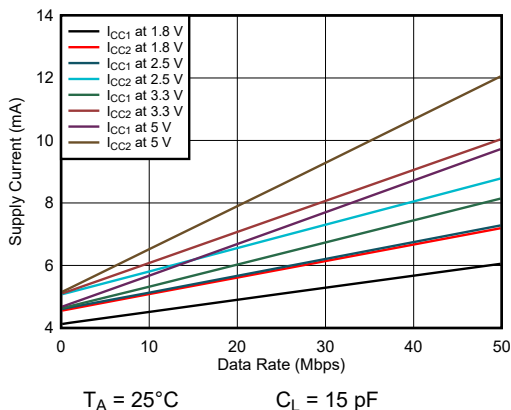


图 6-9. ISO6763-Q1 Supply Current vs Data Rate (With 15-pF Load)

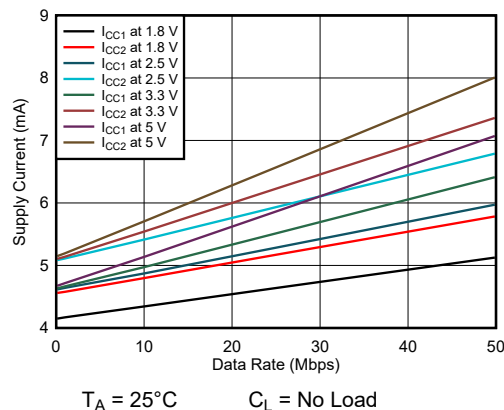


图 6-10. ISO6763-Q1 Supply Current vs Data Rate (With No Load)

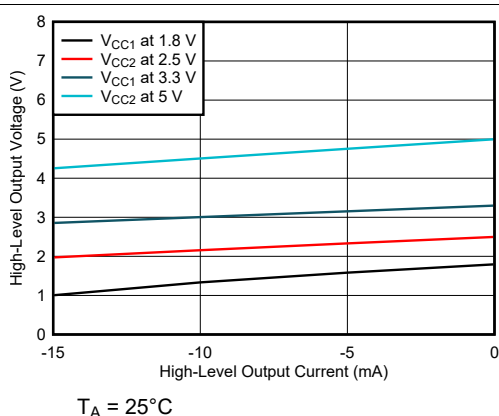


图 6-11. High-Level Output Voltage vs High-level Output Current

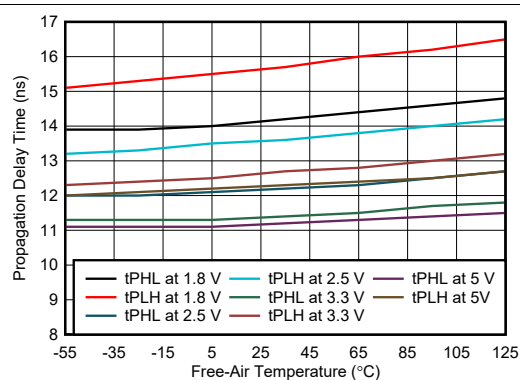


图 6-12. Propagation Delay Time vs Free-Air Temperature

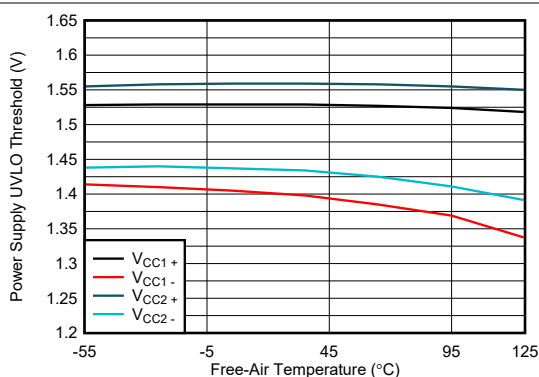


图 6-13. Power Supply Undervoltage Threshold vs Free-Air Temperature

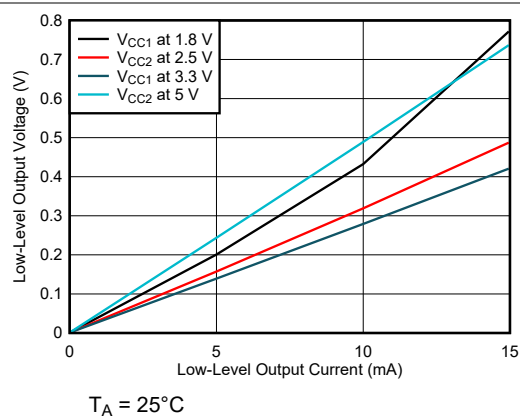
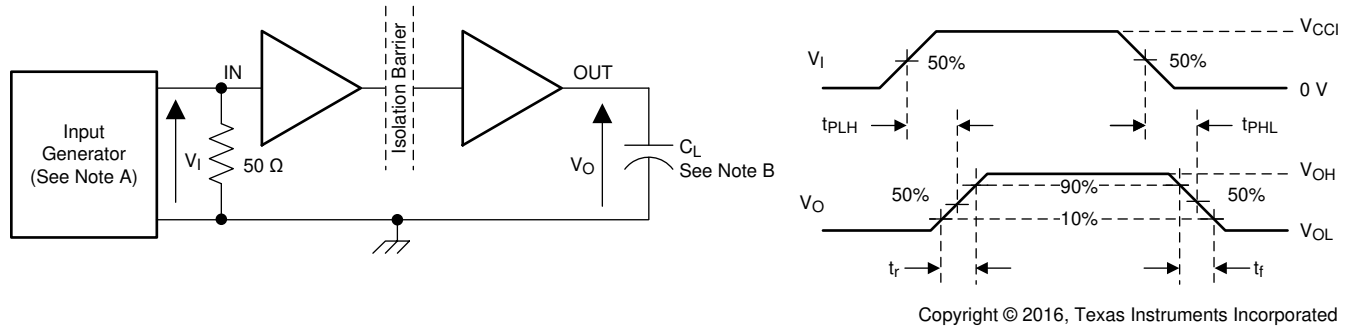


图 6-14. Low-Level Output Voltage vs Low-Level Output Current

7 Parameter Measurement Information



- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50$ kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_o = 50 \Omega$. At the input, 50Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

图 7-1. Switching Characteristics Test Circuit and Voltage Waveforms

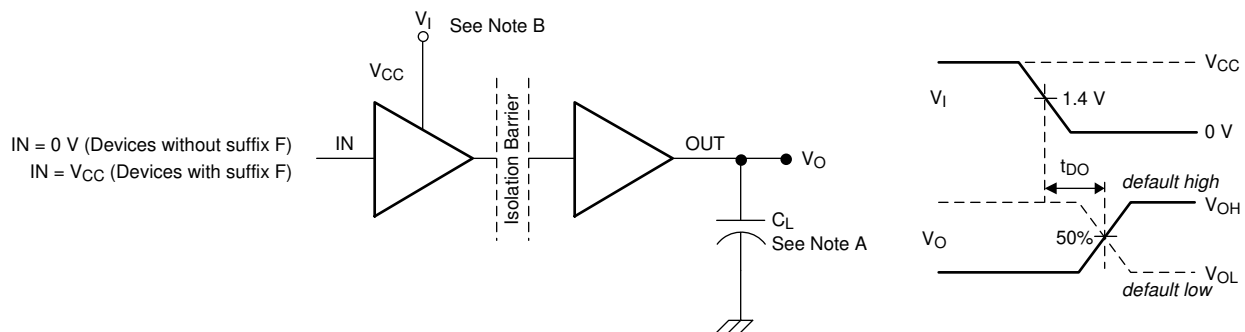
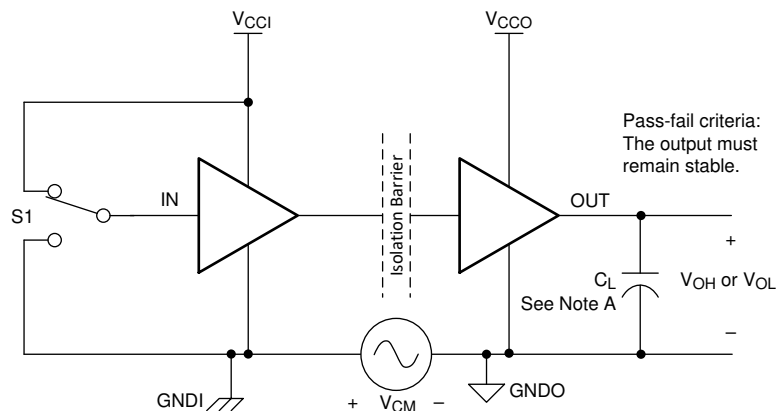


图 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. For optimized CMTI performance, a $0.1 \mu F + 1 \mu F$ decoupling capacitor should be placed close to V_{CC1} and V_{CC2} . Please see 节 11.2 for capacitor placement details. A recommended $0.1 \mu F$ capacitor is LLL185R71A104MA11L (CAP CER 0.1UF 10V X7R 0306 - LW Reversed Low ESL Chip Ceramic Capacitors) or equivalent.

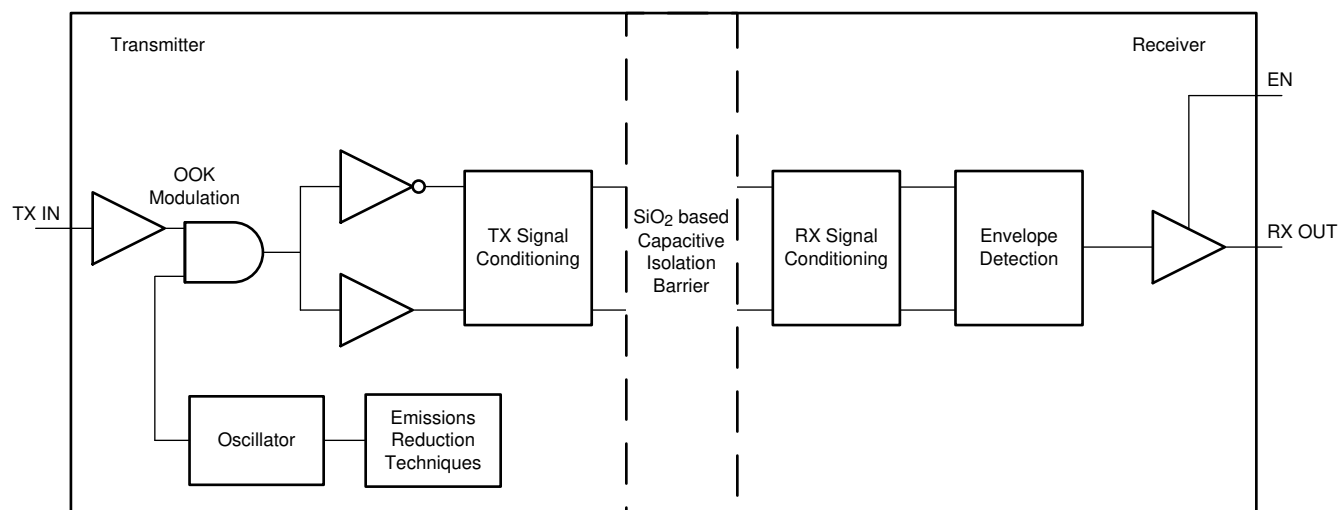
图 7-3. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO676x-Q1 family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO676x-Q1 devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 8-1](#), shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

图 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator

[Figure 8-2](#) shows a conceptual detail of how the ON-OFF keying scheme works.

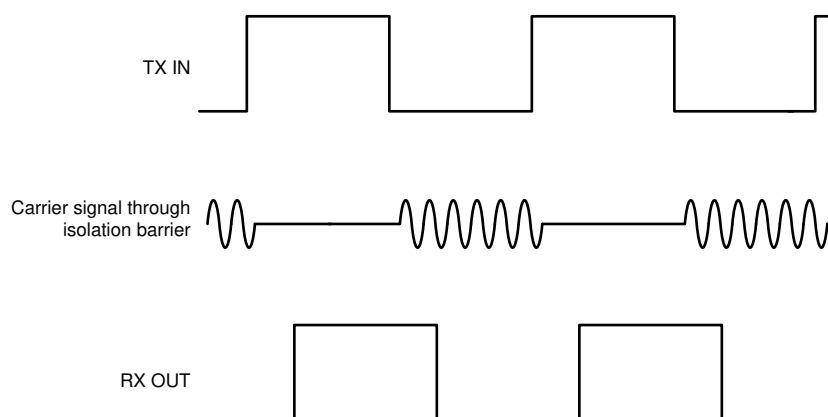


图 8-2. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

表 8-1 provides an overview of the device features.

表 8-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION ⁽¹⁾
ISO6760-Q1	6 Forward, 0 Reverse	50 Mbps	High	DW-16	5000 V _{RMS} / 7071 V _{PK}
ISO6760F-Q1	6 Forward, 0 Reverse	50 Mbps	Low	DW-16	5000 V _{RMS} / 7071 V _{PK}
ISO6761-Q1	5 Forward, 1 Reverse	50 Mbps	High	DW-16	5000 V _{RMS} / 7071 V _{PK}
ISO6761F-Q1	5 Forward, 1 Reverse	50 Mbps	Low	DW-16	5000 V _{RMS} / 7071 V _{PK}
ISO6762-Q1	4 Forward, 2 Reverse	50 Mbps	High	DW-16	5000 V _{RMS} / 7071 V _{PK}
ISO6762F-Q1	4 Forward, 2 Reverse	50 Mbps	Low	DW-16	5000 V _{RMS} / 7071 V _{PK}
ISO6763-Q1	3 Forward, 3 Reverse	50 Mbps	High	DW-16	5000 V _{RMS} / 7071 V _{PK}
ISO6763F-Q1	3 Forward, 3 Reverse	50 Mbps	Low	DW-16	5000 V _{RMS} / 7071 V _{PK}

(1) See [Safety-Related Certifications](#) for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 25. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO676x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

表 8-2 lists the functional modes for the ISO676x-Q1 devices.

表 8-2. Function Table

$V_{CCI}^{(1)}$	V_{CCO}	INPUT (INx) ⁽³⁾	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of its input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is <i>High</i> for ISO676x-Q1 and <i>Low</i> for ISO676x-Q1 with F suffix.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is <i>High</i> for ISO676x-Q1 and <i>Low</i> for ISO676x-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined ⁽²⁾ . When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} ; PU = Powered up ($V_{CC} \geq 1.71$ V); PD = Powered down ($V_{CC} \leq 1.05$ V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance

(2) The outputs are in undetermined state when 1.05 V < V_{CCI} , $V_{CCO} < 1.71$ V and 1.89 V < V_{CCI} , $V_{CCO} < 2.25$ V

(3) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output

8.4.1 Device I/O Schematics

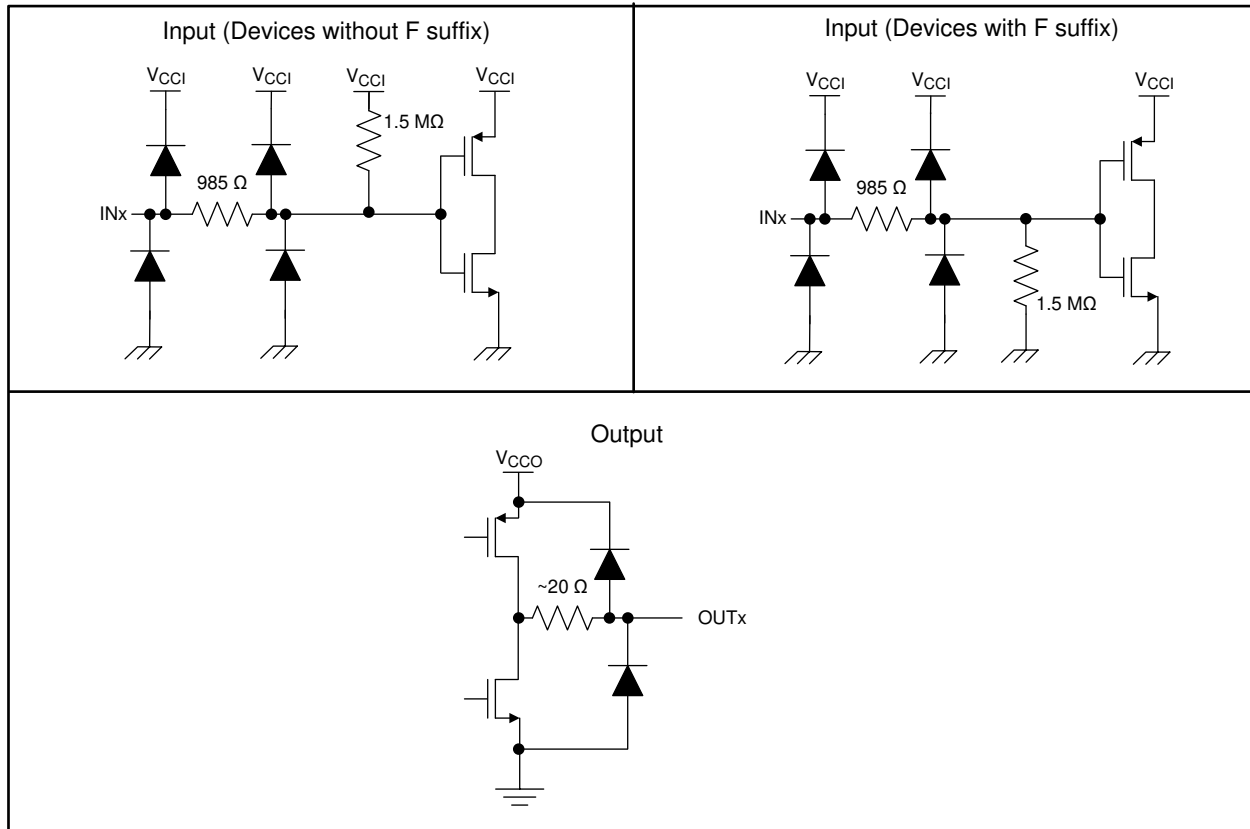


图 8-3. Device I/O Schematics

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO676x-Q1 devices are high-performance, six-channel digital isolators. The ISO676x-Q1 devices use single-ended CMOS-logic switching technology. The supply voltage range is from 1.71 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} . Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, it is possible to supply ISO676x-Q1 V_{CC1} with 3.3 V (which is within 1.71 V to 5.5 V) and V_{CC2} with 5V (which is also within 1.71 V to 5.5 V). You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

图 9-1 shows the isolated serial-peripheral interface (SPI) and controller-area network (CAN) interface implementation.

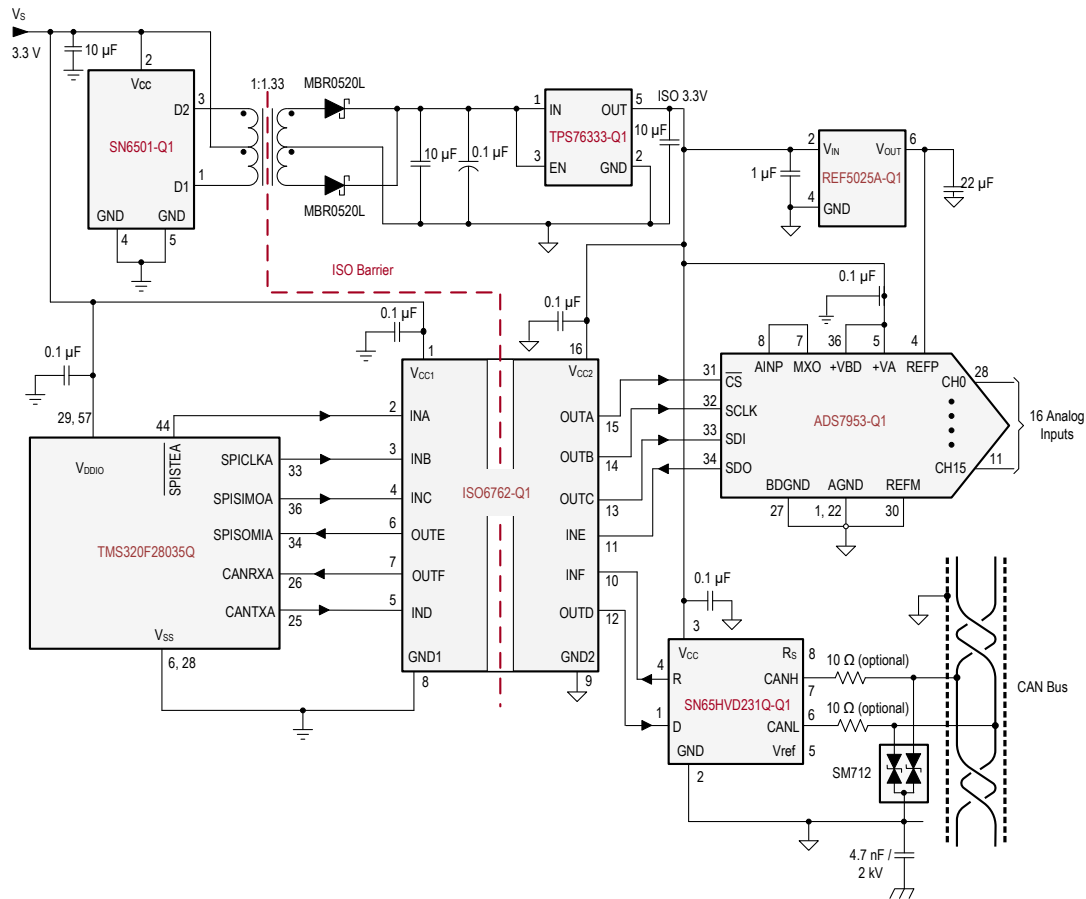


图 9-1. Isolated SPI and CAN Interface

9.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71 V to 1.89 V and 2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μ F
Decoupling capacitor from V_{CC2} and GND2	0.1 μ F

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO676x-Q1 family of devices only require two external bypass capacitors to operate.

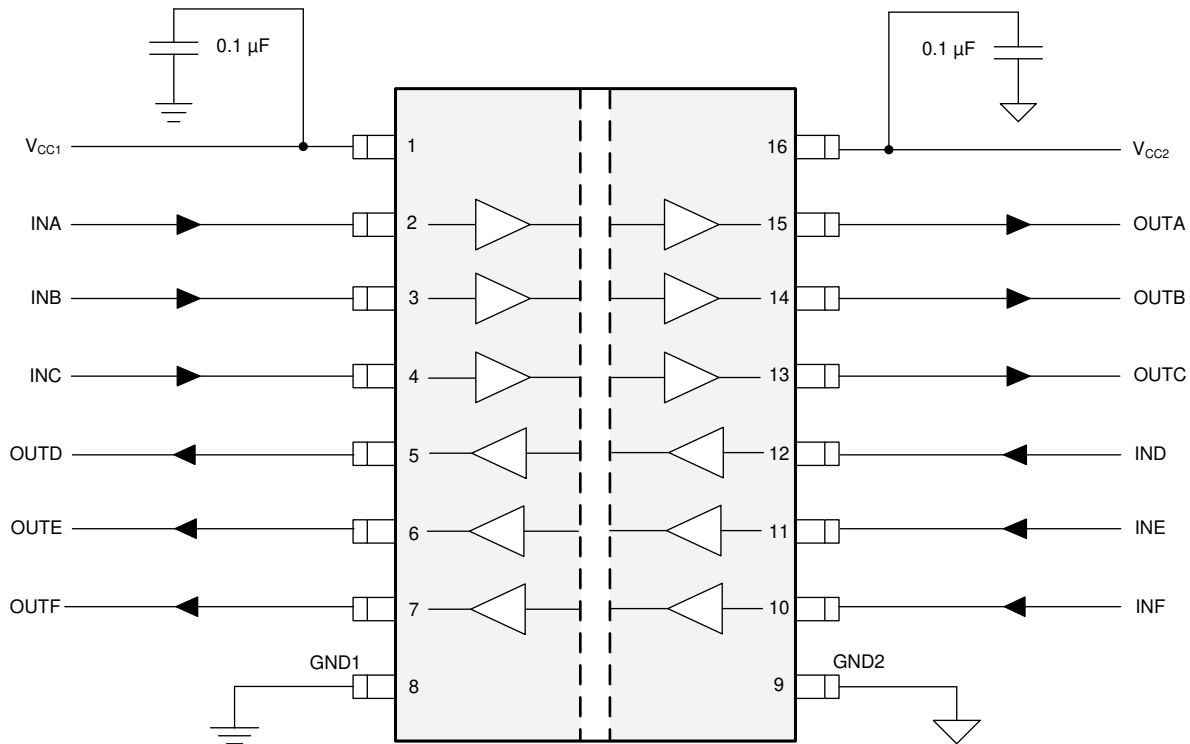


图 9-2. Typical ISO676x-Q1 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO676x-Q1 family of devices indicates low jitter and wide open eye at the maximum data rate of 50 Mbps.

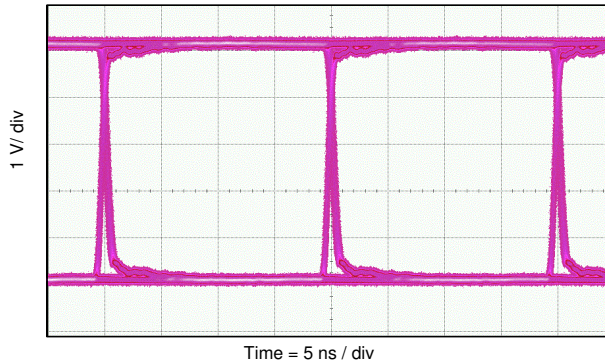


图 9-3. Eye Diagram at 50 Mbps PRBS 2¹⁶ - 1, 5 V and 25°C

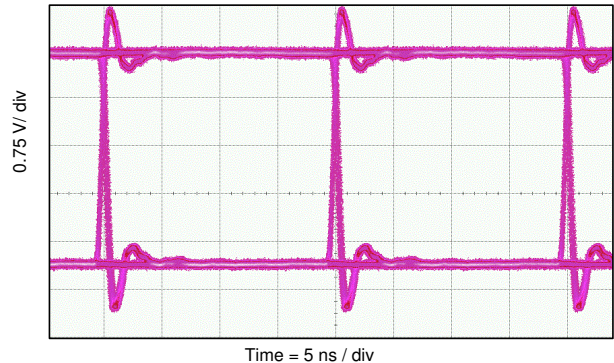


图 9-4. Eye Diagram at 50 Mbps PRBS 2¹⁶ - 1, 3.3 V and 25°C

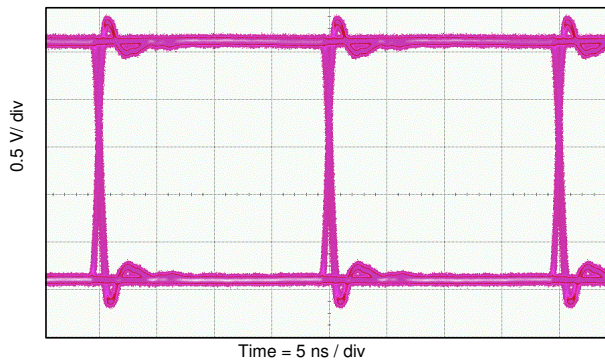


图 9-5. Eye Diagram at 50 Mbps PRBS 2¹⁶ - 1, 2.5 V and 25°C

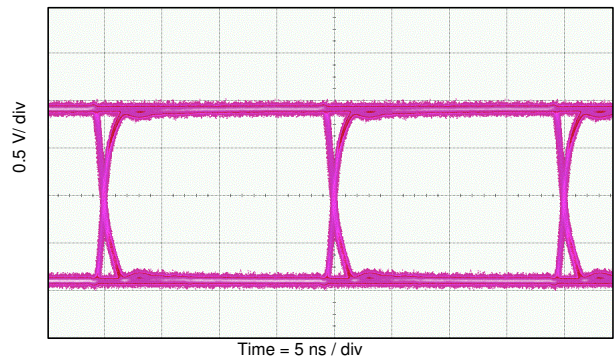


图 9-6. Eye Diagram at 50 Mbps PRBS 2¹⁶ - 1, 1.8 V and 25°C

9.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 图 9-7 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

图 9-8 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.

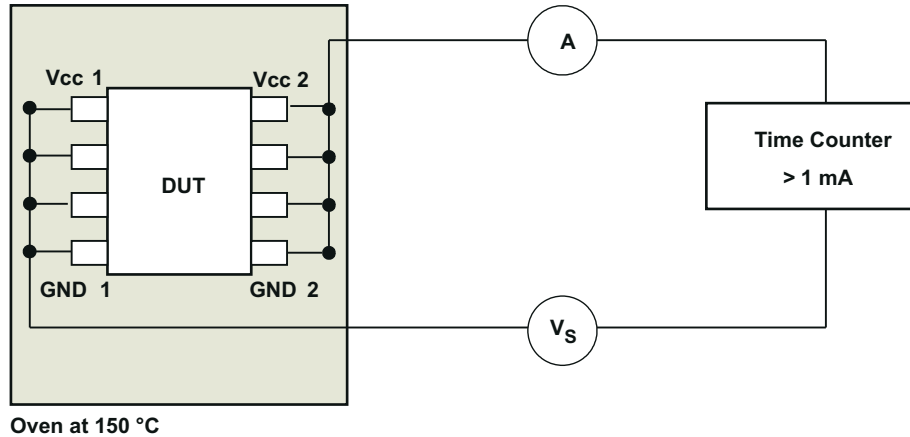


图 9-7. Test Setup for Insulation Lifetime Measurement

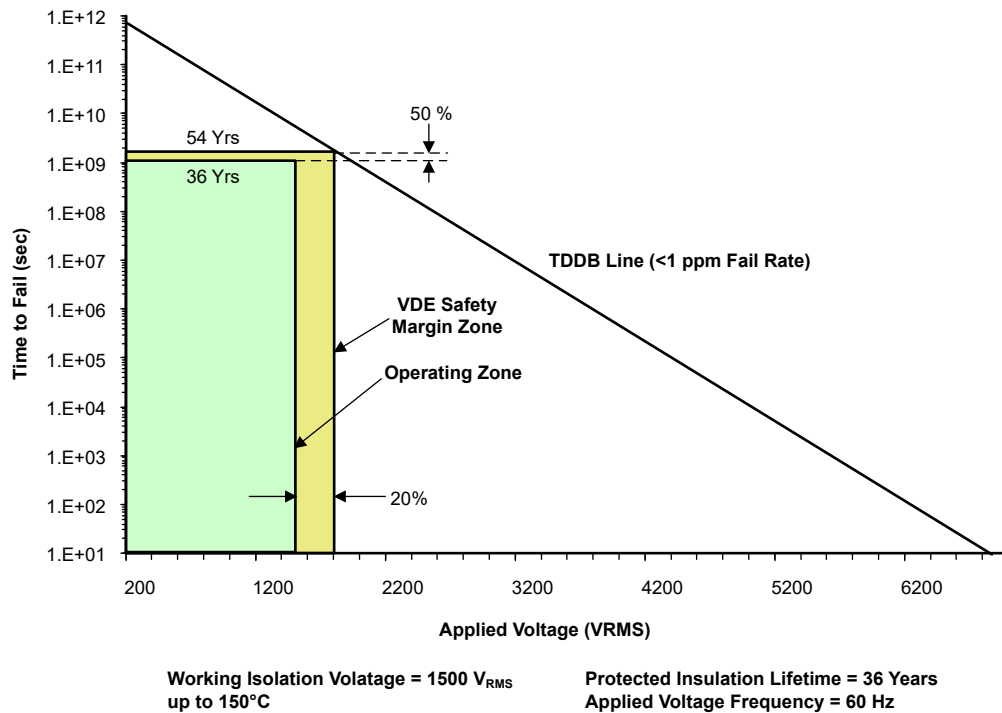


图 9-8. Insulation Lifetime Projection Data

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For automotive applications, please use [SN6501-Q1](#) or [SN6505B-Q1](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501-Q1 Transformer Driver for Isolated Power Supplies](#) or [SN6505B-Q1 Automotive, low-noise, 1-A, 420-kHz transformer driver with soft start for isolated power supplies](#).

11 Layout

11.1 Layout Guidelines

A minimum of two layers is required to accomplish a low EMI PCB design. To further improve EMI, a four layer board can be used (see [Figure 11-2](#)). Layer stacking for a four layer board should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

11.2 Layout Example

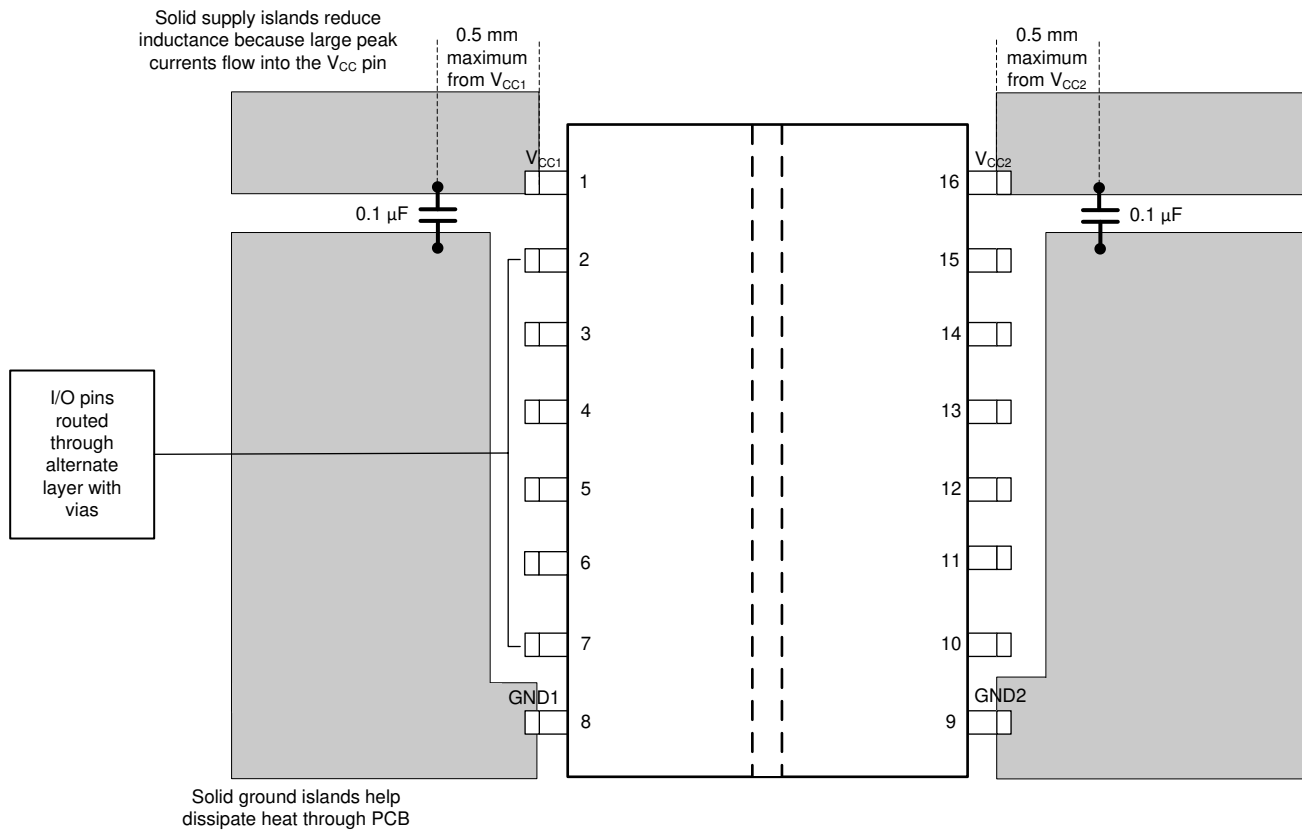


图 11-1. Layout Example

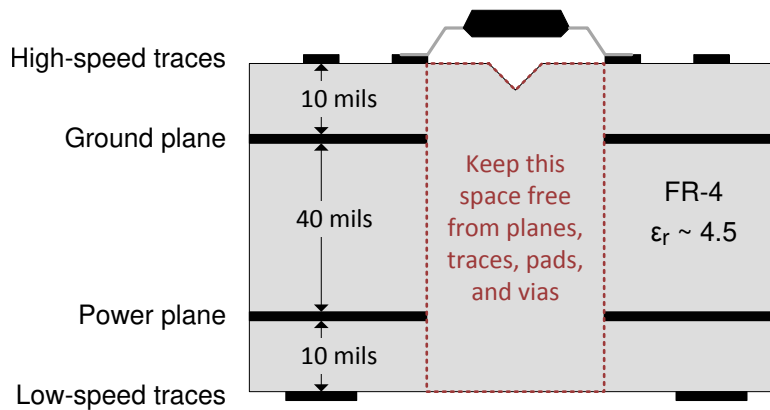


图 11-2. Four Layer Board Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems application report](#)
- Texas Instruments, [SN6505x-Q1 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies](#)
- Texas Instruments, [TCAN1044-Q1 Automotive Fault-Protected CAN FD Transceiver](#)
- Texas Instruments, [TPS763xx-Q1 Low-Power, 150-mA, Low-Dropout Linear Regulators data sheet](#)
- Texas Instruments, [TMS320F2803x Piccolo™ Microcontrollers data sheet](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

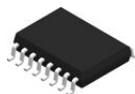
ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

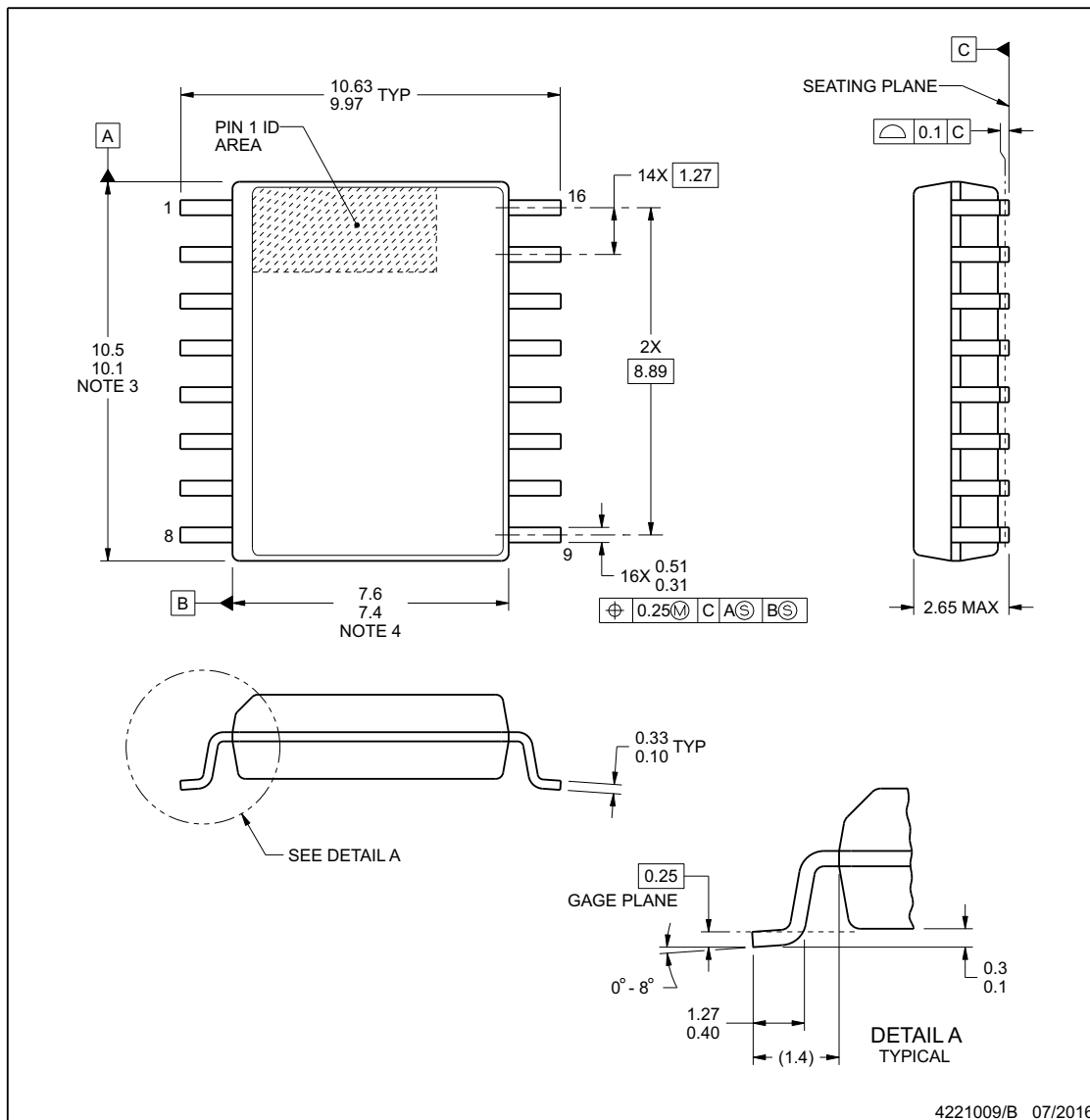


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

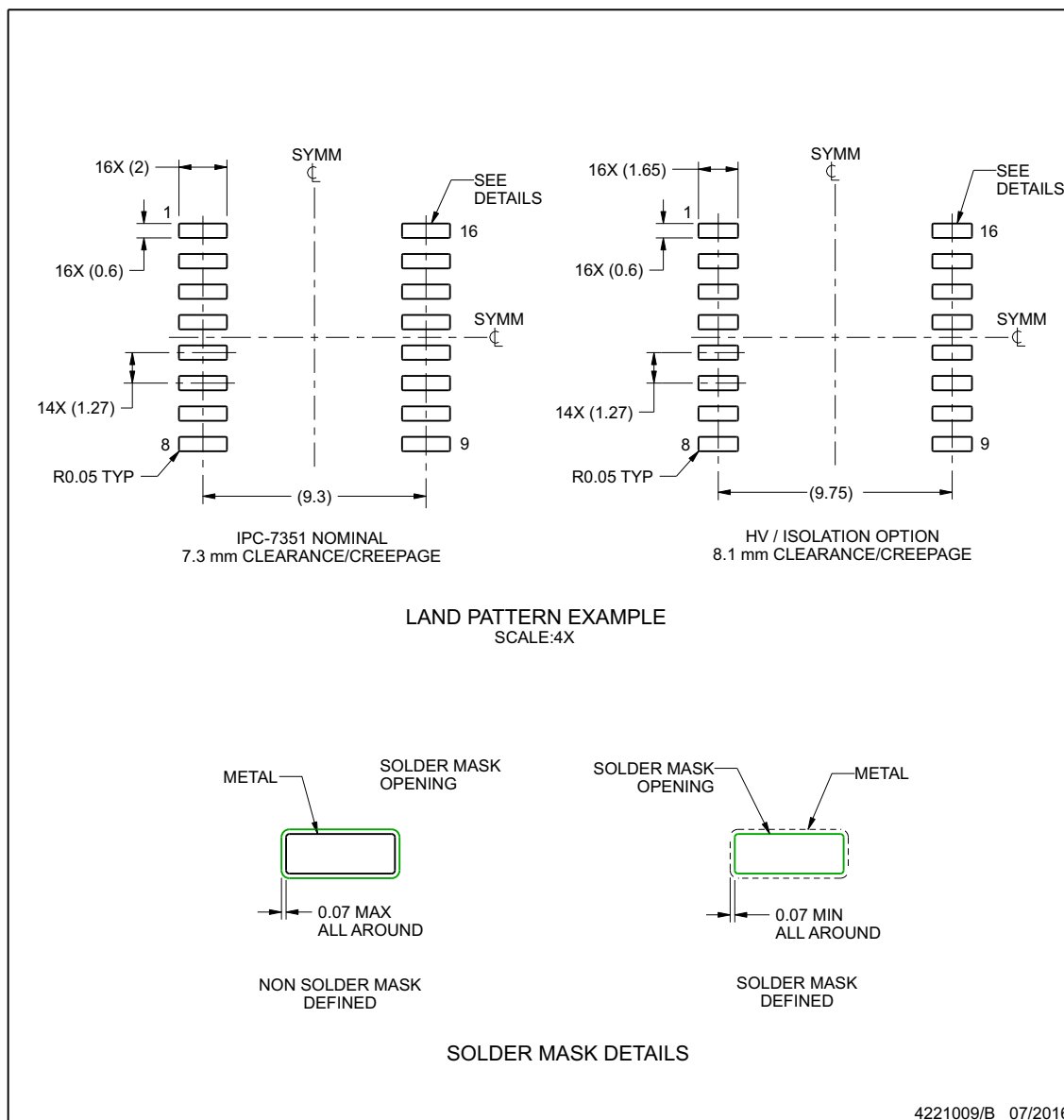
www.ti.com

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

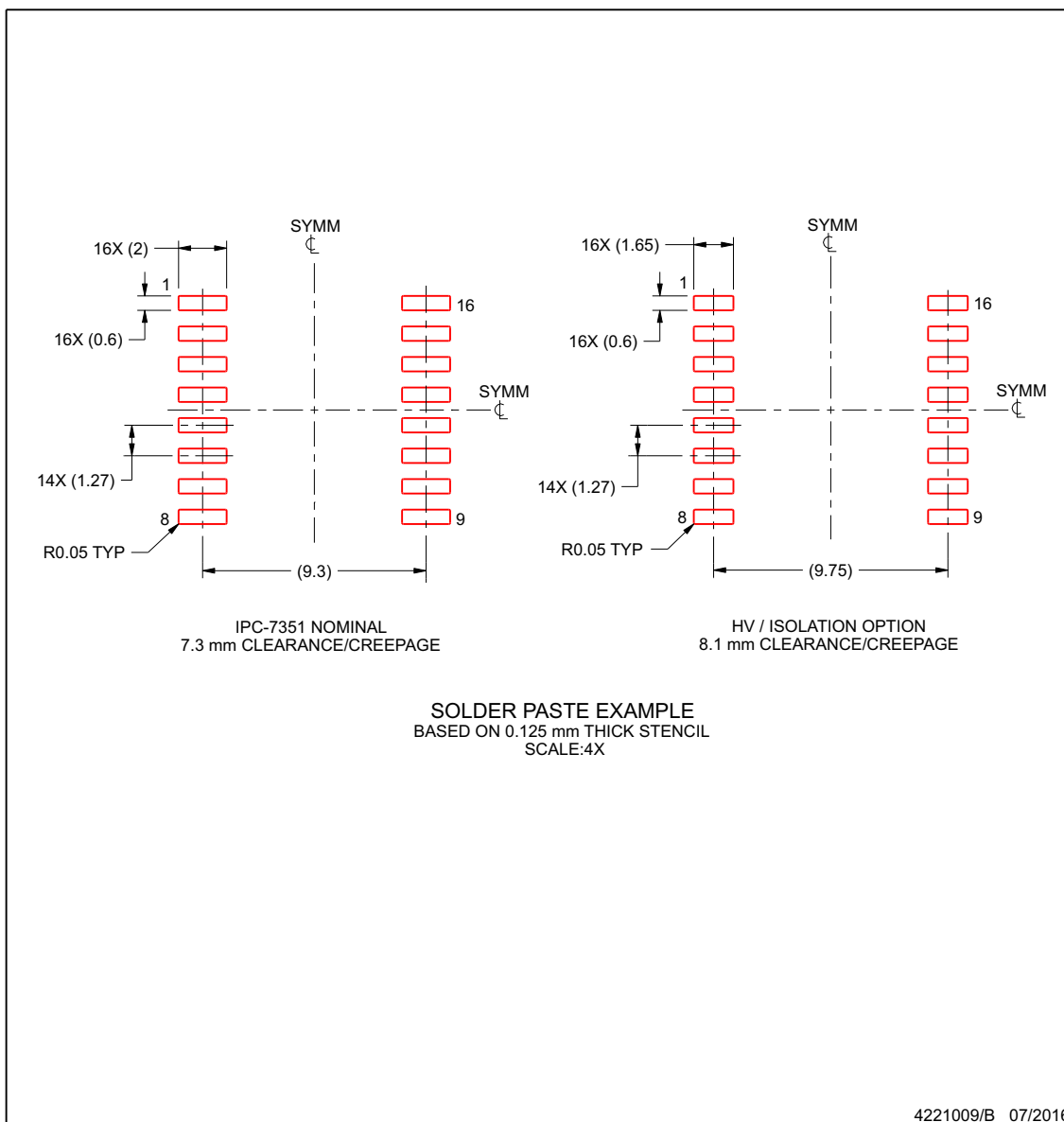
www.ti.com

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO6760FQDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760F
ISO6760FQDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760F
ISO6760FQDWRQ1.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760F
ISO6760QDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760
ISO6760QDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760
ISO6760QDWRQ1.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760
ISO6761FQDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761F
ISO6761FQDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761F
ISO6761FQDWRQ1.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761F
ISO6761QDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761
ISO6761QDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761
ISO6761QDWRQ1.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761
ISO6762FQDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762F
ISO6762FQDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762F
ISO6762FQDWRQ1.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762F
ISO6762QDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762
ISO6762QDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762
ISO6762QDWRQ1.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762
ISO6763FQDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763F
ISO6763FQDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763F
ISO6763FQDWRQ1.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763F
ISO6763QDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763
ISO6763QDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763
ISO6763QDWRQ1.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO6760-Q1, ISO6761-Q1, ISO6762-Q1, ISO6763-Q1 :

- Catalog : [ISO6760](#), [ISO6761](#), [ISO6762](#), [ISO6763](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6760FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6760FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6760FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6760QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6760QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6760QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6760QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6761FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6761FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6761QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6761QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6762FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6762FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6762QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6763FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6763QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6763QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6760FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO6760FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO6760FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6760QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6760QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6760QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO6761FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6761FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6761QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO6761QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6762FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6762FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6762QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6763FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6763QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO6763QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

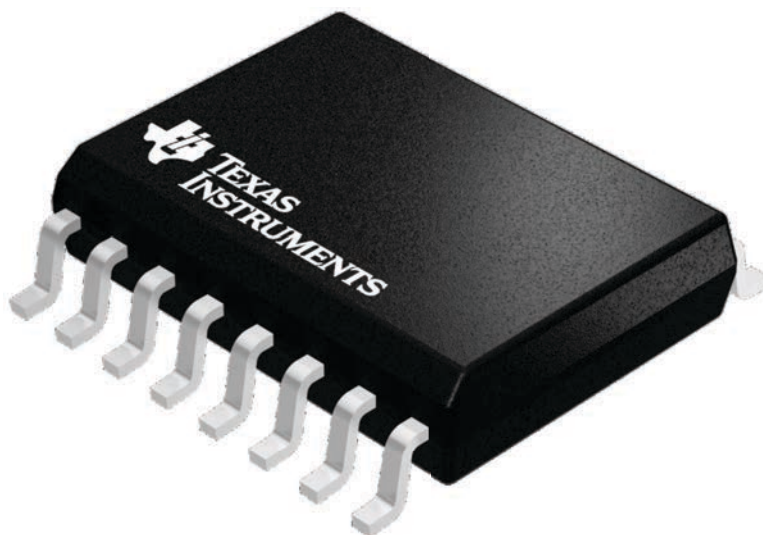
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

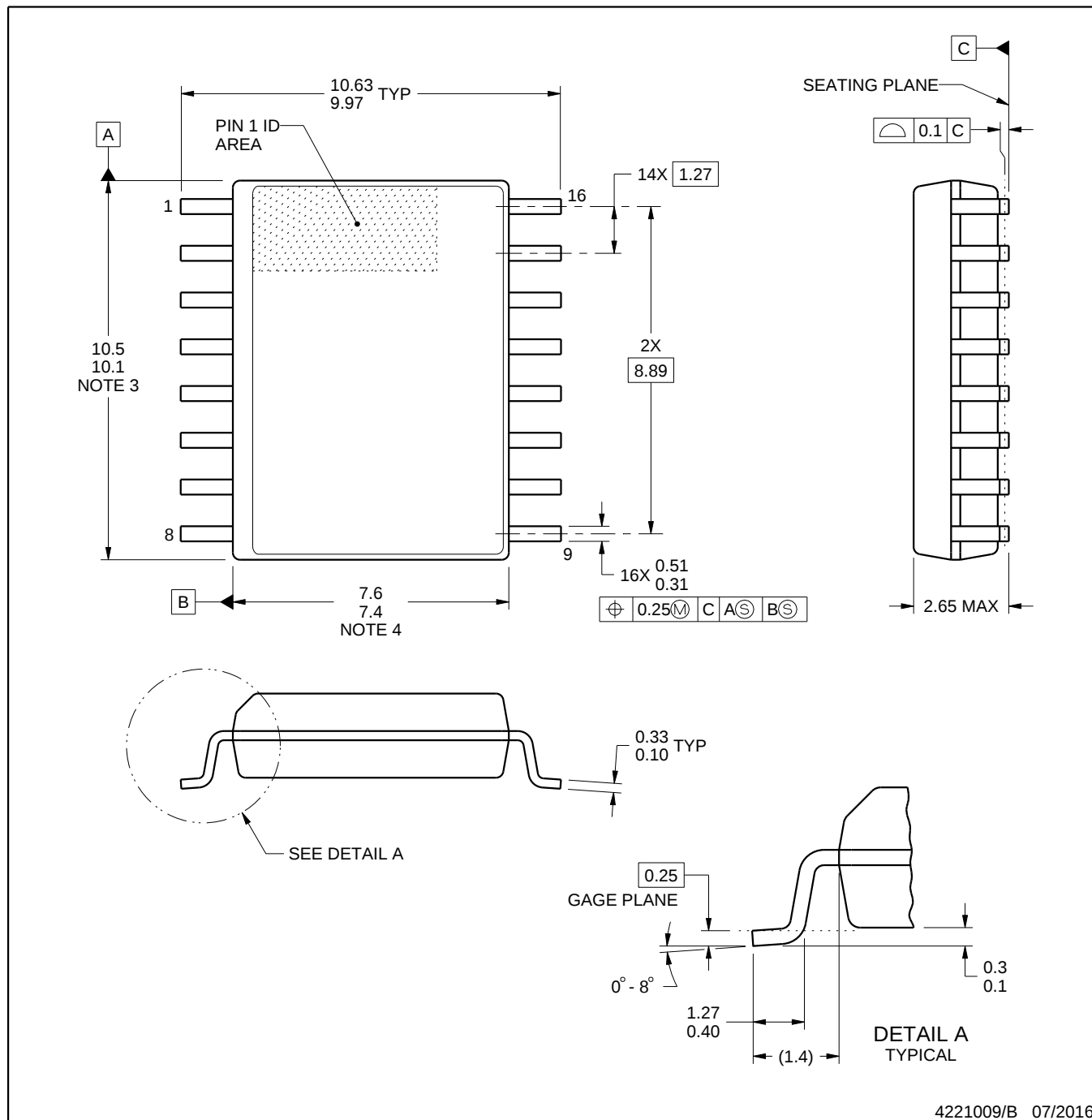


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



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NOTES:

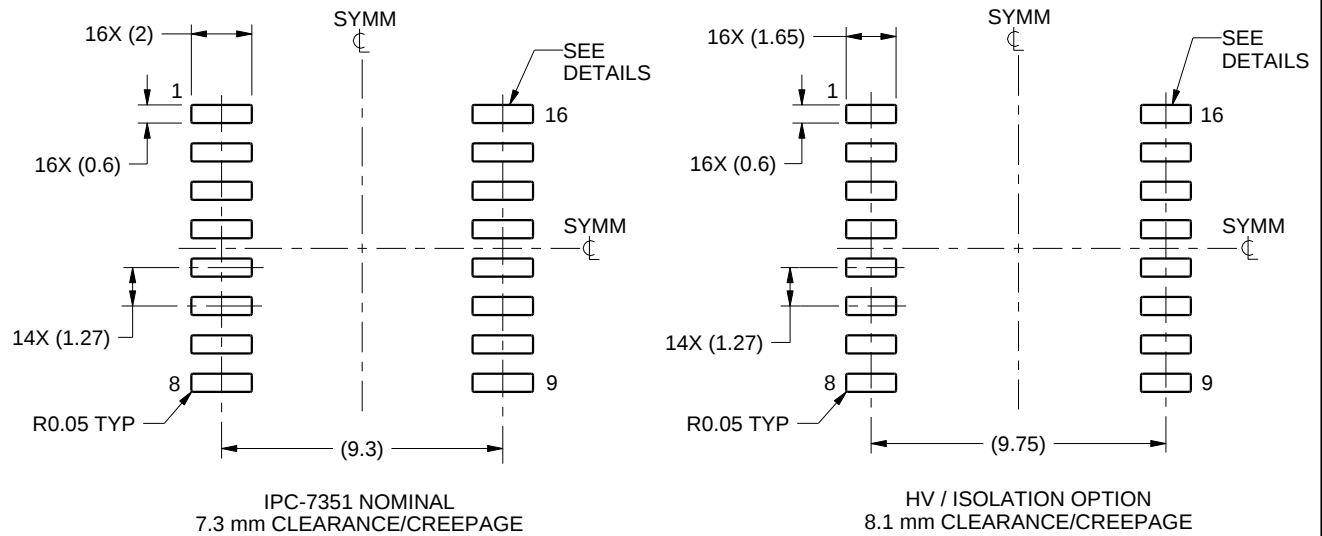
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

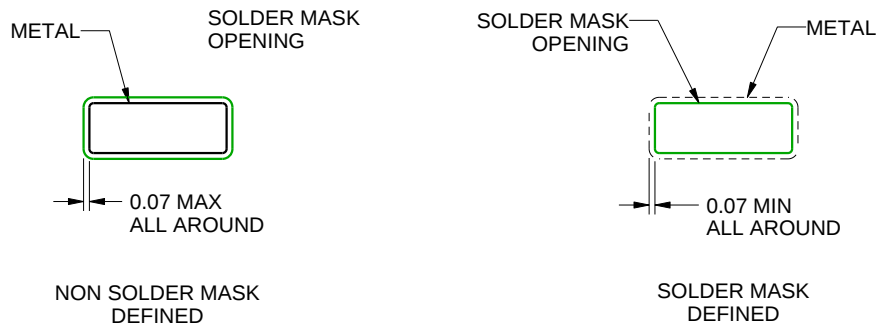
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

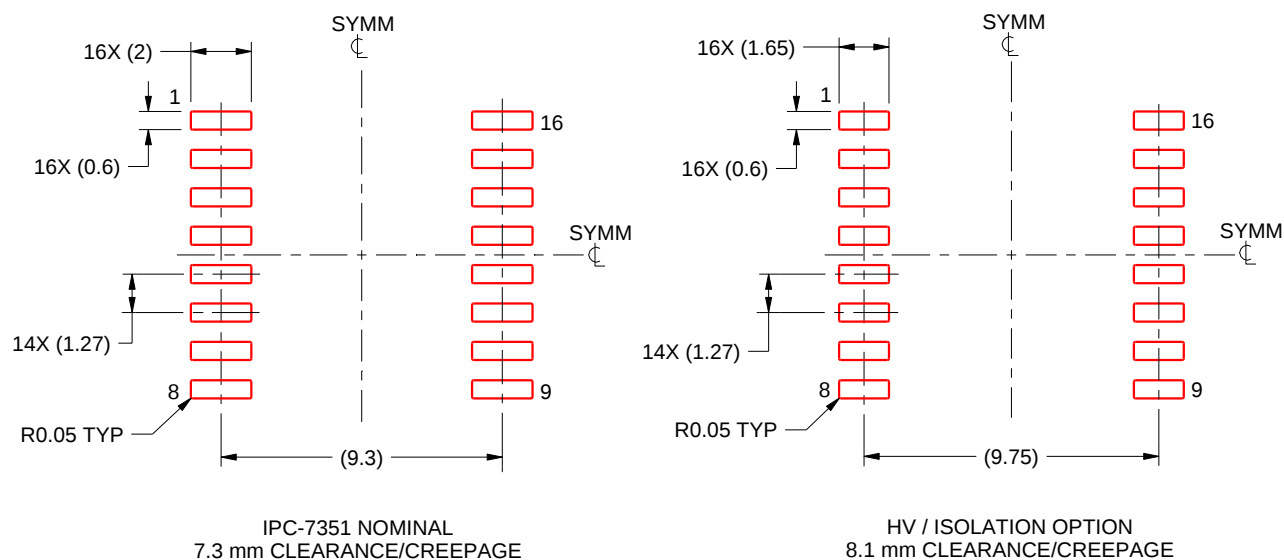
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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