

具有最小 5 倍增益的 INA827 宽电源范围、轨到轨输出仪表放大器

1 特性

- 消除了 5 倍增益下外部电阻器导致的误差
- 共模范围低于负电源
- 输入保护：高达 $\pm 40\text{V}$
- 轨至轨输出
- 出色的精度：
 - 共模抑制：88dB，最小值
 - 低失调电压：150 μV ，最大值
 - 低温漂：2.5 $\mu\text{V}/^\circ\text{C}$ ，最大值
 - 低增益漂移：1ppm/ $^\circ\text{C}$ ，最大值 ($G=5\text{V/V}$)
 - 电源抑制：100dB，最小值 ($G=5$)
 - 噪声：17 nV/ $\sqrt{\text{Hz}}$ ， $G=1000\text{V/V}$
- 高带宽：
 - $G=5$: 600kHz
 - $G=100$: 150kHz
- 电源电流：200 μA ，典型值
- 电源范围：
 - 单电源：3V 至 36V
 - 双电源： $\pm 1.5\text{V}$ 至 $\pm 18\text{V}$
- 额定温度范围： -40°C 至 $+125^\circ\text{C}$
- 封装：8 引脚 VSSOP

2 应用

- 工业过程控制
- 多通道系统
- 电力自动化
- 衡器
- 医疗仪表
- 数据采集

3 说明

INA827 是一款低成本仪表放大器 (INA)，此放大器提供极低功耗并运行在非常宽泛的单电源或者双电源范围内。此器件为了实现 $G=5$ 时只有 1ppm 每摄氏度的最低可能增益漂移而进行了优化，且无需外部电阻器。然而，一个单一外部电阻器可在 5 至 1000 之间设定任一增益。

对 INA827 进行了优化以在高达 5kHz 的频率上提供超过 88dB ($G=5$) 的出色共模抑制比 (CMRR)。 $G=5$ 时，在整个输入共模范围内（从负电源一直到高达 1V 的正电源）CMRR 超过 88dB。通过使用一个轨到轨输出，INA827 非常适合于由 3V 单电源供电以及由高达 $\pm 18\text{V}$ 的双电源供电的低压运行。附加的电路通过将输入电流限制在安全水平来保护输入不受超过电源电压高达 $\pm 40\text{V}$ 的过压影响。

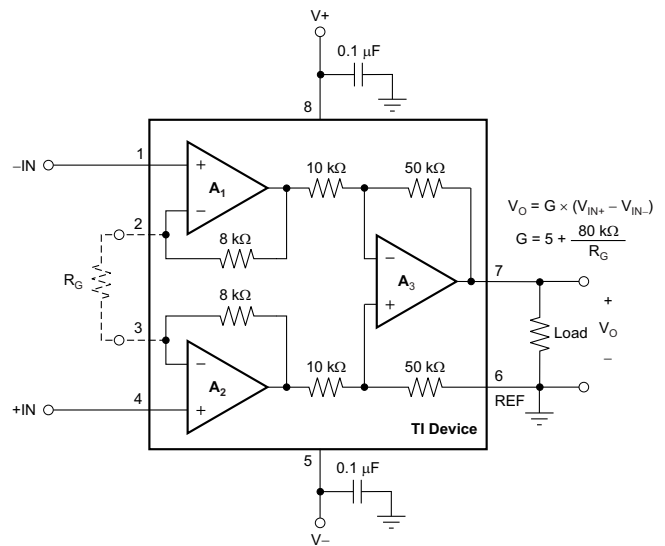
INA827 采用小型 VSSOP-8 封装，额定运行温度范围为 -40°C 至 $+125^\circ\text{C}$ 。有关增益范围介于 1V/V 至 1000V/V 之间的类似仪表放大器的信息，请参阅 [INA826](#)。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
INA827	VSSOP (8)	3.00mm \times 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

Changes from Revision A (July 2013) to Revision B

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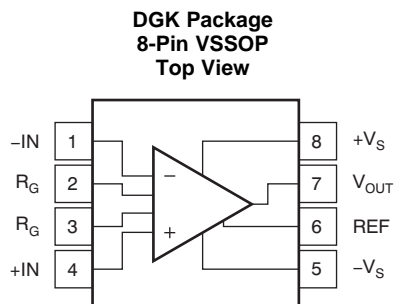
• 添加了器件信息表、ESD 额定值表、建议运行条件表、概述部分、功能块图部分、特性说明部分、器件功能模式部分、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	1
• 从第 1 页的顶部删除了器件图形	1
• 更改了特性部分：更改了电源范围项目的子项目	1
• 通篇将 MSOP 更改成了 VSSOP	1
• 在说明部分的第一段中更改了单电源值	1
• 添加了简化原理图标题	1
• Deleted <i>Package and Ordering Information</i> table	3
• Changed <i>Pin Configuration and Functions</i> section: changed section title, changed <i>Pin Functions</i> title, added I/O column	3
• Changed test conditions of Input, <i>PSRR</i> and <i>V_{CM}</i> parameters in <i>Electrical Characteristics</i> table	5
• Changed minimum specifications of Power Supply, <i>V_S</i> parameter in <i>Electrical Characteristics</i> table	6
• Changed <i>Typical Characteristics</i> section: moved conditions from title to conditions line under curve	7
• Changed conditions of Figure 7 and Figure 8	8
• Changed conditions of Figure 37 and Figure 38	13
• Changed power-supply range in <i>Operating Voltage</i> section	22
• Changed power supply low level in <i>Low-Voltage Operation</i> section	22
• Added <i>Design Requirements</i> , <i>Detailed Design Procedure</i> , and <i>Application Curves</i> to the <i>Typical Application</i> section	25

Changes from Original (June 2012) to Revision A

Page

• 已更改 更改了首页图形	1
• Updated Figure 15	8
• Updated Figure 16	8
• Updated Figure 61	24

5 Pin Configuration and Functions



Pin Functions

NAME	NO.	I/O	DESCRIPTION
-IN	1	I	Negative input
+IN	4	I	Positive input
REF	6	I	Reference input. This pin must be driven by low impedance.
RG	2, 3	—	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
V _{OUT}	7	O	Output
-V _S	5	—	Negative supply
+V _S	8	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply	–20	20	V
	Input	–40	40	
REF input		–20	20	V
Output short-circuit ⁽²⁾		Continuous		
Temperature range	Operating, T_A	–55	150	°C
	Junction, T_J		175	
	Storage, T_{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to $V_S / 2$.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	Single supply	3		36	V
	Dual supply	±1.5		±18	
Specified temperature		–40		125	°C
Operating temperature		–50		150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA827	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	215.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	97.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	96.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V _{OSI}	Offset voltage ⁽¹⁾	Input stage	RTI, V _{OS} = V _{OSI} + (V _{OSO} / G)		40	150	μV
			T _A = −40°C to +125°C		0.5	2.5	μV/°C
V _{OSO}		Output stage	RTI, V _{OS} = V _{OSI} + (V _{OSO} / G)		500	2000	μV
			T _A = −40°C to +125°C		5	30	μV/°C
PSRR	Power-supply rejection ratio		G = 5, V _S = ±1.5 V to ±18 V	100	120	dB	
			G = 10, V _S = ±1.5 V to ±18 V	106	126		
			G > 100, V _S = ±1.5 V to ±18 V	120	140		
Z _{IN}	Impedance	Differential		2 1		GΩ pF	
		Common-mode		10 5			
RFI filter, −3-dB frequency				25		MHz	
V _{CM}	Operating input range ⁽²⁾		V _S = ±1.5 V to ±18 V, V _O = 0 V	(V−) − 0.2	(V+) − 0.9		V
			V _S = ±1.5 V to ±18 V, V _O = 0 V, T _A = +125°C	(V−) − 0.05	(V+) − 0.8		
			V _S = ±1.5 V to ±18 V, V _O = 0 V, T _A = −40°C	(V−) − 0.3	(V+) − 0.95		
Input overvoltage range			T _A = −40°C to +125°C	(V+) − 40	(V−) + 40		V
CMRR	Common-mode rejection ratio		DC to 60 Hz	G = 5, V _{CM} = V− to (V+) − 1 V	88	100	dB
				G = 10, V _{CM} = V− to (V+) − 1 V	94	106	
				G > 100, V _{CM} = V− to (V+) − 1 V	110	126	
			At 5 kHz	G = 5, V _{CM} = V− to (V+) − 1 V	88		
				G = 10, V _{CM} = V− to (V+) − 1 V	94		
				G > 100, V _{CM} = V− to (V+) − 1 V	104		
BIAS CURRENT							
I _B	Input bias current				35	50	nA
			T _A = −40°C to +125°C			95	
I _{OS}	Input offset current			−5	0.7	5	nA
			T _A = −40°C to +125°C			10	
NOISE VOLTAGE ⁽³⁾							
e _{NI}	Voltage noise	Input	f = 1 kHz, G = 1000, R _S = 0 Ω		17	18	nV/√Hz
e _{NO}		Output	f = 1 kHz, G = 5, R _S = 0 Ω		250	285	
RTI	Referred-to-input		G = 5, f _B = 0.1 Hz to 10 Hz, R _S = 0 Ω		1.4	μV _{pp}	
			G = 1000, f _B = 0.1 Hz to 10 Hz, R _S = 0 Ω		0.5		
i _N	Noise current		f = 1 kHz		120	fA/√Hz	
			f _B = 0.1 Hz to 10 Hz		5	pA _{pp}	
GAIN							
G	Gain equation				$5 + \left[\frac{80 \text{ k}\Omega}{R_G} \right]$		V/V
G	Range of gain				5	1000	V/V
GE	Gain error		G = 5, V _O = ±10 V	±0.005%	±0.035%		
			G = 10 to 1000, V _O = ±10 V	±0.1%	±0.4%		
Gain versus temperature ⁽⁴⁾			G = 5, T _A = −40°C to +125°C	±0.1	±1		ppm/°C
			G > 5, T _A = −40°C to +125°C	8	25		
Gain nonlinearity			G = 5 to 100, V _O = −10 V to +10 V, R _L = 10 kΩ	2	5		ppm
			G = 1000, V _O = −10 V to +10 V, R _L = 10 kΩ	20	50		

(1) Total offset, referred-to-input (RTI): $V_{\text{OS}} = V_{\text{OSI}} + (V_{\text{OSO}} / G)$.

(2) Input voltage range of the INA827 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See the [Typical Characteristics](#) section for more information.

(3)

$$\text{Total RTI voltage noise} = \sqrt{(e_{\text{NI}})^2 + \left[\frac{e_{\text{NO}}}{G} \right]^2}$$

(4) The values specified for $G > 5$ do not include the effects of the external gain-setting resistor, R_G .

INA827

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Electrical Characteristics (continued)

 at $T_A = +25^{\circ}\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
Voltage swing		$R_L = 10\text{ k}\Omega$	$(V_-) + 0.1$	$(V_+) - 0.15$		V
Load capacitance stability				1000		pF
Short-circuit current		Continuous to common		± 16		mA
FREQUENCY RESPONSE						
BW	Bandwidth, -3 dB	$G = 5$		600		kHz
		$G = 10$		530		
		$G = 100$		150		
		$G = 1000$		15		
SR	Slew rate	$G = 5, V_O = \pm 14.5\text{ V}$		1.5		V/ μs
		$G = 100, V_O = \pm 14.5\text{ V}$		1.5		
t_S	To 0.01%	$G = 5, V_{\text{STEP}} = 10\text{ V}$		10		μs
		$G = 100, V_{\text{STEP}} = 10\text{ V}$		12		
		$G = 1000, V_{\text{STEP}} = 10\text{ V}$		95		
	To 0.001%	$G = 1, V_{\text{STEP}} = 10\text{ V}$		11		
		$G = 100, V_{\text{STEP}} = 10\text{ V}$		18		
		$G = 1000, V_{\text{STEP}} = 10\text{ V}$		118		
REFERENCE INPUT						
R_{IN}	Input impedance			60		k Ω
Voltage range			V_-		V_+	V
Gain to output				1		V/V
Reference gain error				0.01		%
POWER SUPPLY						
V_S	Power-supply voltage	Single	3.0		36	V
		Dual	± 1.5		± 18	
I_Q	Quiescent current	$V_{\text{IN}} = 0\text{ V}$		200	250	μA
		$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		250	320	
TEMPERATURE RANGE						
Specified			-40		125	$^{\circ}\text{C}$
Operating			-50		150	$^{\circ}\text{C}$
θ_{JA}	Thermal resistance			215		$^{\circ}\text{C/W}$

6.6 Typical Characteristics

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

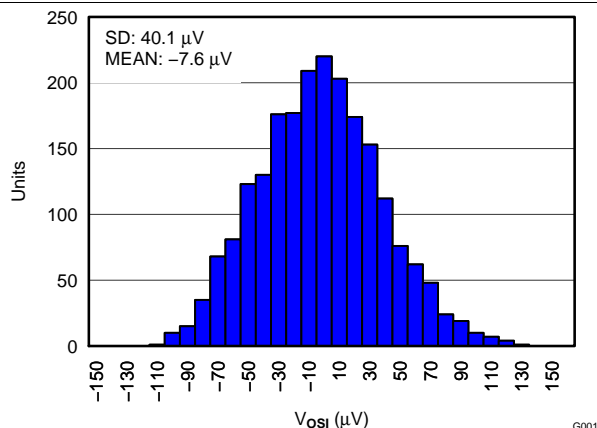


Figure 1. Typical Distribution of Input Offset Voltage

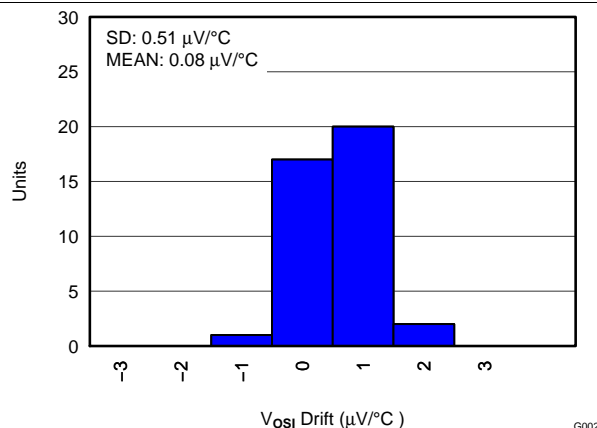


Figure 2. Typical Distribution of Input Offset Voltage Drift

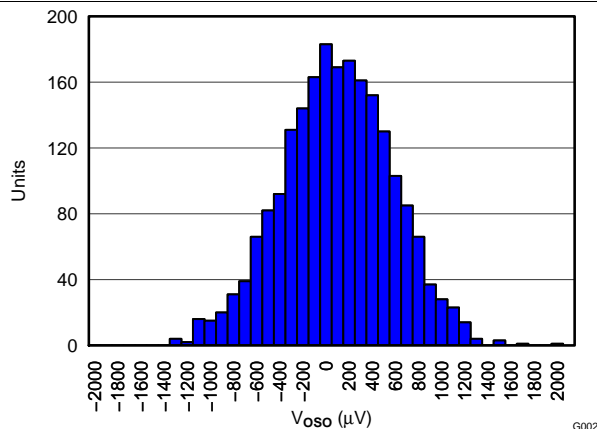


Figure 3. Typical Distribution of Output Offset Voltage

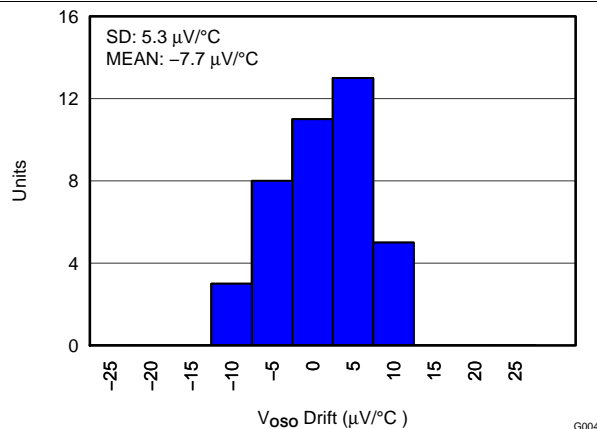


Figure 4. Typical Distribution of Output Offset Voltage Drift

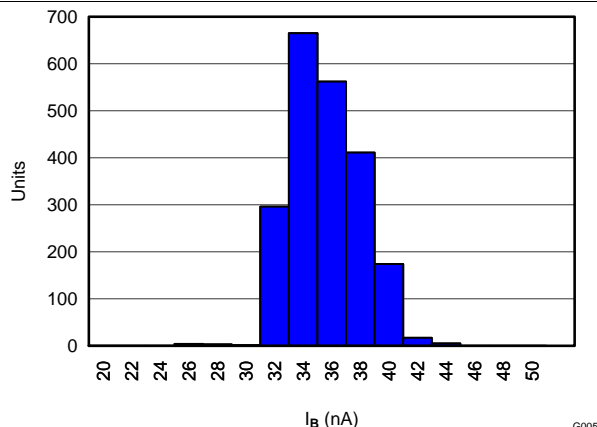


Figure 5. Typical Distribution of Input Bias Current

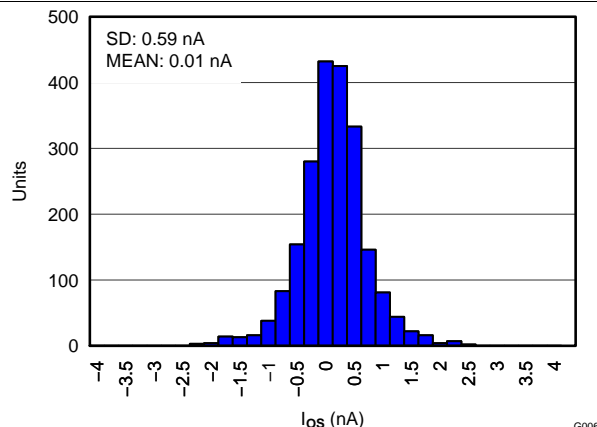
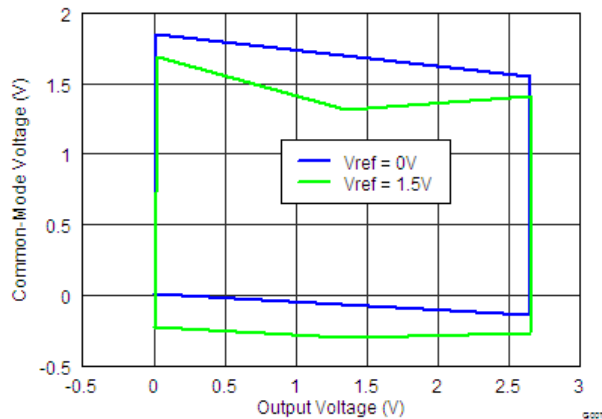


Figure 6. Typical Distribution of Input Offset Current

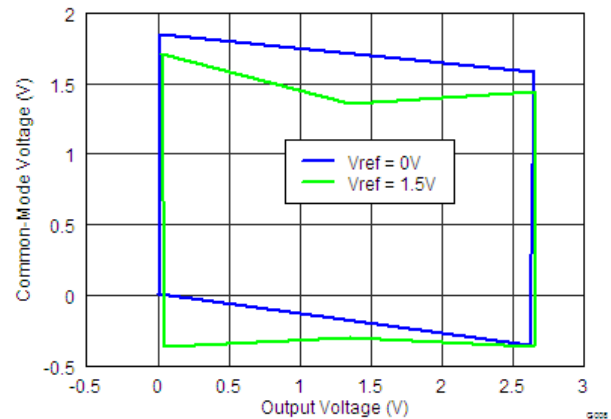
Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{REF} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)



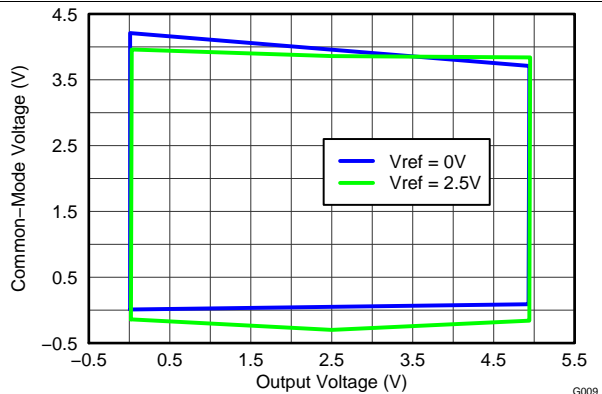
Single supply, $V_S = +3\text{ V}$, $G = 5$

Figure 7. Input Common-Mode Voltage vs Output Voltage



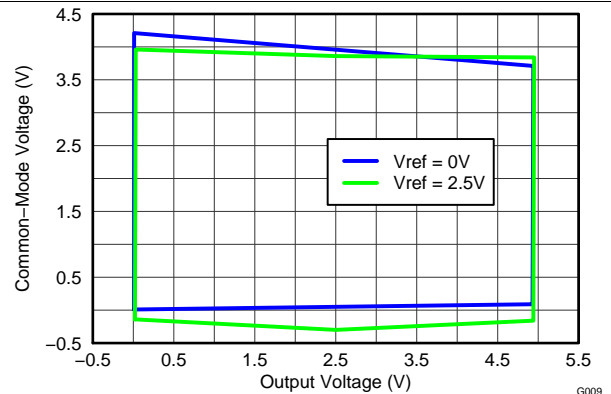
Single supply, $V_S = +3\text{ V}$, $G = 100$

Figure 8. Input Common-Mode Voltage vs Output Voltage



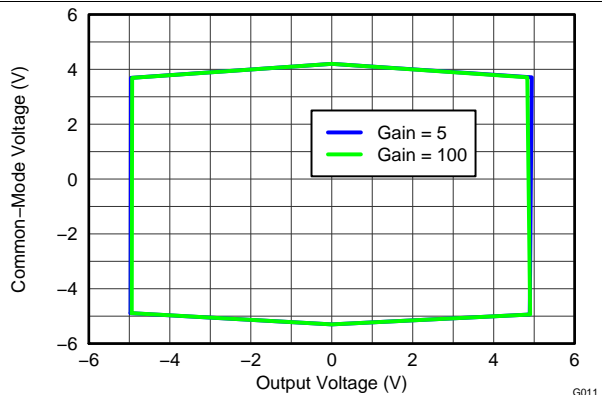
Single supply, $V_S = +5\text{ V}$, $G = 5$

Figure 9. Input Common-Mode Voltage vs Output Voltage



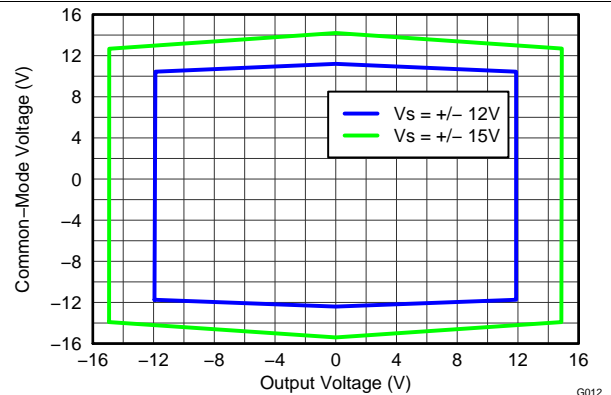
Single supply, $V_S = +5\text{ V}$, $G = 100$

Figure 10. Input Common-Mode Voltage vs Output Voltage



Dual supply, $V_S = \pm 5\text{ V}$

Figure 11. Input Common-Mode Voltage vs Output Voltage



Dual supply, $V_S = \pm 15\text{ V}$, $\pm 12\text{ V}$, $G = 5$

Figure 12. Input Common-Mode Voltage vs Output Voltage

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

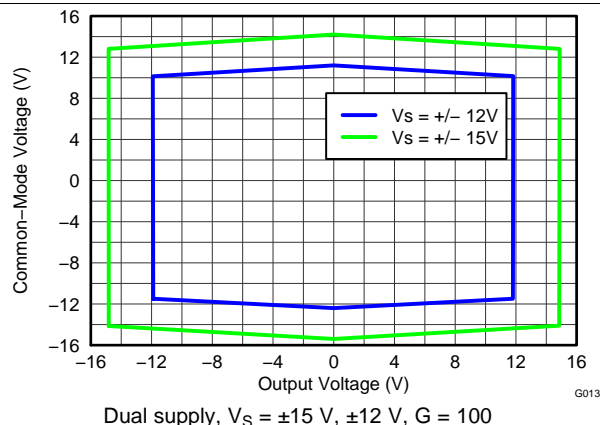


Figure 13. Input Common-Mode Voltage vs Output Voltage

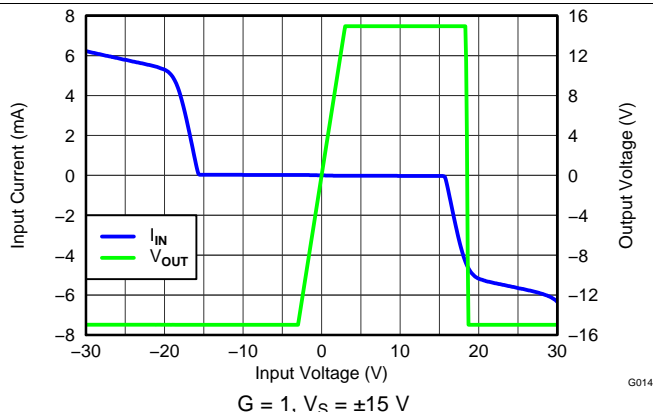


Figure 14. Input Overvoltage vs Input Current

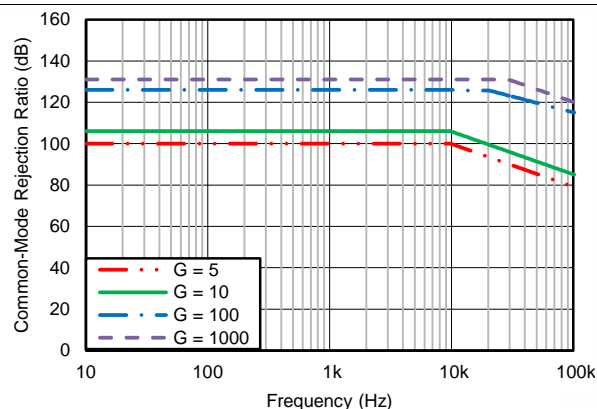


Figure 15. CMRR vs Frequency (RTI)

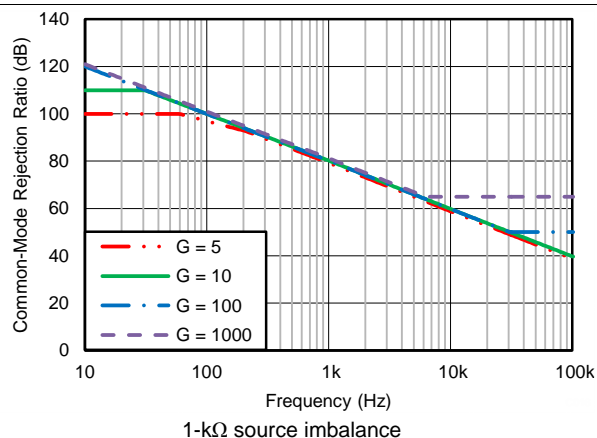


Figure 16. CMRR vs Frequency (RTI)

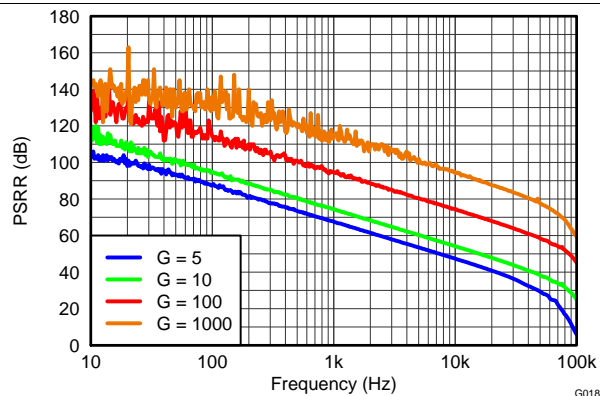


Figure 17. Positive PSRR vs Frequency (RTI)

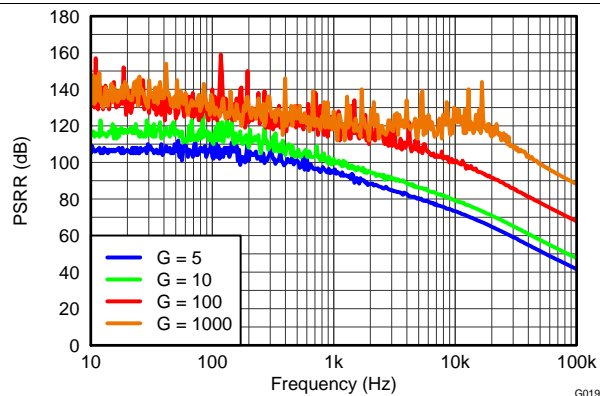


Figure 18. Negative PSRR vs Frequency (RTI)

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

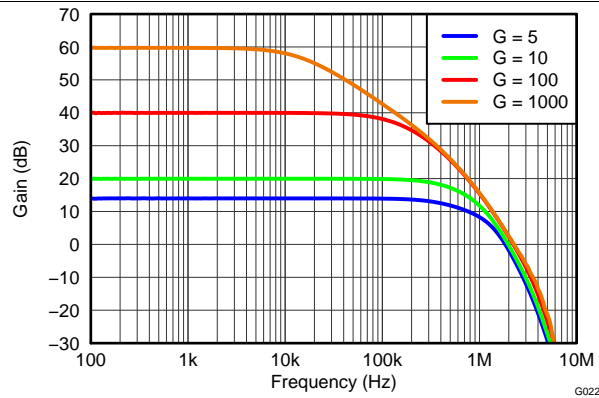


Figure 19. Gain vs Frequency

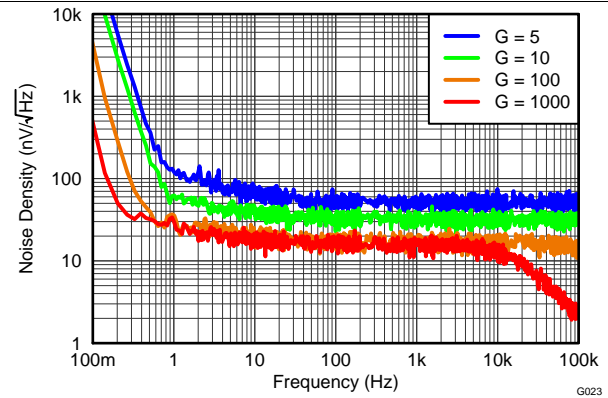


Figure 20. Voltage Noise Spectral Density vs Frequency (RTI)

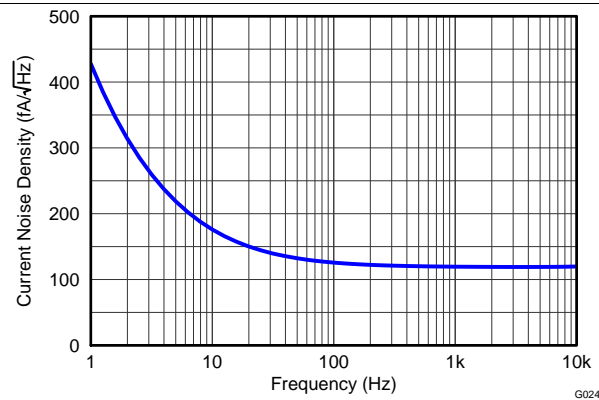


Figure 21. Current Noise Spectral Density vs Frequency (RTI)

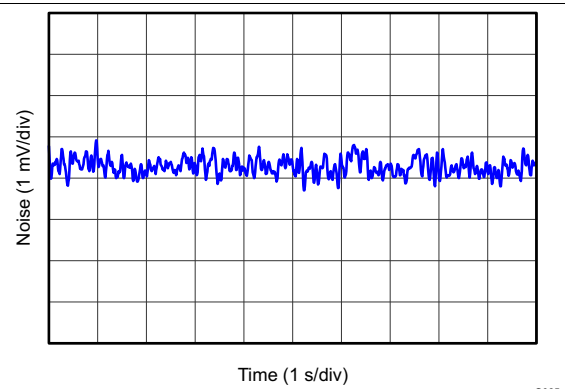


Figure 22. 0.1-Hz to 10-Hz RTI Voltage Noise ($G = 5$)

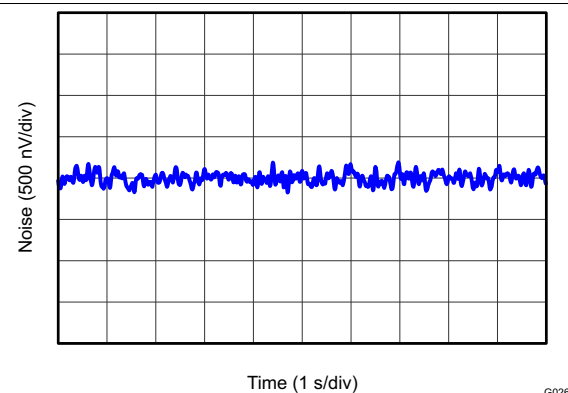


Figure 23. 0.1-Hz to 10-Hz RTI Voltage Noise ($G = 1000$)

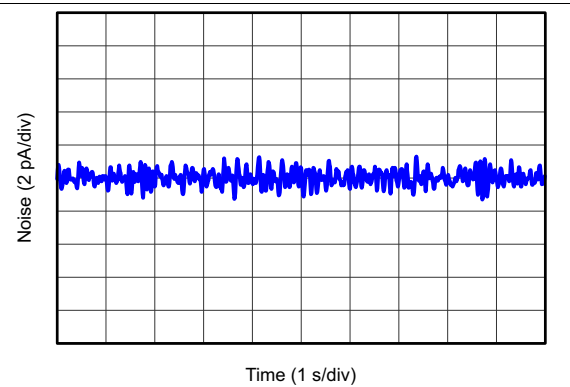


Figure 24. 0.1-Hz to 10-Hz RTI Current Noise

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

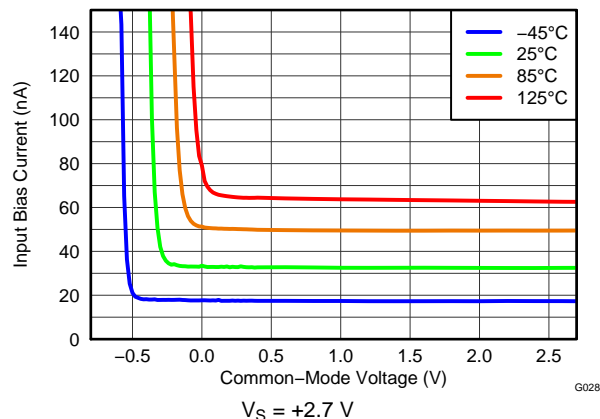


Figure 25. Input Bias Current vs Common-Mode Voltage

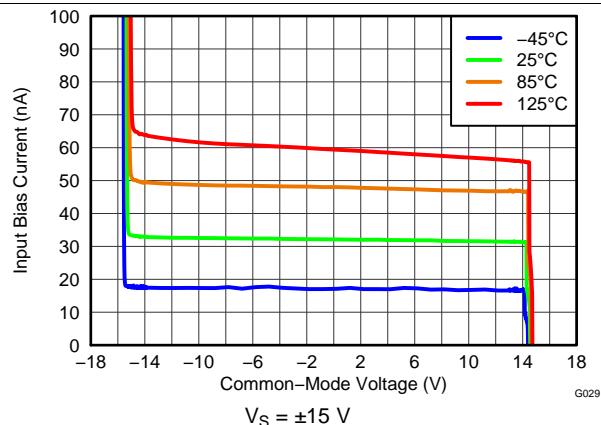


Figure 26. Input Bias Current vs Common-Mode Voltage

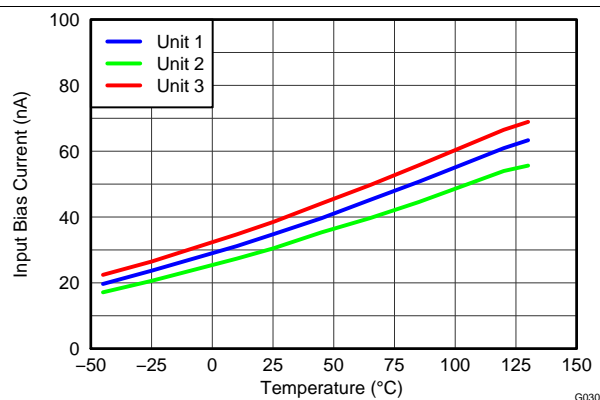


Figure 27. Input Bias Current vs Temperature

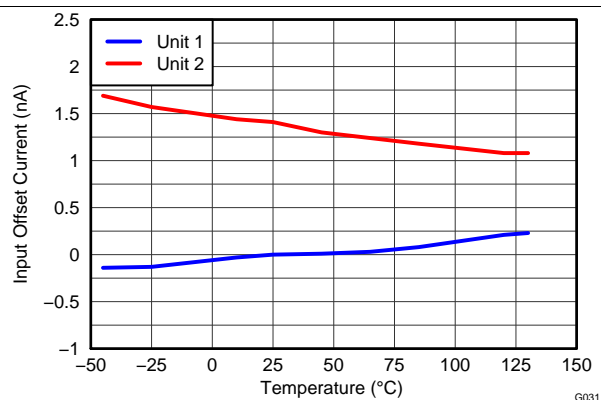


Figure 28. Input Offset Current vs Temperature

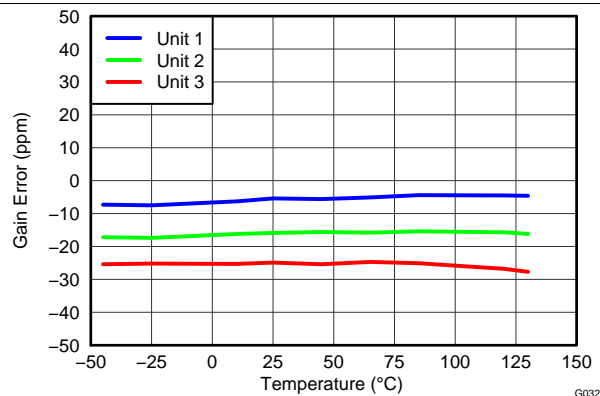


Figure 29. Gain Error vs Temperature ($G = 5$)

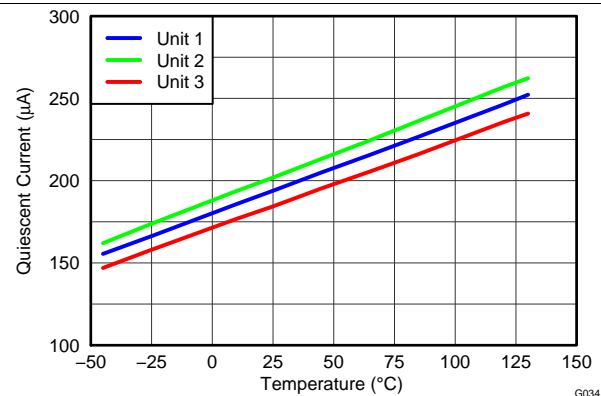


Figure 30. Supply Current vs Temperature

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

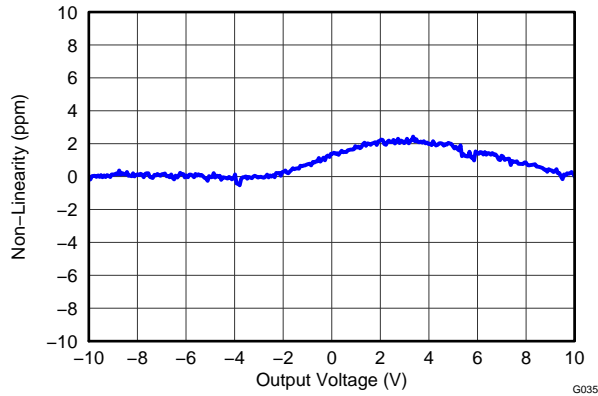


Figure 31. Gain Nonlinearity ($G = 5$)

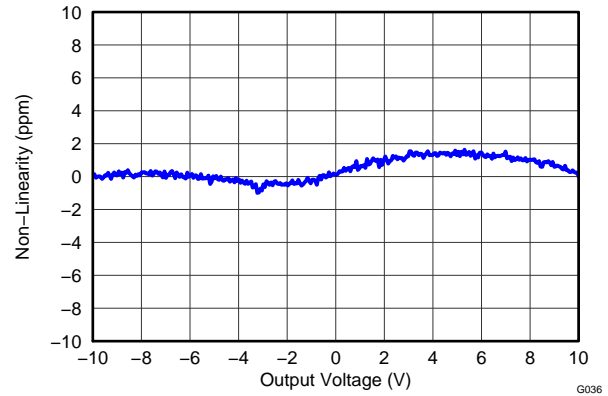


Figure 32. Gain Nonlinearity ($G = 10$)

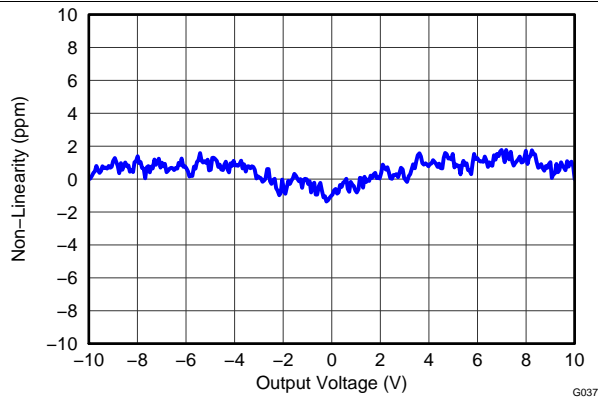


Figure 33. Gain Nonlinearity ($G = 100$)

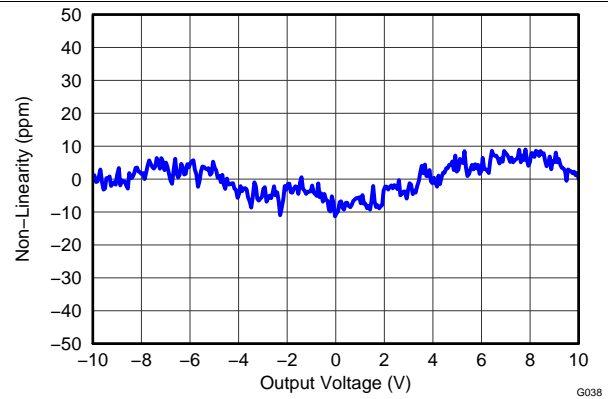


Figure 34. Gain Nonlinearity ($G = 1000$)

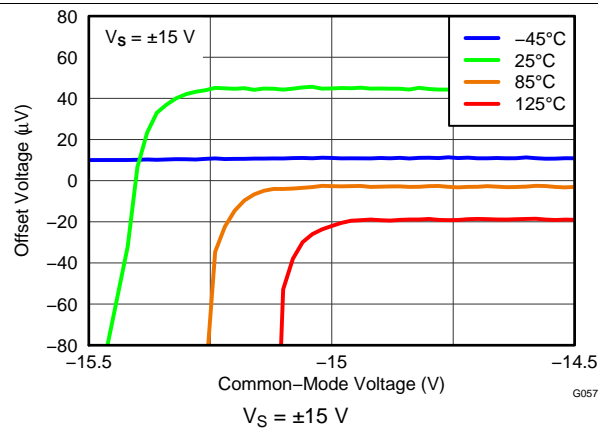


Figure 35. Offset Voltage vs Negative Common-Mode Voltage

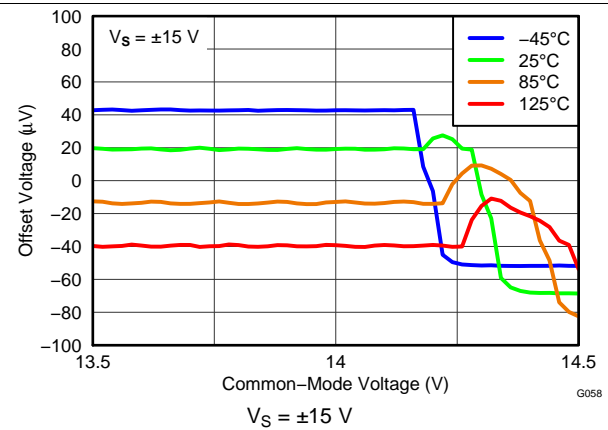


Figure 36. Offset Voltage vs Positive Common-Mode Voltage

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

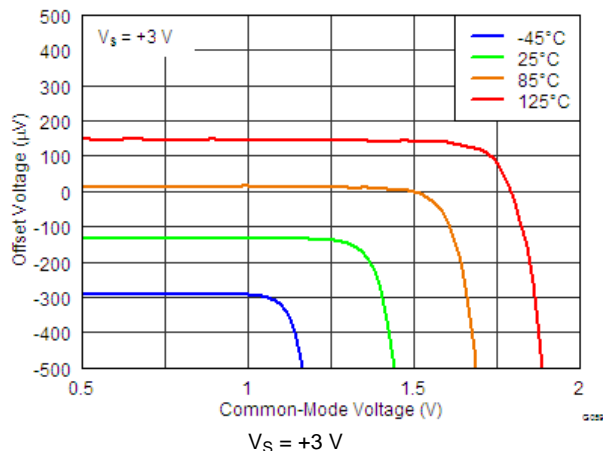


Figure 37. Offset Voltage vs Negative Common-Mode Voltage

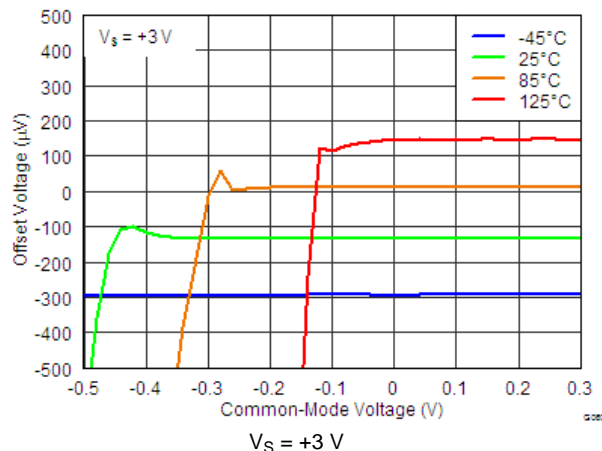


Figure 38. Offset Voltage vs Positive Common-Mode Voltage

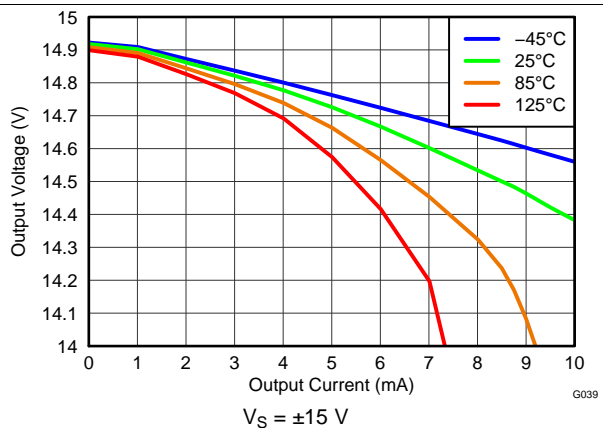


Figure 39. Positive Output Voltage Swing vs Output Current

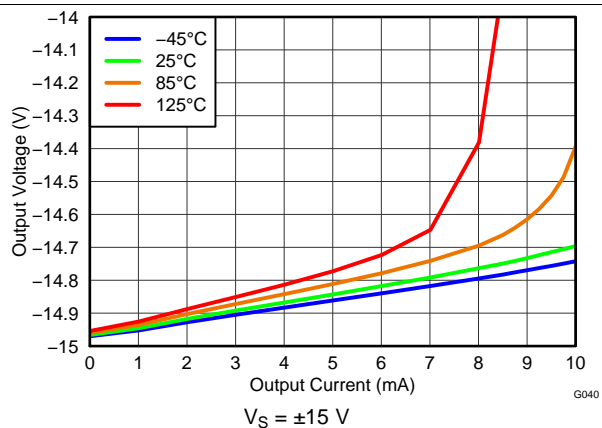


Figure 40. Negative Output Voltage Swing vs Output Current

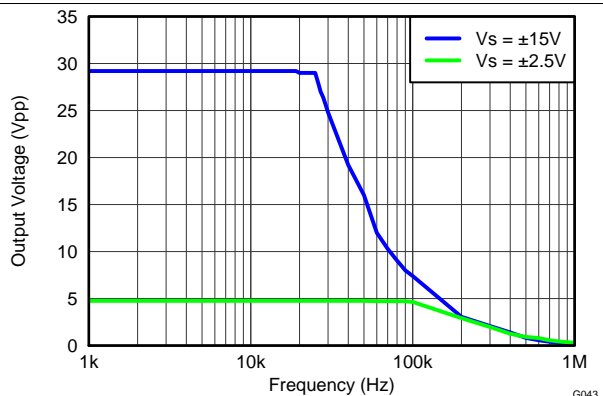


Figure 41. Large-Signal Frequency Response

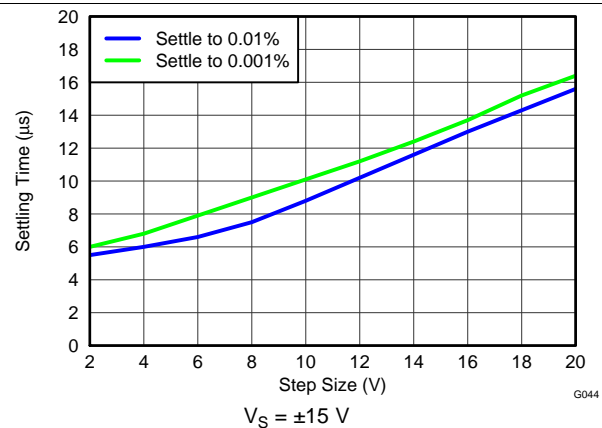


Figure 42. Settling Time vs Step Size

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{REF} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

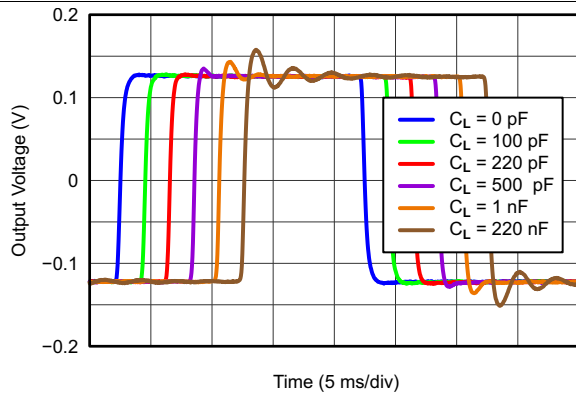


Figure 43. Small-Signal Response Over Capacitive Loads (G = 5)

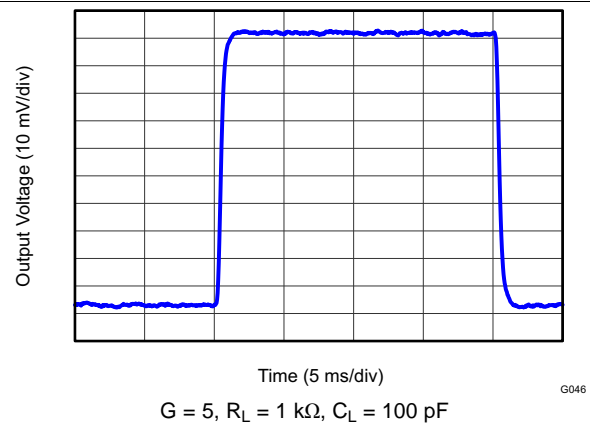


Figure 44. Small-Signal Response

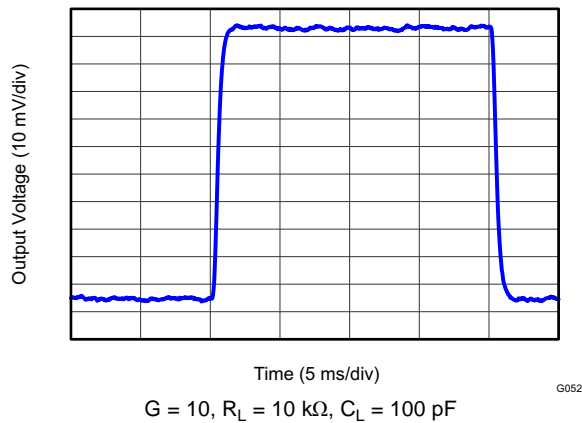


Figure 45. Small-Signal Response

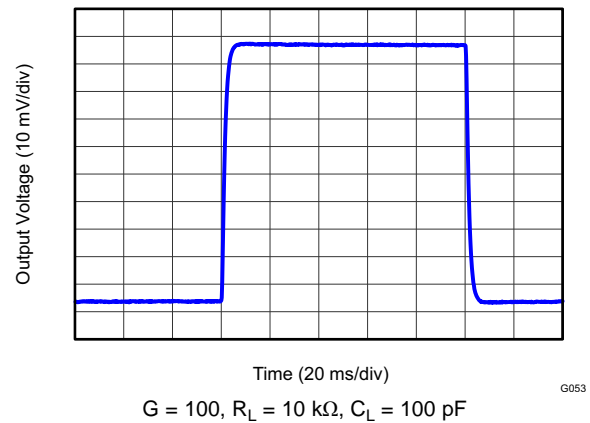


Figure 46. Small-Signal Response

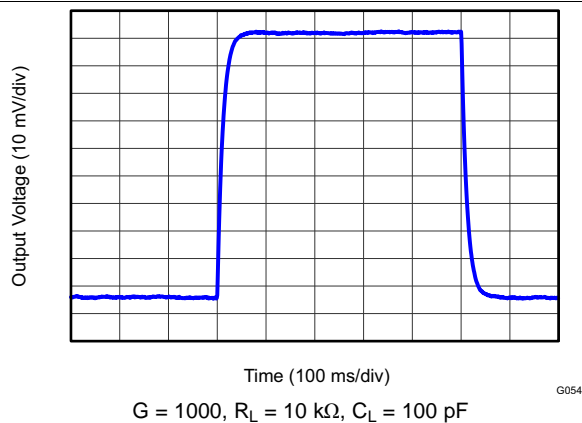


Figure 47. Small-Signal Response

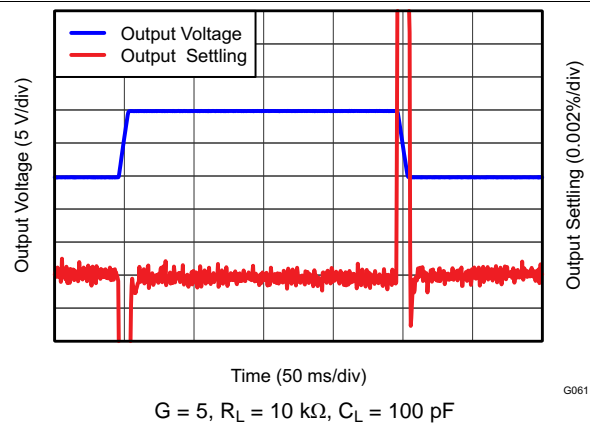


Figure 48. Large-Signal Response and Settling Time

Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, and $G = 5$ (unless otherwise noted)

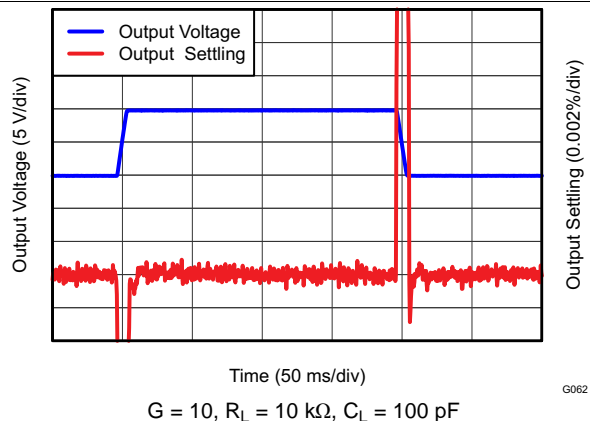


Figure 49. Large-Signal Response and Settling Time

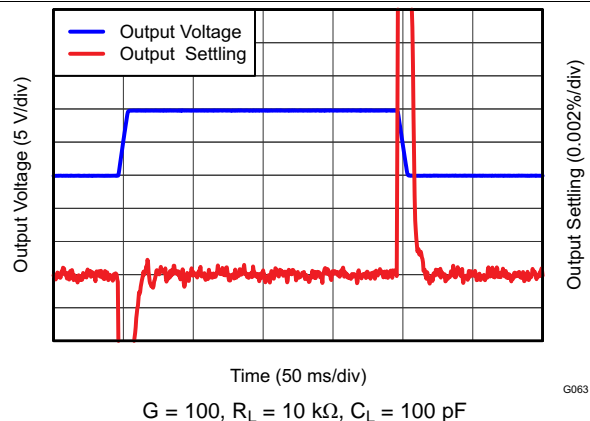


Figure 50. Large-Signal Response and Settling Time

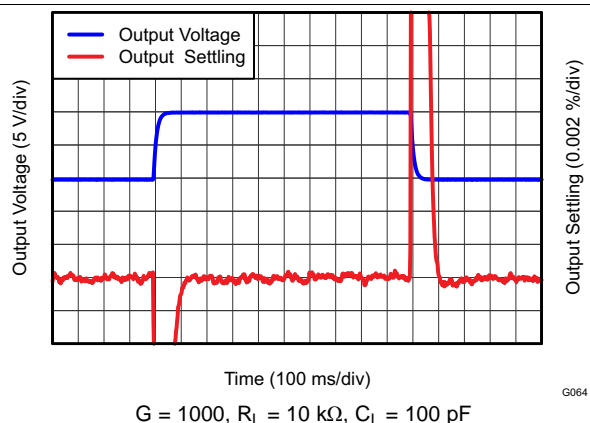


Figure 51. Large-Signal Response and Settling Time

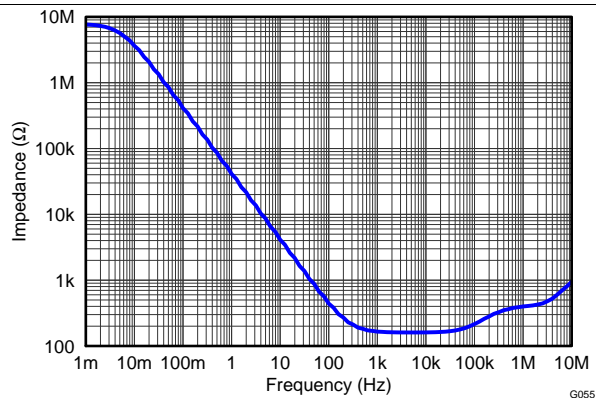


Figure 52. Open-Loop Output Impedance

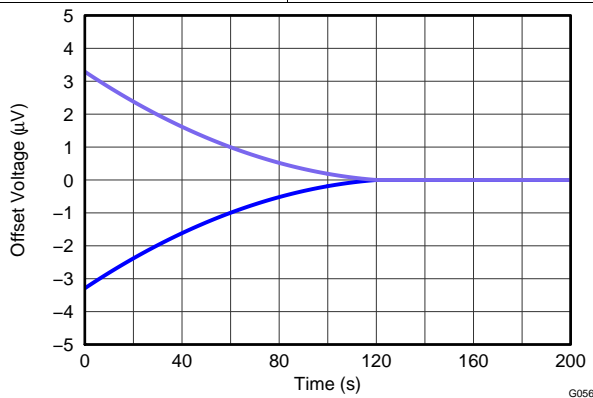


Figure 53. Change In Input Offset Voltage vs Warm-Up Time

7 Detailed Description

7.1 Overview

The INA827 is a monolithic instrumentation amplifier (INA) based on a 36-V and a current feedback input architecture. The INA827 also integrates laser-trimmed resistors to ensure excellent common mode rejection and low gain error. The combination of the current feedback input and the precision resistors allows this device to achieve outstanding dc precision as well as frequency response and high frequency common mode rejection(TBD this is more like a Layout text. Overview is generally an overview of the device.)

The Overview section provides a top-level description of what the device is and what it does. Detailed descriptions of the features and functions appear in subsequent subsections. Guidelines • Include a summary of standards met by the device (if any). • List modes and states of operation (from the user's perspective) and key features within each functional mode for quick reference. Use the following sections to provide detail on these modes and features.

7.2 Functional Block Diagram

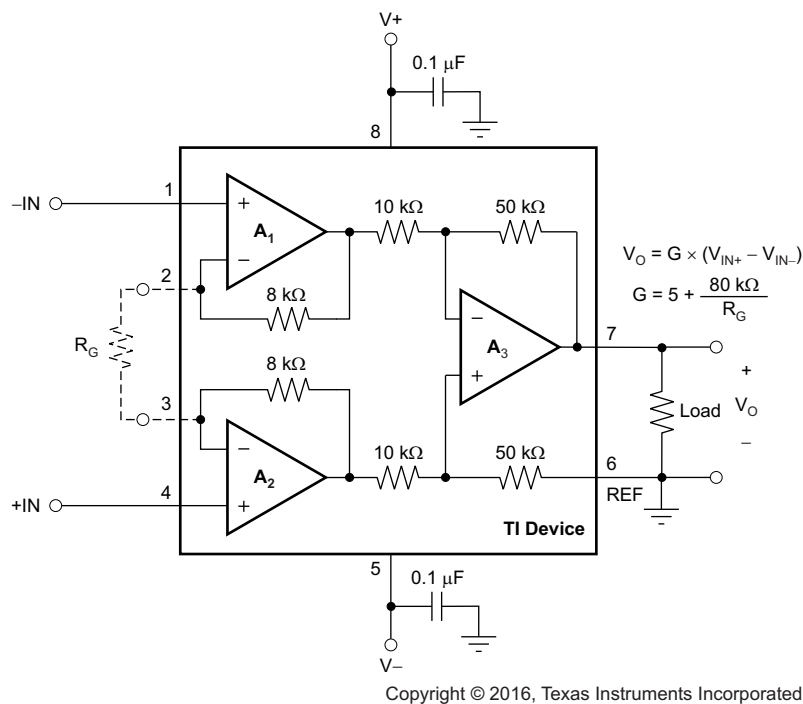


Figure 54. INA827 Block Diagram

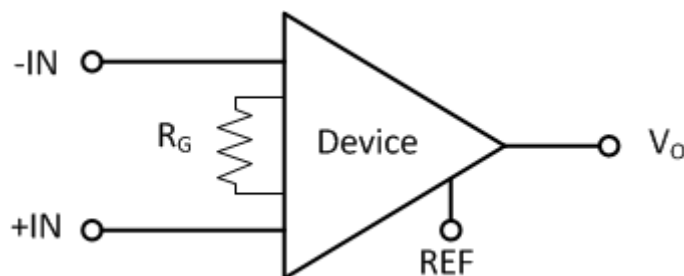


Figure 55. Simplified Block Diagram (TBD only simplified op amp goes here but this is a PNG and I can't edit it)

7.3 Feature Description

7.3.1 Setting the Gain

Device gain is set by a single external resistor (R_G), connected between pins 2 and 3. The value of R_G is selected according to [Equation 1](#):

$$5 + \left[\frac{80 \text{ k}\Omega}{R_G} \right] \quad (1)$$

[Table 1](#) lists several commonly-used gains and resistor values. The on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA827.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G (Ω)
5	—	—
10	16.00k	15.8k
20	5.333k	5.36k
50	1.778k	1.78k
100	842.1	845
200	410.3	412
500	161.6	162
1000	80.40	80.6

7.3.1.1 Gain Drift

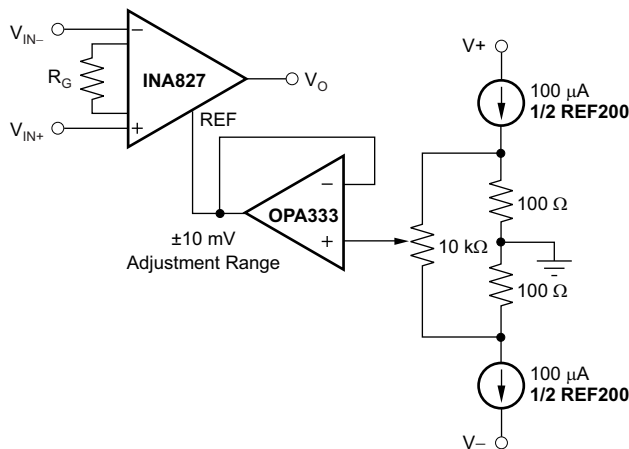
The stability and temperature drift of the external gain setting resistor (R_G) also affects gain. The R_G contribution to gain accuracy and drift can be directly inferred from the gain of [Equation 1](#).

The best gain drift of 1 ppm per degree Celsius can be achieved when the INA827 uses $G = 5$ without R_G connected. In this case, the gain drift is limited only by the slight temperature coefficient mismatch of the integrated 50-k Ω resistors in the differential amplifier (A_3). At gains greater than 5, the gain drift increases as a result of the individual drift of the resistors in the feedback of A_1 and A_2 , relative to the drift of the external gain resistor R_G . Process improvements to the temperature coefficient of the feedback resistors now enable a maximum gain drift of the feedback resistors to be specified at 35 ppm per degree Celsius, thus significantly improving the overall temperature stability of applications using gains greater than 5.

Low resistor values required for high gains can make wiring resistance important. Sockets add to wiring resistance and contribute additional gain error (such as possible unstable gain errors) at gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitances greater than a few picofarads at R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency; see the [Typical Characteristics](#) section.

7.3.2 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF pin. Figure 56 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF pin is summed at the output. The op amp buffer provides low impedance at the REF pin to preserve good common-mode rejection.



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Figure 56. Optional Trimming of Output Offset Voltage

7.3.3 Input Common-Mode Range

The linear input voltage range of the INA827 input circuitry extends from the negative supply voltage to 1 V below the positive supply, and maintains 88-dB (minimum) common-mode rejection throughout this range. The common-mode range for most common operating conditions is described in Figure 14 and Figure 35 through Figure 38. The INA827 can operate over a wide range of power supplies and V_{REF} configurations, thus making a comprehensive guide to common-mode range limits for all possible conditions impractical to provide.

The most commonly overlooked overload condition occurs when a circuit exceeds the output swing of A_1 and A_2 , which are internal circuit nodes that cannot be measured. Calculating the expected voltages at the output of A_1 and A_2 (see Figure 57) provides a check for the most common overload conditions. The A_1 and A_2 designs are identical and the outputs can swing to within approximately 100 mV of the power-supply rails. For example, when the A_2 output is saturated, A_1 can continue to be in linear operation and responding to changes in the noninverting input voltage. This difference can give the appearance of linear operation but the output voltage is invalid.

A single-supply instrumentation amplifier has special design considerations. To achieve a common-mode range that extends to single-supply ground, the INA827 employs a current-feedback topology with PNP input transistors; see Figure 57. The matched PNP transistors (Q_1 and Q_2) shift the input voltages of both inputs up by a diode drop and (through the feedback network) shift the output of A_1 and A_2 by approximately +0.8 V. With both inputs and V_{REF} at single-supply ground (negative power supply), the output of A_1 and A_2 is well within the linear range, allowing differential measurements to be made at the GND level. As a result of this input level-shifting, the voltages at pins 2 and 3 are not equal to the respective input pin voltages (pins 1 and 4). For most applications, this inequality is not important because only the gain-setting resistor connects to these pins.

7.3.4 Inside the INA827

See Figure 61 for a simplified representation of the INA827. A more detailed diagram (shown in Figure 57) provides additional insight into the INA827 operation.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

The differential input voltage is buffered by Q_1 and Q_2 and is applied across R_G , causing a signal current to flow through R_G , R_1 , and R_2 . The output difference amplifier (A_3) removes the common-mode component of the input signal and refers the output signal to the REF pin.

The equations shown in Figure 57 describe the output voltages of A_1 and A_2 . The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V higher than the input voltages.

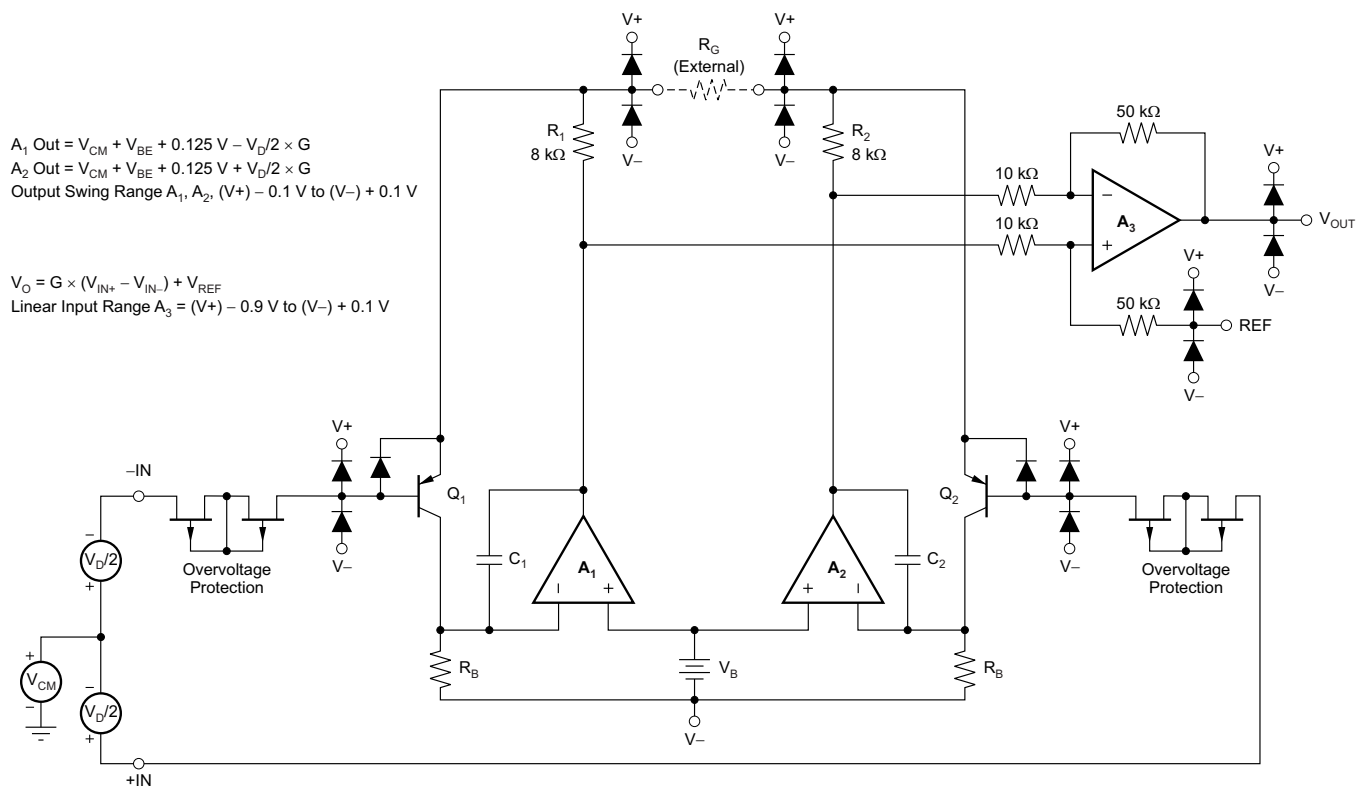


Figure 57. INA827 Simplified Circuit Diagram

7.3.5 Input Protection

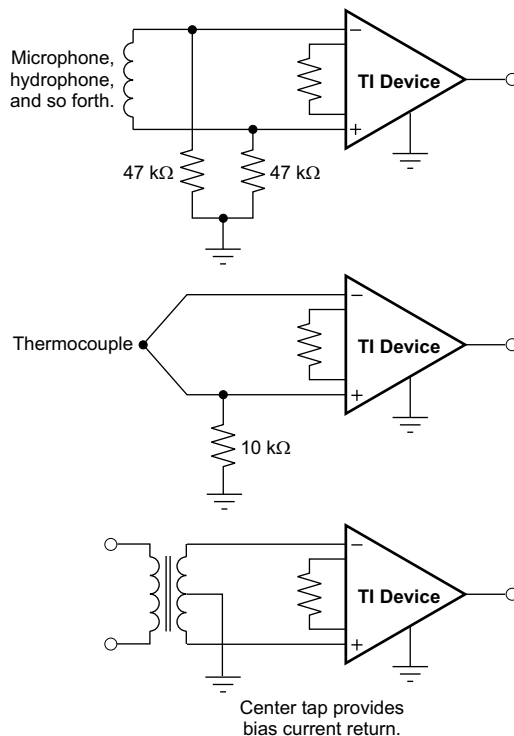
The INA827 inputs are individually protected for voltages up to $\pm 40 \text{ V}$. For example, a condition of -40 V on one input and $+40 \text{ V}$ on the other input does not cause damage. However, if the input voltage exceeds $[(V-) - 2 \text{ V}]$ and the signal source current drive capability exceeds 3.5 mA , the output voltage switches to the opposite polarity; see Figure 14. This polarity reversal can easily be avoided by adding a $10\text{-k}\Omega$ resistance in series with both inputs.

Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 8 mA . Figure 14 illustrates this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

7.3.6 Input Bias Current Return Path

The INA827 input impedance is extremely high—approximately 20 G Ω . However, a path must be provided for the input bias current of both inputs. This input bias current is typically 35 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. [Figure 58](#) shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the INA827 common-mode range, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (as shown in the thermocouple example in [Figure 58](#)). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.



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Figure 58. Providing an Input Common-Mode Current Path

7.3.7 Reference Pin

The INA827 output voltage is developed with respect to the voltage on the reference pin. Often, in dual-supply operation, the reference pin (pin 6) is connected to the low-impedance system ground. Offsetting the output signal to a precise mid-supply level (for example, 2.5 V in a 5-V supply environment) can be useful in single-supply operation. The signal can be shifted by applying a voltage to the device REF pin, which can be useful when driving a single-supply ADC.

For best performance, keep any source impedance to the REF pin below 5 Ω . Referring to [Figure 61](#), the reference resistor is at one end of a 50-k Ω resistor. Additional impedance at the REF pin adds to this 50-k Ω resistor. The imbalance in resistor ratios results in degraded common-mode rejection ratio (CMRR).

[Figure 59](#) shows two different methods of driving the reference pin with low impedance. The [OPA330](#) is a low-power, chopper-stabilized amplifier and therefore offers excellent stability over temperature. The OPA330 is available in the space-saving SC70 and even smaller chip-scale package. The [REF3225](#) is a precision reference in a small SOT23-6 package.

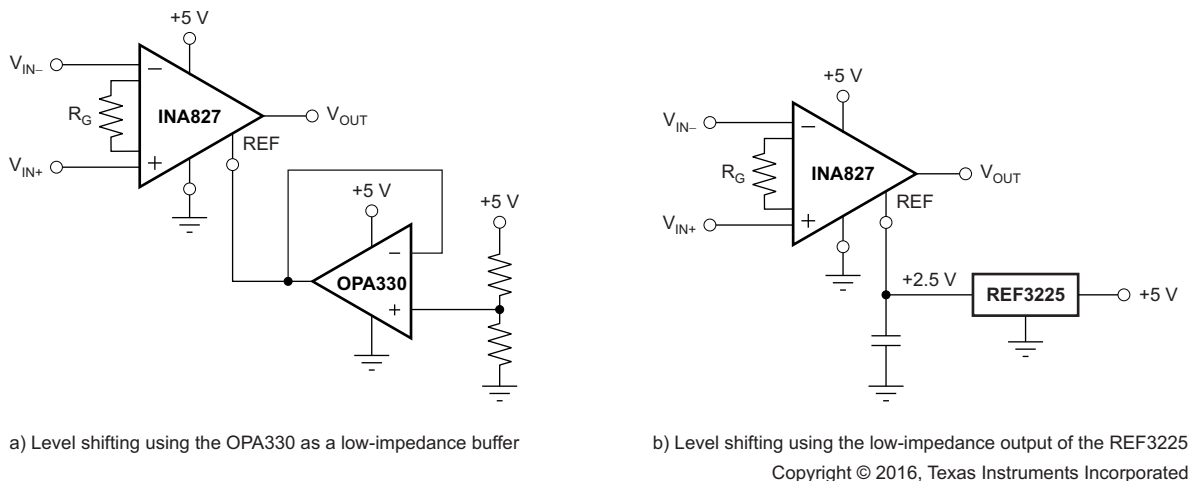


Figure 59. Options for Low-Impedance Level Shifting

7.3.8 Dynamic Performance

[Figure 19](#) illustrates that, despite having low quiescent current of only 200 μ A, the INA827 achieves much wider bandwidth than other instrumentation amplifiers (INAs) in its class. This achievement is a result of using TI's proprietary high-speed precision bipolar process technology. The current-feedback topology provides the INA827 with wide bandwidth even at high gains. Settling time also remains excellent at high gain because of a 1.5-V/ μ s high slew rate.

7.3.9 Operating Voltage

The INA827 operates over a power-supply range of +3 V to +36 V (± 1.5 V to ± 18 V). Supply voltages higher than 40 V (± 20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the [Typical Characteristics](#) section.

7.3.9.1 Low-Voltage Operation

The INA827 can operate on power supplies as low as ± 1.5 V. Most parameters vary only slightly throughout this supply voltage range; see the [Typical Characteristics](#) section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of the internal nodes limit the input common-mode range with low power-supply voltage. [Figure 7](#) to [Figure 13](#) and [Figure 35](#) to [Figure 38](#) describe the linear operation range for various supply voltages, reference connections, and gains.

7.3.10 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, these errors must be minimized by choosing high-precision components such as the INA827 that have improved specifications in critical areas that effect overall system precision. [Figure 60](#) shows an example application.

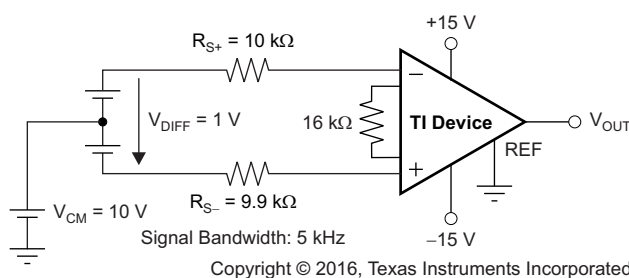


Figure 60. Example Application With $G = 10$ V/V and 1-V Differential Voltage

Resistor-adjustable INAs such as the INA827 yield the lowest gain error at $G = 5$ because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 5 (for instance, $G = 10$ V/V or $G = 100$ V/V) gain error becomes a significant error source because of the resistor drift contribution of the feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, gain drift is by far the largest error contributor compared to other drift errors (such as offset drift). The INA827 offers the lowest gain error over temperature in the marketplace for both $G > 5$ and $G = 5$ (no external gain resistor). Table 2 summarizes the major error sources in common INA applications and compares the two cases of $G = 5$ (no external resistor) and $G = 10$ (with a 16-k Ω external resistor). As shown in Table 2, although the static errors (absolute accuracy errors) in $G = 5$ are almost twice as great as compared to $G = 10$, there is a great reduction in drift errors because of the significantly lower gain error drift. In most applications, these static errors can readily be removed during calibration in production. All calculations refer the error to the input for easy comparison and system evaluation.

Table 2. Error Calculation

ERROR SOURCE	ERROR CALCULATION	INA827		
		SPECIFICATION	G = 10 ERROR (ppm)	G = 1 ERROR (ppm)
ABSOLUTE ACCURACY AT +25°C				
Input offset voltage (μV)	V _{OSI} / V _{DIFF}	150	150	150
Output offset voltage (μV)	V _{OSO} / (G × V _{DIFF})	2000	200	400
Input offset current (nA)	I _{OS} × maximum (R _{S+} , R _{S-}) / V _{DIFF}	5	50	50
CMRR (dB)	V _{CM} / (10 ^{CMRR / 20} × V _{DIFF})	94 (G = 10), 88 (G = 5)	200	398
Total absolute accuracy error (ppm)			600	998
DRIFT TO +105°C				
Gain drift (ppm/°C)	GTC × (T _A – 25)	25 (G = 10), 1 (G = 5)	2000	80
Input offset voltage drift (μV/°C)	(V _{OSL_TC} / V _{DIFF}) × (T _A – 25)	5	200	200
Output offset voltage drift (μV/°C)	[V _{OSO_TC} / (G × V _{DIFF})] × (T _A – 25)	30	240	240
Total drift error (ppm)			2440	760
RESOLUTION				
Gain nonlinearity (ppm of FS)		5	5	5
Voltage noise (1 kHz)	$\sqrt{BW} \times \sqrt{e_{NI}^2 + \left(\frac{e_{NO}}{G}\right)^2} \times \frac{6}{V_{DIFF}}$	e _{NI} = 17 e _{NO} = 250	6	6
Total resolution error (ppm)			11	11
TOTAL ERROR				
Total error	Total error = sum of all error sources		3051	1769

7.4 Device Functional Modes

The INA827 has a single functional mode and is operational when the power-supply voltage is greater than 3 V (± 1.5 V). The maximum power-supply voltage for the INA827 is 36 V (± 18 V).

8 Application and Implementation

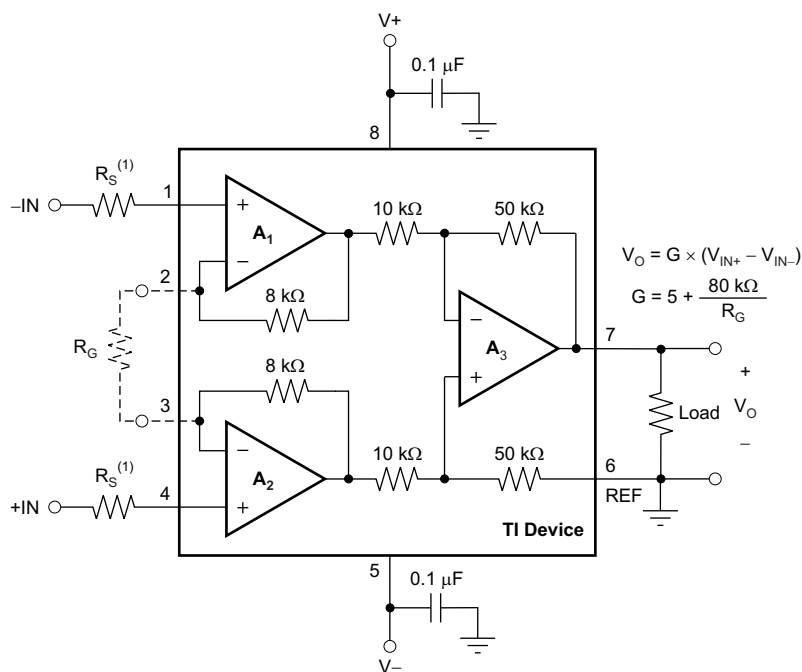
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 61 shows the basic connections required for device operation. Good layout practice mandates that bypass capacitors are placed as close to the device pins as possible.

The INA827 output is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to assure good common-mode rejection. Although 5 Ω or less of stray resistance can be tolerated when maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

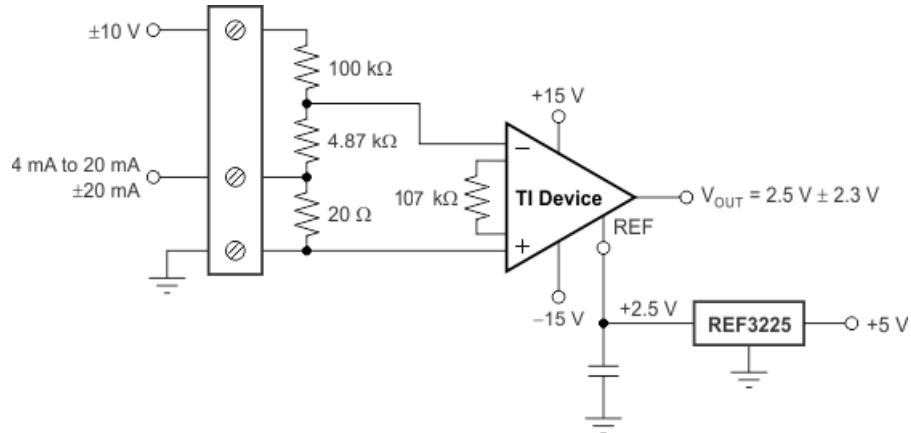


(1) This resistor is optional if the input voltage remains above $[(V-) - 2\text{ V}]$ or if the signal source current drive capability is limited to less than 3.5 mA. See the [Input Protection](#) section for more details.

Figure 61. Basic Connections

8.2 Typical Application

An example programmable logic controller (PLC) input application using an INA827 is shown in [Figure 62](#).



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Figure 62. ±10-V, 4-mA to 20-mA PLC Input

8.2.1 Design Requirements

This design has these requirements:

- Supply voltage: ±15 V, 5 V
- Inputs: ±10 V, ±20 mA
- Output: 2.5 V, ±2.3 V

8.2.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in [Figure 62](#): current input and voltage input. This design requires $R_1 \gg R_2 \gg R_3$. Given this relationship, the current input mode transfer function is given by [Equation 2](#).

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF}$$

where

- G represents the gain of the instrumentation amplifier (2)

The transfer function for the voltage input mode is shown by [Equation 3](#).

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left[V_{IN} \times \frac{R_2}{R_1 + R_2}\right] \times G + V_{REF} \quad (3)$$

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. 100 kΩ is selected for R_1 because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2 . 20 Ω for R_3 is selected because that resistance value is much smaller than R_1 and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

[Equation 4](#) can be used to calculate R_2 given $V_D = \pm 400$ mV, $V_{IN} = \pm 10$ V, and $R_1 = 100$ kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167 \text{ k}\Omega \quad (4)$$

The value obtained from [Equation 4](#) is not a standard 0.1% value, so 4.12 kΩ is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

The ideal gain of the instrumentation amplifier is calculated with [Equation 5](#).

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8 \text{ V} - 2.5 \text{ V}}{400 \text{ mV}} = 5.75 \frac{\text{V}}{\text{V}} \quad (5)$$

Typical Application (continued)

Using the INA827 gain equation, the gain-setting resistor value is calculated as shown by Equation 6.

$$G_{\text{INA827}} = 5 + \frac{80 \text{ k}\Omega}{R_G} \rightarrow R_G = \frac{80 \text{ k}\Omega}{G_{\text{INA827}} - 5} = \frac{80 \text{ k}\Omega}{5.75 - 5} = 107 \text{ k}\Omega \quad (6)$$

107 kΩ is a standard 0.1% resistor value that can be used in this design. Finally, the output RC filter components are selected to have a –3-dB cutoff frequency of 1 MHz.

8.2.3 Application Curves

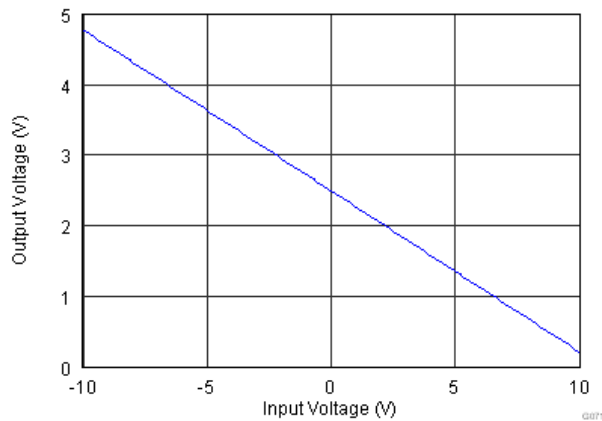


Figure 63. PLC Output Voltage vs Input Voltage

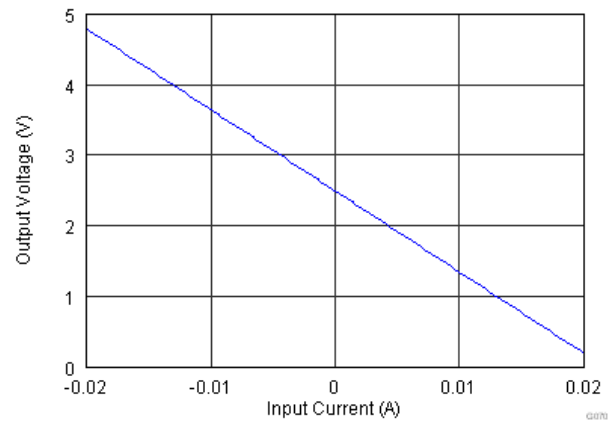


Figure 64. PLC Output Voltage vs Input Current

9 Power Supply Recommendations

The nominal performance of the INA827 is specified with a supply voltage of $\pm 15\text{ V}$ and a mid-supply reference voltage. The device can also be operated using power supplies from $\pm 1.5\text{ V}$ (3 V) to $\pm 18\text{ V}$ (36 V) and non mid-supply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are illustrated in the [Typical Characteristics](#) section.

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place 0.1- μF bypass capacitors close to the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

10.1.1 CMRR vs Frequency

The INA827 pinout is optimized for achieving maximum CMRR performance over a wide range of frequencies. However, care must be taken to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS[®] relays to change the value of R_G , choose the component so that the switch capacitance is as small as possible.

10.2 Layout Example

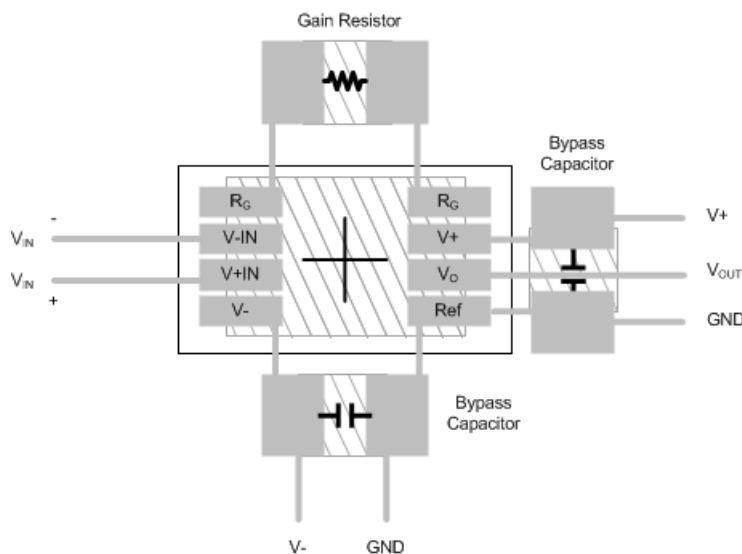


Figure 65. INA827 Example Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 《具有轨至轨输出的 **INA826** 精密 200 μ A 电源电流、3V 至 36V 电源仪表放大器》(SBOS562)
- 《**OPAx330** 50 μ V VOS、0.25 μ V/ $^{\circ}$ C、35 μ A CMOS 运算放大器零漂移系列》(SBOS432)
- 《**REF32xx** 4ppm/ $^{\circ}$ C、100 μ A、SOT23-6 系列电压基准》(文献编号：SBVS058)
- (待定) 是否列出其他内容？

11.2 接收文档更新通知

要接收文档更新通知，请导航至 **Ti.com** 上的器件产品文件夹。单击右上角的**通知我** 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《**使用条款**》。

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设计支持 **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA827AIDGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	IPSI
INA827AIDGK.B	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	IPSI
INA827AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG SN	Level-2-260C-1 YEAR	-40 to 125	IPSI
INA827AIDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	IPSI

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA827AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA827AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA827AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
INA827AIDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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