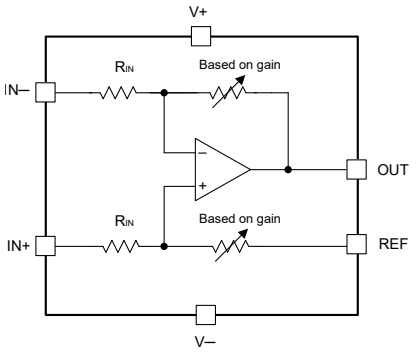
INA600 Low-Power, 2.7V to 40V Attenuating Difference Amplifier With >1MΩ Input Impedance for Cost-Optimized Designs

1 Features

- Ultra-high input impedance: >1MΩ
- Supply range: 2.7V (±1.35V) to 40V (±20V)
- Input voltage range: (V–) – 40V to (V–) + 85V
- Precision voltage monitoring in noisy systems:
  - CMRR: 100dB (typical, G = 1/5)
  - Gain error: ±0.01% (typical)
  - Gain drift : ±1ppm/°C (typical)
- Available gains:
  - INA600A: 1/5
  - INA600B: 1/10
  - INA600C: 1/12
  - INA600D: 1/18
  - INA600E: 1/24
  - INA600F: 1/36
- –3dB bandwidth: ≥200kHz
- Drives 400pF with ≤20% overshoot (typical)
- Low quiescent current: 65µA (typical)
- Specified temperature range: –40°C to +125°C

2 Applications

- Battery cell formation and test equipment
- String inverters
- EV charging station power modules
- Battery energy storage systems
- Power tools
- Industrial AC/DC
- Wearable fitness and activity monitors



INA600 Simplified Internal Schematic

3 Description

The INA600 is a voltage-sensing difference amplifier with precision matched resistors that offer attenuating gain options. The precision matched integrated resistors saves BOM costs and board space by removing the need for precise and low tolerance external resistors.

The INA600 offers high input impedance of >1MΩ and low quiescent current of 65µA. The device can handle up to –40V to +85V of input voltage, attenuate the voltage down with great accuracy, and interface the voltage to the low voltage ADC while rejecting any common-mode errors such as ground bounce, switching ripples, AC mains and so forth. The device achieves a maximum gain error of ±0.05%, and a maximum gain drift of 5ppm/°C along with 89dB of minimum common-mode rejection ratio (G = 1/5).

This combination of specifications makes the INA600 a great choice for a variety of level translation, differential to single-ended applications, including any voltage monitoring of batteries or power rails. The INA600 interfaces directly to low-speed, analog-to-digital converters (ADC) and therefore is an excellent choice for replacing discrete implementation of difference amplifiers built with commodity amplifiers and discrete resistors. The INA600 is offered in standard 6-pin SOT-23 and SC70 packages.

Package Information

PART NUMBER(1)	VERSION	PACKAGE(2)	PACKAGE SIZE(5)
INA600	A	DBV (SOT-23, 6)	2.9mm × 2.8mm
		DCK (SC70, 6)(3)	2.1mm × 1.25mm
	B	DBV (SOT-23, 6)	2.9mm × 2.8mm
		DCK (SC70, 6)(3)	2.1mm × 1.25mm
	C(4)	DBV (SOT-23, 6) (3)	2.9mm × 2.8mm
		DCK (SC70, 6)(3)	2.1mm × 1.25mm
	D(4)	DBV (SOT-23, 6) (3)	2.9mm × 2.8mm
		DCK (SC70, 6)(3)	2.1mm × 1.25mm
	E(4)	DBV (SOT-23, 6) (3)	2.9mm × 2.8mm
		DCK (SC70, 6)(3)	2.1mm × 1.25mm
	F	DBV (SOT-23, 6)	2.9mm × 2.8mm
		DCK (SC70, 6)(3)	2.1mm × 1.25mm

(1) See Device Comparison.
(2) For more information, see Section 11.
(3) This package is preview only.
(4) This version is preview only.
(5) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Device Comparison Table

DEVICE	VERSION	GAIN	NO. OF CHANNELS	PACKAGE LEADS	
				SOT-23 DBV	SC70 DCK(1)
INA600	A	1/5	1	6	6
	B	1/10	1	6	6
	C(2)	1/12	1	6	6
	D(2)	1/18	1	6	6
	E(2)	1/24	1	6	6
	F	1/36	1	6	6

(1) Package is preview only.
(2) Version is preview only.

5 Pin Configuration and Functions

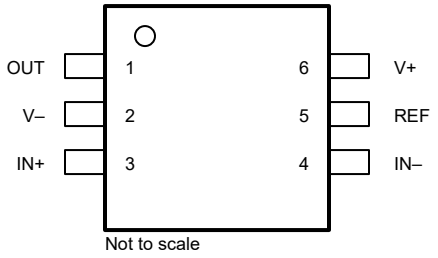


Figure 5-1. INA600 DBV Package, 6-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	SOT-23		
IN–	4	I	Negative (inverting) input
IN+	3	I	Positive (noninverting) input
OUT	1	O	Output
REF	5	I	Reference input
V–	2	—	Negative supply
V+	6	—	Positive supply

(1) I = input, O = output.

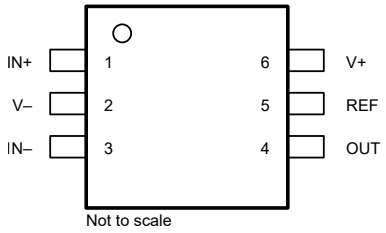


Figure 5-2. INA600 DCK Package, 6-Pin SC70 (Top View)

Table 5-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	SC70		
IN–	3	I	Negative (inverting) input
IN+	1	I	Positive (non-inverting) input
OUT	4	O	Output
REF	5	I	Reference input
V–	2	—	Negative supply
V+	6	—	Positive supply

(1) I = input, O = output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single Supply		42	V
	Dual Supply		±21	V
Signal input pins	Voltage	(V–) – 42	(V–) + 87	V
	Current	–10	10	mA
Output short-circuit(2)		Continuous		
Operating temperature, T_A		–55	150	°C
Junction temperature, T_J			150	
Storage temperature, T_{stg}		–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(1)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage V_S = (V+) – (V–)	Single-supply	2.7	40	V
	Dual-supply	±1.35	±20	
Input voltage range	Single-supply / Dual-supply	(V–) – 40	(V–) + 85	V
C_{BYP}	Bypass capacitor on the power supply pins (1)	0.1		µF
Specified temperature	Specified temperature	–40	125	°C

(1) For C_{BYP}, use low-ESR ceramic capacitors between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Ensure that C_{BYP} is placed as close to the device as possible and the supply trace routes through C_{BYP} before reaching the supply pin.

6.4 Thermal Information

THERMAL METRIC[1]		INA600		UNIT
		DCK (SC70)	DBV (SOT-23)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	166.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	85.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	48.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	24.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	48.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics - INA600A

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1/5, R_L = 10kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET							
V_{OSO}	Offset voltage, RTO	V_S = 2.7V and 40V	T_A = 25°C		±1.1	±4.5	mV
	Offset voltage over T, RTO		T_A = –40°C to 125°C			±5.0	mV
	Offset temp drift, RTO[1]		T_A = –40°C to 125°C		±2	±10	µV/°C
PSRR	Power-supply rejection ratio, RTO	V_S = 4V to 40V	T_A = 25°C		2.5	10	µV/V
PSRR	Power-supply rejection ratio, RTO	V_S = 2.7V to 40V	T_A = 25°C		3	15	µV/V
INPUT IMPEDANCE							
R_{IN-DM}	Differential Resistance				2400		kΩ
R_{IN-CM}	Common-mode Resistance				635		kΩ
INPUT VOLTAGE							
V_{CM}	Input common-mode Range	V_S = 2.7V		(V–) – 2.5		(V–) + 22.5	V
V_{CM}	Input common-mode Range	V_S = 4.5V		(V–) – 25		(V–) + 50	V
V_{CM}	Input common-mode Range	V_S = 9V to 40V		(V–) – 40		(V–) + 85	V
CMRR DC	Common-mode rejection ratio, RTO	2.7V ≤ V_S < 4.5V	V_{CM} = (V–) – 2.5V to (V–) + 22.5V	91			dB
CMRR DC	Common-mode rejection ratio, RTO	4.5V ≤ V_S < 9V	V_{CM} = (V–) – 25V to (V–) + 50V	91			dB
CMRR DC	Common-mode rejection ratio, RTO	9V ≤ V_S ≤ 40V	V_{CM} = (V–) – 40V to (V–) + 85V	91	114		dB
NOISE VOLTAGE							
e_{NI}	Output voltage noise density	V_S = 40V	f = 1kHz		245		nV/√Hz
			f = 10kHz		240		
E_{NI}	Output voltage noise		f_B = 0.1Hz to 10Hz		13.5		μV_{PP}
			f_B = 0.1Hz to 150kHz		650		μV_{PP}
GAIN							
GE	Gain error[2]	V_S = 2.7V, V_{REF} = V_{MID}	V_O = (V–) + 0.15V to (V+) – 0.15V		±0.003	±0.05	%
	Gain drift vs temperature[2]	V_S = 2.7V, V_{REF} = V_{MID}	T_A = –40°C to 125°C			±5	ppm/°C
OUTPUT							

6.5 Electrical Characteristics - INA600A (continued)

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1/5, R_L = 10kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	Positive and negative rail headroom	V_S = 40V, V_{REF} = V_S, R_L = 10kΩ to V_{MID}			80	150	mV
V_{OL}		V_S = 40V, V_{REF} = V_S, R_L = 2kΩ to V_{MID}			400	650	mV
C_L Drive	Load capacitance drive	V_O = 100mV step, Overshoot < 20%			200		pF
Z_O	Closed-loop output impedance	f = 10kHz			50		Ω
I_{SC}	Short-circuit current	V_S = 40V			±50		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	V_{IN} = 10mV_{pk-pk}			225		kHz
THD + N	Total harmonic distortion + noise	V_S = 40V, V_{REF} = 2.5V, V_O = 5V_{PP}, R_L = 100kΩ f = 1kHz, 80kHz measurement BW			0.03		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1GHz, V_{IN_EMIRR} = 100mV, Differential Mode			125		dB
SR	Slew rate	V_S = 40V, V_O = 1V step			0.32		V/µs
t_S	Settling time	To 0.1%, V_S = 40V, V_{OUT_STEP} = 1V, C_L = 10pF			10		µs
t_S	Settling time	To 0.01%, V_S = 40V, V_{OUT_STEP} = 1V, C_L = 10pF			16		µs
t_S	Settling time	To 0.1%, V_S = 40V, V_{OUT_STEP} = 5V, C_L = 10pF			18		µs
t_S	Settling time	To 0.01%, V_S = 40V, V_{OUT_STEP} = 5V, C_L = 10pF			24		µs
	Overload recovery	V_S = 2.7V, $V_{IN–}$ = 0V, V_{IN+} = 85V, and V_{REF} = V_S / 2			7.5		µs
REFERENCE INPUT							
REF - V_{IN}	Input voltage range	V_S = 40V, V_{REF} = V_{MID}		(V–)		(V+)	V
REF - G	Reference gain to output				1		V/V
REF - GE	Reference gain error(2)	V_S = 40V			±0.002	±0.05	%
POWER SUPPLY							
V_S	Power-supply voltage	Dual-supply		±1.35		±20	V
I_Q	Quiescent current	V_S = 2.7V			50		µA
I_Q	Quiescent current	V_S = 40V			65	90	µA
		V_S = 40V	T_A = –40°C to 125°C			95	

(1) Offset drifts are uncorrelated.
(2) Minimum and maximum values are specified by characterization.

6.6 Electrical Characteristics - INA600B

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1/10, R_L = 10kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET							
V_{OSO}	Offset voltage, RTO	V_S = 2.7V and 40V	T_A = 25°C		±0.6	±3.0	mV
	Offset voltage over T, RTO		T_A = –40°C to 125°C			±3.5	mV
	Offset temp drift, RTO(1)		T_A = –40°C to 125°C		±1.5	±7	µV/°C
PSRR	Power-supply rejection ratio, RTO	V_S = 4V to 40V	T_A = 25°C		2.5	10	µV/V
PSRR	Power-supply rejection ratio, RTO	V_S = 2.7V to 40V	T_A = 25°C		3	15	µV/V
INPUT IMPEDANCE							
R_{IN-DM}	Differential Resistance				2400		kΩ
R_{IN-CM}	Common-mode Resistance				635		kΩ

6.6 Electrical Characteristics - INA600B (continued)

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1/10, R_L = 10kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CM}	Input common-mode Range	V_S = 2.7V		(V–) – 5		(V–) + 25	V
V_{CM}	Input common-mode Range	V_S = 4.5V		(V–) – 30		(V–) + 55	V
INPUT VOLTAGE							
V_{CM}	Input common-mode Range	V_S = 9V to 40V		(V–) – 40		(V–) + 85	V
CMRR DC	Common-mode rejection ratio, RTO	2.7V ≤ V_S < 4.5V	V_{CM} = (V–) – 5V to (V–) + 25V	97			dB
CMRR DC	Common-mode rejection ratio, RTO	4.5V ≤ V_S < 9V	V_{CM} = (V–) – 30V to (V–) + 55V	97			dB
CMRR DC	Common-mode rejection ratio, RTO	9V ≤ V_S ≤ 40V	V_{CM} = (V–) – 40V to (V–) + 85V	97	125		dB
NOISE VOLTAGE							
e_{NI}	Output voltage noise density	V_S = 40V	f = 1kHz		145		nV/√Hz
			f = 10kHz		155		
E_{NI}	Output voltage noise		f_B = 0.1Hz to 10Hz		9		μV_{PP}
			f_B = 0.1Hz to 150kHz		400		μV_{PP}
GAIN							
GE	Gain error(2)	V_S = 2.7V, V_{REF} = V_{MID}	V_O = (V–) + 0.15V to (V+) – 0.15V		±0.003	±0.05	%
	Gain drift vs temperature(2)	V_S = 2.7V, V_{REF} = V_{MID}	T_A = –40°C to 125°C			±5	ppm/°C
OUTPUT							
V_{OH}	Positive and negative rail headroom	V_S = 40V, V_{REF} = V_S, R_L = 10kΩ to V_{MID}			80	150	mV
V_{OL}		V_S = 40V, V_{REF} = V_S, R_L = 2kΩ to V_{MID}			400	650	mV
C_L Drive	Load capacitance drive	V_O = 100mV step, Overshoot < 20%			200		pF
Z_O	Closed-loop output impedance	f = 10kHz			45		Ω
I_{SC}	Short-circuit current	V_S = 40V			±50		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	V_{IN} = 10mV_{pk-pk}			250		kHz
THD + N	Total harmonic distortion + noise	V_S = 40V, V_{REF} = 2.5V, V_O = 5V_{PP}, R_L = 100kΩ f = 1kHz, 80kHz measurement BW			0.03		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1GHz, V_{IN_EMIRR} = 100mV, Differential Mode			126		dB
SR	Slew rate	V_S = 40V, V_O = 1V step			0.22		V/µs
t_S	Settling time	To 0.1%, V_S = 40V, V_{STEP} = 1V, C_L = 10pF			12		µs
t_S	Settling time	To 0.01%, V_S = 40V, V_{STEP} = 1V, C_L = 10pF			15		µs
	Overload recovery	V_S = 2.7V, $V_{IN–}$ = 0V, V_{IN+} = 85V, and V_{REF} = V_S / 2			11		µs
REFERENCE INPUT							
REF - V_{IN}	Input voltage range	V_S = 40V, V_{REF} = V_{MID}		(V–)		(V+)	V
REF - G	Reference gain to output				1		V/V
REF - GE	Reference gain error(2)	V_S = 40V			±0.002	±0.05	%
POWER SUPPLY							
V_S	Power-supply voltage	Dual-supply		±1.35		±20	V
I_Q	Quiescent current	V_S = 2.7V			50		µA

6.6 Electrical Characteristics - INA600B (continued)

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1/10, R_L = 10kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current	V_S = 40V			65	90	µA
		V_S = 40V	T_A = –40°C to 125°C			95	

(1) Offset drifts are uncorrelated.
(2) Minimum and maximum values are specified by characterization.

6.7 Electrical Characteristics - INA600F

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1/36, R_L = 10kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET							
V_{OSO}	Offset voltage, RTO	V_S = 2.7V and 40V	T_A = 25°C		±0.4	±2.0	mV
	Offset voltage over T, RTO		T_A = –40°C to 125°C			±2.4	mV
	Offset temp drift, RTO(1)		T_A = –40°C to 125°C		±0.8	±4.0	µV/°C
PSRR	Power-supply rejection ratio, RTO	V_S = 4V to 40V	T_A = 25°C		2.5	10	µV/V
PSRR	Power-supply rejection ratio, RTO	V_S = 2.7V to 40V	T_A = 25°C		3	15	µV/V
INPUT IMPEDANCE							
R_{IN-DM}	Differential Resistance	V_S = 4.5V to 40V			2400		kΩ
R_{IN-CM}	Common-mode Resistance	V_S = 2.7V to 4.5V			610		kΩ
V_{CM}	Input common-mode Range	V_S = 2.7V		(V–) – 20		(V–) + 30	V
INPUT VOLTAGE							
V_{CM}	Input common-mode Range	V_S = 4.5V to 40V		(V–) – 40		(V–) + 85	V
CMRR DC	Common-mode rejection ratio, RTO	2.7V ≤ V_S < 4.5V	V_{CM} = (V–) – 20V to (V–) + 30V	109			dB
CMRR DC	Common-mode rejection ratio, RTO	4.5V ≤ V_S ≤ 40V	V_{CM} = (V–) – 40V to (V–) + 85V	109	132		dB
NOISE VOLTAGE							
e_{NI}	Output voltage noise density	V_S = 40V	f = 1kHz		70		nV/√Hz
			f = 10kHz		85		
E_{NI}	Output voltage noise		f_B = 0.1Hz to 10Hz		5.5		$µV_{PP}$
			f_B = 0.1Hz to 150kHz		200		$µV_{PP}$
GAIN							
GE	Gain error(2)	V_S = 2.7V, V_{REF} = V_{MID}	V_O = (V–) + 0.15V to (V+) – 0.15V		±0.003	±0.05	%
	Gain drift vs temperature(2)	V_S = 2.7V, V_{REF} = V_{MID}	T_A = –40°C to 125°C			±5	ppm/°C
OUTPUT							
V_{OH}	Positive and negative rail headroom	V_S = 40V, V_{REF} = V_S, R_L = 10kΩ to V_{MID}			80	150	mV
V_{OL}		V_S = 40V, V_{REF} = V_S, R_L = 2kΩ to V_{MID}			400	650	mV
C_L Drive	Load capacitance drive	V_O = 100mV step, Overshoot < 20%			200		pF
Z_O	Closed-loop output impedance	f = 10kHz			35		Ω
I_{SC}	Short-circuit current	V_S = 40V			±50		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	V_{IN} = 10mV_{pk-pk}			300		kHz

6.7 Electrical Characteristics - INA600F (continued)

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1/36, R_L = 10kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion + noise	V_S = 40V, V_{REF} = 2.5V, V_O = 1V_{PP}, R_L = 100kΩ f = 1kHz, 80kHz measurement BW			0.03		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1GHz, V_{IN_EMIRR} = 100mV, Differential Mode			130		dB
SR	Slew rate	V_S = 40V, V_O = 1V step			0.14		V/µs
t_S	Settling time	To 0.1%, V_S = 40V, V_{OUT_STEP} = 1V, C_L = 10pF			17		µs
t_S	Settling time	To 0.01%, V_S = 40V, V_{OUT_STEP} = 1V, C_L = 10pF			22		µs
	Overload recovery	V_S = 2.7V, $V_{IN–}$ = 0V, V_{IN+} = 85V, and V_{REF} = V_S / 2			13		µs
REFERENCE INPUT							
REF - V_{IN}	Input voltage range	V_S = 40V, V_{REF} = V_{MID}		(V–)		(V+)	V
REF - G	Reference gain to output				1		V/V
REF - GE	Reference gain error(2)	V_S = 40V			±0.002	±0.05	%
POWER SUPPLY							
V_S	Power-supply voltage	Dual-supply		±1.35		±20	V
I_Q	Quiescent current	V_S = 2.7V			50		µA
I_Q	Quiescent current	V_S = 40V			65	90	µA
		V_S = 40V	T_A = –40°C to 125°C			95	

(1) Offset drifts are uncorrelated.
(2) Minimum and maximum values are specified by characterization.

6.8 Typical Characteristics

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)

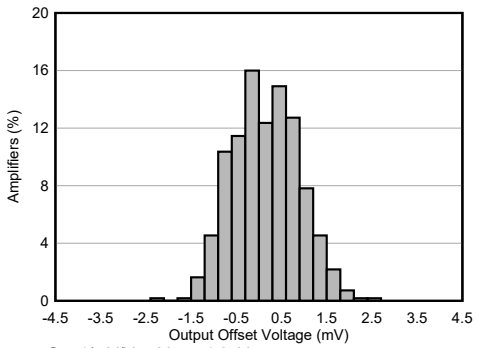


Figure 6-1. Typical Distribution of Output-Referred Offset Voltage (INA600A, V_S = ±1.35V)

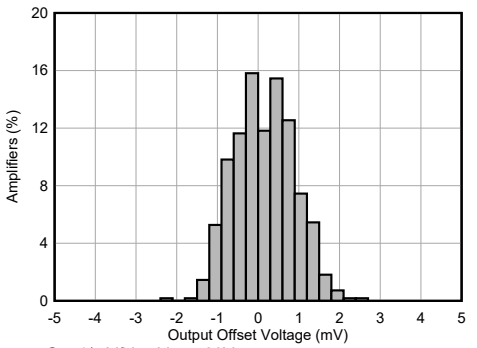


Figure 6-2. Typical Distribution of Output-Referred Offset Voltage (INA600A, V_S = ±20V)

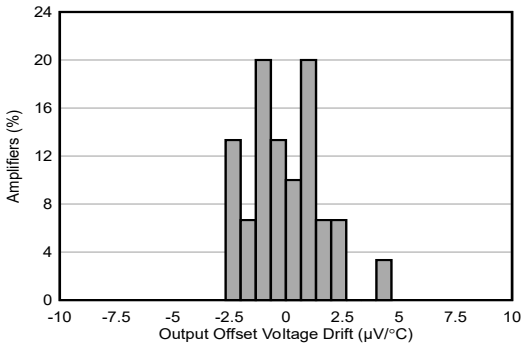


Figure 6-3. Typical Distribution of Output Offset Voltage Drift (INA600A)

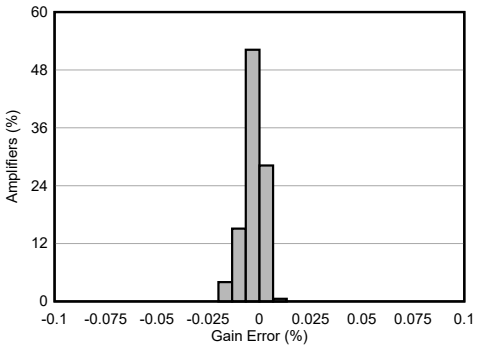


Figure 6-4. Typical Distribution of Gain Error (INA600A)

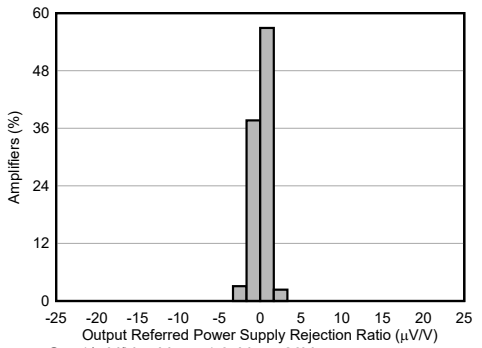


Figure 6-5. Typical Distribution of PSRR (INA600A)

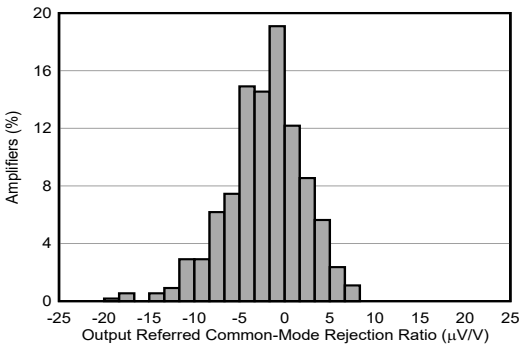


Figure 6-6. Typical Distribution of CMRR (INA600A)

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)

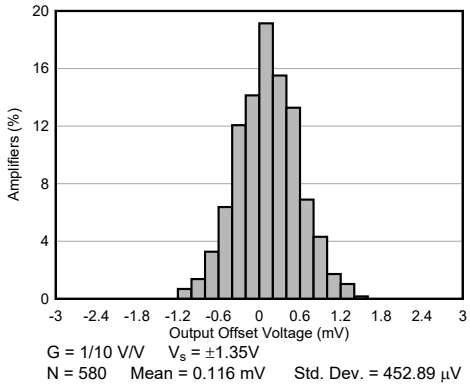


Figure 6-7. Typical Distribution of Output-Referred Offset (INA600B, V_S = ±1.35V)

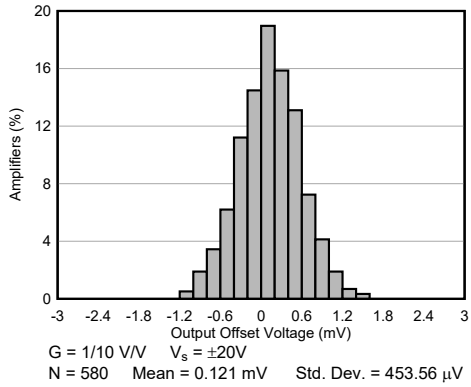


Figure 6-8. Typical Distribution of Output-Referred Offset Voltage (INA600B, V_S = ±20V)

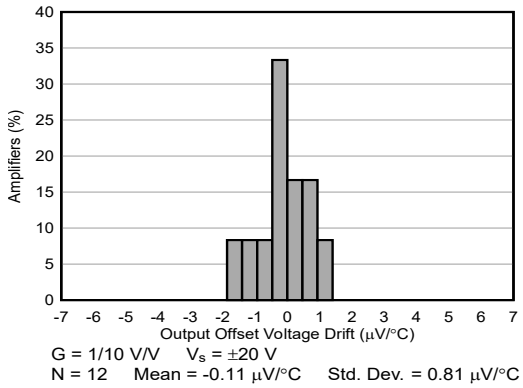


Figure 6-9. Typical Distribution of Output Offset Voltage Drift (INA600B)

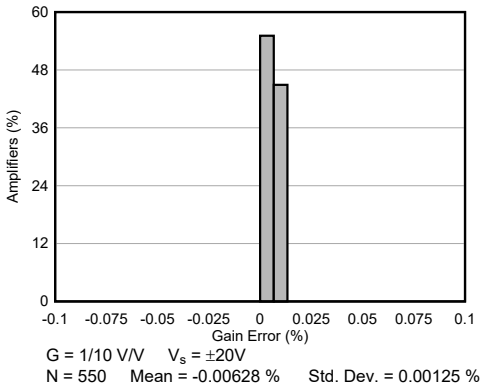


Figure 6-10. Typical Distribution of Gain Error (INA600B)

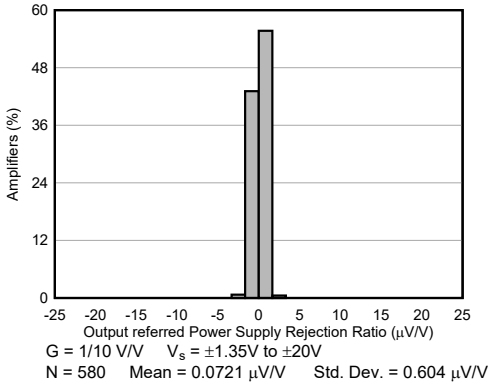


Figure 6-11. Typical Distribution of PSRR (INA600B)

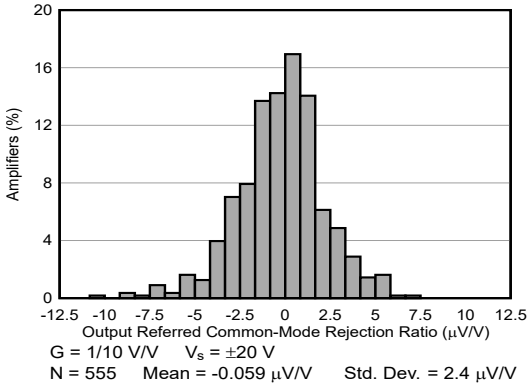


Figure 6-12. Typical Distribution of CMRR (INA600B)

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)

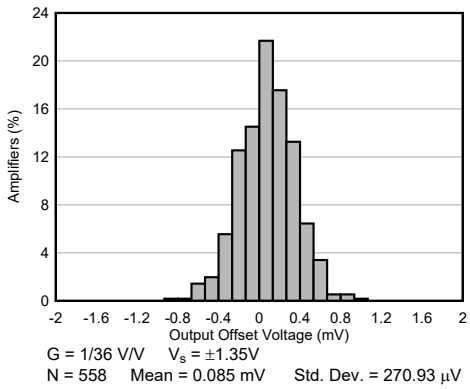


Figure 6-13. Typical Distribution of Output-Referred Offset (INA600F, V_S = ±1.35V)

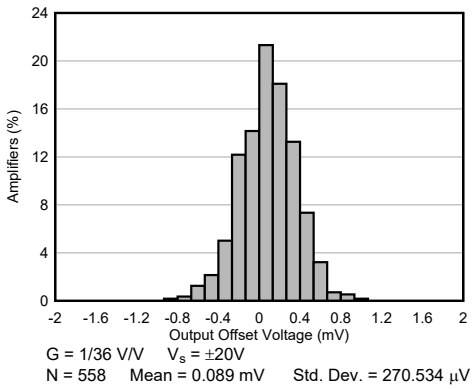


Figure 6-14. Typical Distribution of Output-Referred Offset Voltage (INA600F, V_S = ±20V)

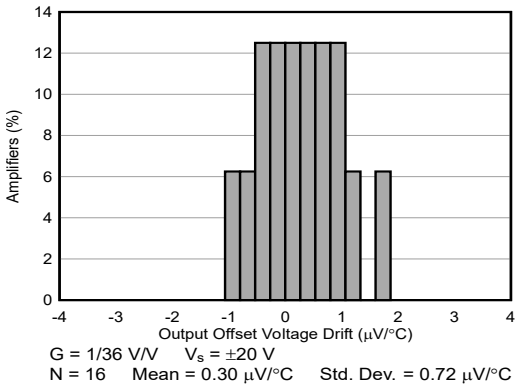


Figure 6-15. Typical Distribution of Output Offset Voltage Drift (INA600F)

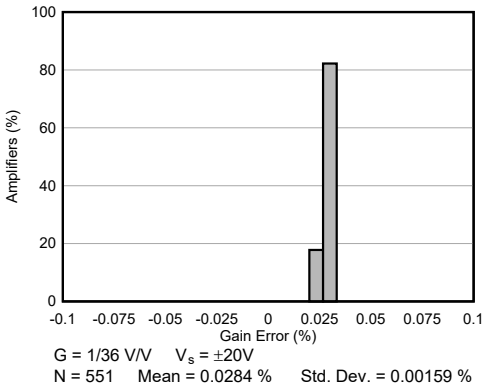


Figure 6-16. Typical Distribution of Gain Error (INA600F)

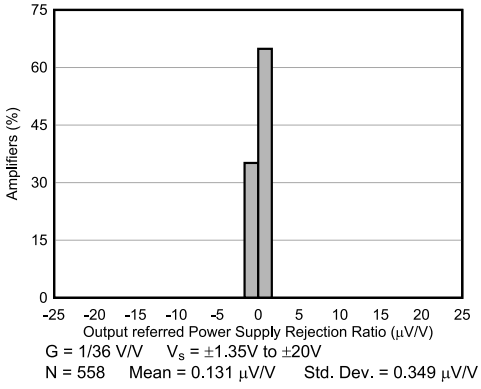


Figure 6-17. Typical Distribution of PSRR (INA600F)

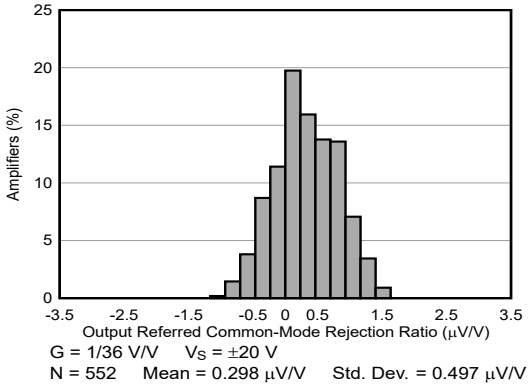
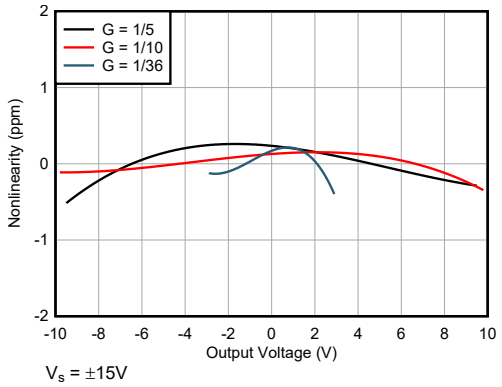


Figure 6-18. Typical Distribution of CMRR (INA600F)

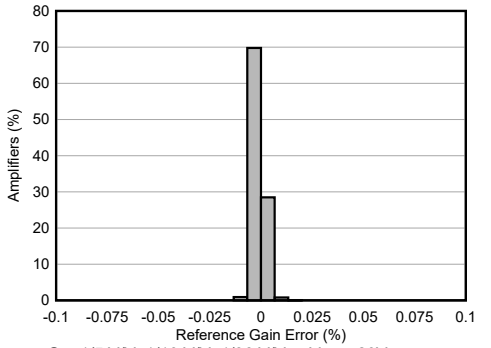
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)



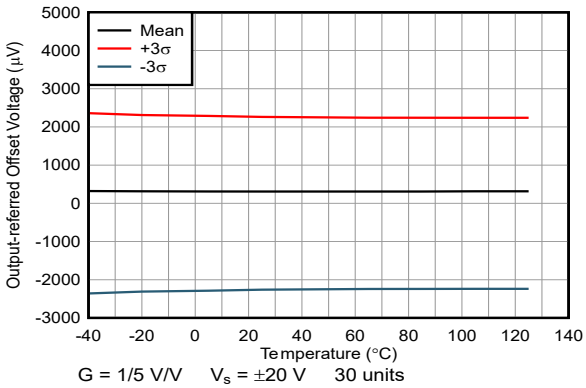
V_s = ±15V

Figure 6-19. Nonlinearity vs Output Voltage, All Gains



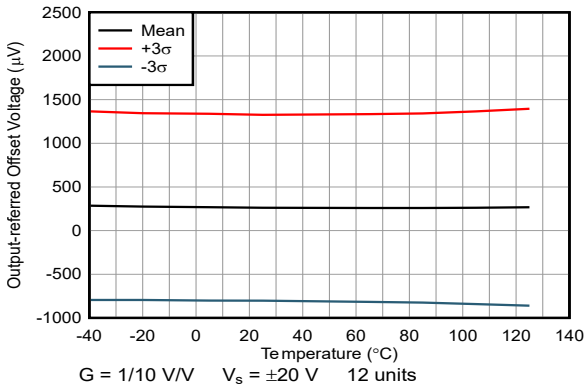
G = 1/5 V/V, 1/10 V/V, 1/36 V/V V_s = ±20V
N = 1651 Mean = -0.000836 % Std. Dev. = 0.0022 %

Figure 6-20. Typical Distribution of Reference Gain Error, All Gains



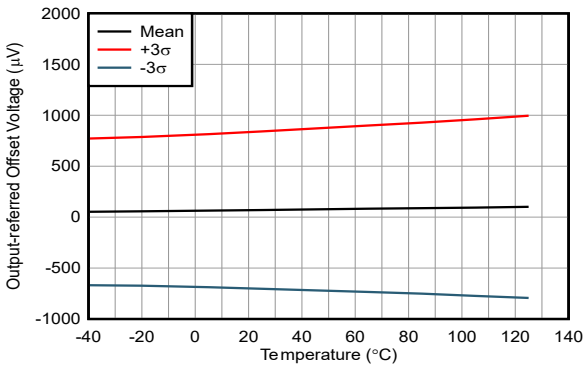
G = 1/5 V/V V_s = ±20 V 30 units

Figure 6-21. Output-Referred Offset Voltage vs Temperature (INA600A)



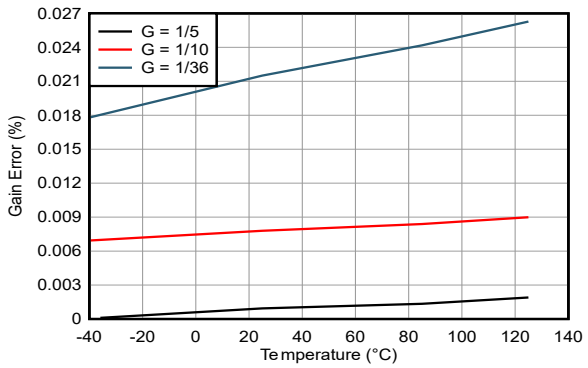
G = 1/10 V/V V_s = ±20 V 12 units

Figure 6-22. Output-Referred Offset Voltage vs Temperature (INA600B)



G = 1/36 V/V V_s = ±20 V 16 units

Figure 6-23. Output-Referred Offset Voltage vs Temperature(INA600F)



V_s = ±1.35 V

Figure 6-24. Gain Error vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)

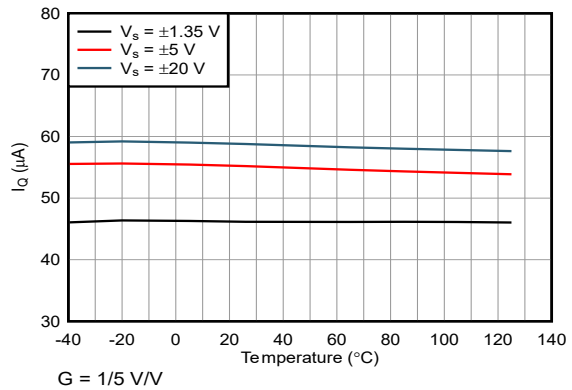


Figure 6-25. Quiescent Current vs Temperature

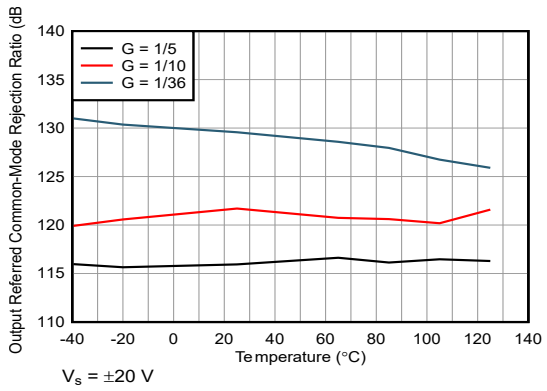


Figure 6-26. CMRR vs Temperature

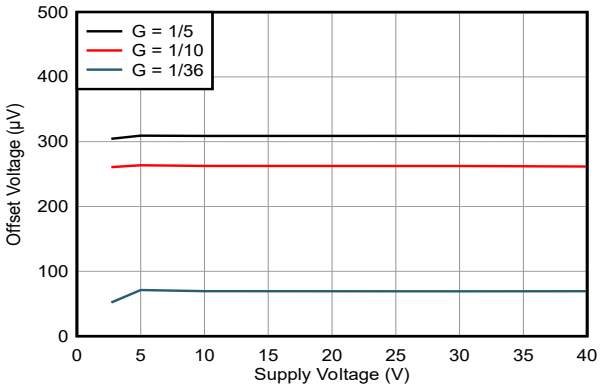


Figure 6-27. Offset Voltage vs Supply Voltage

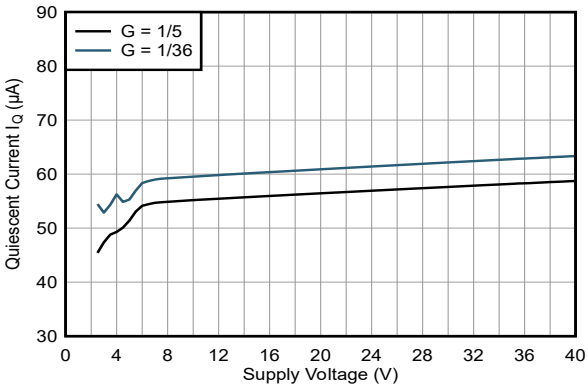


Figure 6-28. Quiescent Current vs Supply Voltage

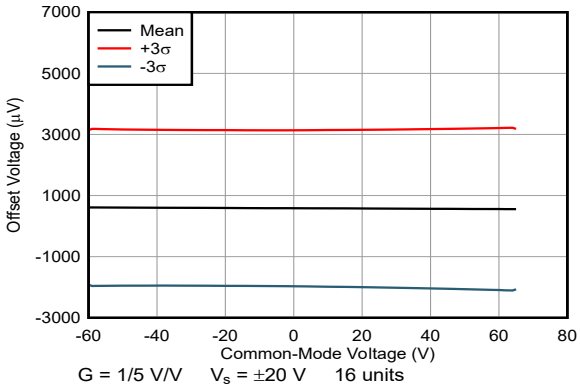


Figure 6-29. Output-Referred Offset Voltage vs Common-Mode Voltage (INA600A)

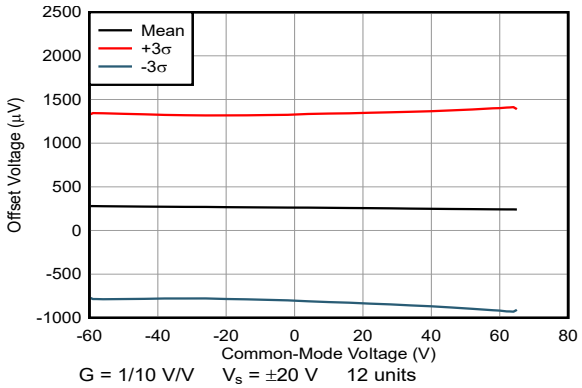


Figure 6-30. Output-Referred Offset Voltage vs Common-Mode Voltage (INA600B)

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)

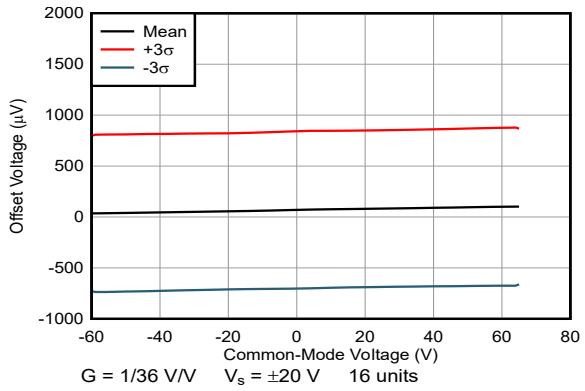


Figure 6-31. Output-Referred Offset Voltage vs Common-Mode Voltage (INA600F)

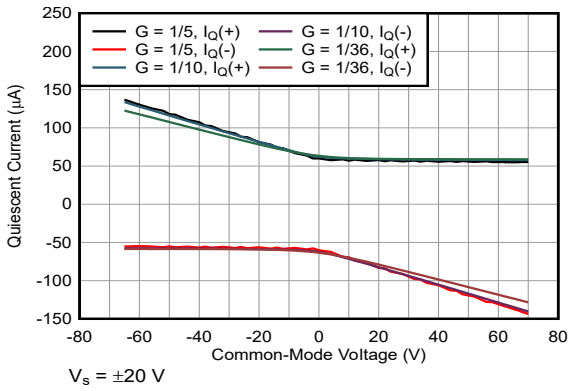


Figure 6-32. Quiescent Current vs Common-Mode Voltage

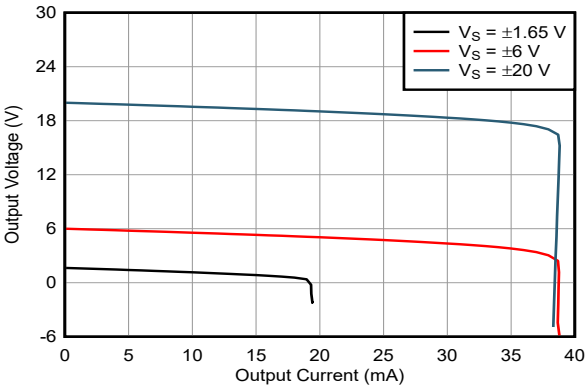


Figure 6-33. Output Voltage Swing vs Output Current (Sourcing)

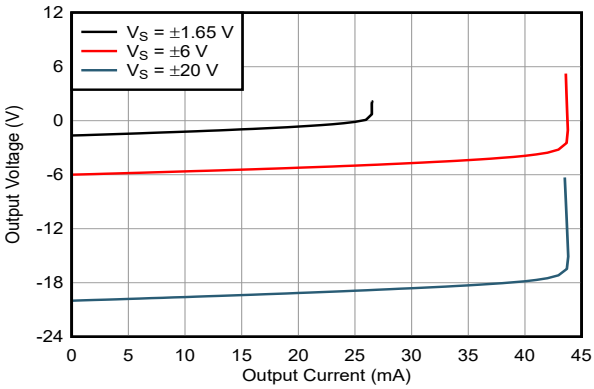


Figure 6-34. Output Voltage Swing vs Output Current (Sinking)

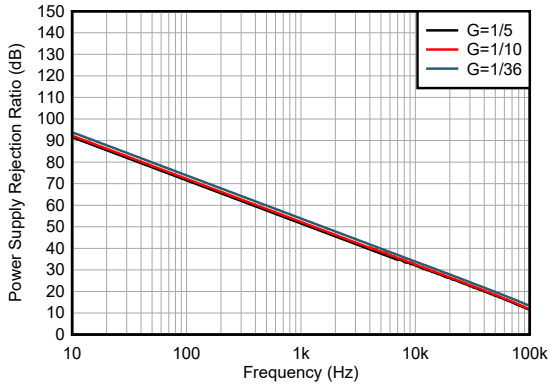


Figure 6-35. Negative Power-Supply Rejection Ratio (dB) vs Frequency, All Gains

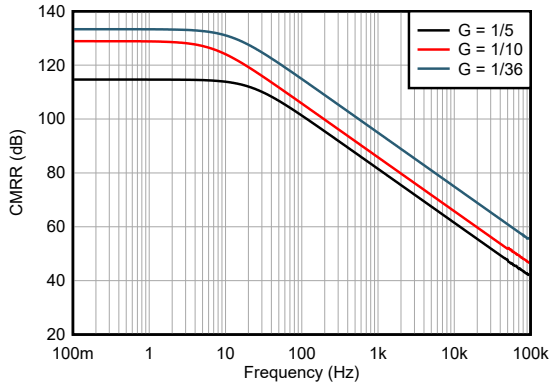


Figure 6-36. Output-Referred CMRR vs Frequency, All Gains

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)

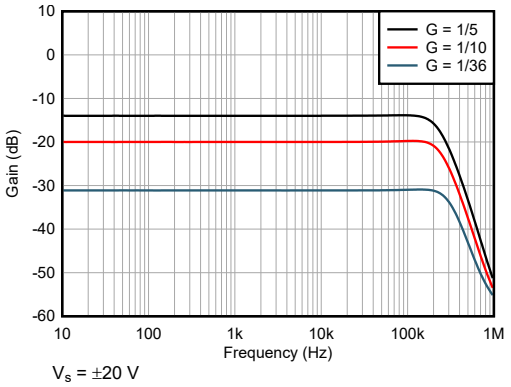


Figure 6-37. Closed-Loop Gain vs Frequency

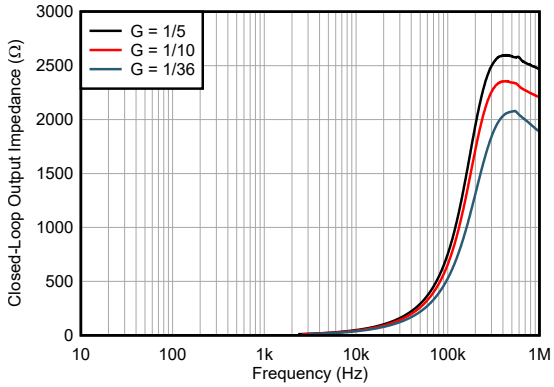


Figure 6-38. Closed-Loop Output Impedance vs Frequency

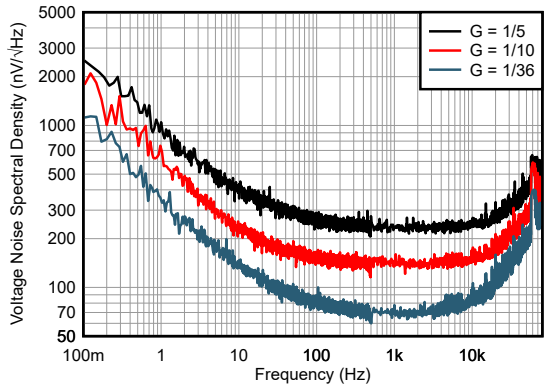


Figure 6-39. Output-Referred Voltage Noise Spectral Density

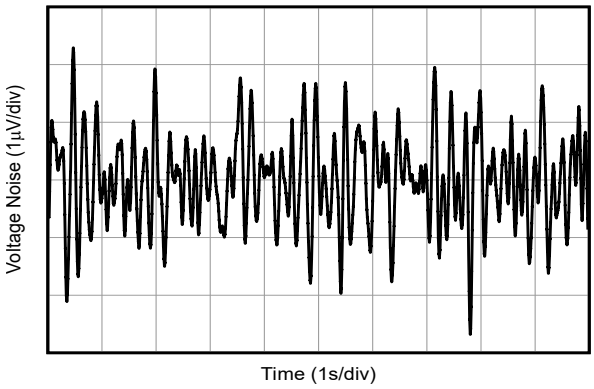


Figure 6-40. Output-Referred 0.1Hz to 10Hz Noise in Time Domain (INA600A)

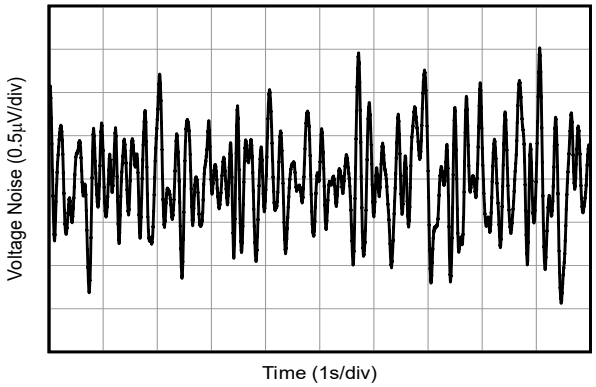


Figure 6-41. Output-Referred 0.1Hz to 10Hz Noise in Time Domain (INA600B)

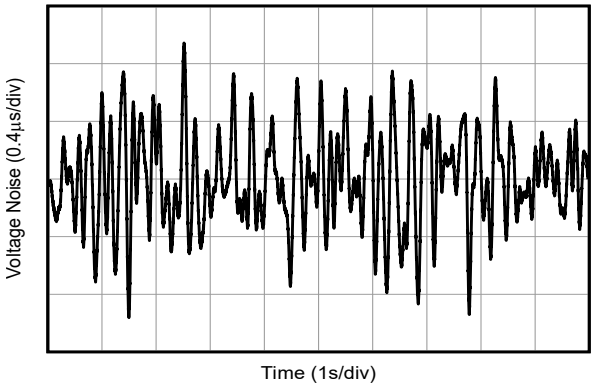


Figure 6-42. Output-Referred 0.1Hz to 10Hz Noise in Time Domain (INA600F)

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)

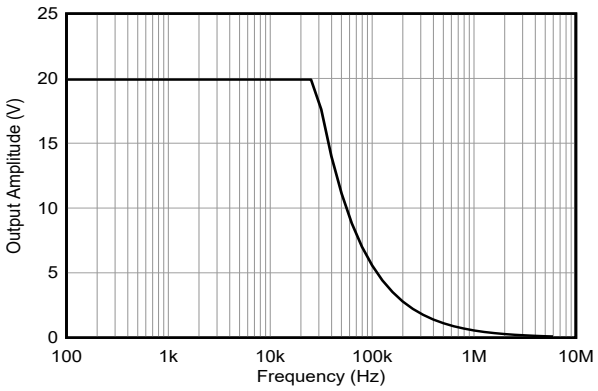
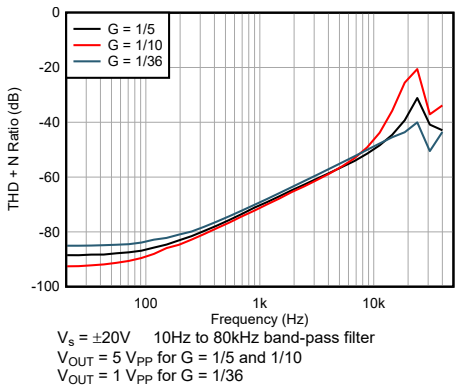


Figure 6-43. Maximum Output Voltage vs Frequency

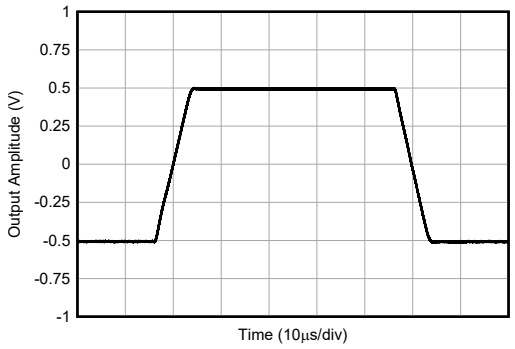


V_s = ±20V 10Hz to 80kHz band-pass filter
V_{OUT} = 5 V_{PP} for G = 1/5 and 1/10
V_{OUT} = 1 V_{PP} for G = 1/36

Figure 6-44. THD+N Frequency

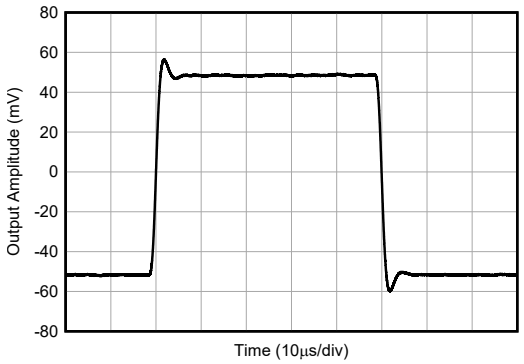
G = 1/5 V/V V_s = ±20V C_L = 100pF

Figure 6-45. Large-Signal Step Response (INA600A)



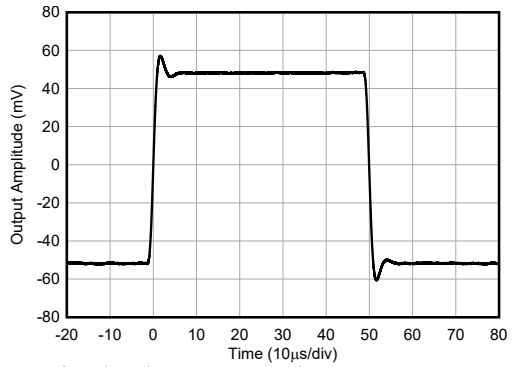
G = 1/36 V/V V_s = ±20V C_L = 100pF

Figure 6-46. Large-Signal Step Response (INA600F)



G = 1/5 V/V V_s = ±20V C_L = 100pF

Figure 6-47. Small-Signal Step Response (INA600A)

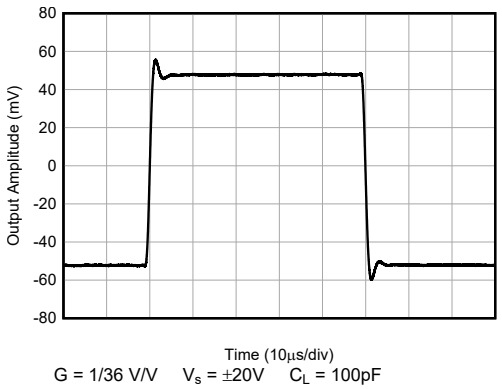


G = 1/10 V/V V_s = ±20V C_L = 100pF

Figure 6-48. Small-Signal Step Response (INA600B)

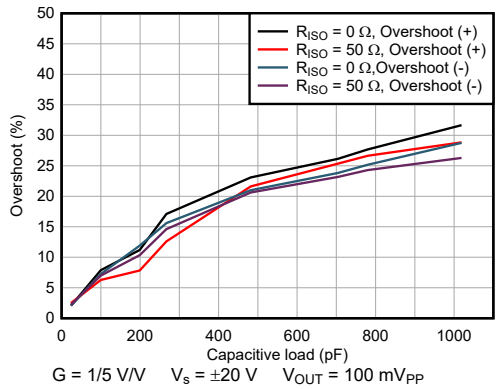
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)



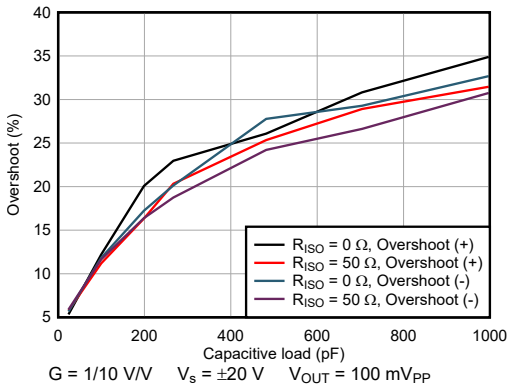
G = 1/36 V/V V_s = ±20V C_L = 100pF

Figure 6-49. Small-Signal Step Response (INA600F)



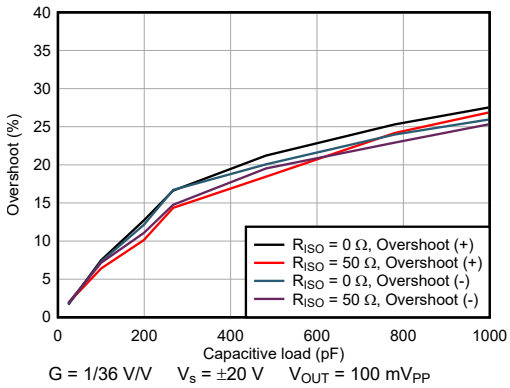
G = 1/5 V/V V_s = ±20 V V_{OUT} = 100 mV_{PP}

Figure 6-50. Small-Signal Overshoot vs Capacitive Load (INA600A)



G = 1/10 V/V V_s = ±20 V V_{OUT} = 100 mV_{PP}

Figure 6-51. Small-Signal Overshoot vs Capacitive Load (INA600B)



G = 1/36 V/V V_s = ±20 V V_{OUT} = 100 mV_{PP}

Figure 6-52. Small-Signal Overshoot vs Capacitive Load (INA600F)

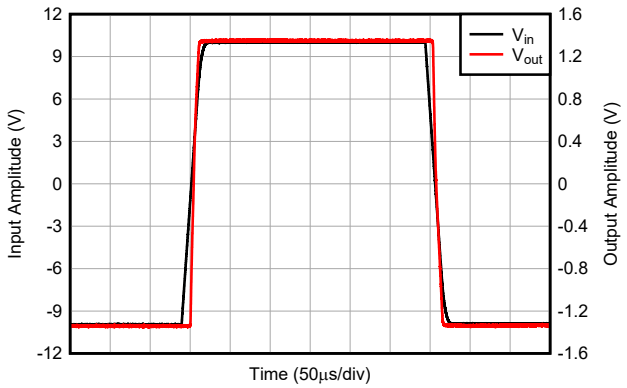


Figure 6-53. Overload Recovery (INA600A)

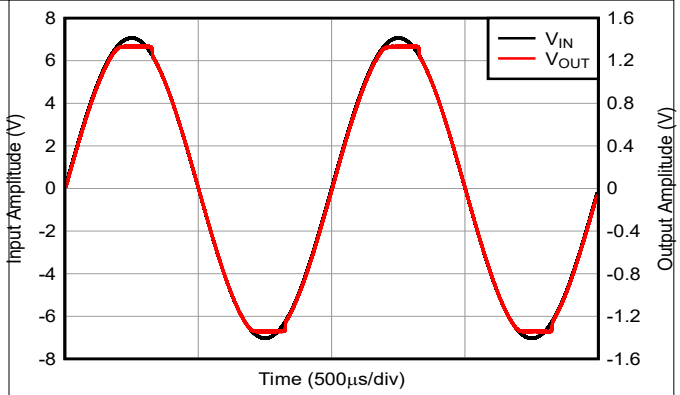


Figure 6-54. No Phase Reversal (INA600A)

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V), V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2, and G = 1/5 (unless otherwise noted)

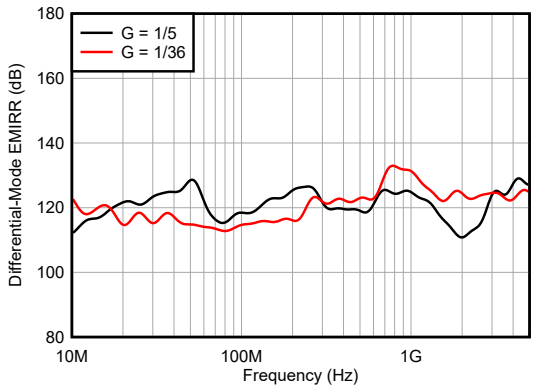


Figure 6-55. Differential-Mode EMIRR vs Frequency (INA600A and INA600F)

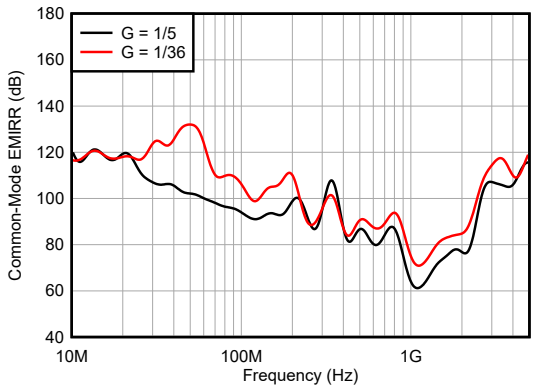


Figure 6-56. Common-Mode EMIRR vs Frequency (INA600A and INA600F)

7 Detailed Description

7.1 Overview

The INA600 is a voltage-sensing difference amplifier with precision matched resistors that offer attenuating gain options. The precision matched integrated resistors saves bill of materials (BOM) costs and board space by removing the need for precise and low-tolerance external resistors. The device achieves ±0.05% maximum gain error, 5ppm/°C maximum gain drift, and 92dB of minimum common-mode rejection ratio (G = 1/5). The INA600 does not typically require calibration when used in 8-bit to 10-bit systems. Further calibration of offset and gain error at a system level helps improve system resolution and accuracy, enabling use in higher resolution systems.

High input impedance of >1MΩ with just 65µA of quiescent current makes the INA600 very useful in single-cell, battery-monitoring applications. Referred to negative rail, the device handles input voltages up to –40V to +85V and attenuates the voltage down with great accuracy. The device rejects any common-mode errors such as ground bounce, switching ripples, and AC mains and is capable of interfacing the attenuated voltage to the low-voltage, low-speed ADCs. Most errors (including offset, offset drift, CMRR, and noise) are referred to the output. Doing so enables easy calculation of the signal-to-noise ratio (SNR) and effective number of bits (ENOB) closer to the analog-to-digital converter (ADC).

The INA600 is offered in six attenuating gain options across six variants. The INA600A version offers the lowest attenuation gain option of 1/5, whereas the INA600F offers the highest attenuation gain option of 1/36. The INA600 gain options are designed for level translation applications that interface with a wide variety of differential and single-ended high-voltage signals. Differential signals include ±24V, ±12V, ±10V, ±5V, and so forth. Single-ended signals include 0V to 48V, 0V to 24V, 0V to 12V, 0V to 10V, 0V to 5V, and so forth, These high-voltage signals are level translated into a wide variety of low-voltage (0V to 5V, 0V to 3.3V, 0V to 2.5V, and so forth) ADC ranges. This is useful in a variety of end equipments and applications where multiple high-voltage signals and supply domains are monitored. Examples include battery testers, solar string inverters, power tools, analog input modules, and battery energy storage systems. The device also has enough bandwidth (≥200kHz) to directly drive low-speed (≤10kSPS) ADCs.

The INA600 is designed for space-constrained applications such as robotics, power banks, and chargers. As such, the device saves valuable PCB area compared to the discrete implementation of difference amplifiers. For easy use in automotive and industrial applications, the device is available in standard, leaded packages such as SOT-23 and SC70.

7.2 Functional Block Diagram

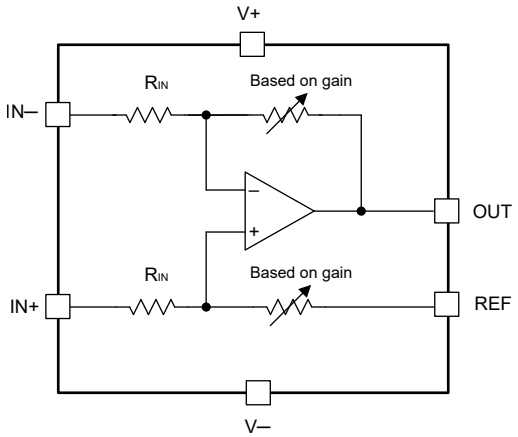


Figure 7-1. INA600 Simplified Internal Schematic

7.3 Feature Description

7.3.1 Gain Options and Resistors

The gain value of the INA600 is given by the ratio of feedback resistor and input resistor. The gain options are offered across different device variants as provided in Table 7-1. While the typical value of input and feedback resistors are shown in the following table, it is important to note that these values can vary together by approximately ±15% while maintaining tighter gain error (tolerance) numbers as specified in the *Electrical Characteristics* table.

Table 7-1. Gain Selection

DEVICE	VERSION	INPUT RESISTOR	FEEDBACK RESISTOR	GAIN
INA600	A	1.2MΩ	240kΩ	1/5
	B	1.2MΩ	120kΩ	1/10
	C	1.2MΩ	100kΩ	1/12
	D	1.2MΩ	66.66kΩ	1/18
	E	1.2MΩ	50kΩ	1/24
	F	1.2MΩ	33.33kΩ	1/36

7.3.1.1 Gain Error and Drift

Gain error in the INA600 is dictated by the mismatch of the integrated precision resistors. Gain error is a tested parameter and maximum gain error is under or at ±0.05% for all gains. Gain drift of the INA600 is limited by the mismatch of the temperature coefficient of the integrated resistors. Maximum gain drift is under 5ppm/°C for all gains. These integrated resistors are already precision matched with low temperature coefficient resistors. Thus, the overall gain drift is much better in comparison to discrete implementation of difference amplifiers built using external resistors. Gain drift is not a tested parameter and the maximum gain drift is specified based on characterization results with sufficient guard banding. Maximum gain error of ±0.05% is expected for inputs from the reference pin that sets output common-mode voltage.

7.3.2 Input Common-Mode Voltage Range

The INA600 difference amplifier rejects the input common mode. This rejection capability is largely based on the matching of the internal resistors. The INA600 input voltage range is extended well beyond the supply rails using a special design technique. This technique causes the input voltage range not to be overly limited by gain configuration or supply voltage. The input voltage range spans from –40V below the negative rail to +85V above the negative rail for supply voltages starting from 9V across all gains. Below 9V, see the valid input range values within the *Electrical Characteristics* table for the gain option of interest.

Common-mode rejection ratio values are referred to the output to enable easy error calculation with respect to the ADC full scale. For example, a 1V input common-mode error signal at the INA600A input (G = 1/5) at a 12V supply is attenuated to 2µV at the INA600A output. In this example, the typical CMRR specification (referred to output) is 114dB starting from a 9V supply.

7.3.3 EMI Rejection

The INA600 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from a variety of sources. These sources include wireless communications and densely-populated boards with a mix of analog signal chain and digital components. Texas Instruments accurately measures and quantifies the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. The *EMI Rejection Ratio of Operational Amplifiers* application note is available for download from www.ti.com. This application note contains detailed information on the topic of EMIRR performance relating to op amps.

Figure 7-2 shows the results of this testing on the INA600 for differential EMI interference. Figure 7-3 shows the results of this testing on the INA600 for common-mode EMI interference. Table 7-2 provides the EMIRR IN+ values for the INA600 at particular frequencies commonly encountered in real-world applications.

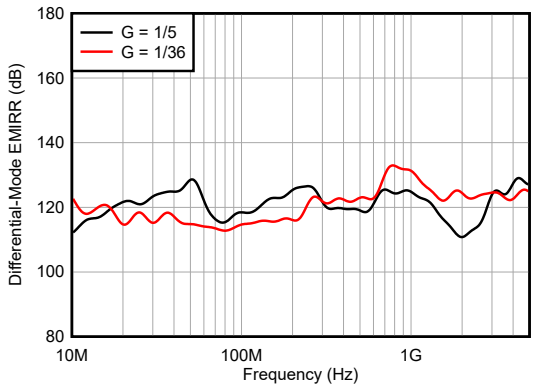


Figure 7-2. Electromagnetic Interference Rejection Ratio Referred to Output vs Frequency (Differential Input)

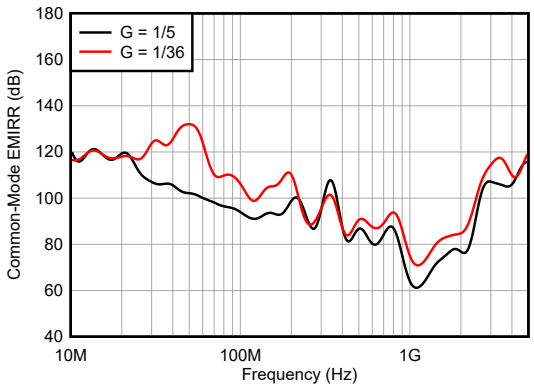


Figure 7-3. Electromagnetic Interference Rejection Ratio Referred to Output vs Frequency (Common-Mode Input)

Table 7-2. INA600 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR DIFFERNTIAL (G = 1/36)	EMIRR COMMON-MODE (G = 1/36)
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	122dB	83dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	132dB	82dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	121dB	84dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	122dB	100dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	123dB	118dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	125dB	118dB

7.3.4 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier when designing a more robust circuit. Because of natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value. The offset voltage of an amplifier is one such example. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions. Thus, allowing circuit designers to leverage this information to guard band the system, even when a minimum or maximum specification is not in the *Electrical Characteristics* table.

Figure 7-4 shows an example distribution. In this figure, μ (or *mu*), is the mean of the distribution, and σ (or *sigma*), is the standard deviation of a system. For specifications exhibiting this kind of distribution, approximately two-thirds (68.26%) of all units are expected to have a value within one standard deviation of the mean. One standard deviation of the mean is $\mu - \sigma$ to $\mu + \sigma$.

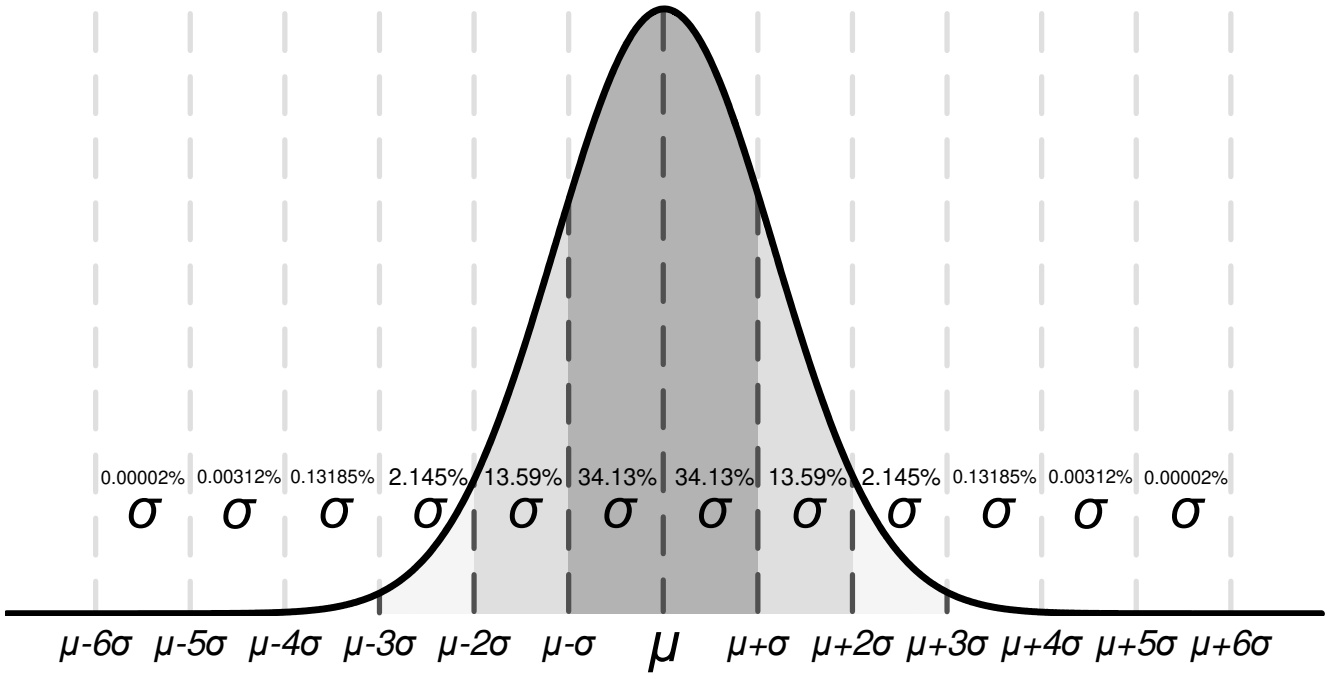


Figure 7-4. Ideal Gaussian Distribution

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. Generally, if a specification naturally has a nonzero mean (for example, gain bandwidth), then the typical value is equal to the mean (μ). Some specifications (such as offset voltage) have a mean near zero. In this case, the typical value equals the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Use this chart to calculate the approximate probability of a specification in a unit. For example, the INA600A typical offset voltage is 1100μV. Thus, 68.2% of all INA600A devices are expected to have an offset from –1100μV to +1100μV. At 4σ (±4400μV), 99.9937% of the distribution has an offset voltage less than ±4400μV. Therefore, 0.0063% of the population is outside of these limits, which corresponds to approximately 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are verified by TI, and units outside these limits are removed from production material. For example, the INA600A family has a maximum gain error of ±0.05% at 25°C. Even though this error corresponds to 5σ, TI verifies that any units with gain error larger than ±0.05% are removed from production material. This error equals approximately 1 in 3.5 million units, which is extremely unlikely.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for the application. Design worst-case conditions using this value. A 6σ value corresponds to approximately 1 in 500 million units, which is extremely unlikely. This 6σ value is an option as a wide guard band for designing a system around. Histograms for some of the important specifications (such as offset, offset drift, CMRR, and gain error) are shown in the *Typical Characteristics* section.

For gain error drift, the INA600 family does not specify a maximum value based on final test. Instead, this value is based on characterization, as mentioned in the *Electrical Characteristics* table. The corresponding distribution mentioned in Figure 6-4 has a mean of –0.00216% and sigma of 0.0047%. Thus, the mean plus 6σ value for gain error is calculated to be approximately 0.025%. When designing for system conditions with 6σ guard band, use this method and value to estimate the worst possible gain error. However, process variation and adjustments over time potentially shift typical means and standard deviations. Unless there is a value in the minimum or maximum specification column that is specified based on final test, TI cannot verify device performance.

Thus, the maximum gain error specification in the *Electrical Characteristics* table is relaxed beyond 6σ guard band to be ±0.05%.

7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 7-5 shows the ESD circuits contained in the INA600 devices. On the input pins, the ESD protection circuitry involves local high impedance diode structures and do not route the ESD current to power supply ESD cell. On the output pin, there are reverse biased diodes to both the power supply rails. These diode structures route the ESD current back to the internal power supply lines, where there is an absorption power supply ESD cell internal to the difference amplifier. On the reference pin, the ESD protection is local and does not route current to the power supply ESD cell.

All of the ESD protection circuitry is intended to remain inactive during normal circuit operation.

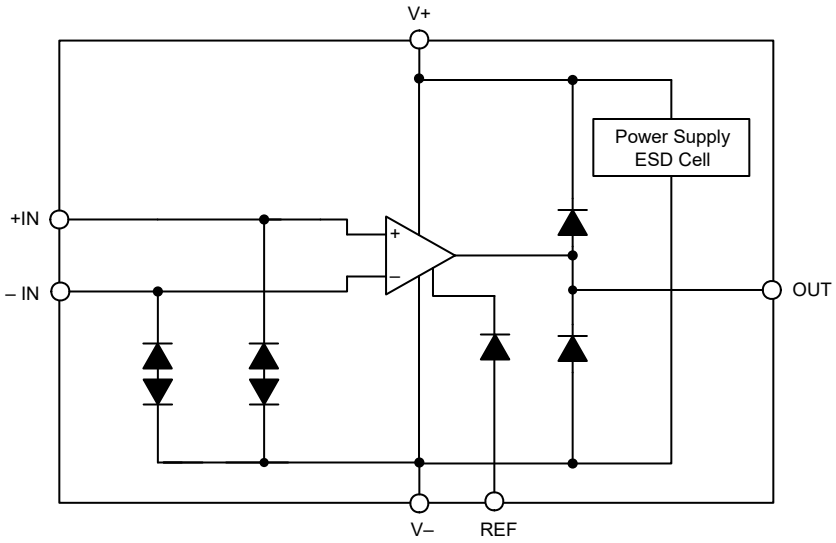


Figure 7-5. Equivalent Internal ESD Circuitry

7.4 Device Functional Modes

The INA600 has only one functional mode. The device powers on, starts drawing quiescent current and is functional as long as the power supply voltages are in the recommended operating voltage range of 2.7V (±1.35V) to 40V (±20V). Operational temperature range of INA600 is from –40°C to 125°C.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Reference Pin

The output voltage of the INA600 is developed with respect to the voltage on the reference pin (REF). Often in dual-supply operation, REF pin connects to the system ground. However, in single-supply operation, offsetting the output signal to a precise mid-supply level is useful and required (for example, 2.5V in a 5.0V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA can drive a single-supply ADC. This is accomplished using an external reference buffer configured in unity gain, voltage follower configuration as shown in Figure 8-1.

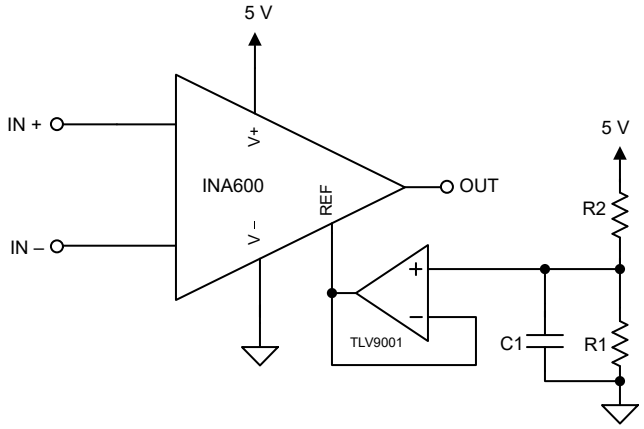


Figure 8-1. INA600 with External Reference Buffer

8.2 Typical Applications

8.2.1 48V Battery Monitoring Using Difference Amplifier

The INA600 is an integrated difference amplifier that processes large differential voltages while simultaneously rejecting larger common-mode voltages. The device offers a low power consumption of 65µA (typical) and has a smaller form factor.

With the specifications above, the device is a good fit for applications using 48V batteries such as robotics, power tools and so forth. While, battery monitoring ICs are often used to perform sophisticated functions including cell balancing, protection, voltage and current sensing and so forth, these systems still require basic monitoring of battery voltages, internal DC bus voltages, and load voltages when driving various motors using control-loops. In these scenarios, the amplifier-based monitoring application shown below can be used.

Figure 8-2 shows an example circuit that monitors a 48V battery voltage and interfaces the voltage to an ADC that is powered using a 5V power supply. The main advantage for using difference amplifiers in this application is the elimination of ground bounce, which is a common-mode signal, when measuring the battery voltage. These ground bounce signals, when not rejected, are capable of causing errors in the range of few milli-volts to tens or hundreds of milli-volts.

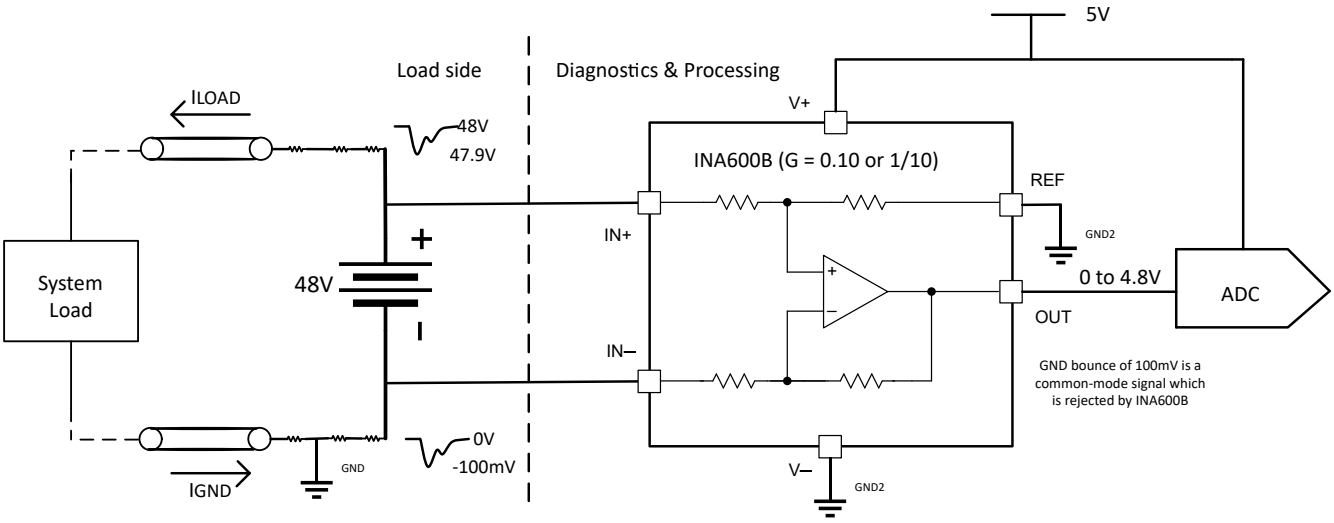


Figure 8-2. 48V Battery Monitoring Circuitry

8.2.1.1 Design Requirements

For this application, the design requirements are as provided in Table 8-1.

Table 8-1. Design Requirements

DESCRIPTION	VALUE
Battery voltage	V_{BAT} = 48V
Supply voltage	V_S = 5V
Full-scale range of ADC	$V_{ADC(fs)}$ = V_{OUT} = 5V
Quiescent current	125µA
ADC Resolution	8 bits
Effective number of bis (ENOB)	7.5 bits
Common-mode rejection ratio	80dB or a factor of 10000

8.2.1.2 Detailed Design Procedure

This section provides basic calculations for the INA600B difference amplifier with respect to the given design requirements.

Firstly, the 48V battery voltage must be attenuated and interfaced to ADC reference voltage of 5V. This requires a G = 1/10 or 0.10V/V and therefore the INA600B is chosen for the application.

$$\text{Gain} = \frac{V_{ADC}}{V_{BAT}} = \frac{5}{48} \text{ is approximately } 0.10 \quad (1)$$

The maximum common-mode range of INA600 in a gain of 1/10 at 5V supply is given to be (V–) + 55V from the INA600B *Electrical Characteristics* table.

This is well within the requirements for sensing 48V battery voltage and the common-mode rejection ratio (CMRR) referred to output is a minimum of 95dB as per INA600B *Electrical Characteristics* table. This corresponds to a attenuation factor of $\frac{1}{56234}$. This helps attenuate the 100mV common-mode error shown in the Figure 8-2 to just under 2µV.

When referring to the INA600B output, Equation 2 calculates the common-mode error, RTO to approximately 2µV.

$$CM_{Err\_RTO} = \frac{100mV}{56231} \cong 2\mu V \quad (2)$$

Next, INA600B has input impedance of 1.2MΩ as per the *Electrical Characteristics* table. Assuming a full battery voltage of 48V, the input current through the resistor is calculated as:

$$I_{R_{IN}} = \frac{V_{BAT}}{R_{IN}} = \frac{48}{1.20M} = 40\mu A \quad (3)$$

This input current through the resistor adds to the amplifier quiescent current of 65µA resulting in a total current consumption of 105µA, which meets the design requirement of 125µA.

$$I_{total} = I_{R_{IN}} + I_Q \quad (4)$$

The next step is to calculate the other error sources in the application. Maximum gain error and offset error as per *Electrical Characteristics* table are 0.05% and 3.0mV for the Gain = 0.2V/V.

$$\text{Total Error} = \sqrt{(0.0005 \times 48)^2 + 0.0030^2} = 24.2mV \quad (5)$$

For an 8-bit, 5V ADC, V_{LSB} is calculated as:

$$V_{LSB} = \frac{5}{2^8} = 19.5mV \quad (6)$$

The total error of 24.2mV that was calculated is approximately 1.25LSB of ADC full scale voltage of 5V and hence achieves almost 8 bits (approximately 7.998) of ENOB, comfortably meeting the requirement of 7.5 bits.

Note that the errors across temperature are not calculated here but can be easily included in the error analysis based on the drift specifications provided in the *Electrical Characteristics* table as per the temperature requirements of the application. These drift errors and noise often do not heavily affect the performance at 8-bit accuracy levels. Finally, calibration of offset and gain error can improve the accuracy beyond 10 to 12 bits as these factors can be the major sources of error in the application.

8.2.1.3 Application Curves

The following typical characteristic curve is for the circuit in Figure 8-2.

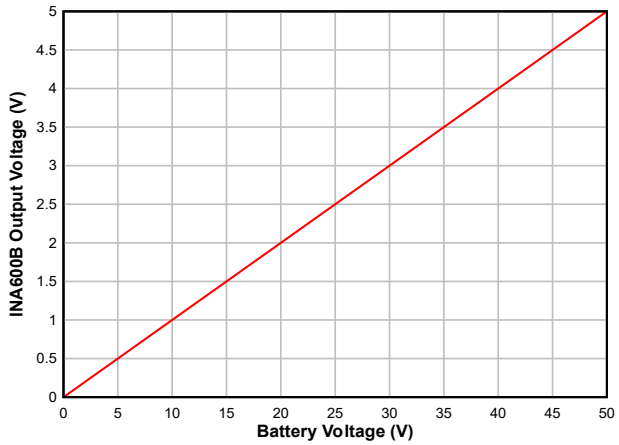


Figure 8-3. Battery Input Voltage vs INA600B Output Voltage

8.3 Power Supply Recommendations

The nominal performance of the INA600 is specified with a midsupply reference voltage from ±1.35 (2.7V) to ±20V (40V). The device also operates using non-midsupply reference voltages with good performance. Many specifications apply from –40°C to +125°C. The *Electrical Characteristics* table presents parameters that can exhibit significant variance because of operating voltage or temperature.

Add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Place the C_{BYP} as close to the device as possible to reduce coupling errors from noisy or high-impedance power supplies. Verify the power supply trace routes through C_{BYP} before reaching the amplifier power supply terminals. For more information, see the *Layout Guidelines*.

8.4 Layout

8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use the following PCB layout practices:

- Ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Route the input traces as far away from the supply or output traces as possible to reduce parasitic coupling. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

8.4.2 Layout Example

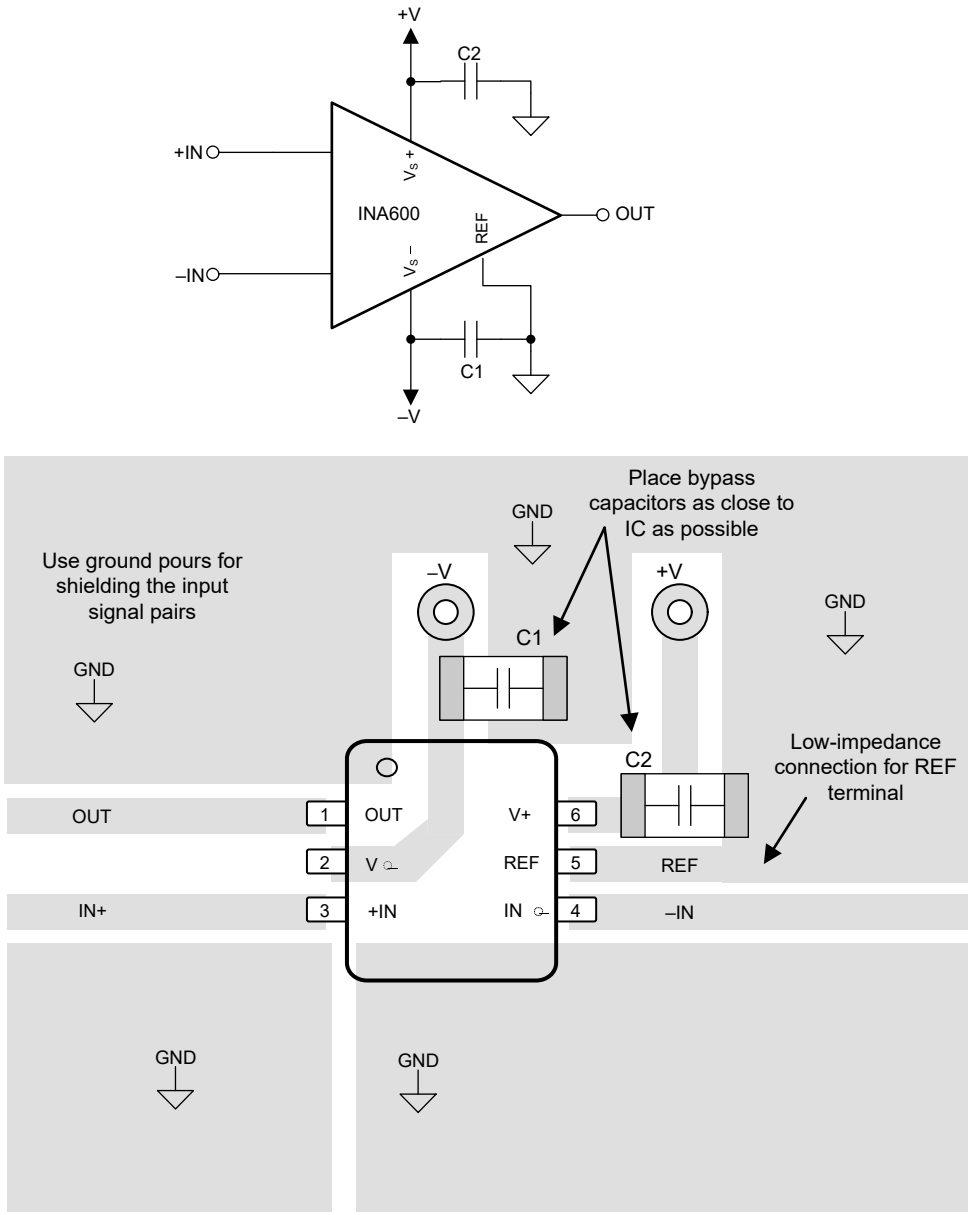


Figure 8-4. Example Schematic and Associated PCB Layout for DBV Package

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

- *SPICE-based analog simulation program — TINA-TI software folder*
- *Analog Engineers Calculator*

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2025) to Revision A (August 2025)	Page
• Changed DBV package status from *Advance Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA600AIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I600A
INA600BIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I600B
INA600FIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I600F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

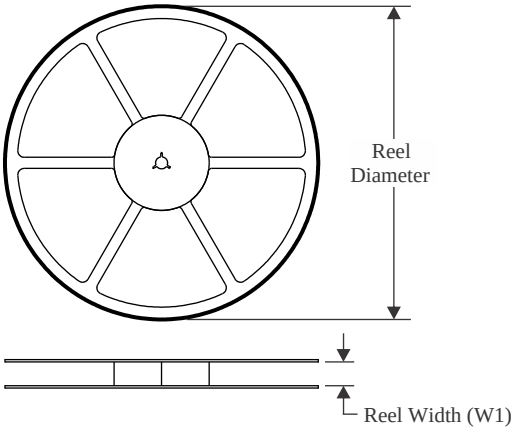
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

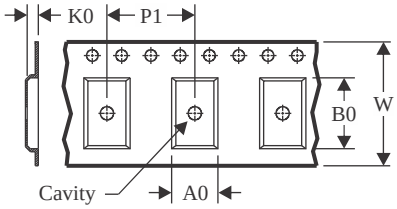
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

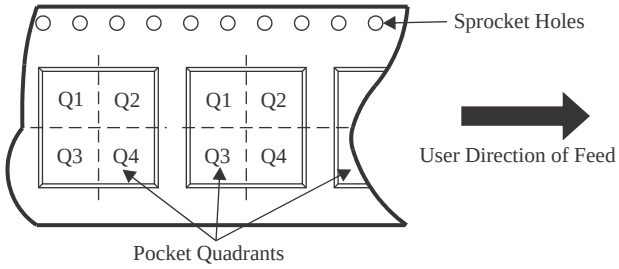


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

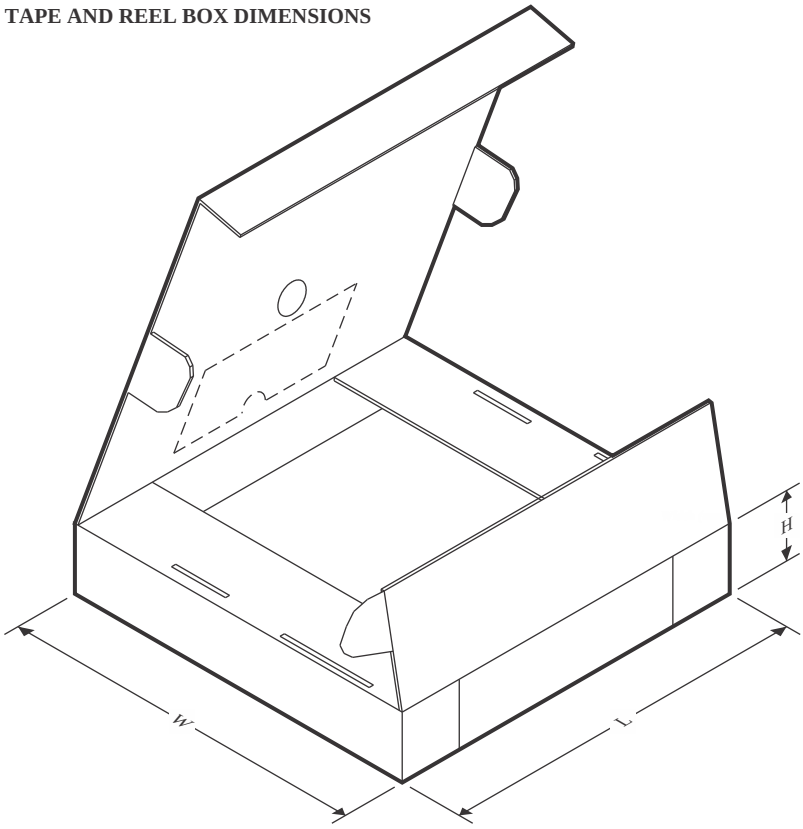
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA600AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA600BIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA600FIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

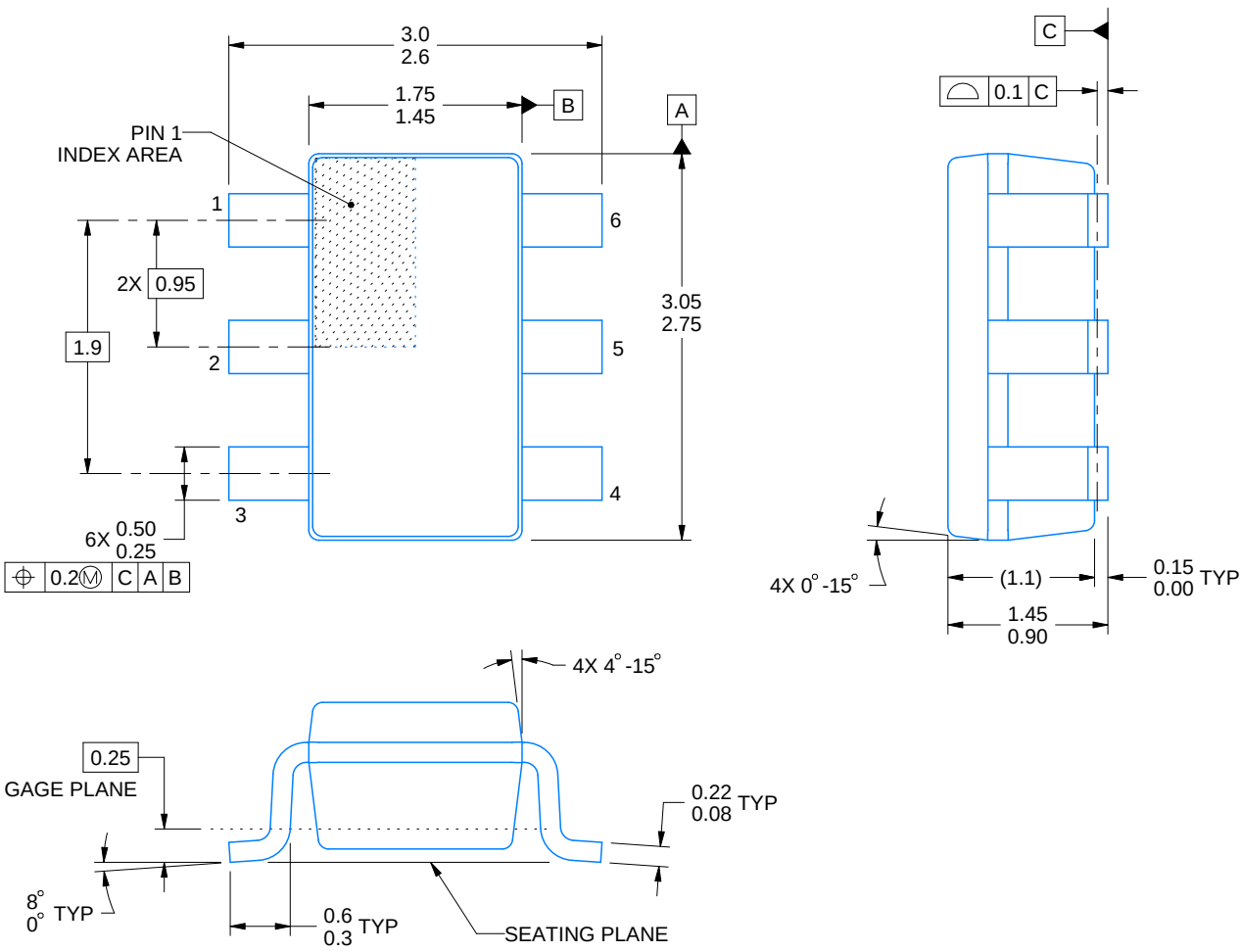
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA600AIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA600BIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA600FIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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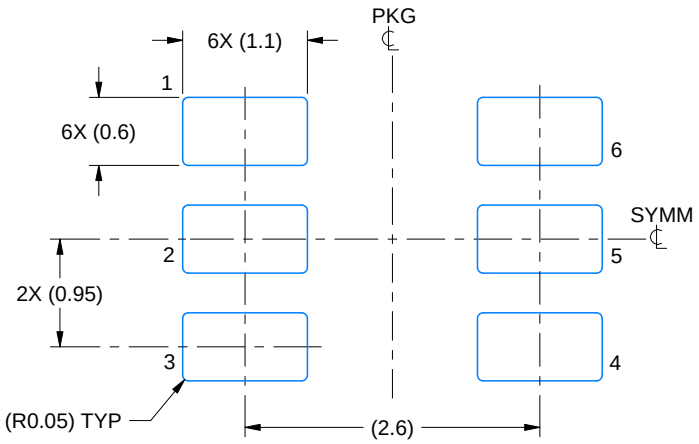
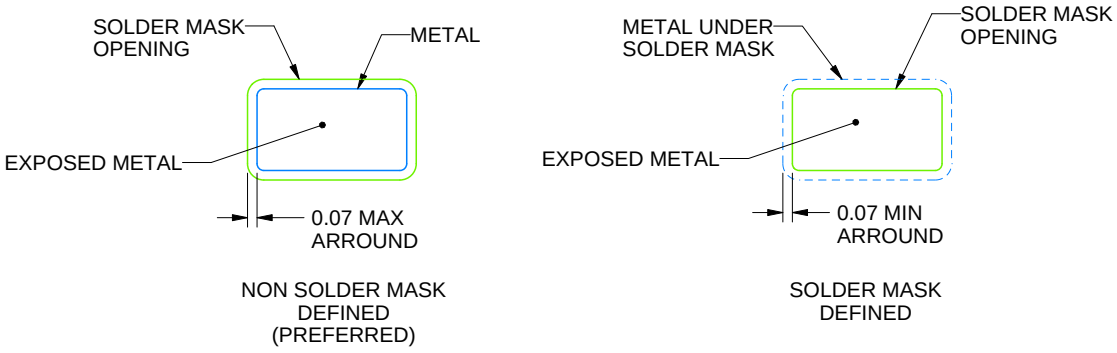
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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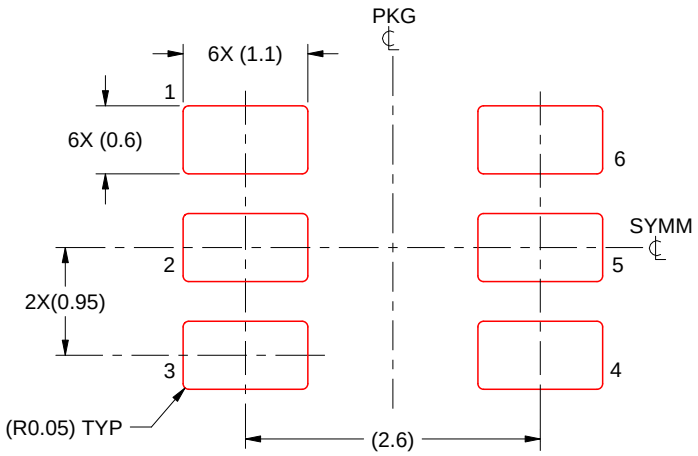
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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