

INA141 $G = 10V/V$ 或 $100V/V$ 的低功耗精密仪表放大器

1 特性

- 低失调电压：
 - $G = 100V/V$ 时为 $50\mu V$ (最大值)
- 低温漂：
 - $G = 100V/V$ 时为 $0.5\mu V/^{\circ}C$ (最大值)
- 准确增益：
 - $G = 10V/V$ 时为 $\pm 0.05\%$
- 低输入偏置电流：
 - $5nA$ (最大值)
- 高 CMR：
 - $117dB$ (最小值)
- 输入保护电压可达 $\pm 40V$
- 宽电源电压范围： $\pm 2.25V$ 至 $\pm 18V$
- 低静态电流： $750\mu A$

2 应用

- 温度变送器
- 医疗仪器
- 数据采集 (DAQ)
- 过程分析 (pH、气体、浓度、力和湿度)

3 说明

INA141 是一款低功耗通用仪表放大器，可提供出色的准确性。此器件采用多功能三级运算放大器设计，尺寸小巧，适用于多种应用。即使在高增益 ($G = 100V/V$ 时为 $200kHz$) 情况下，电流反馈输入电路也可提供宽带宽。

通过简单的引脚连接设置 $10V/V$ 或 $100V/V$ 的准确增益，无需外部电阻器。内部输入保护可经受高达 $\pm 40V$ 的电压且无损坏。

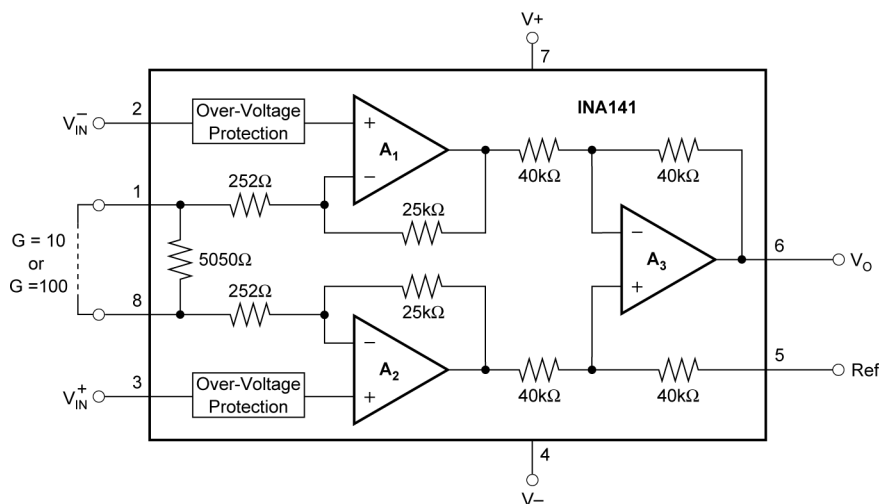
INA141 经过激光修整，具有超低失调电压 ($50\mu V$)、超低温漂 ($0.5\mu V/^{\circ}C$) 和高共模抑制 ($G \geq 100V/V$ 时为 $117dB$)。该器件采用低至 $\pm 2.25V$ 的电源电压，静态电流仅为 $750\mu A$ 。

INA141 采用 8 引脚 SOIC 封装，额定温度范围为 $-40^{\circ}C$ 至 $+85^{\circ}C$ 。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
INA141	D (SOIC, 8)	4.9mm × 6mm

- 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
- 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



基本连接



Table of Contents

1 特性	1	6.6 Typical Characteristics	7
2 应用	1	7 Application and Implementation	11
3 说明	1	7.1 Application Information.....	11
4 Revision History	2	8 Device and Documentation Support	16
5 Pin Configuration and Functions	3	8.1 接收文档更新通知.....	16
6 Specifications	4	8.2 支持资源.....	16
6.1 Absolute Maximum Ratings.....	4	8.3 Trademarks.....	16
6.2 ESD Ratings	4	8.4 静电放电警告.....	16
6.3 Recommended Operating Conditions.....	4	8.5 术语表.....	16
6.4 Thermal Information.....	4	9 Mechanical, Packaging, and Orderable Information ..	16
6.5 Electrical Characteristics.....	5		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2000) to Revision A (August 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 删除了数据表中的 PDIP 封装.....	1
• Added single supply specification to Absolute Maximum Ratings.....	4
• Added note that output short-circuit (to ground) means short-circuit to $V_S/2$ in Absolute Maximum Ratings.....	4
• Added "TA = - 40°C to +85°C" test condition to Offset voltage vs temperature specification in the Electrical Characteristics and renamed to Offset voltage drift.....	5
• Added test conditions "VREF = 0 V, VCM = $V_S / 2$ and G = 10 below the title.....	5
• Deleted common-mode voltage typical values in the Electrical Characteristics and combined to one line.....	5
• Added "TA = - 40°C to +85°C" test condition to Bias current vs temperature specification in the Electrical Characteristics and renamed to Input bias current drift for clarity.....	5
• Added "TA = - 40°C to +85°C" test condition to Offset current vs temperature specification in Electrical Characteristics and renamed to Input offset current drift for clarity.....	5
• Added "TA = - 40°C to +85°C" test condition for Gain error vs temperature in the Electrical Characteristics and renamed to Gain drift for clarity.....	5
• Changed parameter names from "Voltage - Positive" and "Voltage - Negative" to "Output voltage" in the Electrical Characteristics.....	5
• Added "Continuous to $V_S / 2$ " test condition short-circuit current specification in the Electrical Characteristics for clarity.....	5
• Changed short-circuit current typical value from +6/-15 mA ± 20 mA.....	5
• Changed bandwidth typical value from 1 MHz to 610 kHz in the Electrical Characteristics.....	5
• Changed slew rate typical value from 4 V/ μ s to 2 V/ μ s in the Electrical Characteristics.....	5
• Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from Electrical Characteristics.....	5
• Changed Figure 6-2, <i>Common-Mode Rejection vs Frequency</i>	7
• Changed Figure 6-8, <i>Quiescent Current and Slew Rate vs Temperature</i>	7
• Changed <i>Output Voltage Swing vs Output Current</i> single plot to Figure 6-12, <i>Positive Output Voltage Swing vs Output Current</i> and Figure 6-12, <i>Negative Output Voltage Swing vs Output Current</i>	7
• Changed Figure 6-18, <i>Small-Signal Step Response</i>	7
• Changed Figure 6-19, <i>Large-Signal Step Response</i>	7
• Changed Figure 6-20, <i>0.1-Hz to 10-Hz Input-Referred Voltage Noise</i>	7
• Changed G from 1 to 10 V/V at the end of the <i>Application Information</i> section.....	11
• Deleted reference to <i>Input Bias Current vs Common-Mode Input Voltage</i> plot.....	13

5 Pin Configuration and Functions

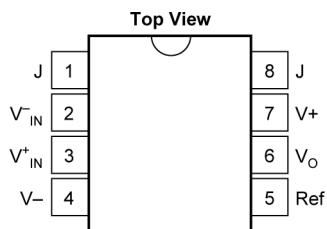


图 5-1. D Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
J	1, 8	Input	Gain selection. G = 10 V/V if not shorted G = 100 V/V if shorted A resistance of 0.5 Ω decreases gain by 0.1%.
Ref	5	Input	Reference input. This pin must be driven by low impedance
V -	4	—	Negative supply
V+	7	—	Positive supply
V ⁻ _{IN}	2	Input	Negative (inverting) input
V ⁺ _{IN}	3	Input	Positive (noninverting) input
V _O	6	Output	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage	Dual supply, V _S = (V ₊) – (V _–)		±18	V
		Single supply, V _S = (V ₊) – 0 V		36	
	Input voltage			±40	V
	Output short-circuit (to ground) ⁽²⁾		Continuous		
T _A	Operating temperature		– 40	125	°C
T _{stg}	Storage temperature		– 40	125	°C
T _J	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			300	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V _S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
T _A	Specified temperature		– 40		85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA141	UNIT
		D (SOIC)	
		8 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	150	°C/W
R _{θJA}	Junction-to-ambient thermal resistance	110	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	57	°C/W
R _{θJB}	Junction-to-board thermal resistance	54	°C/W
ψ _{JT}	Junction-to-top characterization parameter	11	°C/W
ψ _{JB}	Junction-to-board characterization parameter	53	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, $V_{\text{CM}} = V_S / 2$, and $G = 10\text{ V/V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT	
INPUT									
V_{OS}	Offset voltage (RTI)	INA141P, INA141U	$G = 10\text{ V/V}$			± 50	± 100	μV	
			$G = 100\text{ V/V}$			± 20	± 50		
		INA141PA, INA141UA	$G = 10\text{ V/V}$			± 50	± 250		
			$G = 100\text{ V/V}$			± 20	± 125		
	Offset voltage drift (RTI)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	INA141P, INA141U	$G = 10\text{ V/V}$		± 0.5	± 2	$\mu\text{V}/^\circ\text{C}$	
				$G = 100\text{ V/V}$		± 0.2	± 0.5		
			INA141PA, INA141UA	$G = 10\text{ V/V}$		± 0.5	± 2.5		
				$G = 100\text{ V/V}$		± 0.2	± 1.5		
PSRR	Power-supply rejection ratio (RTI)	$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$	INA141P, INA141U	$G = 10\text{ V/V}$		± 2	± 10	$\mu\text{V/V}$	
				$G = 100\text{ V/V}$		± 0.4	± 1		
			INA141PA, INA141UA	$G = 10\text{ V/V}$		± 2	± 20		
				$G = 100\text{ V/V}$		± 0.4	± 3		
	Long-term stability	$G = 10\text{ V/V}$				0.5		$\mu\text{V}/\text{mo}$	
		$G = 100\text{ V/V}$				0.2		$\mu\text{V}/\text{mo}$	
	Input impedance	Differential				100 2		$\text{G}\Omega \parallel \text{pF}$	
		Common-mode				100 9			
V_{CM}	Common-mode voltage ⁽¹⁾	$V_O = 0\text{ V}$				$(V^-) + 2$	$(V^+) - 2$	V	
CMRR	Common-mode rejection	$V_{\text{CM}} = \pm 13\text{ V}$, $\Delta R_S = 1\text{ k}\Omega$	INA141P, INA141U	$G = 10\text{ V/V}$	100	106		dB	
				$G = 100\text{ V/V}$	117	125			
			INA141PA, INA141UA	$G = 10\text{ V/V}$	93	100			
				$G = 100\text{ V/V}$	110	120			
INPUT BIAS CURRENT									
I_B	Input bias current	INA141P, INA141U				± 2	± 5	nA	
		INA141PA, INA141UA				± 2	± 10		
	Input bias current drift	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				± 30		$\text{pA}/^\circ\text{C}$	
I_{OS}	Input offset current	INA141P, INA141U				± 1	± 5	nA	
		INA141PA, INA141UA				± 1	± 10	nA	
	Input offset current drift	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				± 30		$\text{pA}/^\circ\text{C}$	
NOISE									
e_N	Voltage noise (RTI)	$R_S = 0\ \Omega$	$G = 10\text{ V/V}$	$f = 10\text{ Hz}$		22		$\text{nV}/\sqrt{\text{Hz}}$	
				$f = 100\text{ Hz}$		13			
				$f = 1\text{ kHz}$		12			
				$f_B = 0.1\text{ Hz to } 10\text{ Hz}$		0.6		μV_{PP}	
			$G = 100\text{ V/V}$	$f = 10\text{ Hz}$		10		$\text{nV}/\sqrt{\text{Hz}}$	
				$f = 100\text{ Hz}$		8			
				$f = 1\text{ kHz}$		8			
				$f_B = 0.1\text{ Hz to } 10\text{ Hz}$		0.2		μV_{PP}	
I_n	Current noise	$f = 10\text{ Hz}$				0.9		$\text{pA}/\sqrt{\text{Hz}}$	
		$f = 1\text{ kHz}$				0.3			
		$f_B = 0.1\text{ Hz to } 10\text{ Hz}$				30		pA_{PP}	

6.5 Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = 0\text{ V}$, $V_{\text{CM}} = V_S / 2$, and $G = 10\text{ V/V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
GAIN								
G	Gain				10	100		V/V
GE	Gain error	V _O = ±13.6 V	INA141P, INA141U	G = 10 V/V	±0.01	±0.05	%	
				G = 100 V/V	±0.03	±0.075		
			INA141PA, INA141UA	G = 10 V/V	±0.01	±0.15		
				G = 100 V/V	±0.03	±0.15		
	Gain drift ⁽⁶⁾	G = 10 V/V or 100 V/V, T _A = - 40°C to +85°C			±2	±10		ppm/°C
	Gain nonlinearity	INA141P, INA141U	G = 10 V/V		±0.0003	±0.001	% of FSR	
			G = 100 V/V		±0.0005	±0.002		
		INA141PA, INA141UA	G = 10 V/V		±0.0003	±0.002		
			G = 100 V/V		±0.0005	±0.004		
			OUTPUT					
	Output voltage				(V ⁻) + 1.4	(V _±) ± 0.9	(V ⁺) - 1.4	V
C _L	Load capacitance	Stable operation			1000			pF
I _{SC}	Short-circuit current	Continuous to V _S / 2			±20			mA
FREQUENCY RESPONSE								
BW	Bandwidth, - 3 dB	G = 10 V/V			610			kHz
		G = 100 V/V			200			kHz
SR	Slew rate	G = 10 V/V, V _O = ±10 V			2			V/μs
t _S	Settling time	To 0.01%, V _O = ±5 V	G = 10 V/V		7		μs	
			G = 100 V/V		9			
	Overload recovery	50% input overload			4			μs
POWER SUPPLY								
I _Q	Quiescent current	V _{IN} = 0 V			±750		±800	μA

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.

(2) Specified by wafer test.

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $V_{\text{REF}} = 0\text{ V}$, $G = 10\text{ V/V}$, $V_{\text{CM}} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

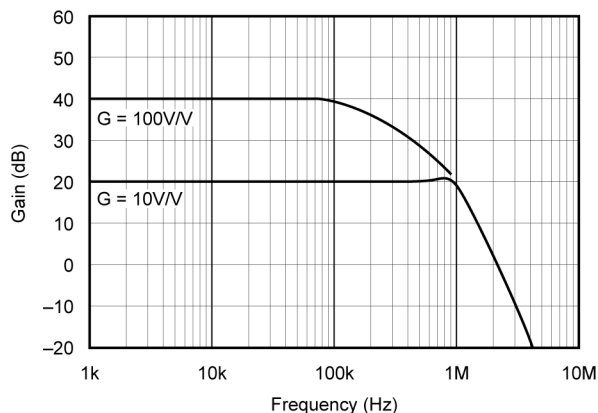


图 6-1. Gain vs Frequency

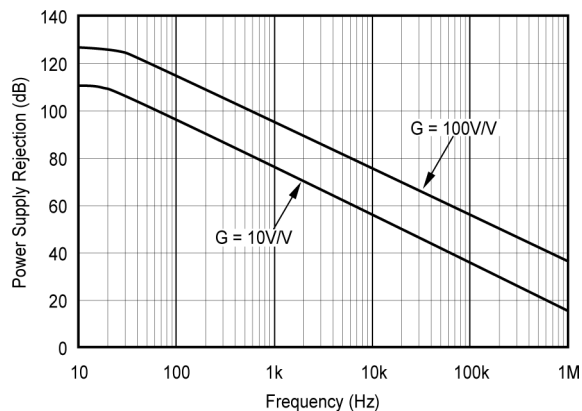


图 6-2. Common-Mode Rejection vs Frequency

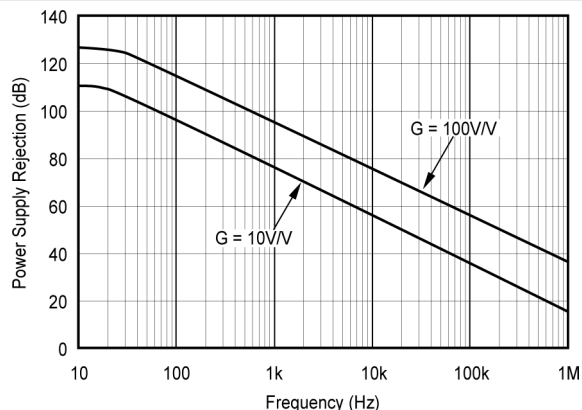


图 6-3. Positive Power Supply Rejection vs Frequency

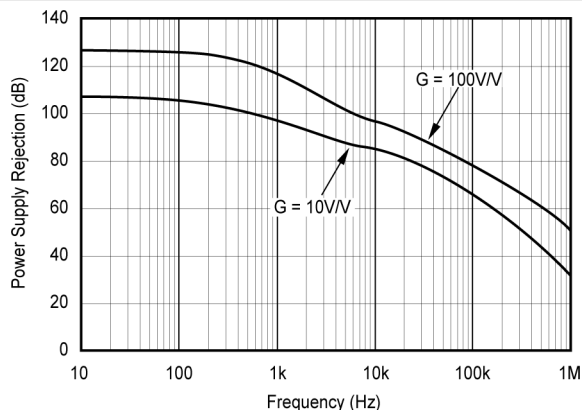


图 6-4. Negative Power Supply Rejection vs Frequency

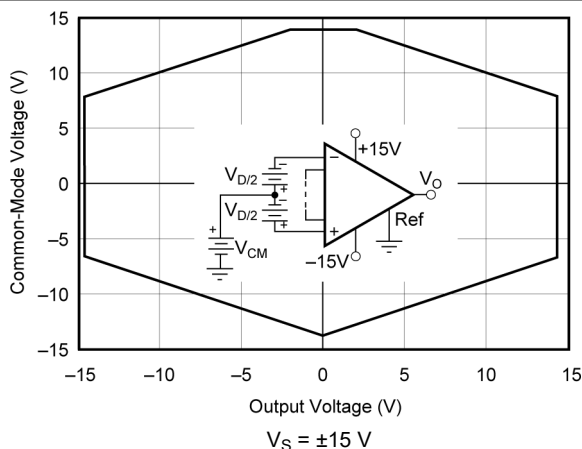


图 6-5. Input Common-Mode Range vs Output Voltage

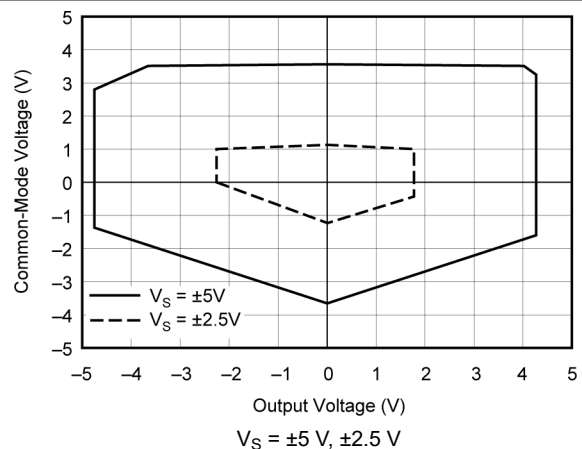


图 6-6. Input Common-Mode Range vs Output Voltage

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $V_{\text{REF}} = 0\text{ V}$, $G = 10\text{ V/V}$, $V_{\text{CM}} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

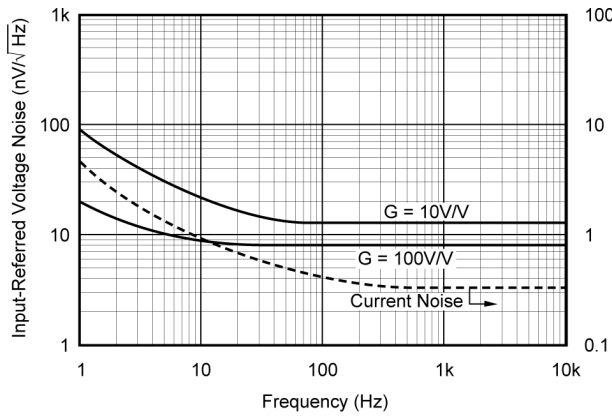


图 6-7. Input-Referred Noise vs Frequency

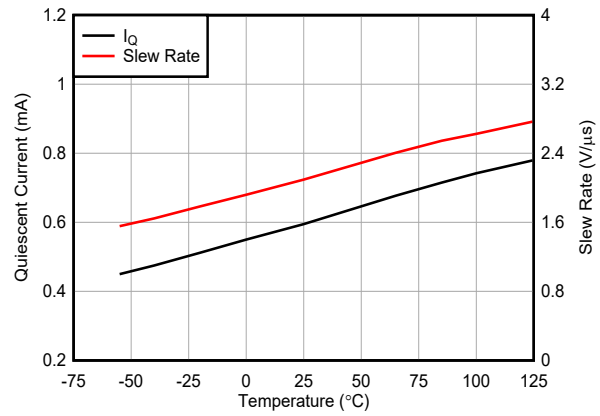


图 6-8. Quiescent Current and Slew Rate vs Temperature

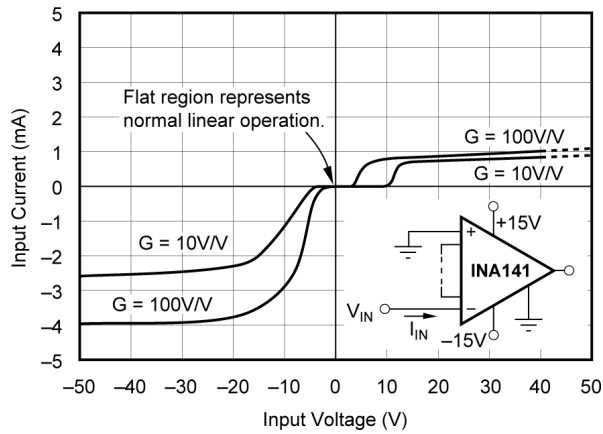


图 6-9. Input Overvoltage V/I Characteristics

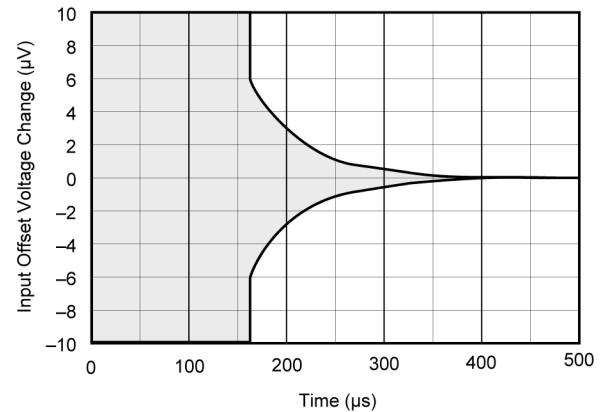


图 6-10. Input Offset Voltage Warmup

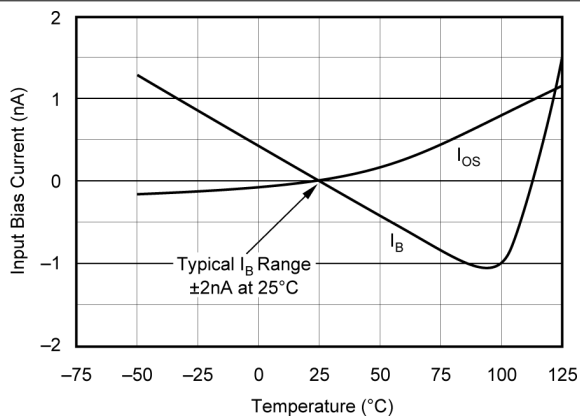


图 6-11. Input Bias Current vs Temperature

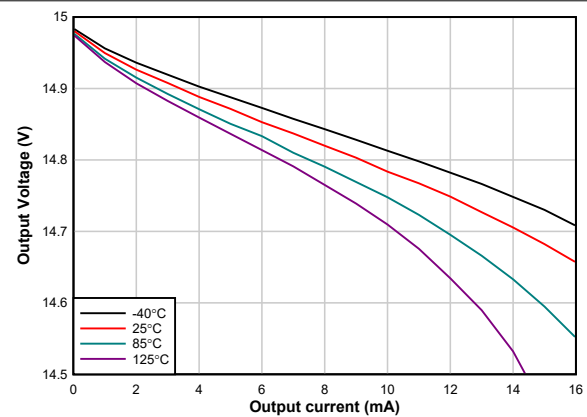


图 6-12. Positive Output Voltage Swing vs Output Current

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $V_{\text{REF}} = 0\text{ V}$, $G = 10\text{ V/V}$, $V_{\text{CM}} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

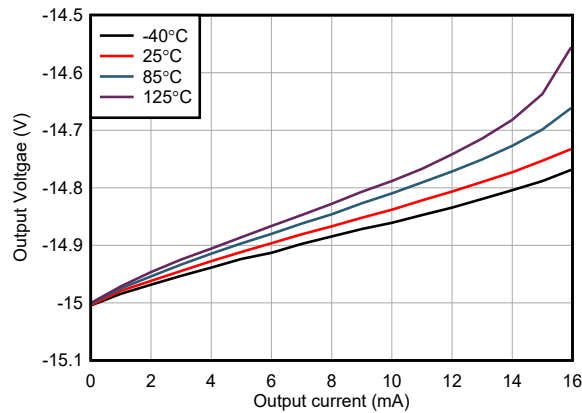


图 6-13. Negative Output Voltage Swing vs Output Current

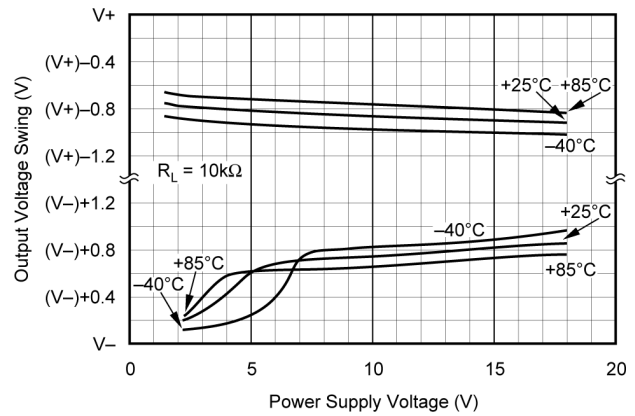


图 6-14. Output Voltage Swing vs Power Supply Voltage

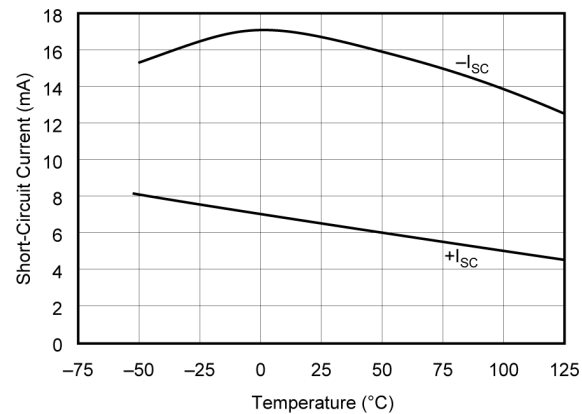


图 6-15. Short-circuit Output Current vs Temperature

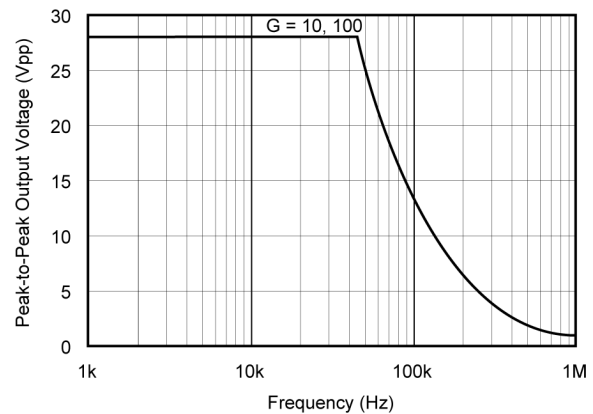


图 6-16. Maximum Output Voltage vs Frequency

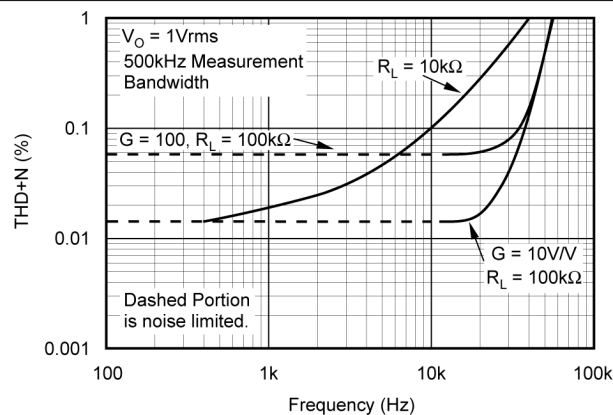


图 6-17. Total Harmonic Distortion + Noise vs Frequency

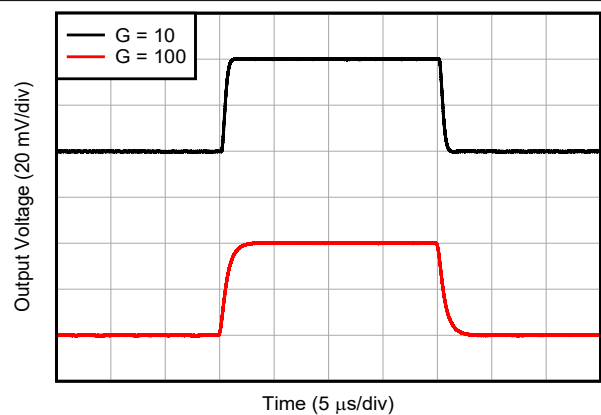


图 6-18. Small-Signal Step Response

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $V_{\text{REF}} = 0\text{ V}$, $G = 10\text{ V/V}$, $V_{\text{CM}} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

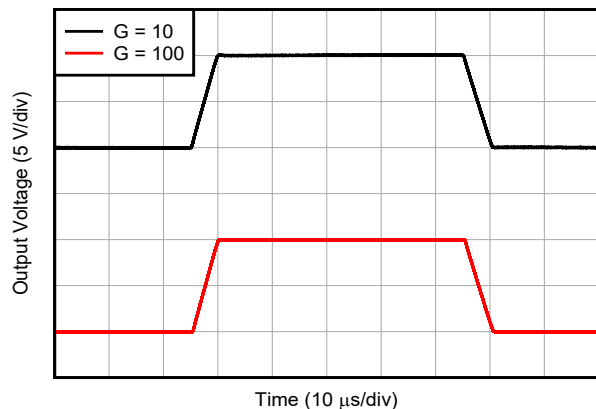


图 6-19. Large-Signal Step Response

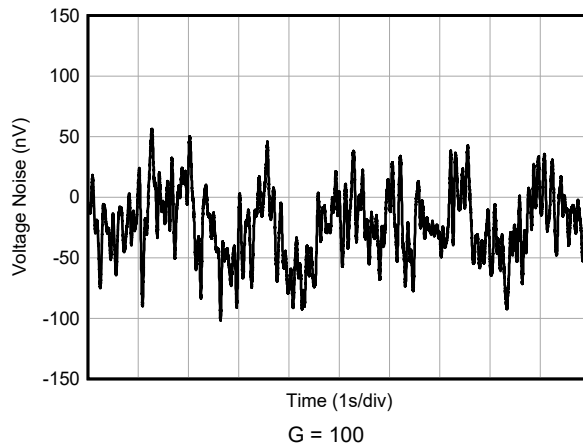


图 6-20. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

图 7-1 shows the basic connections required for operation of the INA141. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins as shown.

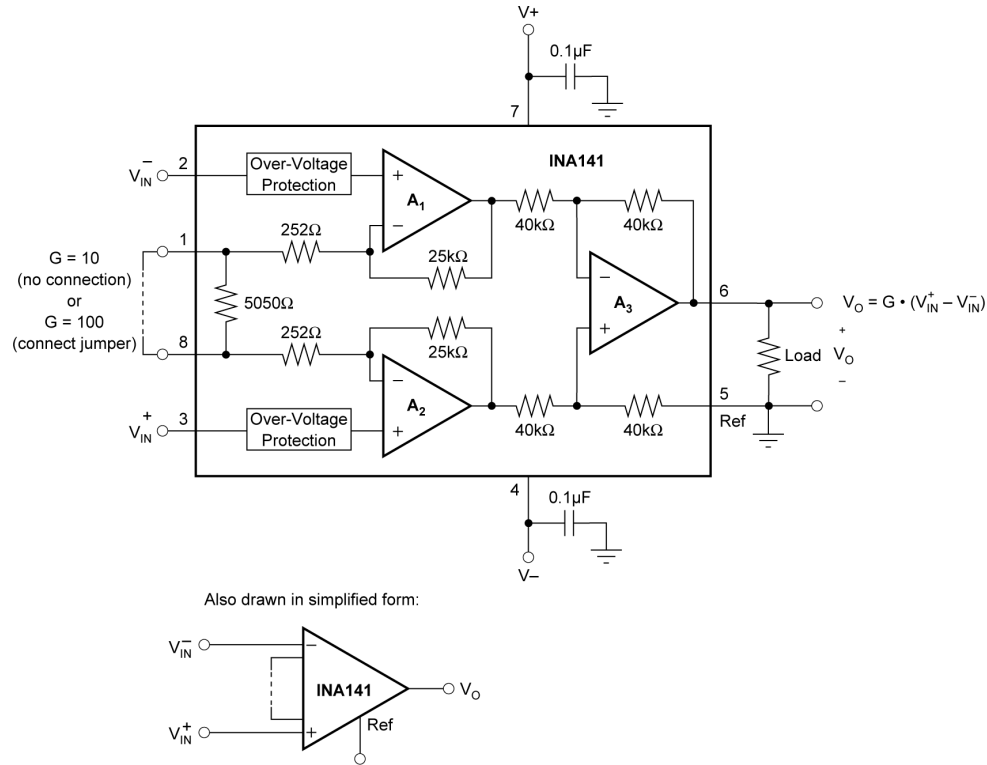


图 7-1. Basic Connections.

The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. A resistance of $8\ \Omega$ in series with the Ref pin causes a typical device to degrade to approximately 80 dB CMR ($G = 10\ \text{V/V}$).

7.1.1 Setting the Gain

Gain is selected with a jumper connection (see 图 7-1). With no jumper installed, $G = 10\ \text{V/V}$. With a jumper installed, $G = 100\ \text{V/V}$. To preserve good gain accuracy, this jumper must have low series resistance. A resistance of $0.5\ \Omega$ in series with the jumper decreases the gain by 0.1%.

Internal resistor ratios are laser trimmed to provide excellent gain accuracy. Actual resistor values can vary by approximately $\pm 25\%$ from the nominal values shown.

Gains between $10\ \text{V/V}$ and $100\ \text{V/V}$ are achieved by connecting an external resistor to the jumper pins. However, this configuration is not recommended because the $\pm 25\%$ variation of internal resistor values makes the required external resistor value uncertain. A companion model, the [INA128](#), features accurately trimmed internal resistors so that gains from $1\ \text{V/V}$ to $10,000\ \text{V/V}$ can be set with an external resistor.

7.1.2 Dynamic Performance

Typical performance curve *Gain vs Frequency* (图 6-1) shows that, despite the low quiescent current, the INA141 achieves wide bandwidth, even at $G = 100$ V/V. This wide bandwidth is a result of the current-feedback topology of the INA141. Settling time also remains excellent at $G = 100$ V/V.

7.1.3 Noise Performance

The INA141 provides very low noise in most applications. Low-frequency noise is approximately $0.2 \mu\text{V}_{\text{PP}}$ measured from 0.1 Hz to 10 Hz ($G = 100$ V/V). The INA141 provides dramatically improved noise when compared to state-of-the-art, chopper-stabilized amplifiers.

7.1.4 Offset Trimming

The INA141 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. 图 7-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref pin is summed with the output. The op-amp buffer provides low impedance at the Ref pin to preserve good common-mode rejection.

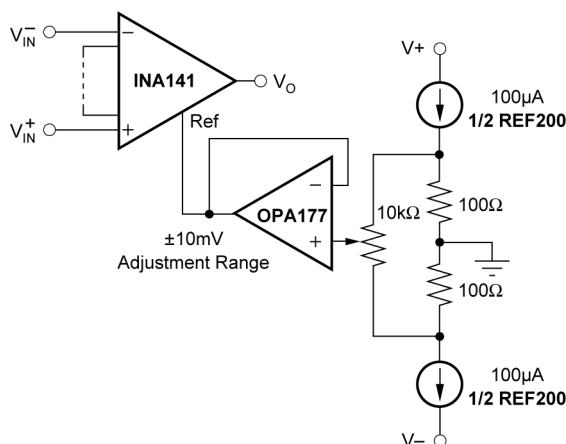


图 7-2. Optional Trimming of Output Offset Voltage.

7.1.5 Input Bias Current Return Path

The input impedance of the INA141 is extremely high—approximately $10^{10} \Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ± 2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 图 7-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA141 and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in 图 7-3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

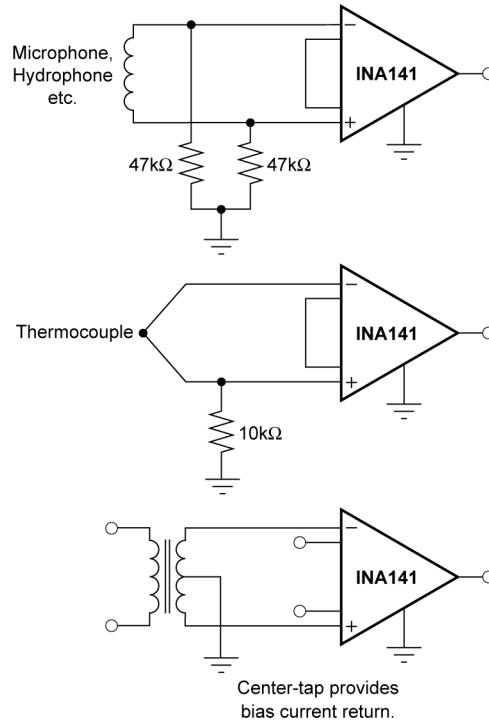


图 7-3. Providing an Input Common-Mode Current Path.

7.1.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA141 is from approximately 1.4 V less than the positive supply voltage to 1.7 V greater than the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2 . Therefore, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see the *Input Common-Mode Range vs Output Voltage* plots, 图 6-5 and 图 6-6).

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA141 is near 0 V even though both inputs are overloaded.

7.1.7 Low-Voltage Operation

The INA141 operates on power supplies as low as ± 2.25 V. Performance remains excellent with power supplies ranging from ± 2.25 V to ± 18 V. Most parameters vary only slightly through this supply voltage range—see Typical Performance Curves. Operation at a very low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The *Input Common-Mode Range vs Output Voltage* typical characteristics plots, 图 6-5 and 图 6-6, show the range of linear operation for ± 15 -V, ± 5 -V, and ± 2.5 -V supplies.

7.1.8 Input Protection

The inputs of the INA141 are individually protected for voltages up to ± 40 V. For example, a condition of -40 V on one input and $+40$ V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contributes excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.50 mA to 5 mA. The inputs are protected even if the power supplies are disconnected or turned off.

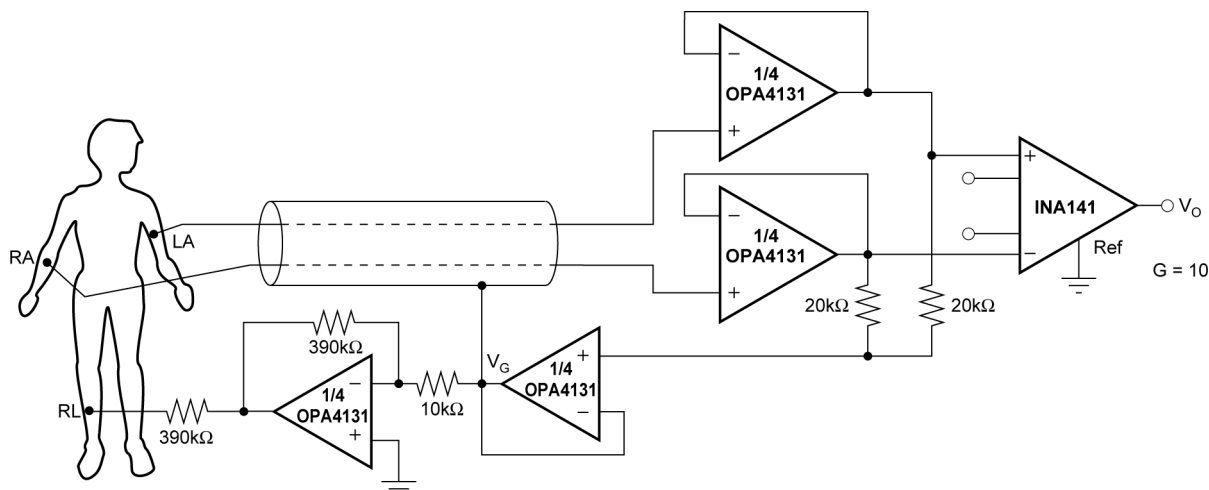


图 7-4. ECG Amplifier With Right-Leg Drive

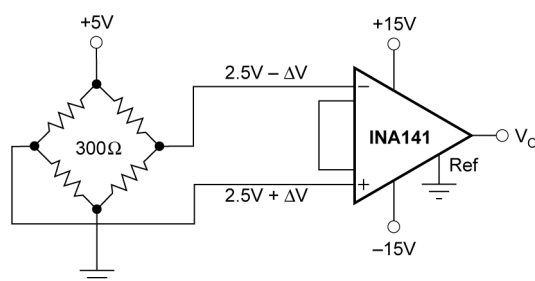


图 7-5. Bridge Amplifier

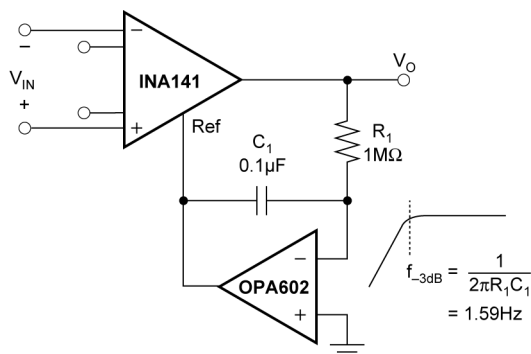
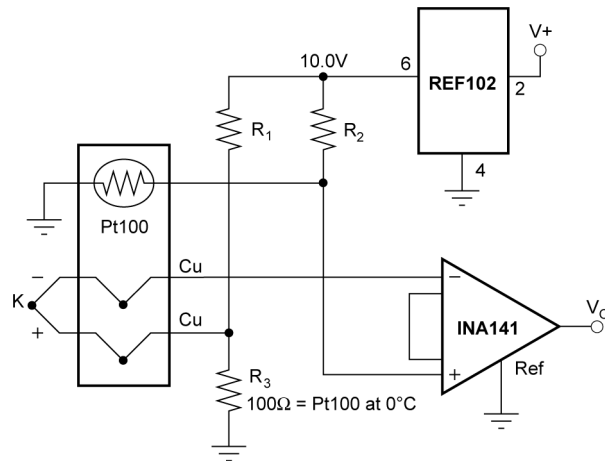


图 7-6. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R ₁ , R ₂
E	+ Chromel - Constantan	58.5	66.5kΩ
J	+ Iron - Constantan	50.2	76.8kΩ
K	+ Chromel - Alumel	39.4	97.6kΩ
T	+ Copper - Constantan	38.0	102kΩ

图 7-7. Thermocouple Amplifier With RTD Cold-Junction Compensation

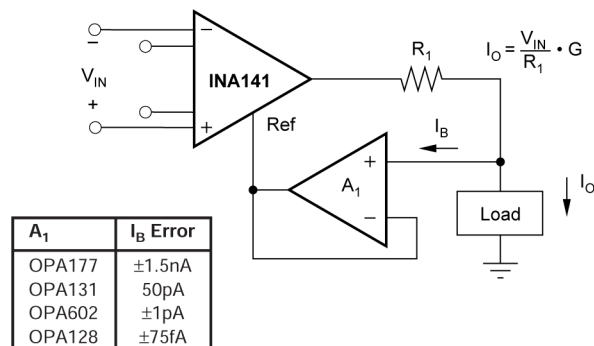


图 7-8. Differential Voltage-to-Current Converter

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA141U	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 141U
INA141U.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U
INA141U/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 141U
INA141U/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U
INA141UA	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI Nipdau	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA141U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA141UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA141U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA141UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA141U	D	SOIC	8	75	506.6	8	3940	4.32
INA141U.B	D	SOIC	8	75	506.6	8	3940	4.32
INA141UA	D	SOIC	8	75	506.6	8	3940	4.32
INA141UA.B	D	SOIC	8	75	506.6	8	3940	4.32

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司