

INA114 精密仪表放大器

1 特性

- 低失调电压：最大值为 $50\mu\text{V}$ (对于高增益)
- 低温漂：最大值为 $0.3\mu\text{V}/^\circ\text{C}$ (对于高增益)
- 低输入偏置电流： 2nA (最大值)
- 高共模抑制： 115dB (最小值)
- 输入过压保护： $\pm 40\text{V}$
- 宽电源电压范围： $\pm 2.25\text{V}$ 至 $\pm 18\text{V}$
- 封装：PDIP-8 和 SOIC-16

2 应用

- 外科手术设备
- 传声器
- 多功能继电器
- 火车控制和管理
- 轨道旁信令和控制

3 说明

INA114 是一款低成本通用仪表放大器，可提供出色的精度。此器件采用多功能三级运算放大器设计，尺寸小巧，适用于多种应用。

可通过单个外部电阻器在 1 到 10,000 范围内设置任意增益。内部输入保护可耐受高达 $\pm 40\text{V}$ 的电压且不会造成损坏。

INA114 经过激光修整，具有极低失调电压 ($50\mu\text{V}$)、低温漂 ($0.3\mu\text{V}/^\circ\text{C}$) 和高共模抑制 ($G = 1000$ 时为 115dB)。该器件可由低至 $\pm 2.25\text{V}$ 的电源供电，适用于电池供电型和 5V 单电源系统。

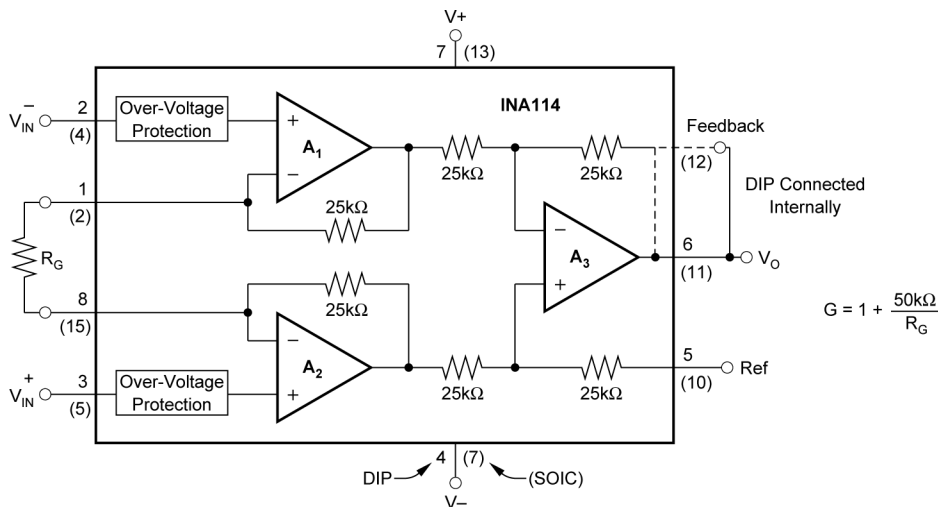
INA114 采用 8 引脚 PDIP 和 16 引脚 SOIC 表面贴装封装。采用两种封装时，额定工作温度范围均为 -40°C 至 $+85^\circ\text{C}$ 。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
INA114	P (PDIP, 8)	9.81mm × 9.43mm
	DW (SOIC, 16)	10.3mm × 10.3mm

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



原理图



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4 Pin Configuration and Functions

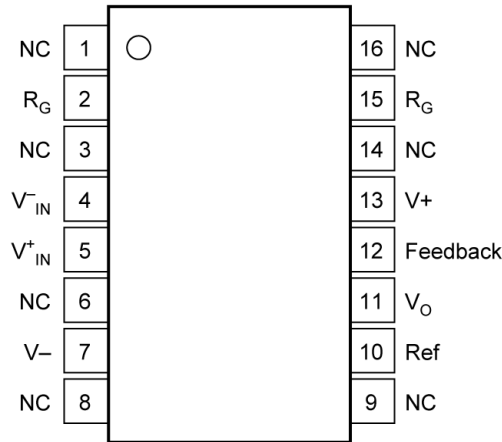


图 4-1. DW Package, 16-Pin SOIC (Top View)

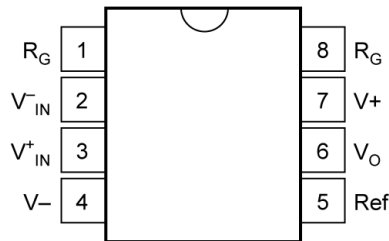


图 4-2. P Package, 8-Pin PDIP (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage	Single supply, V _S = (+V _S)		36	V
		Dual supply, V _S = (+V _S) - (-V _S)	- 18	18	V
	Signal input pins		- 40	40	V
V _O	Signal output voltage		(- V _S) - 0.5	(+V _S) + 0.5	V
I _S	Output short-circuit (to V _S /2)		Continuous		
T _A	Operating temperature		- 40	125	°C
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		- 40	125	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _S	Supply voltage	Single supply, V _S = (+V _S)	4.5	36	V
		Dual supply, V _S = (+V _S) - (-V _S)	±2.25	±18	
T _A	Specified temperature		- 40	85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA114		UNIT
		DW (SOIC)	P (PDIP)	
		16 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	74.2	110.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$, $V_{\text{REF}} = 0\text{V}$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V _{OS}	Offset voltage	RTI	INA114BP, BU		±10 + 20/G	±50 + 150/G		μV
			INA114AP, AU		±25 + 30/G	±125 + 500/G		
	Offset voltage drift	T _A = - 40°C to +85°C, RTI	INA114BP, BU		±0.1 + 0.5/G	±0.3 + 5/G		μV/°C
			INA114AP, AU		±0.25 + 5/G	±1 + 10/G		
	Long-term stability				±0.2 + 0.5/G			μV/mo
	Differential impedance				100 6			G Ω pF
	Common-mode impedance				100 6			G Ω pF
	Operating input voltage				(V ⁻) + 4	(V ⁺) - 4		V
PSRR	Power-supply rejection ratio	RTI, ±2.25V to ±18V			0.5 + 2/G	3 + 10/G		μV/V
CMRR	Common-mode rejection ratio	At dc to 60Hz, RTI, V _{CM} = ±10V, ΔR _S = 1kΩ	G = 1	INA114BP, BU	80	96		dB
				INA114AP, AU	75	90		
			G = 10	INA114BP, BU	96	115		
				INA114AP, AU	90	106		
			G = 100	INA114BP, BU	110	120		
				INA114AP, AU	106	110		
			G = 1000	INA114BP, BU	115	120		
				INA114AP, AU	106	110		
BIAS CURRENT								
I _B	Input bias current	V _{CM} = V _S / 2	INA114BP, BU		±0.5	±2		nA
			INA114AP, AU		±0.5	±5		
	Input bias current drift	T _A = - 40°C to +85°C	INA114BP, BU		±8			pA/°C
			INA114AP, AU		±8			
I _{OS}	Input offset current	V _{CM} = V _S / 2	INA114BP, BU		±0.5	±2		nA
			INA114AP, AU		±0.5	±5		
	Input offset current drift	T _A = - 40°C to +85°C	INA114BP, BU		±8			pA/°C
			INA114AP, AU		±8			
NOISE VOLTAGE								
	Voltage noise	G = 1000, R _S = 0 Ω	f = 10Hz		15			nV/ √ Hz
			f = 100Hz		11			
			f = 1kHz		11			
			f _B = 0.1Hz to 10Hz		0.4			μV _{PP}
	Noise current	f = 10Hz			0.4			pA/ √ Hz
		f = 1kHz			0.2			pA/ √ Hz
		f _B = 0.1Hz to 10Hz			18			pA _{PP}

5.5 Electrical Characteristics (续)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$, $V_{\text{REF}} = 0\text{V}$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
GAIN								
G	Gain equation				1 + (50kΩ / R _G)			V/V
	Range of gain				1		10000	V/V
GE	Gain error	V _O = ±10V, G = 1			±0.01		±0.05	%
			G = 10	INA114BP, BU	±0.02		±0.4	
				INA114AP, AU	±0.02		±0.5	
			G = 100	INA114BP, BU	±0.05		±0.5	
				INA114AP, AU	±0.05		±0.7	
			G = 1000	INA114BP, BU	±0.5		±1	
				INA114AP, AU	±0.5		±2	
	Gain drift				±2		±10	ppm/°C
		R _S = 50kΩ ⁽¹⁾			±25		±100	
	Gain nonlinearity	V _O = - 10V to +10V	G = 1	INA114BP, BU	±0.0001		±0.001	% of FSR
				INA114AP, AU	±0.0001		±0.002	
			G = 10, 100	INA114BP, BU	±0.0005		±0.002	
				INA114AP, AU	±0.0005		±0.004	
			G = 1000	INA114BP, BU	±0.002		±0.01	
				INA114AP, AU	±0.002		±0.02	
OUTPUT								
	Output voltage	I _O = 5mA, T _A = - 40°C to 85°C			(V -) +1.5	(V+) - 1.5		V
			V _S = ±11.4V		(V -) + 1.4	(V+) - 1.4		
			V _S = ±2.25V		(V -) +1	(V+) - 1		
	Load capacitance stability				1000			pF
I _{SC}	Short-circuit current	Continuous to V _S / 2			+20 / - 15			mA
FREQUENCY RESPONSE								
BW	Bandwidth, - 3dB	G = 1			1			MHz
		G = 10			100			kHz
		G = 100			10			
		G = 1000			1			
SR	Slew rate	G = 10, V _O = ±10V			0.3	0.6		V/μs
t _S	Settling time	0.01%, V _{STEP} = 10V	G = 1		18			μs
			G = 10		20			
			G = 100		120			
			G = 1000		1100			
	Overload recovery	50% overdrive			20			μs
POWER SUPPLY								
I _Q	Quiescent current	V _S = ±2.25V to ±18V, V _{IN} = 0V			±2.2		±3	mA

(1) Temperature coefficient of the "50k Ω " term in the gain equation.

5.6 Typical Characteristics

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 1\text{V/V}$ (unless otherwise noted)

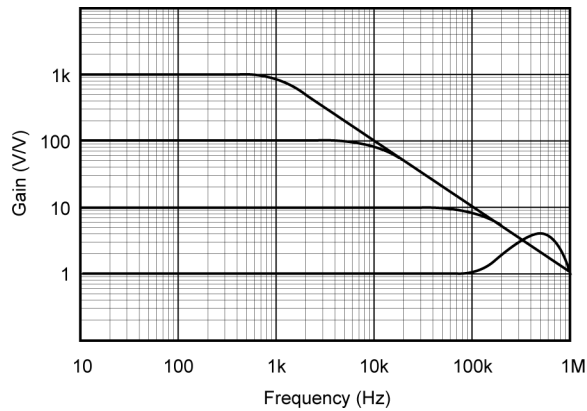


图 5-1. Gain vs Frequency

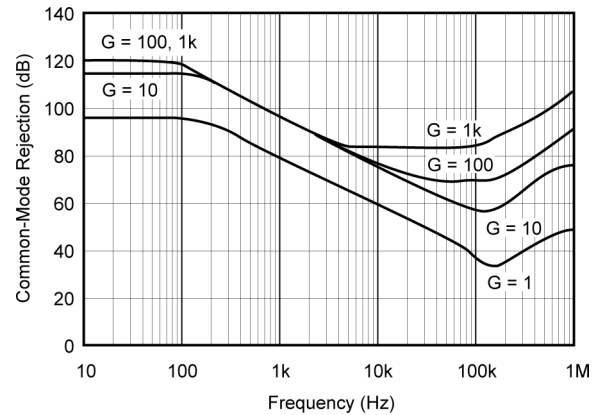


图 5-2. Common-mode Rejection vs Frequency

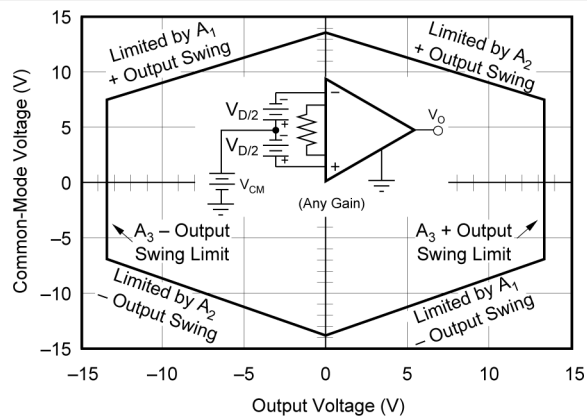


图 5-3. Input Common-mode Voltage Range vs Output Voltage

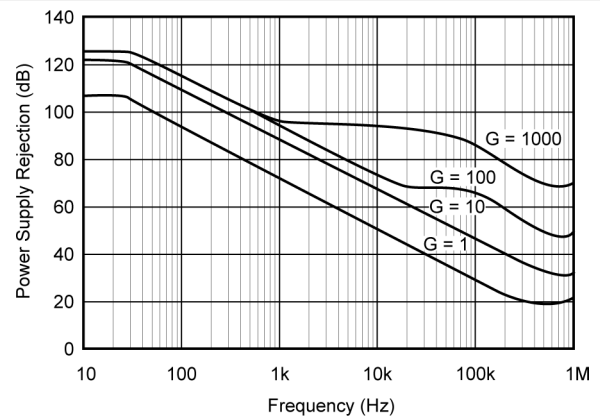


图 5-4. Positive Power Supply Rejection vs Frequency

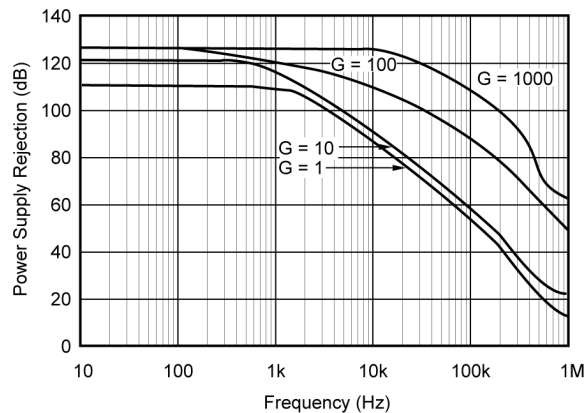


图 5-5. Negative Power Supply Rejection vs Frequency

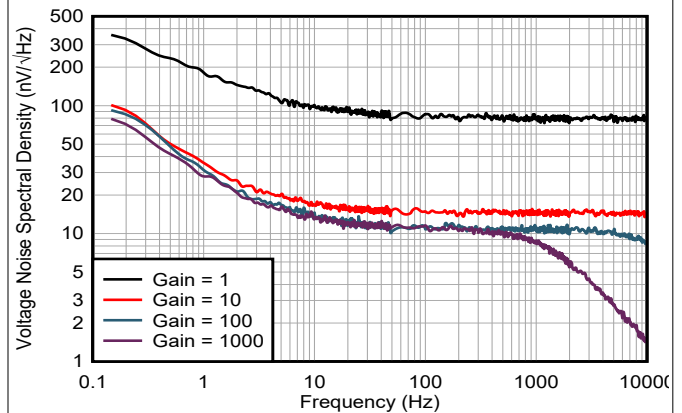


图 5-6. Input-Referred Noise Voltage vs Frequency

5.6 Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 1\text{V/V}$ (unless otherwise noted)

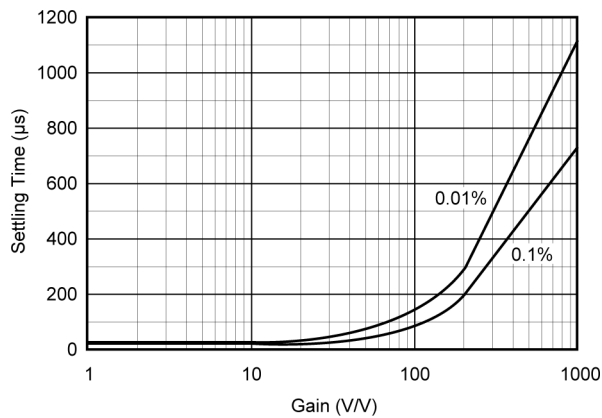


图 5-7. Settling Time vs Gain

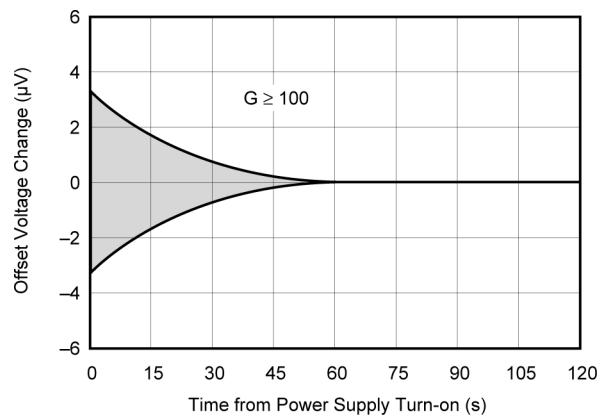


图 5-8. Offset Voltage Warm-up vs Time

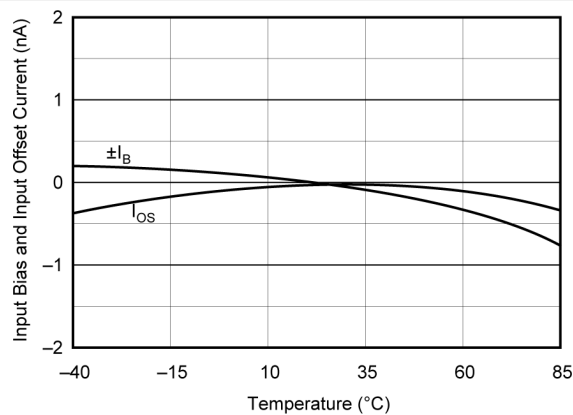


图 5-9. Input Bias and Input Offset Current vs Temperature

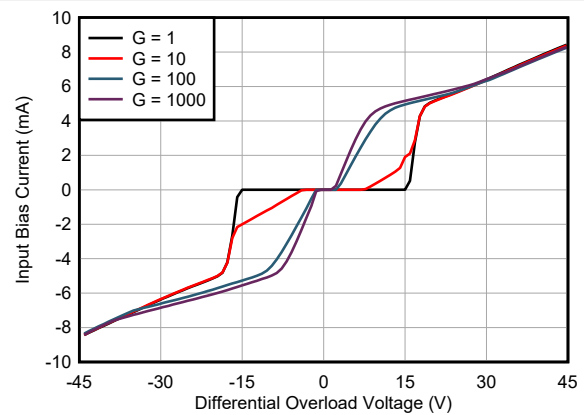


图 5-10. Input Bias Current vs Differential Input Voltage

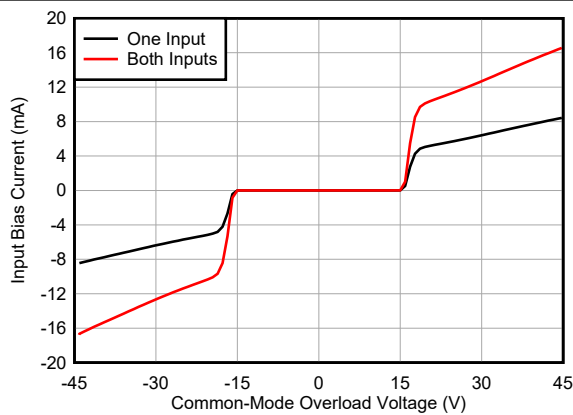


图 5-11. Input Bias Current vs Common-Mode Input Voltage

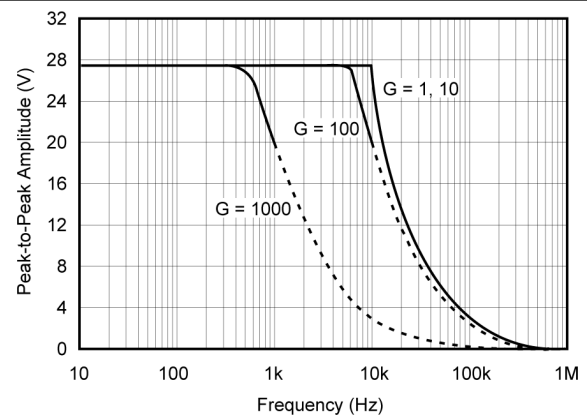


图 5-12. Maximum Output Swing vs Frequency

5.6 Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 1\text{V/V}$ (unless otherwise noted)

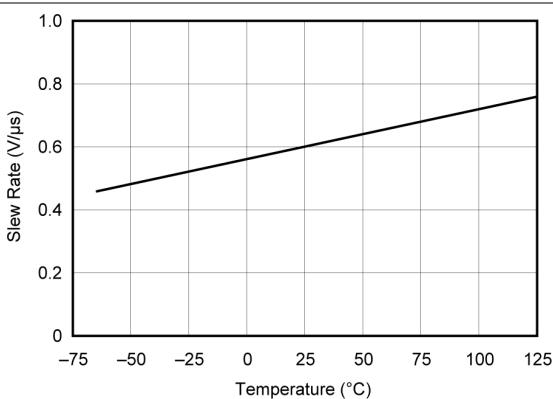


图 5-13. Slew Rate vs Temperature

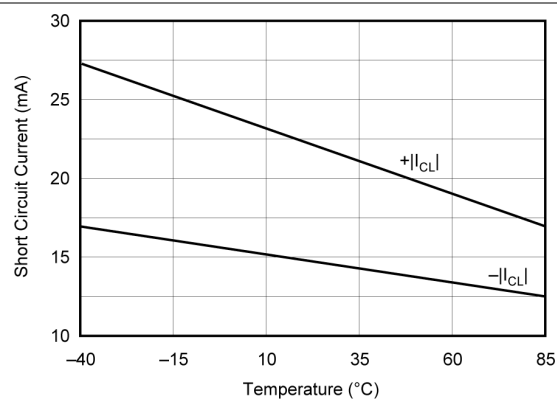


图 5-14. Output Current Limit vs Temperature

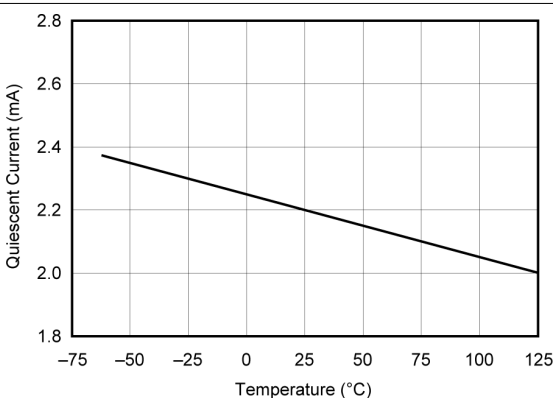


图 5-15. Quiescent Current vs Temperature

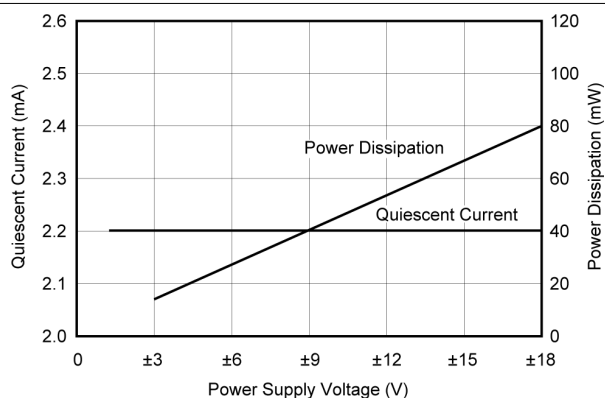


图 5-16. Quiescent Current and Power Dissipation vs Power Supply Voltage

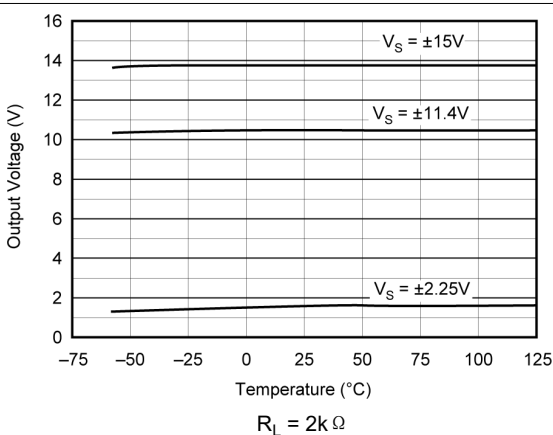


图 5-17. Positive Signal Swing vs Temperature

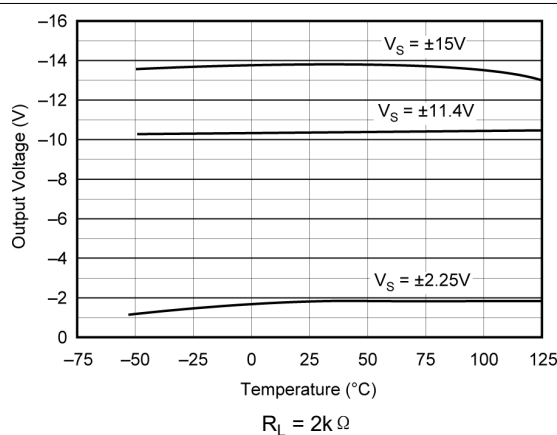


图 5-18. Negative Signal Swing vs Temperature

5.6 Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 1\text{V/V}$ (unless otherwise noted)

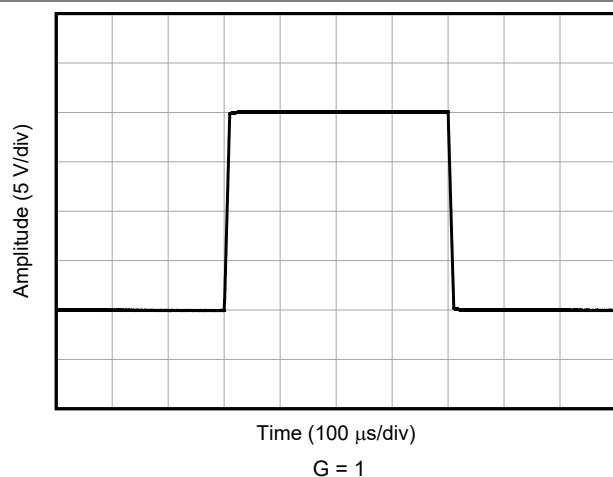


图 5-19. Large-Signal Response

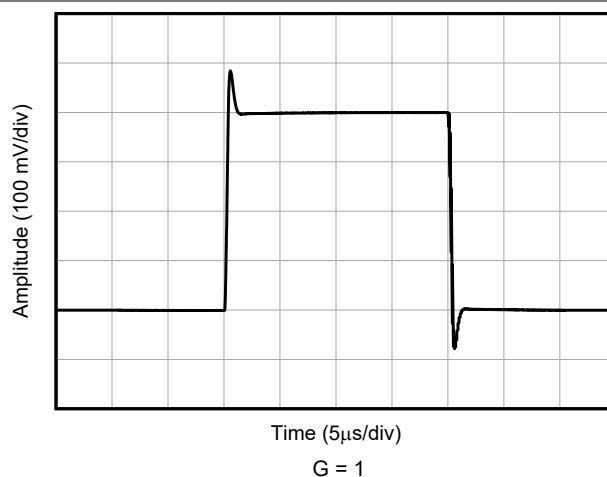


图 5-20. Small-Signal Response

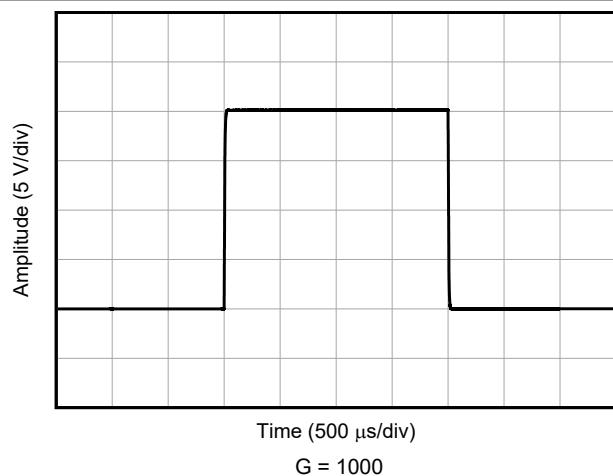


图 5-21. Large-Signal Response

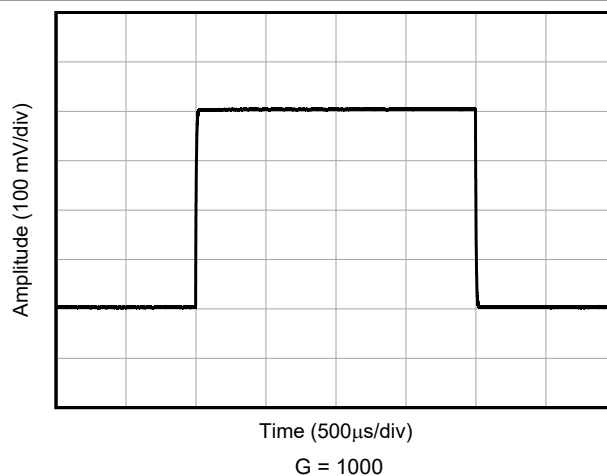


图 5-22. Small-Signal Response

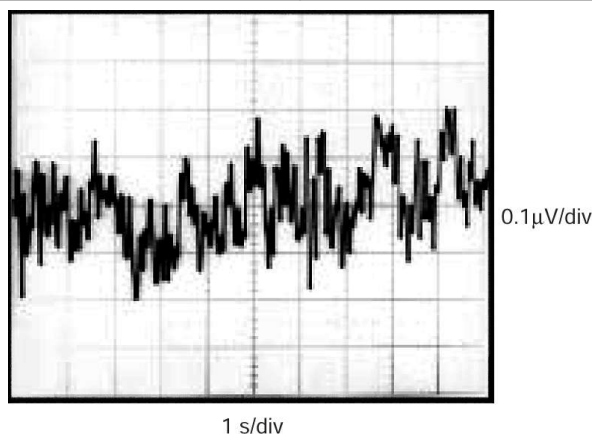


图 5-23. Input-Referred Noise, 0.1Hz to 10Hz

6 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

6.1 Application Information

图 6-1 shows the basic connections required for operation of the INA114. Applications with noisy or high-impedance power supplies can require decoupling capacitors close to the device pins as shown.

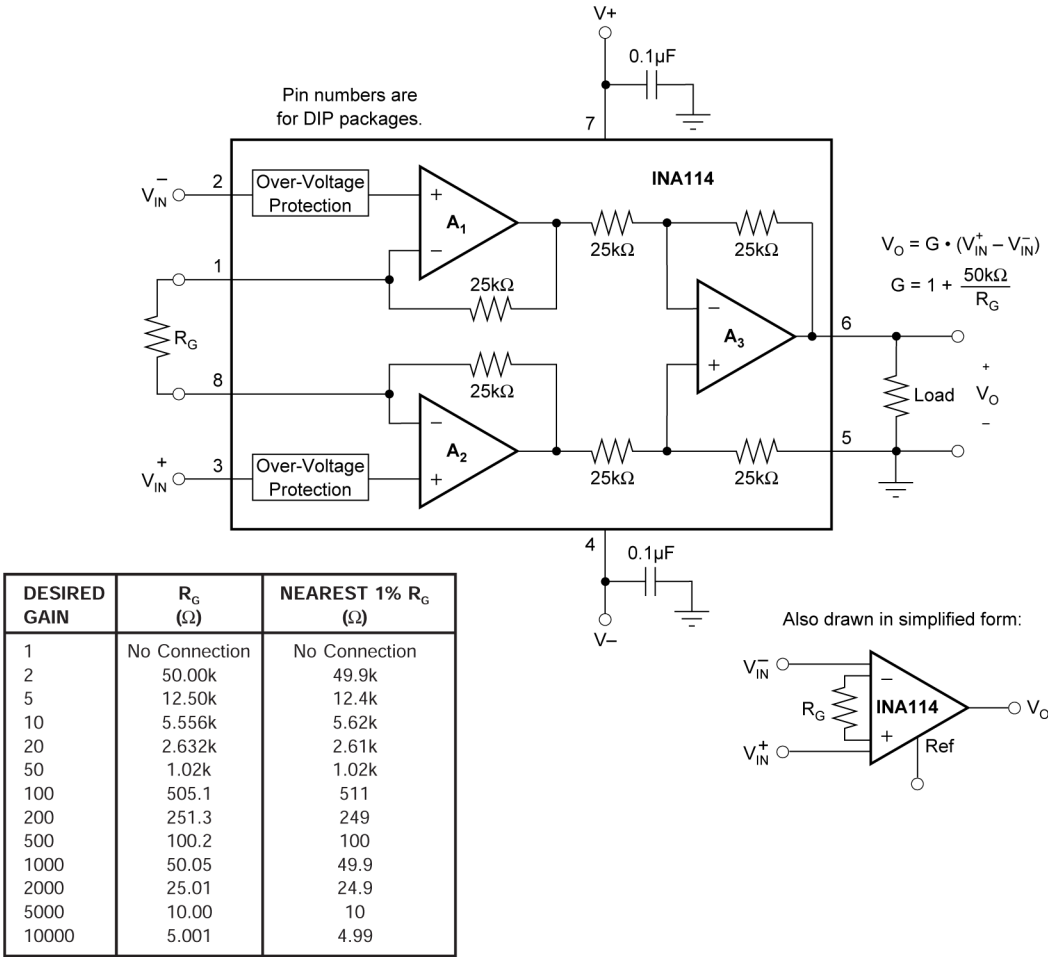


图 6-1. Basic Connections.

The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to provide good common-mode rejection. A resistance of 5 Ω in series with the Ref pin causes a typical device to degrade to approximately 80dB CMR ($G = 1$).

6.1.1 Setting the Gain

Gain of the INA114 is set by connecting a single external resistor, R_G :

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

图 6-1 shows commonly used gains and resistor values.

The 50-k Ω term in 方程式 1 comes from the sum of the two internal feedback resistors. These resistors are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. The contribution of R_G to gain accuracy and drift is directly inferred from the gain 方程式 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

6.1.2 Noise Performance

The INA114 provides very low noise in most applications. For differential source impedances less than 1k Ω , the INA103 can provide lower noise. For source impedances greater than 50k Ω , the INA111 FET-input instrumentation amplifier can provide lower noise.

Low frequency noise of the INA114 is approximately 0.4 μV_{PP} measured from 0.1Hz to 10Hz. This noise is approximately one-tenth the noise of *low noise* chopper-stabilized amplifiers.

6.1.3 Offset Trimming

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. 图 6-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref pin is summed at the output. Maintain low impedance at this node to maintain good common-mode rejection by buffering trim voltage with an op amp as shown.

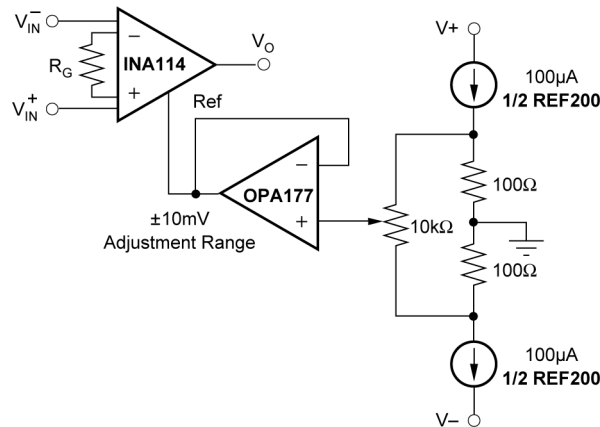


图 6-2. Optional Trimming of Output Offset Voltage.

6.1.4 Input Bias Current Return Path

The input impedance of the INA114 is extremely high—approximately $10^{10} \Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than $\pm 1 \text{ nA}$, and can be either polarity as a result of cancellation circuitry. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. 图 6-3 shows various provisions for an input bias current path. Without a bias current return path, the inputs float to a potential that exceeds the common-mode range of the INA114 and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see thermocouple example in 图 6-3). With higher source impedance, use two resistors to provide a balanced input, with the possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

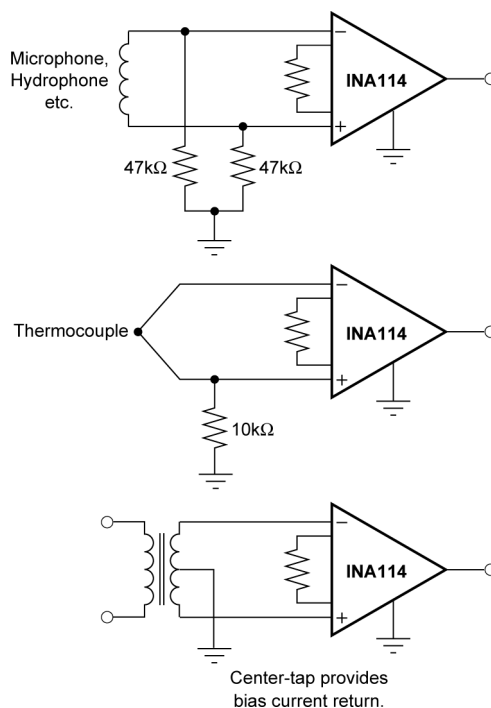


图 6-3. Providing an Input Common-Mode Current Path.

6.1.5 Input Common-Mode Range

The linear common-mode range of the input op amps of the INA114 is approximately $\pm 13.75\text{V}$ (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range is limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The common-mode range is related to the output voltage of the complete amplifier—see typical characteristic curve *Input Common-Mode Range vs Output Voltage*.

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. 图 6-4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3 . For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve *Input Common-Mode Voltage Range vs Output Voltage*). If necessary, add gain after the INA114 to increase the voltage swing.

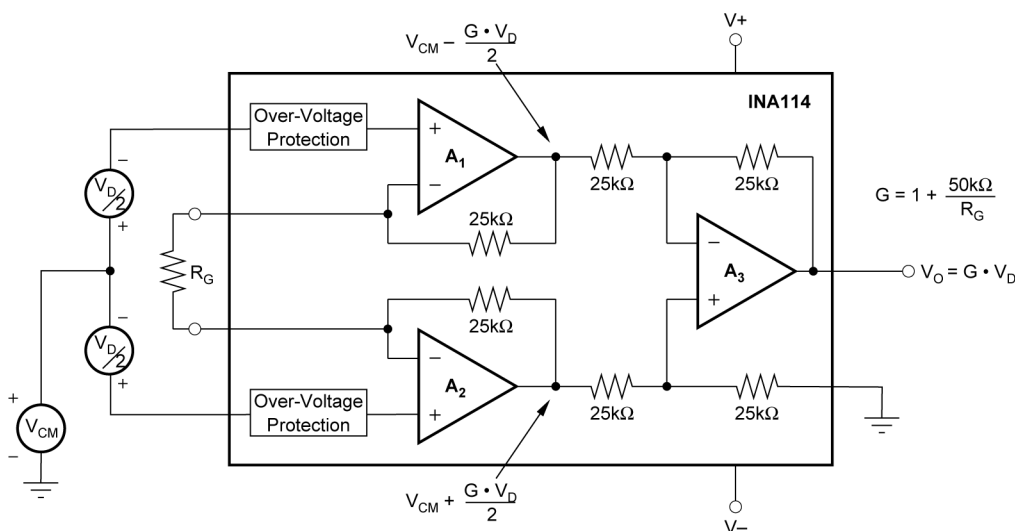


图 6-4. Voltage Swing of A_1 and A_2

Input overload often produces an output voltage that appears normal. For example, an input voltage of 20V on one input and 40V on the other input obviously exceeds the linear common-mode range of both input amplifiers. Both input amplifiers are saturated to nearly the same output voltage limit; therefore, the difference voltage measured by the output amplifier is near zero. The output of the INA114 is near 0V even though both inputs are overloaded.

6.1.6 Input Protection

The inputs of the INA114 are individually protected for voltages up to $\pm 40\text{V}$. For example, a condition of -40V on one input and $+40\text{V}$ on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). Typical performance curve *Input Bias Current vs Common-Mode Input Voltage* shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

6.1.7 Output Voltage Sense (SOIC-16 Package Only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. 图 6-5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths can cause instability. This instability can be generally be eliminated with a high-frequency feedback path through C_1 . Drive heavy loads or long lines by connecting a buffer inside the feedback path (see 图 6-6).

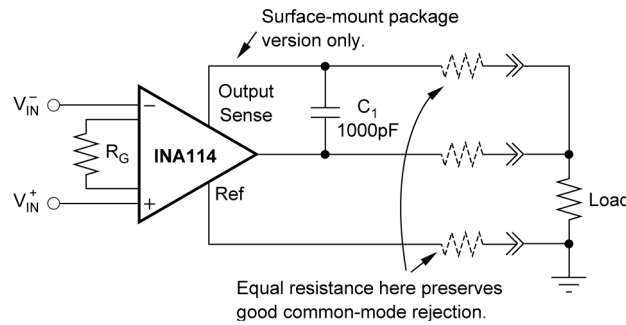


图 6-5. Remote Load and Ground Sensing

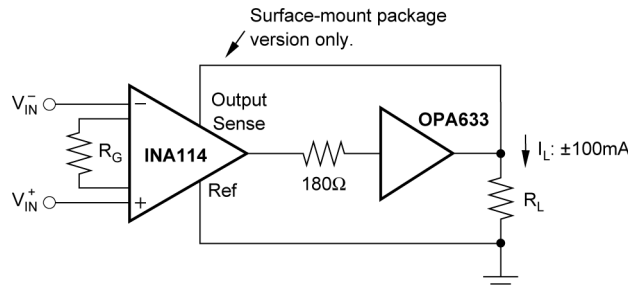


图 6-6. Buffered Output for Heavy Loads

7 Typical Applications

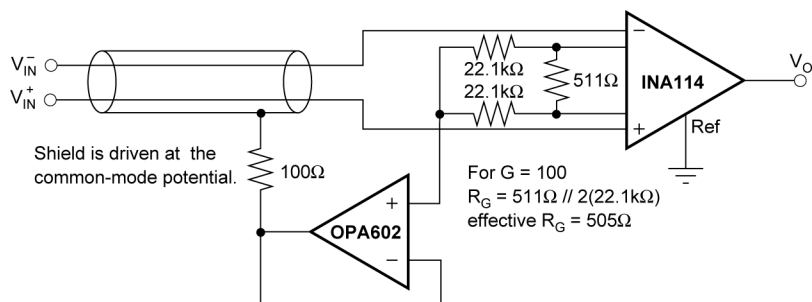


图 7-1. Shield Driver Circuit

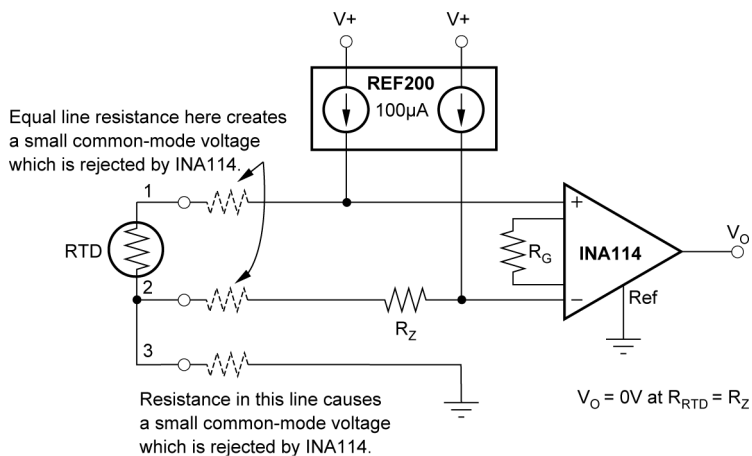
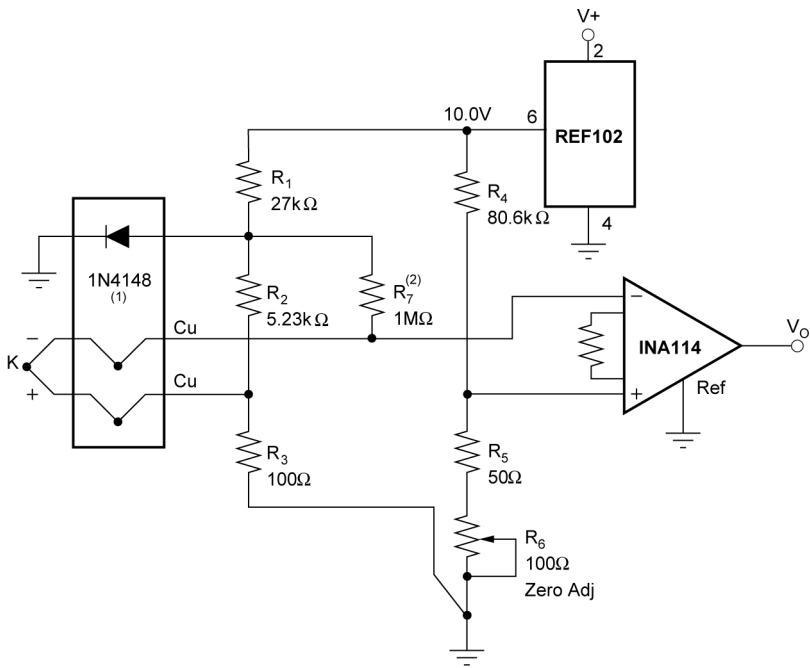


图 7-2. RTD Temperature Measurement Circuit



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT ($\mu\text{V}/^\circ\text{C}$)	R_2 ($R_3 = 100\Omega$)	R_4 ($R_5 + R_6 = 100\Omega$)
E	Chromel Constantan	58.5	3.48k Ω	56.2k Ω
J	Iron Constantan	50.2	4.12k Ω	64.9k Ω
K	Chromel Alumel	39.4	5.23k Ω	80.6k Ω
T	Copper Constantan	38.0	5.49k Ω	84.5k Ω

NOTES: (1) $-2.1\text{mV}/^\circ\text{C}$ at $200\mu\text{A}$. (2) R_7 provides down-scale burn-out indication.

图 7-3. Thermocouple Amplifier with Cold Junction Compensation

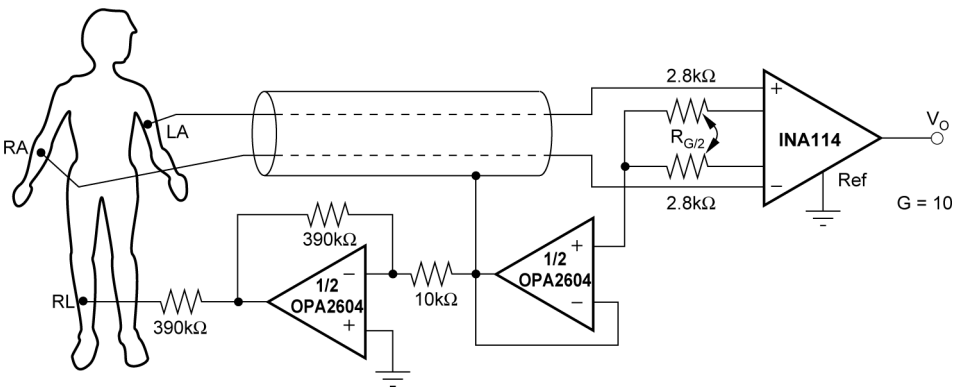


图 7-4. ECG Amplifier with Right-Leg Drive

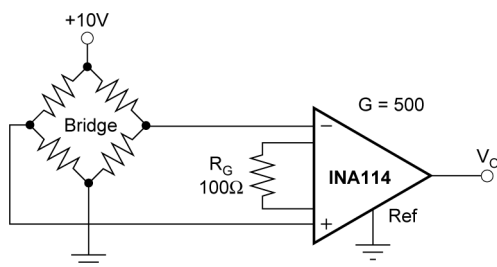


图 7-5. Bridge Transducer Amplifier

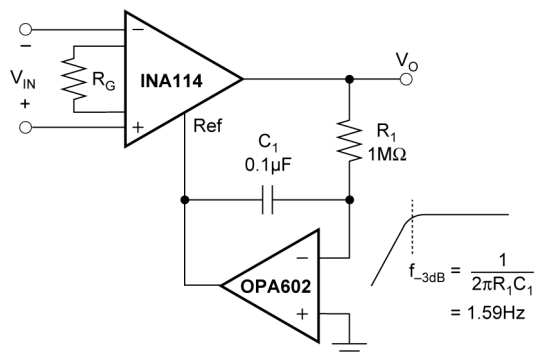
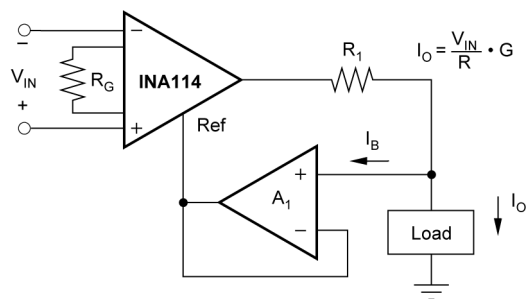


图 7-6. AC-Coupled Instrumentation Amplifier



A ₁	I _B Error
OPA177	±1.5nA
OPA602	1pA
OPA128	75fA

图 7-7. Differential Voltage-to-Current Converter

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.3 Trademarks

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (March 1998) to Revision A (January 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 添加了 ESD 等级、建议运行条件、热性能信息、应用和实施、典型应用、器件和文档支持 以及 机械、封装和可订购信息 部分.....	1
• 将整个数据表中的 SOL 封装名称更改为 SOIC.....	1
• 向 特性 中的低失调电压和低温漂要点中添加了 “ (对于高增益) ”	1
• 将 特性 中低温漂要点的值从 0.25μV/°C 更改为 0.3μV/°C.....	1
• 更新了 应用 中的要点.....	1
• Added symbols in <i>Absolute Maximum Ratings</i>	3
• Changed supply voltage to show dual supply and single supply in <i>Absolute Maximum Ratings</i>	3
• Changed "Input Voltage Range" to "Signal input pins" in <i>Absolute Maximum Ratings</i>	3
• Added signal output voltage to <i>Absolute Maximum Ratings</i>	3
• Changed output short-circuit from "ground" to "V _S / 2" in <i>Absolute Maximum Ratings</i>	3
• Added DW (SOIC) package ambient thermal resistance value.....	3
• Changed ambient thermal resistance value for P (PDIP) package from 80°C/W to 110.2°C/W.....	3
• Added symbols in <i>Electrical Characteristics</i>	4
• Changed offset voltage maximum value from ±50 + 100/G to ±50 + 150/G.....	4
• Changed "Offset Voltage vs Temperature" to "Offset voltage drift".....	4
• Changed offset voltage drift test condition from T _A = T _{MIN} to T _{MAX} to T _A = - 40°C to +85°C	4

• Changed offset voltage drift maximum value from $\pm 0.25 + 5/G$ to $\pm 0.3 + 5/G$	4
• Deleted safe input voltage from <i>Electrical Characteristics</i>	4
• Changed "Input Common-Mode Range" to "Operating input voltage".....	4
• Changed "Offset Voltage vs Power Supply" to "Power-supply rejection ratio".....	4
• Changed "Bias current vs Temperature" to "Input bias current drift".....	4
• Added " $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ " test condition to input bias current drift.....	4
• Changed "Offset Current vs Temperature" to "Input offset current drift".....	4
• Added " $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ " test condition to input offset current drift.....	4
• Added " $V_O = \pm 10\text{V}$ " test condition to gain error.....	4
• Changed "Gain vs Temperature" to "Gain drift".....	4
• Added " $V_O = -10\text{V}$ to $+10\text{V}$ " test condition to gain nonlinearity.....	4
• Changed output voltage values from ± 13.5 (min) and ± 13.7 (typ) to $(V-) + 1.5$ (min) and $(V+) - 1.5$ (max).....	4
• Changed output voltage test condition from T_{MIN} to T_{MAX} to $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4
• Added output voltage test conditions for $V_S = \pm 11.4\text{V}$ and $V_S = \pm 2.25\text{V}$	4
• Added $V_{\text{STEP}} = 10\text{V}$ test condition to settling time.....	4
• Deleted power supply voltage range typical value of $\pm 15\text{V}$	4
• Moved voltage range, operating temperature range, and thermal resistance from <i>Electrical Characteristics</i> to <i>Recommended Operating Conditions</i> and <i>Thermal Information</i>	4
• Updated Figure 5-6, <i>Input-referred Noise Voltage vs Frequency</i>	6
• Updated Figure 5-10, <i>Input Bias Current vs Differential Input Voltage</i>	6
• Updated Figure 5-11, <i>Input Bias Current vs Common-Mode Input Voltage</i>	6
• Updated Figure 5-19 to Figure 22, Small- and Large-Signal Response plots.....	6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA114AP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	INA114AP
INA114AP.B	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA114AP
INA114AU	Active	Production	SOIC (DW) 16	40 TUBE	Yes	Call TI Nipdau	Level-3-260C-168 HR	-40 to 85	INA114AU
INA114AU.B	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114AU
INA114AU/1K	Active	Production	SOIC (DW) 16	1000 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-40 to 85	INA114AU
INA114AU/1K.B	Active	Production	SOIC (DW) 16	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114AU
INA114BP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	INA114BP
INA114BP.B	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA114BP
INA114BU	Active	Production	SOIC (DW) 16	40 TUBE	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA114BU
INA114BU.B	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114BU
INA114BU/1K	Active	Production	SOIC (DW) 16	1000 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA114BU
INA114BU/1K.B	Active	Production	SOIC (DW) 16	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114BU

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

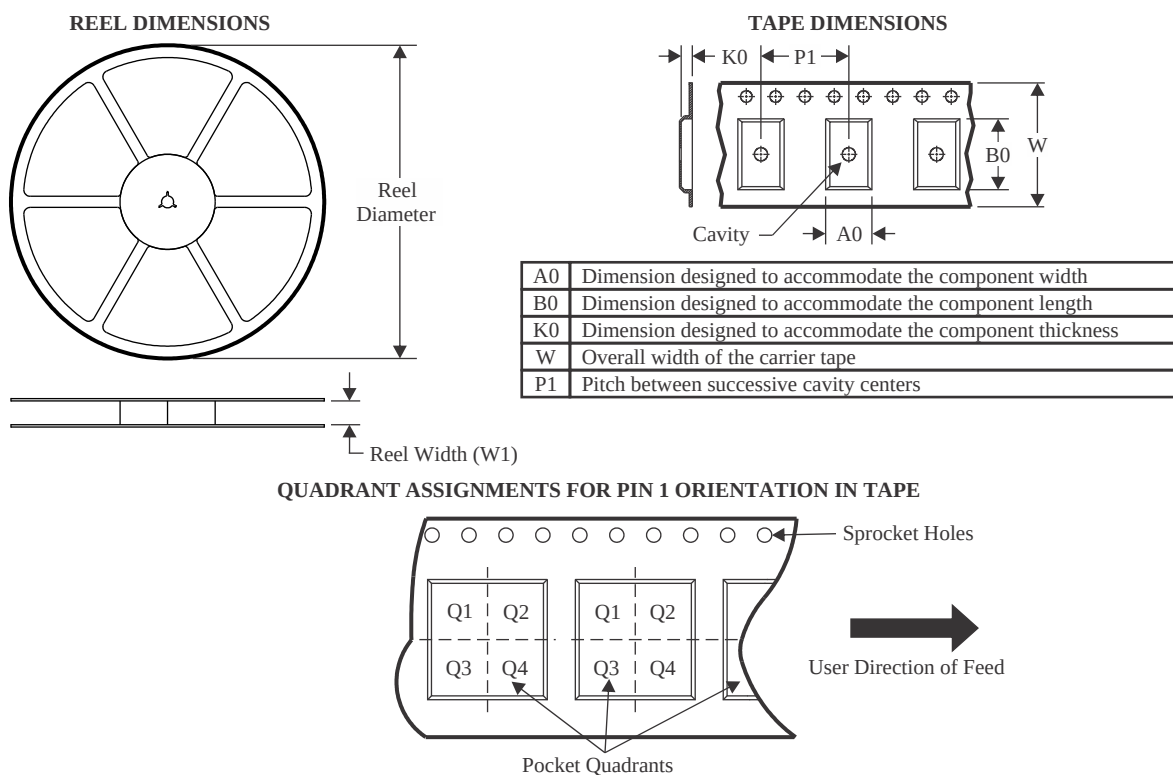
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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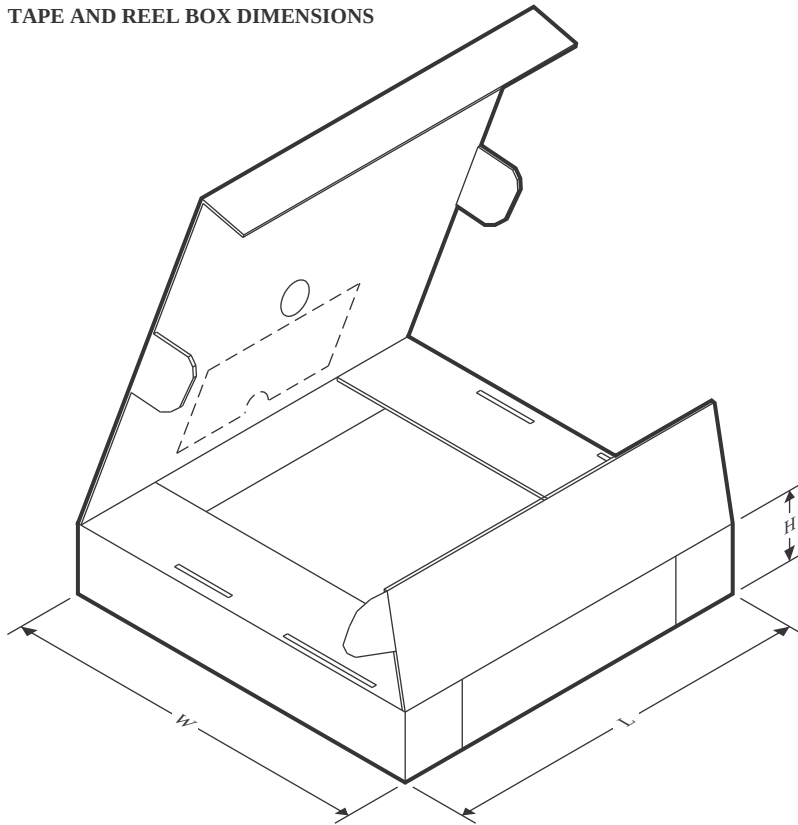
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA114AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA114BU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

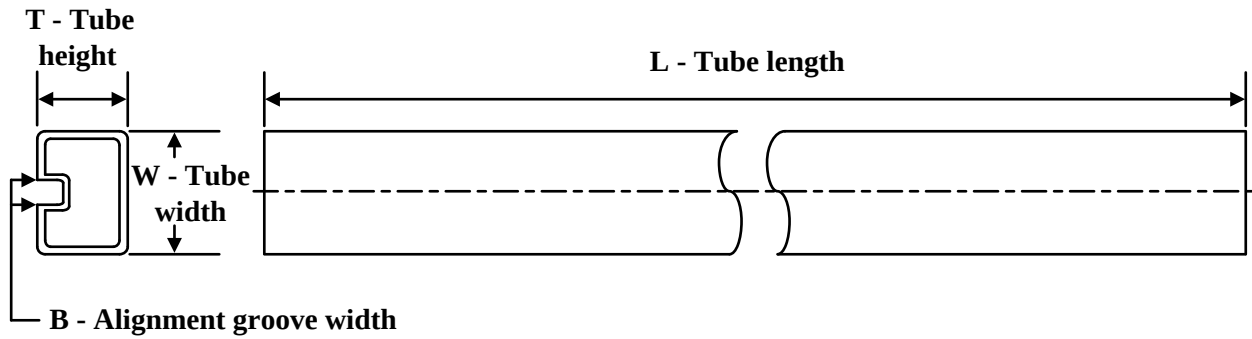
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA114AU/1K	SOIC	DW	16	1000	353.0	353.0	32.0
INA114BU/1K	SOIC	DW	16	1000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA114AP	P	PDIP	8	50	506	13.97	11230	4.32
INA114AP.B	P	PDIP	8	50	506	13.97	11230	4.32
INA114AU	DW	SOIC	16	40	507	12.83	5080	6.6
INA114AU.B	DW	SOIC	16	40	507	12.83	5080	6.6
INA114BP	P	PDIP	8	50	506	13.97	11230	4.32
INA114BP.B	P	PDIP	8	50	506	13.97	11230	4.32
INA114BU	DW	SOIC	16	40	507	12.83	5080	6.6
INA114BU.B	DW	SOIC	16	40	507	12.83	5080	6.6

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