DS90LVRA2 LVDS 双路差分线路接收器

1 特性

- 600Mbps (300MHz) 转换速率
- 50ps 差分延迟（典型值）
- 0.1ns 通道间延迟（典型值）
- 1.8V 电源
- 直通引脚排列
- 在断电模式下，LVDS 输入端具有高阻抗
- 输出压摆率控制
- LVDS 输入可接受 LVDS/CML/LVPECL 信号
- 符合 ANSI/TIA/EIA-644 标准
- 引脚与 DS90LV028A-Q1 兼容
- OPN 型号
  - 标准：0°C 至 70°C
  - 工业：-40°C 至 +85°C

2 应用

- 通信设备
- 企业系统
- 工业
- 个人电子产品

3 说明

DS90LVRA2 是一款专为需要高输入共模范围、高数据速率和具有压摆率控制 CMOS 输出的应用而设计的双路 CMOS 差分线路接收器。该器件旨在利用低电压差分信号 (LVDS) 技术支持 600Mbps (300MHz) 的数据速率。

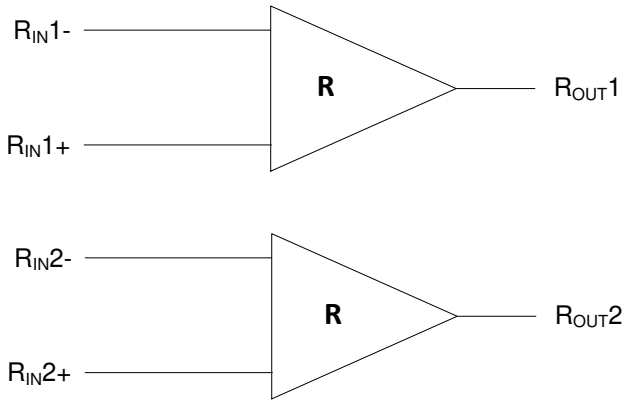
DS90LVRA2 可接受低电压（350mV 典型值）差分输入信号，并根据电源电压将其转换为 1.8V CMOS 输出电平。DS90LVRA2 采用直通式设计，可简化 PCB 布局。

DS90LVRA2 和配套的 LVDS 线路驱动器 DS90LV027AQ 可为高速点对点接口应用提供针对高功耗 PECL/ECL 器件的全新替代方案。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
DS90LVRA2	DEM（WSON，8）	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能图

Table of Contents

4 Revision History

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Pin Configuration and Functions

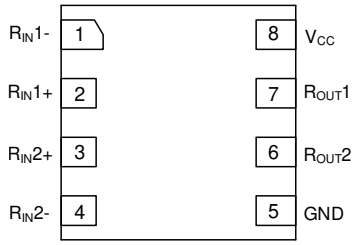


图 5-1. DEM Package, WSON 8 Pin (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	5	G	Ground pin
$R_{IN}1-$	1	I	Inverting receiver input pin
$R_{IN}2-$	4	I	
$R_{IN}1+$	2	I	Non-inverting receiver input pin
$R_{IN}2+$	3	I	
$R_{OUT}2$	6	O	Receiver output pin
$R_{OUT}1$	7	O	
V_{CC}	8	P	Power supply pin

(1) I = input, O = output, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply Voltage (V_{CC})		–0.3	4	V
Input Voltage (R_{IN}+, R_{IN}–)		–5	6	V
Differential Voltage (R_{IN}+ - R_{IN}–) for LVDS		0	3	V
Output Voltage (R_{OUT})		–0.3	1.98	V
Lead Temperature Range Soldering	(4 sec.)		260	°C
Maximum Junction Temperature			135	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended* Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, and performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±5000	V
		Charged-device model (CDM), per JEDEC specification JS-002[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (1.8 V mode)	1.62	1.80	1.98	V
V_R	Receiver input voltage (LVDS)	0		3.0	V
T_A	Operating free-air temperature (Standard)	0		70	°C
T_A	Operating free-air temperature (Industrial)	–40		85	°C
T_{PCB}	PCB temperature (Standard)			80	°C
T_{PCB}	PCB temperature (Industrial)			95	°C
T_J	Junction temperature (Standard)			95	°C
T_J	Junction temperature (Industrial)			110	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		DEM (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	143.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ITH}	Positive-going differential input voltage threshold	V_{IB} = -1 V or 2 V, VCC = 1.62 V to 1.98 V			100	mV
V_{ITL}	Negative-going differential input voltage threshold		-100			
V_{HYS}	Differential input voltage hysteresis, $V_{IT1} - V_{IT2}$	VCC = 1.62 V to 1.98 V	20	40	90	mV
V_{CM_RANGE}	Input common mode voltage range	VCC = 1.62 - 1.98 V	-1	1.2	2	V
V_{OH_1V8}	High-level output voltage	I_{OH} = – 4 mA, VCC=1.8 V ±10%	1.3			V
V_{OL_1V8}	Low-level output voltage	I_{OL} = 4 mA, VCC=1.8 V ±10%			0.2	V
I_{CC_ACTIVE}	Supply current	V_{CC} = 1.98 V, No load, Steady-state, VID=200 mV/-200 mV			25	mA
I_I	Input current (A or B inputs)	V_I = -1.0 V, Other input open			±35	µA
I_I	Input current (A or B inputs)	V_I = 2.0 V, Other input open			±20	µA
$I_{I(OFF)}$	Power-off output current (Y or Z outputs)	V_Y or V_Z = 1.98 V, V_{CC} = 0 V			±20	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_A or V_B = -1 V or 2.0 V, V_{CC} = 0 V			±35	µA

(1) All typical values are at 25°C and with a 1.8 V supply.

6.6 Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(2) (3) (4)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
t_{PHLD_1p8}	Differential Propagation Delay High to Low	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC 1.8 V ±10%	2.7	4.3	7.7	ns
$t_{PHLD\_1p8\_5}$	Differential Propagation Delay High to Low	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC 1.8 V ±5%	2.8	4.3	7.1	ns
t_{PLHD_1p8}	Differential Propagation Delay Low to High	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC 1.8 V ±10%	2.7	4.4	7.7	ns
$t_{PLHD\_1p8\_5}$	Differential Propagation Delay Low to High	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC 1.8 V ±5%	2.8	4.4	7.1	ns
$t_{SKD1\_1p8\_S}$	Differential Pulse Skew ($t_{PHLD} - t_{PLHD}$)((7))	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC=1.8 V±10%	-500		500	ps
$t_{SKD1\_1p8\_5\_S}$	Differential Pulse Skew ($t_{PHLD} - t_{PLHD}$)((7))	V_{ID} = 200 mV, C_L = 10 pF, trf=1 ns, VCC=1.8 V±5%	-400		400	ps
$t_{SKD1\_1p8\_S\_400M}$	Differential Pulse Skew ($t_{PHLD} - t_{PLHD}$) ((7))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns DR=400M, VCC=1.8 V±10%	-500		500	ps
$t_{SKD1\_1p8\_5\_S\_400M}$	Differential Pulse Skew ($t_{PHLD} - t_{PLHD}$) ((7))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns DR=400M,VCC=1.8 V±5%	-400		400	ps
t_{SKD2_1p8}	Differential Channel-to-Channel Skew-same device (6)	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±10%			0.5	ns

6.6 Switching Characteristics (continued)

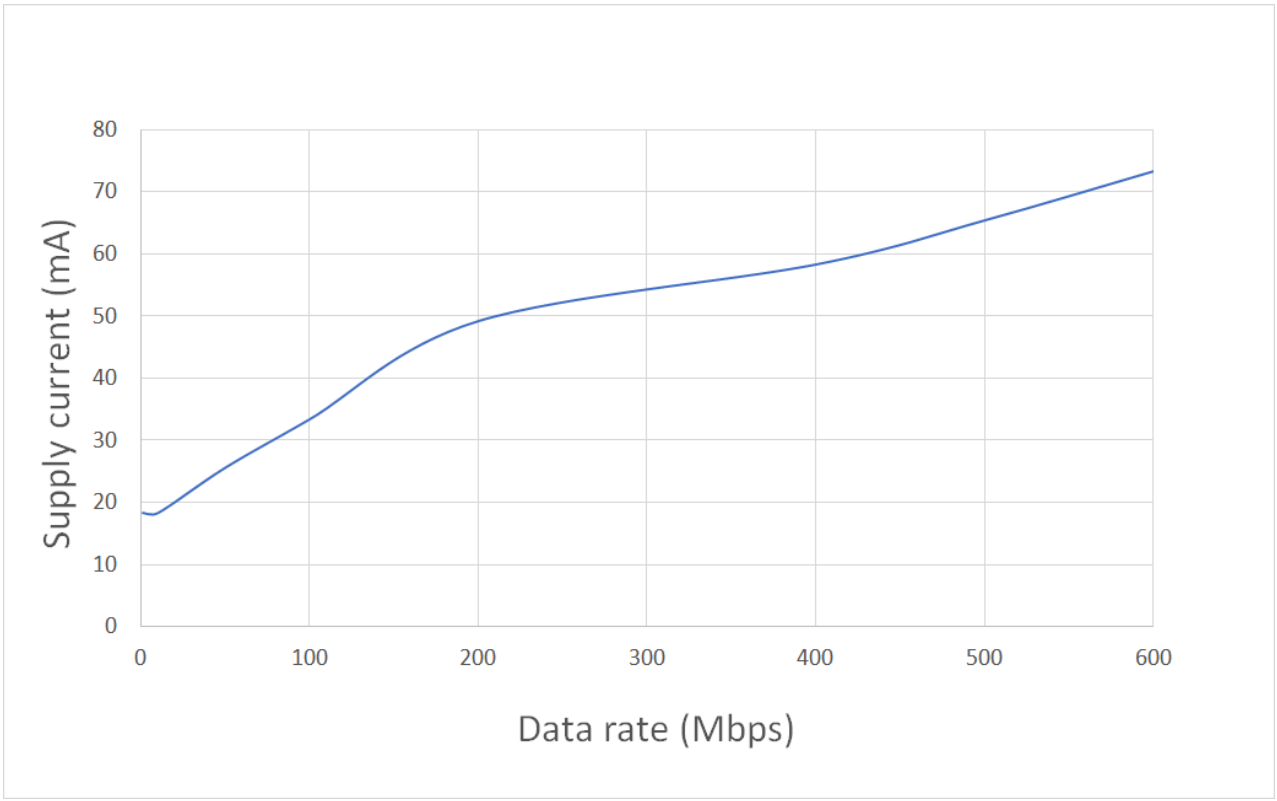
Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(2) (3) (4)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
$t_{SKD2\_1p8\_5}$	Differential Channel-to-Channel Skew-same device ((8))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5%			0.4	ns
$t_{SKD3\_1p8\_5}$	Differential Part to Part Skew ((9))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5% at same temperature			2.7	ns
$t_{SKD3\_1p8\_5\_25C}$	Differential Part to Part Skew ((9))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5% at TJ =25℃			2.6	ns
$t_{SKD3\_1p8\_5\_70C}$	Differential Part to Part Skew ((9))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5% at TJ =70℃			2.7	ns
$t_{SKD3\_1p8\_5\_125C}$	Differential Part to Part Skew ((9))	V_{ID} = 200 mV, C_L = 10 pF, trf=0.25 ns VCC=1.8 V±5% at TJ= 125℃			2.7	ns
t_{TLH_1p8}	Rise Time		250	500	720	ps
t_{THL_1p8}	Fall Time		250	500	720	ps
f_{MAX}	Maximum Operating Frequency ((11))		300			MHz

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
(2) All typicals are given for: V_{CC} = 1.8V and T_A = +25°C.
(3) C_L includes probe and jig capacitance.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω , t_r and t_f (0% to 100%) ⩽ 3 ns for R_{IN}.
(5) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(6) t_{SKD2} is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(7) t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(8) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max), V_{OH} (min), load = 15 pF (stray plus probes).

6.7 Typical Characteristics

Typical power supply current -vs- data rate (VCC 1.8 V, 5 pF output load, 2 channels)



7 Parameter Measurement Information

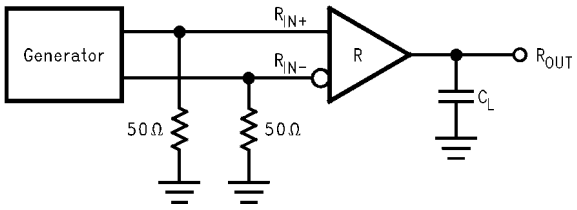


图 7-1. Receiver Propagation Delay and Transition Time Test Circuit

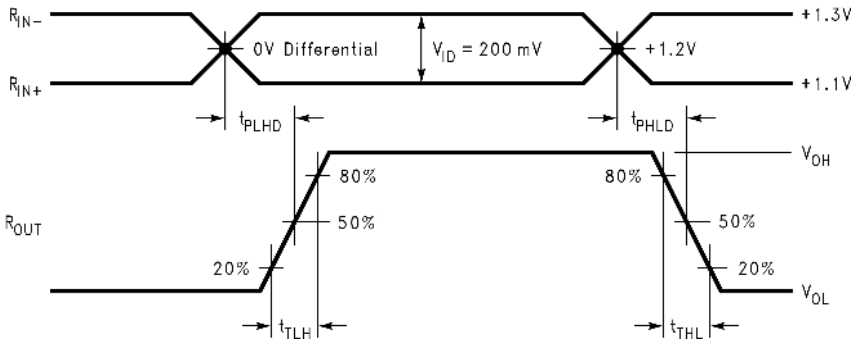


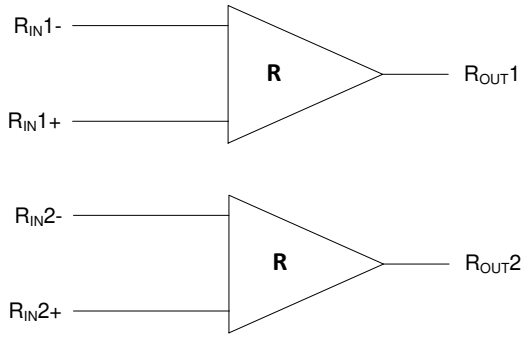
图 7-2. Receiver Propagation Delay and Transition Time Waveforms

8 Detailed Description

8.1 Overview

图 9-1 shows how LVDS drivers and receivers are intended to be primarily used in a simple point-to-point configuration. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the source through a impedance controlled 100 Ω differential PCB traces. A termination resistor of 100 Ω should be used, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver.

8.2 Functional Block Diagram



8.3 Feature Description

The DS90LVRA2 differential line receiver is capable of detecting signals as low as 100 mV, over a common-mode range of −1 V to 2 V (V_{CC} at 1.8 V). This is related to the driver offset voltage which is typically +1.2 V. The driven signal is centered around this voltage and may shift around this center point. The shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of +0 V to +3 V (measured from each pin to ground).

8.4 Device Functional Modes

表 8-1. Truth Table

INPUTS	OUTPUT
$[R_{IN}+] - [R_{IN}-]$	R_{OUT}
$V_{ID} \geq 0.1$ V	H
$V_{ID} \leq -0.1$ V	L
-0.1 V $\leq V_{ID} \leq 0.1$ V	?(1)

(1) ? indicates state is indeterminate

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

For general application guidelines and hints about LVDS drivers and receivers, refer to the *LVDS application notes and design guides*.

9.2 Typical Application

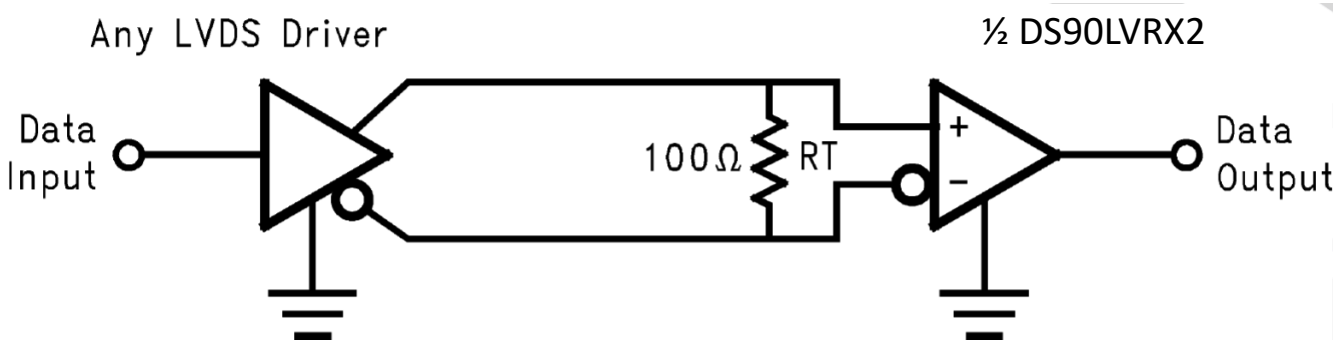


图 9-1. Balanced System Point-to-Point Application

9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces. All components of the transmission media must have a matched differential impedance of 100 Ω. They must not introduce major impedance discontinuities.

9.2.2 Detailed Design Procedure

9.2.2.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1 µF and 0.01 µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10 µF (35 V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

9.2.2.2 Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90 Ω and 110 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10 mm (12 mm maximum).

9.2.2.3 Input Failsafe Biasing

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5 kΩ to 15 kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2 V to be compatible with the internal circuitry. For more information, refer to application note AN-1194 *Failsafe Biasing of LVDS Interfaces*.

9.2.2.4 Probing LVDS Transmission Lines

Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

9.3 Application Curves

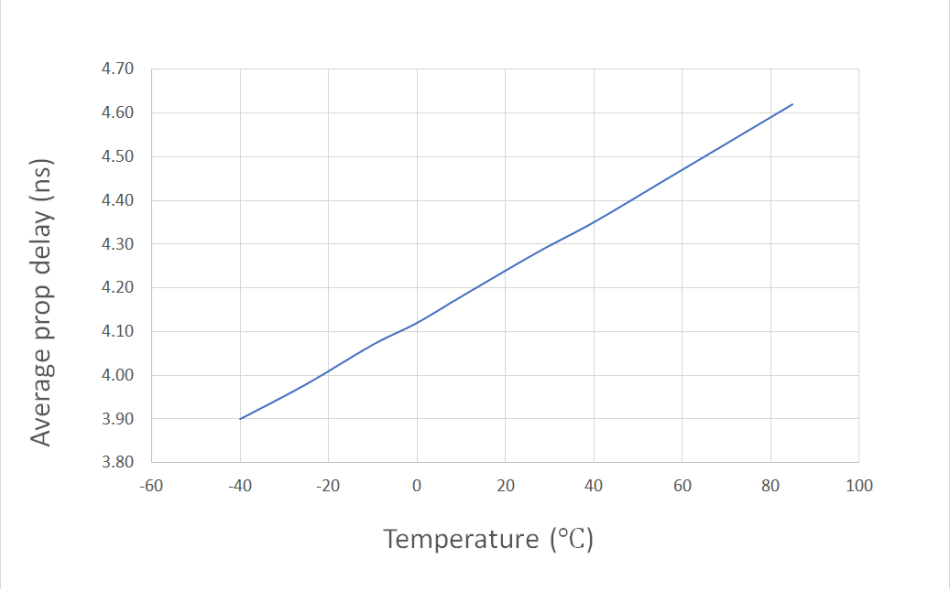


图 9-2. Typical Propagation Delay -vs- Temperature (VCC 1.8 V, 10 pF Output Load, Average of 2 Channels)

10 Power Supply Recommendations

Bypass capacitors must be used on power pins. TI recommends using high-frequency, ceramic, 0.1-µF and 0.01-µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-µF bulk capacitor, 35-V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.

11 Layout

11.1 Layout Guidelines

11.1.1 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission trace and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10 mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. It is important to note: skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note that the velocity of propagation, v = c/E $_r$ where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

11.1.2 PC Board Considerations

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, and TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by one or more power or ground planes.

11.2 Layout Examples

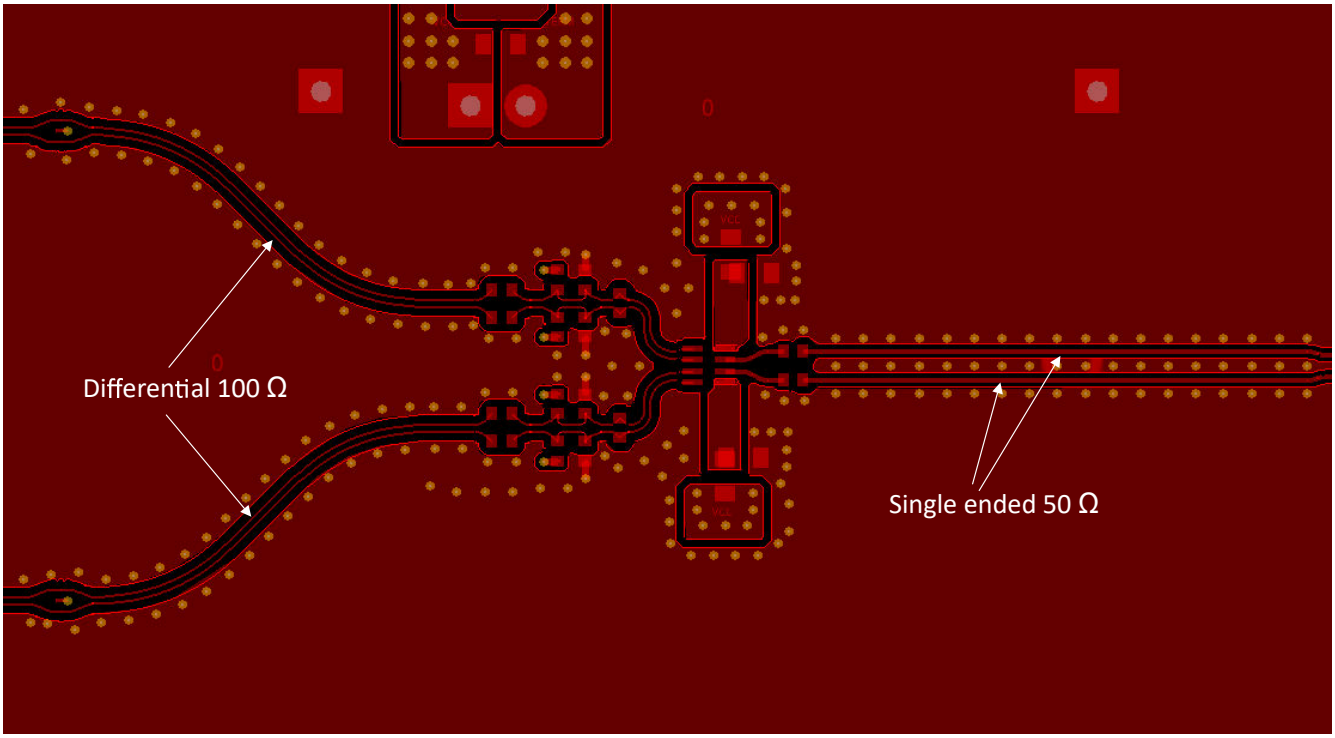


图 11-1. EVM Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Failsafe Biasing of LVDS Interfaces* application note

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
D9LVRA2DEMR	Active	Production	WSON (DEM) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LR2
D9LVRA2DEMR.A	Active	Production	WSON (DEM) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LR2
D9LVRA2DEMT	Active	Production	WSON (DEM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LR2
D9LVRA2DEMT.A	Active	Production	WSON (DEM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LR2
D9LVRA2IDEMR	Active	Production	WSON (DEM) | 8	3000 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LR2
D9LVRA2IDEMR.A	Active	Production	WSON (DEM) | 8	3000 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LR2
D9LVRA2IDEMT	Active	Production	WSON (DEM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LR2
D9LVRA2IDEMT.A	Active	Production	WSON (DEM) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LR2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DS90LVRA2 :

- Automotive : DS90LVRA2-Q1

NOTE: Qualified Version Definitions:

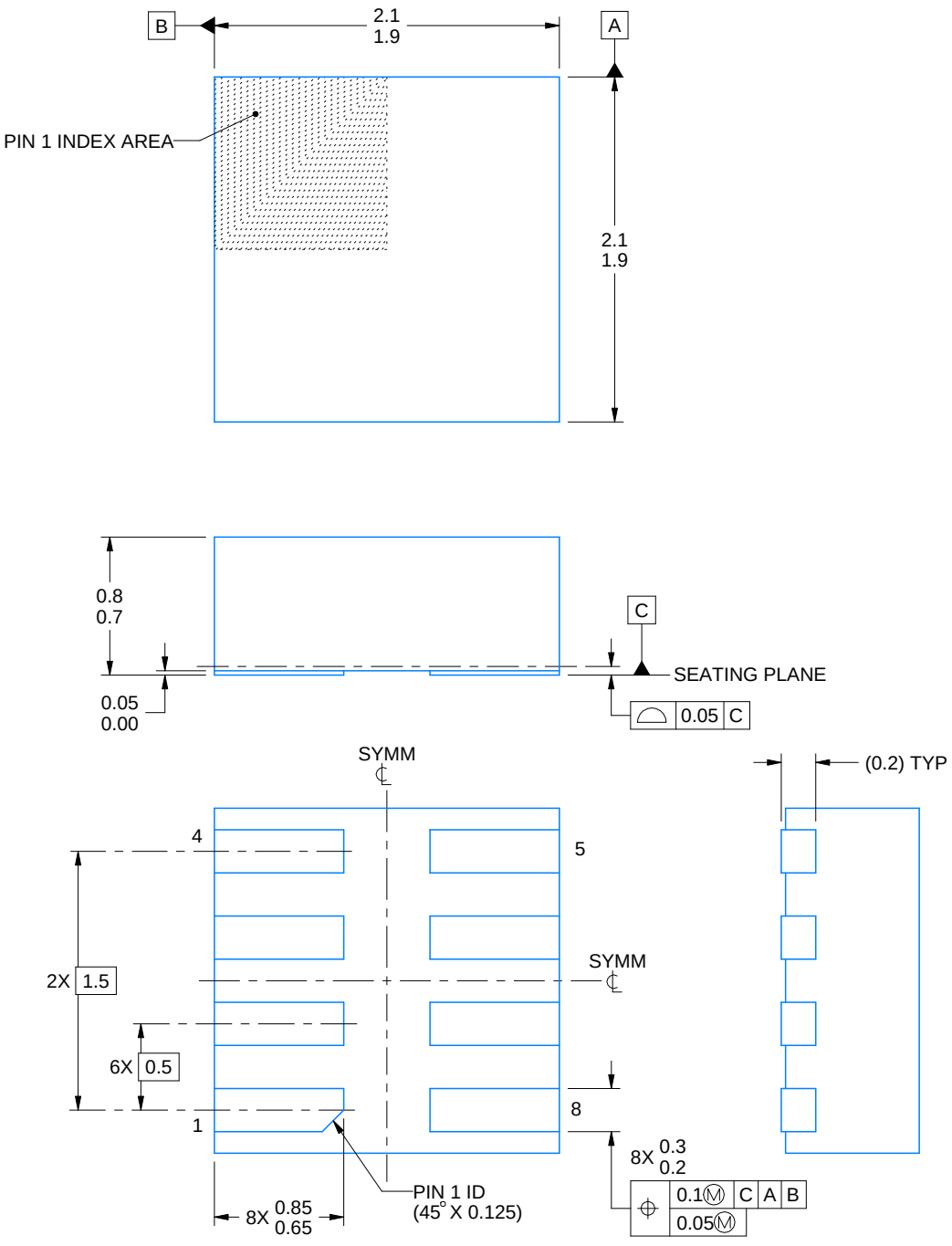
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

DEM0008A

PACKAGE OUTLINE

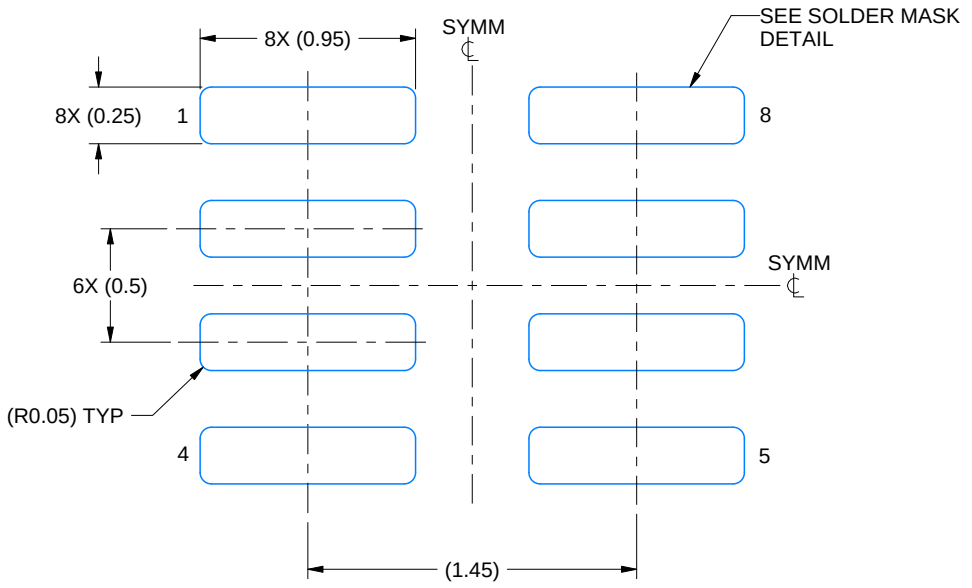
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

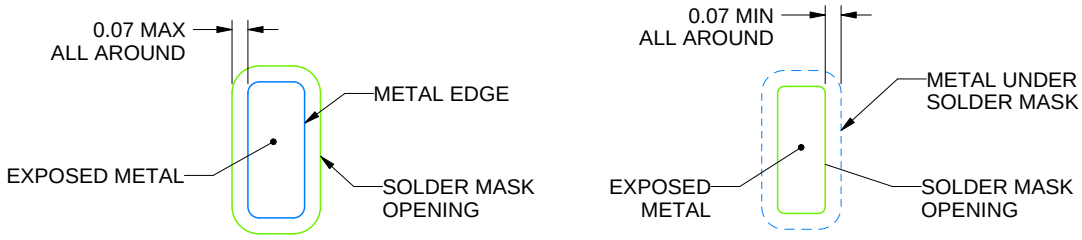


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4228323/A 12/2021

NOTES: (continued)

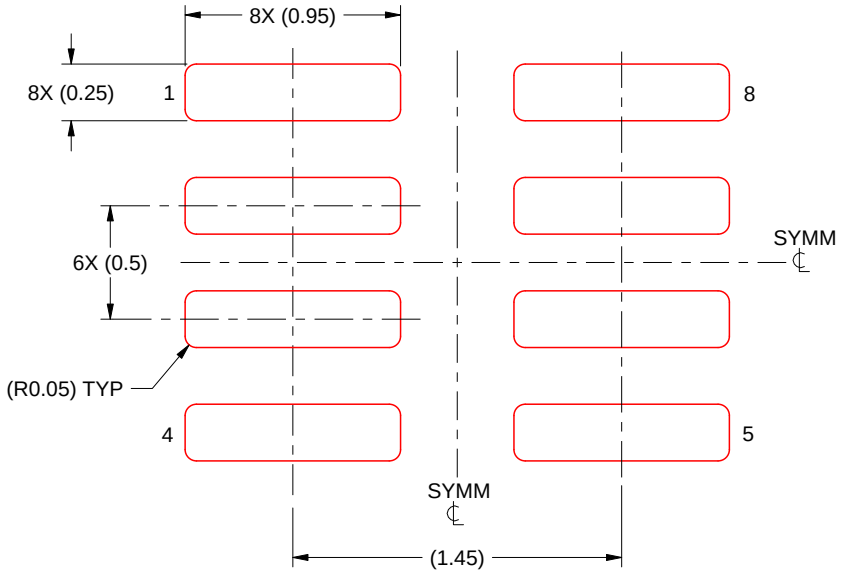
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DEM0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4228323/A 12/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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