

# DS125BR800 具有输入 CTLE 和输出加重功能的低功耗 12.5Gbps 8 通道中继器

## 1 特性

- 广泛的产品系列，经实践检验的系统互操作性
  - DS125BR111: 单通道中继器
  - DS125BR401: 四通道中继器
  - DS125BR800: 八通道中继器
  - DS125MB203: 双端口 2:1/1:2 多路复用/开关
  - DS125DF410: 具有 CDR 功能的四通道重定时器
- 低功耗: 每通道 65mW (典型值), 可选择关闭不使用的通道
- 支持 PCIe“非限制性”输出和 10G-KR 链路协商
- 高级信号调节功能
  - 频率为 6.25GHz 时, 最高可支持 30dB 的接收均衡功能
  - 发送去加重功能高达 -12dB
  - 发送输出电压控制: 700mV 至 1300mV
- 可通过引脚选择、EEPROM 或 SMBus 接口进行编程
- 单电源电压: 2.5V 或 3.3V (可选)
- 工作温度范围为 -40°C 至 85°C
- 3kV 人体放电模型 (HBM) 静电放电 (ESD) 额定电压
- 直通引脚分配: 54 引脚超薄型四方扁平无引线 (WQFN) 封装 (10mm × 5.5mm, 0.5mm 间距)
- 支持的协议
  - sRIO, Infiniband, Interlaken, 通用公共无线接口 (CPRI), 开放基站架构协议 (OBSAI)
  - 其它私有接口高达 12.5Gbps

## 2 应用

- SAS/SATA (高达 6Gbps), 光纤通道 (高达 10GFC)
- PCIe 1 代/2 代/3 代、10G-KR、10GbE、XAUI、RXAUI

## 3 说明

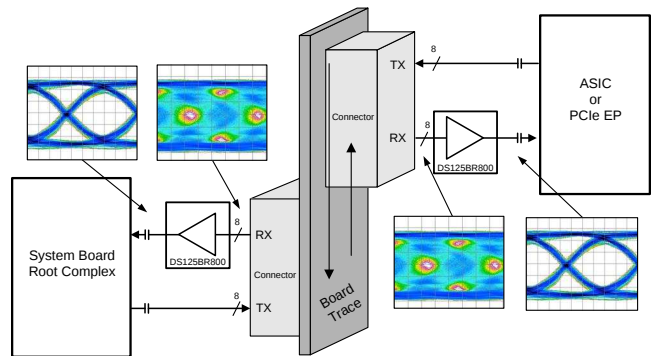
DS125BR800 器件是一款超低功耗、高性能的多协议中继器/转接驱动器, 设计用于支持速率高达 12.5Gbps 的八通道 PCIe 3 代/2 代/1 代、10G-KR 以及其他高速接口串行协议。接收器的连续时间线性均衡器 (CTLE) 可在 6.25GHz (12.5Gbps) 时为八个通道分别提供高达 +30dB 的增强功能, 能够打开一个因码间干扰 (ISI) (由 30in 以上电路板迹线或 8m 以上铜缆等互连介质引起) 而完全关闭的输入眼型状态, 从而通过主机控制器确保实现无错误端到端链接。发送器提供高达 -12dB 的去加重增强以及 700mV 至 1300mV 的输出电压幅度控制, 以便在互连通道内的实体布局方面实现最大限度的灵活性。

器件信息<sup>(1)</sup>

| 器件型号       | 封装        | 封装尺寸 (标称值)       |
|------------|-----------|------------------|
| DS125BR800 | WQFN (54) | 10.00mm × 5.50mm |

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

典型应用



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## 4 修订历史记录

| Changes from Revision E (January 2015) to Revision F                                                                                                             | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed $1/3 \times V_{DD}$ and $2/3 \times V_{DD}$ to $1/3 \times V_{IN}$ and $2/3 \times V_{IN}$ in the 3.3-V MODE column of the 4-Level Input Voltage table | 12   |
| • Changed $V_{IN} - 0.04 \text{ V}$ to $V_{DD} - 0.04 \text{ V}$ in the 2.5-V MODE column of the 4-Level Input Voltage table                                     | 12   |
| • 添加了接收文档更新通知 部分                                                                                                                                                 | 51   |

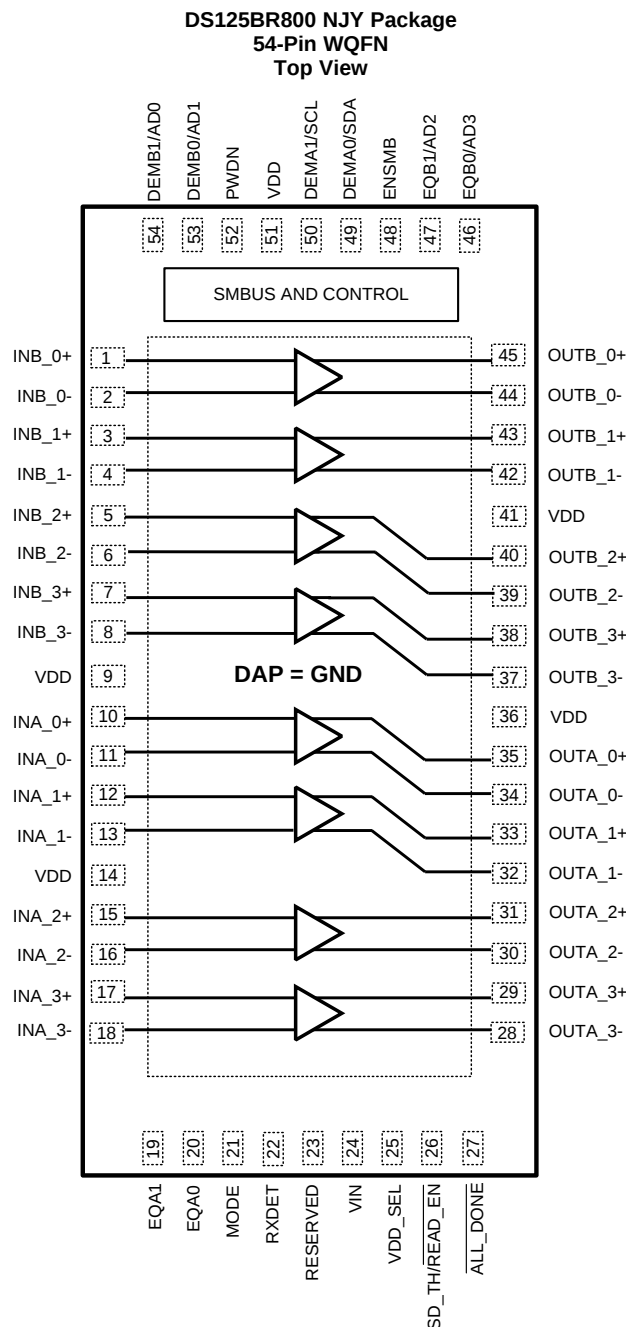
| Changes from Revision D (March 2013) to Revision E                                          | Page |
|---------------------------------------------------------------------------------------------|------|
| • 已添加引脚配置和功能 部分、ESD 额定值 表、特性 说明 部分、器件功能模式、应用和实施 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 | 1    |

## 5 说明（续）

在 10G-KR 和 PCIe 3 代模式下运行时，DS125BR800 允许主控制器和端点优化完整链路并协商发射均衡器系数。这种链路协商协议的无缝管理可确保系统级互操作性和最小延迟。DS125BR800 拥有每通道 65mW（典型值）的低功耗，可选择关闭不使用的通道，能够实现高效节能的系统设计。需要一个 3.3V 或 2.5V 单电源来为此器件供电。

可通过引脚、软件（SMBus 或 I2C）轻松应用这些可编程设置，或者通过外部 EEPROM 加载这些设置。当运行在 EEPROM 模式下时，配置信息在加电时自动载入，这样就免除了对于外部微控制器或软件驱动程序的需要。

## 6 Pin Configuration and Functions



**Pin Functions<sup>(1)</sup>**

| PIN                                                                              |                                   | TYPE                                    | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------------------------------------------------------|-----------------------------------|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                                             | NO.                               |                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| DIFFERENTIAL HIGH SPEED I/O'S                                                    |                                   |                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| INA_0+, INA_0-, INA_1+,<br>INA_1-, INA_2+, INA_2-<br>,INA_3+, INA_3-             | 10, 11, 12, 13,<br>15, 16, 17, 18 | I                                       | Inverting and noninverting CML differential inputs to the equalizer. On-chip, 50-Ω termination resistor connects INA_n+ to VDD and INA_n- to VDD when enabled.<br>AC coupling required on high-speed I/O                                                                                                                                                                                                                                                                                                           |
| INB_0+, INB_0-, INB_1+,<br>INB_1-, INB_2+, INB_2-<br>,INB_3+, INB_3-,            | 1, 2, 3, 4,<br>5, 6, 7, 8,        | I                                       | Inverting and noninverting CML differential inputs to the equalizer. On-chip, 50-Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD when enabled.<br>AC coupling required on high-speed I/O                                                                                                                                                                                                                                                                                                           |
| OUTA_0+, OUTA_0-,<br>OUTA_1+, OUTA_1-,<br>OUTA_2+, OUTA_2-,<br>OUTA_3+, OUTA_3-  | 35, 34, 33, 32,<br>31, 30, 29, 28 | O                                       | Inverting and noninverting 50-Ω driver outputs with de-emphasis. Compatible with AC-coupled CML inputs.<br>AC coupling required on high-speed I/O                                                                                                                                                                                                                                                                                                                                                                  |
| OUTB_0+, OUTB_0-,<br>OUTB_1+, OUTB_1-,<br>OUTB_2+, OUTB_2-,<br>OUTB_3+, OUTB_3-, | 45, 44, 43, 42,<br>40, 39, 38, 37 | O                                       | Inverting and noninverting 50-Ω driver outputs with de-emphasis. Compatible with AC-coupled CML inputs.<br>AC coupling required on high-speed I/O                                                                                                                                                                                                                                                                                                                                                                  |
| CONTROL PINS — SHARED (LVCMOS)                                                   |                                   |                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| ENSMB                                                                            | 48                                | I, 4-LEVEL,<br>LVCMOS                   | System Management Bus (SMBus) Enable pin<br>Tie 1 kΩ to VDD = Register Access SMBus Slave Mode<br>FLOAT = Read External EEPROM (Master SMBUS Mode)<br>Tie 1 kΩ to GND = Pin Mode                                                                                                                                                                                                                                                                                                                                   |
| ENSMB = 1 (SMBUS MODE)                                                           |                                   |                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| AD0-AD3                                                                          | 54, 53, 47, 46                    | I, 4-LEVEL,<br>LVCMOS                   | ENSMB Master or Slave mode<br>SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs.<br>There are 16 addresses supported by these pins. Pins must be tied LOW or HIGH when used to define the device SMBus address.                                                                                                                                                                                                                                                    |
| READ_EN                                                                          | 26                                | I, 2-LEVEL,<br>LVCMOS                   | When using an External EEPROM, a transition from high to low starts the load from the external EEPROM                                                                                                                                                                                                                                                                                                                                                                                                              |
| SCL                                                                              | 50                                | I, 2-LEVEL,<br>LVCMOS,<br>O, OPEN Drain | Clock output when loading EEPROM configuration, reverting to SMBus clock input when EEPROM load is complete (ALL_DONE = 0). External 2-kΩ to 5-kΩ pullup resistor to VDD (2.5-V Mode) or VIN (3.3-V Mode) recommended as per SMBus interface standards.                                                                                                                                                                                                                                                            |
| SDA                                                                              | 49                                | I, 2-LEVEL,<br>LVCMOS,<br>O, OPEN Drain | In both SMBus Modes, this pin is the SMBus data I/O. Data input or open-drain output. External 2-kΩ to 5-kΩ pullup resistor to VDD (2.5-V Mode) or VIN (3.3-V Mode) recommended as per SMBus interface standards.                                                                                                                                                                                                                                                                                                  |
| ENSMB = 0 (PIN MODE)                                                             |                                   |                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| DEMA0, DEMA1,<br>DEMB0, DEMB1                                                    | 49, 50,<br>53, 54                 | I, 4-LEVEL,<br>LVCMOS                   | DEMA[1:0] and DEMB[1:0] control the level of de-emphasis of the output driver. The pins are only active when ENSMB is de-asserted (low). The 8 channels are organized into two banks. Bank A is controlled with the DEMA[1:0] pins and bank B is controlled with the DEMB[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The DEMA[1:0] pins are converted to SMBUS SCL/SDA and DEMB[1:0] pins are converted to AD0, AD1 inputs.<br>See <a href="#">Table 3</a> . |
| EQA0, EQA1,<br>EQB0, EQB1                                                        | 20, 19,<br>46, 47                 | I, 4-LEVEL,<br>LVCMOS                   | EQA[1:0] and EQB[1:0] control the level of equalization on the input pins. The pins are active only when ENSMB is deasserted (low). The 8 channels are organized into two banks. Bank A is controlled with the EQA[1:0] pins and bank B is controlled with the EQB[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The EQB[1:0] pins are converted to SMBUS AD2/AD3 inputs. See <a href="#">Table 2</a> .                                                         |

- (1) LVCMOS inputs without the FLOAT conditions must be driven to a logic low or high at all times or operation is not ensured.  
 Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.  
 For 3.3-V Mode operation, VIN pin = 3.3 V and the VDD for the 4-level input is 3.3 V.  
 For 2.5-V Mode operation, VDD pin = 2.5 V and the VDD for the 4-level input is 2.5 V.

### Pin Functions<sup>(1)</sup> (continued)

| PIN                                                     |                   | TYPE               | DESCRIPTION                                                                                                                                                                                                                                                                                                             |
|---------------------------------------------------------|-------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                    | NO.               |                    |                                                                                                                                                                                                                                                                                                                         |
| MODE                                                    | 21                | I, 4-LEVEL, LVCMOS | MODE control pin selects operating modes.<br>Tie 1 k $\Omega$ to GND = PCIe Gen-1 or PCIe Gen-2 and SAS/SATA (up to 6 Gbps)<br>FLOAT = AUTO Rate Select (for PCIe)<br>Tie 20 k $\Omega$ to GND = PCIe Gen-3 without De-emphasis<br>Tie 1 k $\Omega$ to VDD = PCIe Gen-3 with De-emphasis<br>See <a href="#">Table 6</a> |
| SD_TH                                                   | 26                | I, 4-LEVEL, LVCMOS | Controls the internal Signal Detect Threshold.<br>For data rates above 8 Gbps the Signal Detect function should be disabled to avoid potential for intermittent data loss. See <a href="#">Table 5</a> for additional information.                                                                                      |
| <b>CONTROL PINS — BOTH PIN AND SMBus MODES (LVCMOS)</b> |                   |                    |                                                                                                                                                                                                                                                                                                                         |
| PWDN                                                    | 52                | I, LVCMOS          | Tie High = Low power - power down<br>Tie GND = Normal Operation<br>See <a href="#">Table 4</a> .                                                                                                                                                                                                                        |
| RESERVED                                                | 23                | I, FLOAT           | Float (leave pin open) = Normal Operation                                                                                                                                                                                                                                                                               |
| RXDET                                                   | 22                | I, 4-LEVEL, LVCMOS | The RXDET pin controls the receiver detect function. Depending on the input level, a 50 $\Omega$ or >50-k $\Omega$ termination to the power rail is enabled.<br>See <a href="#">Table 4</a> .                                                                                                                           |
| VDD_SEL                                                 | 25                | I, LVCMOS          | Controls the internal regulator<br>FLOAT = 2.5-V mode<br>Tie GND = 3.3-V mode                                                                                                                                                                                                                                           |
| <b>OUTPUTS</b>                                          |                   |                    |                                                                                                                                                                                                                                                                                                                         |
| ALL_DONE                                                | 27                | O, LVCMOS          | Valid Register Load Status Output<br>HIGH = External EEPROM load failed<br>LOW = External EEPROM load passed                                                                                                                                                                                                            |
| <b>POWER</b>                                            |                   |                    |                                                                                                                                                                                                                                                                                                                         |
| GND                                                     | DAP               | Power              | Ground pad (DAP - die attach pad)                                                                                                                                                                                                                                                                                       |
| VDD                                                     | 9, 14, 36, 41, 51 | Power              | Power supply pins CML/analog<br>2.5-V Mode, connect to 2.5-V supply<br>3.3-V mode, connect 0.1- $\mu$ F cap to each VDD pin<br>See <a href="#">Power Supply Recommendations</a> for proper power supply decoupling.                                                                                                     |
| VIN                                                     | 24                | Power              | In 3.3-V mode, feed 3.3 V to VIN<br>In 2.5-V mode, leave floating                                                                                                                                                                                                                                                       |

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

|                                       | MIN  | MAX       | UNIT |
|---------------------------------------|------|-----------|------|
| Supply voltage (VDD - 2.5-V mode)     | −0.5 | 2.75      | V    |
| Supply voltage (VIN - 3.3-V mode)     | −0.5 | 4         | V    |
| LVC MOS Input/Output Voltage          | −0.5 | 4         | V    |
| CML input voltage                     | −0.5 | VDD + 0.5 | V    |
| CML input current                     | −30  | 30        | mA   |
| Junction temperature                  |      | 125       | °C   |
| Lead temperature soldering (4 sec.)   |      | 260       | °C   |
| Storage temperature, T <sub>stg</sub> | −40  | 125       | °C   |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the [Recommended Operating Conditions](#) is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are specified for a junction temperature range of −40°C to +125°C. Models are validated to Maximum Operating Voltages only.
- (2) For soldering specifications: see product folder at [Absolute Maximum Ratings for Soldering](#) (SNOA549).
- (3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

### 7.2 ESD Ratings

|                    |                         | VALUE                                                                                    | UNIT  |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±3000 |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1000 |
|                    |                         | Machine model, STD - JESD22-A115-A                                                       | ±200  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

|                                          | MIN   | TYP | MAX   | UNIT  |
|------------------------------------------|-------|-----|-------|-------|
| Supply voltage (2.5-V mode)              | 2.375 | 2.5 | 2.625 | V     |
| Supply voltage (3.3-V mode)              | 3     | 3.3 | 3.6   | V     |
| Ambient temperature                      | −40   | 25  | 85    | °C    |
| SMBus (SDA, SCL)                         |       |     | 3.6   | V     |
| Supply noise up to 50 MHz <sup>(1)</sup> |       |     | 100   | mVp-p |

- (1) Allowed supply noise (mVp-p sine wave) under typical conditions.

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | DS125BR800 | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | NJY (WQFN) |      |
|                               |                                              | 54 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 26.6       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 10.8       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 4.4        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.2        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 4.3        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 1.5        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

## 7.5 Electrical Characteristics<sup>(1)(2)(3)</sup>

| PARAMETER                          |                                                                | TEST CONDITIONS                                                                                                                                    | MIN  | TYP | MAX | UNIT  |
|------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|-----|-------|
| POWER                              |                                                                |                                                                                                                                                    |      |     |     |       |
| PD                                 | Power Dissipation                                              | VDD = 2.5-V supply,<br>EQ Enabled,<br>VOD = 1.0 Vp-p,<br>RXDET = 1, PWDN = 0                                                                       | 500  | 700 |     | mW    |
|                                    |                                                                | VIN = 3.3-V supply,<br>EQ Enabled,<br>VOD = 1.0 Vp-p,<br>RXDET = 1, PWDN = 0                                                                       | 660  | 900 |     | mW    |
| LVCMOS / LVTTTL DC SPECIFICATIONS  |                                                                |                                                                                                                                                    |      |     |     |       |
| V <sub>IH25</sub>                  | High Level Input Voltage                                       | 2.5 V-Mode                                                                                                                                         | 2    | VDD |     | V     |
| V <sub>IH33</sub>                  | High Level Input Voltage                                       | 3.3 V-Mode                                                                                                                                         | 2    | VIN |     | V     |
| V <sub>IL</sub>                    | Low Level Input Voltage                                        |                                                                                                                                                    | 0    | 0.8 |     | V     |
| V <sub>OH</sub>                    | High Level Output Voltage<br>(ALL_DONE pin)                    | I <sub>oh</sub> = −4 mA                                                                                                                            | 2    |     |     | V     |
| V <sub>OL</sub>                    | Low Level Output Voltage<br>(ALL_DONE pin)                     | I <sub>ol</sub> = 4 mA                                                                                                                             |      | 0.4 |     | V     |
| I <sub>IH</sub>                    | Input High Current (PWDN pin)                                  | VIN = 3.6 V, LVCMOS = 3.6 V                                                                                                                        | −15  | 15  |     | μA    |
|                                    | Input High Current with internal resistors (4-level input pin) |                                                                                                                                                    | 20   | 150 |     | μA    |
| I <sub>IL</sub>                    | Input Low Current (PWDN pin)                                   | VIN = 3.6 V, LVCMOS = 0 V                                                                                                                          | −15  | 15  |     | μA    |
|                                    | Input Low Current with internal resistors (4-level input pin)  |                                                                                                                                                    | −160 | −40 |     | μA    |
| CML RECEIVER INPUTS (IN_n+, IN_n-) |                                                                |                                                                                                                                                    |      |     |     |       |
| RL <sub>RX-DIFF</sub>              | RX Differential return loss                                    | 0.05 - 7.5 GHz                                                                                                                                     | −15  |     |     | dB    |
|                                    |                                                                | 7.5 - 15 GHz                                                                                                                                       | −5   |     |     | dB    |
| RL <sub>RX-CM</sub>                | RX Common mode return loss                                     | 0.05 - 5 GHz                                                                                                                                       | −10  |     |     | dB    |
| Z <sub>RX-DC</sub>                 | RX DC common mode impedance                                    | Tested at VDD = 2.5 V                                                                                                                              | 40   | 50  | 60  | Ω     |
| Z <sub>RX-DIFF-DC</sub>            | RX DC differential mode impedance                              | Tested at VDD = 2.5 V                                                                                                                              | 80   | 100 | 120 | Ω     |
| V <sub>RX-DIFF-DC</sub>            | Differential RX peak to peak voltage (VID)                     | Tested at pins                                                                                                                                     |      | 1.2 |     | V     |
| V <sub>RX-SIGNAL-DET-DIFF-PP</sub> | Signal detect assert level for active data signal              | SD_TH = float,<br>0101 pattern at 8 Gbps                                                                                                           |      | 180 |     | mVp-p |
| V <sub>RX-IDLE-DET-DIFF-PP</sub>   | Signal detect de-assert level for electrical idle              | SD_TH = float,<br>0101 pattern at 8 Gbps                                                                                                           |      | 110 |     | mVp-p |
| HIGH SPEED OUTPUTS                 |                                                                |                                                                                                                                                    |      |     |     |       |
| V <sub>TX-DIFF-PP</sub>            | Output Voltage Differential Swing                              | Differential measurement with OUT_n+ and OUT_n-,<br>terminated by 50 Ω to GND,<br>AC-Coupled, VID = 1.0 Vp-p,<br>DEM0 = 1, DEM1 = 0 <sup>(4)</sup> | 0.8  | 1   | 1.2 | Vp-p  |
| V <sub>TX-DE-RATIO_3.5</sub>       | TX de-emphasis ratio                                           | VOD = 1.0 Vp-p,<br>DEM0 = 0, DEM1 = R<br>PCIe Gen-1 or PCIe Gen-2 and SAS/SATA (up to 6 Gbps)                                                      | −3.5 |     |     | dB    |

- (1) Typical values represent most likely parametric norms at VDD = 2.5 V, TA = 25°C., and at the [Recommended Operating Conditions](#) at the time of product characterization and are not guaranteed.
- (2) The Electrical Characteristics tables list specified specifications under the listed [Recommended Operating Conditions](#) except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are **not** guaranteed.
- (3) Specified by device characterization.
- (4) In PCIe Gen-3 mode, the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEMA/B[1:0] in this MODE is dependent on the VID level and the frequency content. The DS125BR800 repeater is designed to be non-limiting in this MODE, so the TX-FIR (de-emphasis) is passed to the RX to support the handshake negotiation link training.

**Electrical Characteristics<sup>(1)(2)(3)</sup> (continued)**

| PARAMETER                                                                 |                                                                        | TEST CONDITIONS                                                                                                                            | MIN | TYP  | MAX | UNIT     |
|---------------------------------------------------------------------------|------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|----------|
| $V_{TX-DE-RATIO\_6}$                                                      | TX de-emphasis ratio                                                   | VOD = 1.0 Vp-p,<br>DEM0 = R, DEM1 = R<br>PCIe Gen-1 or PCIe Gen-2 and SAS/SATA (up to 6 Gbps)                                              |     | -6   |     | dB       |
| $T_{TX-DJ}$                                                               | Deterministic Jitter                                                   | VID = 800 mV, PRBS15 pattern, 8.0 Gbps, VOD = 1.0 V, EQ = 0x00, DE = 0 dB, (no input or output trace loss)                                 |     | 0.05 |     | Upp      |
| $T_{TX-RJ}$                                                               | Random Jitter                                                          | VID = 800 mV, 0101 pattern, 8.0 Gbps, VOD = 1.0 V, EQ = 0x00, DE = 0 dB, (no input or output trace loss)                                   |     | 0.3  |     | ps RMS   |
| $T_{TX-RISE-FALL}$                                                        | TX rise/fall time                                                      | 20% to 80% of differential output voltage                                                                                                  | 35  | 45   |     | ps       |
| $T_{RF-MISMATCH}$                                                         | TX rise/fall mismatch                                                  | 20% to 80% of differential output voltage                                                                                                  |     | 0.01 | 0.1 | UI       |
| $RL_{TX-DIFF}$                                                            | TX Differential return loss                                            | 0.05 - 7.5 GHz                                                                                                                             |     | -15  |     | dB       |
|                                                                           |                                                                        | 7.5 - 15 GHz                                                                                                                               |     | -5   |     | dB       |
| $RL_{TX-CM}$                                                              | TX Common mode return loss                                             | 0.05 - 5 GHz                                                                                                                               |     | -10  |     | dB       |
| $Z_{TX-DIFF-DC}$                                                          | DC differential TX impedance                                           |                                                                                                                                            |     | 100  |     | $\Omega$ |
| $V_{TX-CM-AC-PP}$                                                         | TX AC common mode voltage                                              | VOD = 1.0 Vp-p,<br>DEM0 = 1, DEM1 = 0                                                                                                      |     |      | 100 | mVp-p    |
| $I_{TX-SHORT}$                                                            | TX short circuit current limit                                         | Total current the transmitter can supply when shorted to VDD or GND                                                                        |     | 20   |     | mA       |
| $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$                                          | Absolute delta of DC common mode voltage during L0 and electrical idle |                                                                                                                                            |     |      | 100 | mV       |
| $V_{TX-CM-DC-LINE-DELTA}$                                                 | Absolute delta of DC common mode voltage between TX+ and TX-           |                                                                                                                                            |     |      | 25  | mV       |
| $T_{TX-IDLE-DATA}$                                                        | Max time to transition to differential DATA signal after IDLE          | VID = 1.0 Vp-p, 8 Gbps                                                                                                                     |     | 3.5  |     | ns       |
| $T_{TX-DATA-IDLE}$                                                        | Max time to transition to IDLE after differential DATA signal          | VID = 1.0 Vp-p, 8 Gbps                                                                                                                     |     | 6.2  |     | ns       |
| $T_{PLHD/PHLD}$                                                           | Differential Propagation Delay                                         | EQ = 00 <sup>(5)</sup>                                                                                                                     |     | 200  |     | ps       |
| $T_{LSK}$                                                                 | Lane to lane skew                                                      | T = 25°C, VDD = 2.5 V                                                                                                                      |     | 25   |     | ps       |
| $T_{PPSK}$                                                                | Part to part propagation delay skew                                    | T = 25°C, VDD = 2.5 V                                                                                                                      |     | 40   |     | ps       |
| <b>EQUALIZATION</b>                                                       |                                                                        |                                                                                                                                            |     |      |     |          |
| DJE1                                                                      | Residual deterministic jitter at 12 Gbps                               | 30in 5mils FR4, VID = 0.6 Vp-p, PRBS15, EQ = 0x07, DEM = 0 dB                                                                              |     | 0.18 |     | Upp      |
| DJE2                                                                      | Residual deterministic jitter at 8 Gbps                                | 30in 5mils FR4, VID = 0.6 Vp-p, PRBS15, EQ = 0x07, DEM = 0 dB                                                                              |     | 0.11 |     | Upp      |
| DJE3                                                                      | Residual deterministic jitter at 5 Gbps                                | 30in 5mils FR4, VID = 0.6 Vp-p, PRBS15, EQ = 0x07, DEM = 0 dB                                                                              |     | 0.07 |     | Upp      |
| DJE4                                                                      | Residual deterministic jitter at 12 Gbps                               | 5m 30 awg cable, VID = 0.6 Vp-p, PRBS15, EQ = 0x07, DEM = 0 dB                                                                             |     | 0.25 |     | Upp      |
| DJE5                                                                      | Residual deterministic jitter at 5 Gbps                                | 8m 30 awg cable, VID = 0.6 Vp-p, PRBS15, EQ = 0x0F, DEM = 0 dB                                                                             |     | 0.33 |     | Upp      |
| <b>DE-EMPHASIS — PCIe Gen-1 or PCIe Gen-2 and SAS/SATA (up to 6 Gbps)</b> |                                                                        |                                                                                                                                            |     |      |     |          |
| DJD1                                                                      | Residual deterministic jitter at 12 Gbps                               | Input Channel: 20in 5mils FR4,<br>Output Channel: 10in 5mils FR4<br>VID = 0.6 Vp-p,<br>PRBS15, EQ = 0x03,<br>VOD = 1.0 Vp-p, DEM = -3.5 dB |     | 0.1  |     | Upp      |

(5) Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 00 will result in the longest propagation delays.

## 7.6 Electrical Characteristics: Serial Management Bus Interface

over recommended operating supply and temperature ranges unless other specified.

| PARAMETER                                     |                                                                                     | TEST CONDITIONS                                       | MIN   | TYP  | MAX | UNIT |
|-----------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------|-------|------|-----|------|
| <b>SERIAL BUS INTERFACE DC SPECIFICATIONS</b> |                                                                                     |                                                       |       |      |     |      |
| V <sub>IL</sub>                               | Data, Clock Input Low Voltage                                                       |                                                       |       |      | 0.8 | V    |
| V <sub>IH</sub>                               | Data, Clock Input High Voltage                                                      |                                                       | 2.1   |      | 3.6 | V    |
| I <sub>PULLUP</sub>                           | Current Through Pull-Up Resistor or Current Source                                  | High Power Specification                              | 4     |      |     | mA   |
| V <sub>DD</sub>                               | Nominal Bus Voltage                                                                 |                                                       | 2.375 |      | 3.6 | V    |
| I <sub>LEAK-BUS</sub>                         | Input Leakage Per Bus Segment                                                       | (1)                                                   | –200  |      | 200 | μA   |
| I <sub>LEAK-Pin</sub>                         | Input Leakage Per Device Pin                                                        |                                                       |       | –15  |     | μA   |
| C <sub>I</sub>                                | Capacitance for SDA and SCL                                                         | (1) (2)                                               |       |      | 10  | pF   |
| R <sub>TERM</sub>                             | External Termination Resistance pull to V <sub>DD</sub> = 2.5 V ± 5% or 3.3 V ± 10% | Pullup V <sub>DD</sub> = 3.3 V <sup>(1) (2) (3)</sup> |       | 2000 |     | Ω    |
|                                               |                                                                                     | Pullup V <sub>DD</sub> = 2.5 V <sup>(1) (2) (3)</sup> |       | 1000 |     | Ω    |

(1) Recommended value.

(2) Recommended maximum capacitance load per bus segment is 400 pF.

(3) Maximum termination voltage should be identical to the device supply voltage.

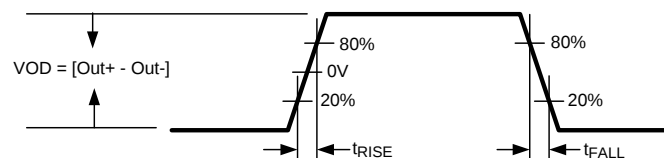
## 7.7 Timing Requirements

|                                                   |                                                                                              |                              | MIN                | TYP | MAX | UNIT |
|---------------------------------------------------|----------------------------------------------------------------------------------------------|------------------------------|--------------------|-----|-----|------|
| <b>SERIAL BUS INTERFACE TIMING SPECIFICATIONS</b> |                                                                                              |                              |                    |     |     |      |
| FSMB                                              | Bus Operating Frequency <sup>(1)</sup>                                                       | ENSMB = VDD (Slave Mode)     |                    |     | 400 | kHz  |
|                                                   |                                                                                              | ENSMB = FLOAT (Master Mode)  | 280                | 400 | 520 | kHz  |
| TBUF                                              | Bus Free Time Between Stop and Start Condition                                               |                              | 1.3                |     |     | μs   |
| THD:STA                                           | Hold time after (Repeated) Start Condition. After this period, the first clock is generated. | At I <sub>PULLUP</sub> , Max | 0.6                |     |     | μs   |
| TSU:STA                                           | Repeated Start Condition Setup Time                                                          |                              | 0.6                |     |     | μs   |
| TSU:STO                                           | Stop Condition Setup Time                                                                    |                              | 0.6                |     |     | μs   |
| THD:DAT                                           | Data Hold Time                                                                               |                              | 0                  |     |     | ns   |
| TSU:DAT                                           | Data Setup Time                                                                              |                              | 100                |     |     | ns   |
| T <sub>LOW</sub>                                  | Clock Low Period                                                                             |                              | 1.3                |     |     | μs   |
| T <sub>HIGH</sub>                                 | Clock High Period                                                                            |                              | <sup>(2)</sup> 0.6 |     | 50  | μs   |
| t <sub>F</sub>                                    | Clock/Data Fall Time                                                                         | (2)                          |                    |     | 300 | ns   |
| t <sub>R</sub>                                    | Clock/Data Rise Time                                                                         | (2)                          |                    |     | 300 | ns   |
| t <sub>POR</sub>                                  | Time in which a device must be operational after power-on reset                              | (2) (3)                      |                    |     | 500 | ms   |

(1) In Master Mode, a serial EEPROM with a minimum rating of 520 KHz is required.

(2) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1.1 SMBus common AC specifications for details.

(3) Specified by Design. Parameter not tested in production.

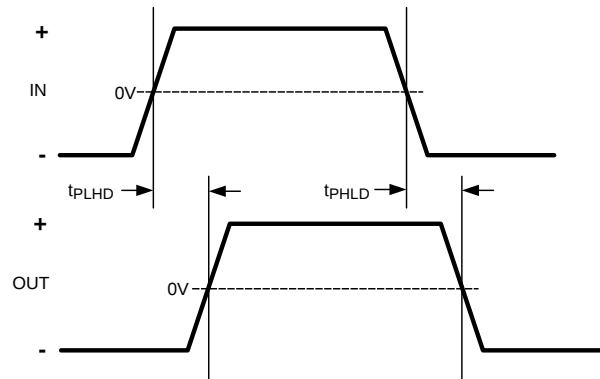


**Figure 1. CML Output and Rise and FALL Transition Time**

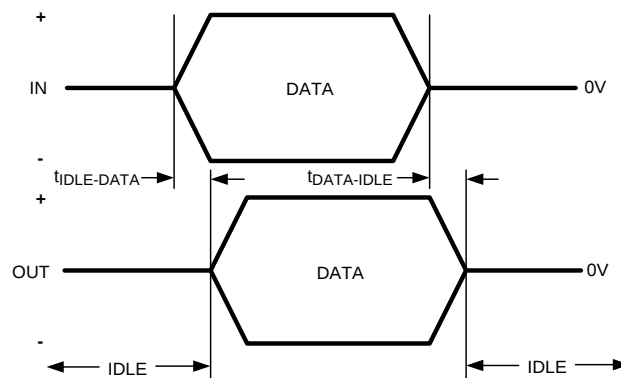
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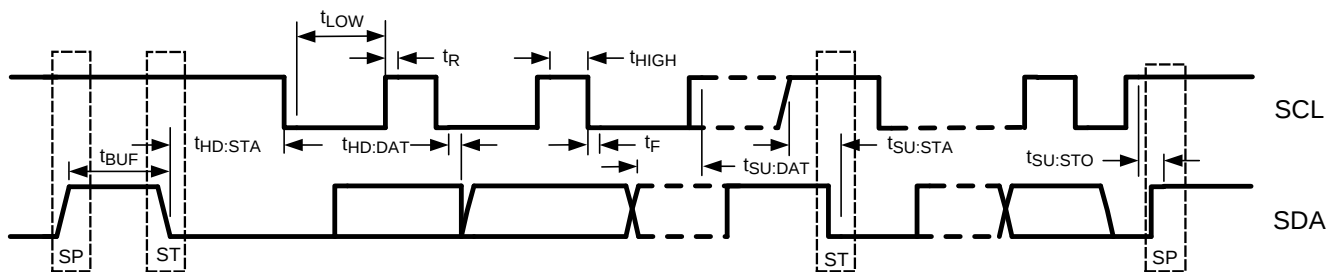
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**Figure 2. Propagation Delay Timing Diagram**

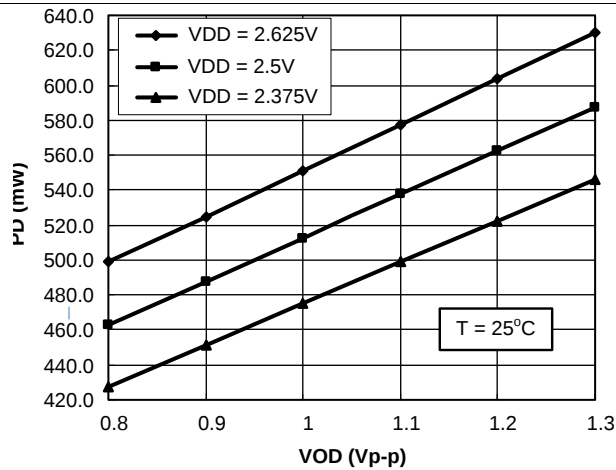


**Figure 3. Transmit IDLE-DATA and DATA-IDLE Response Time**

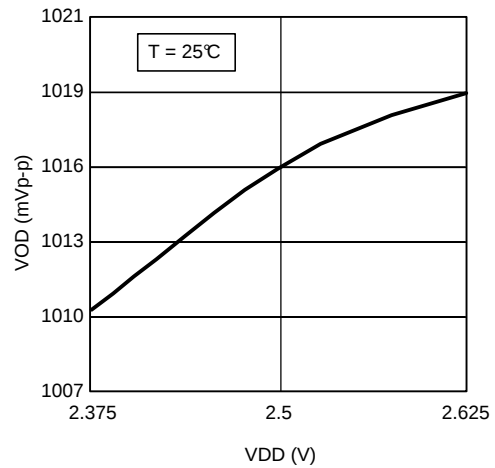


**Figure 4. SMBus Timing Parameters**

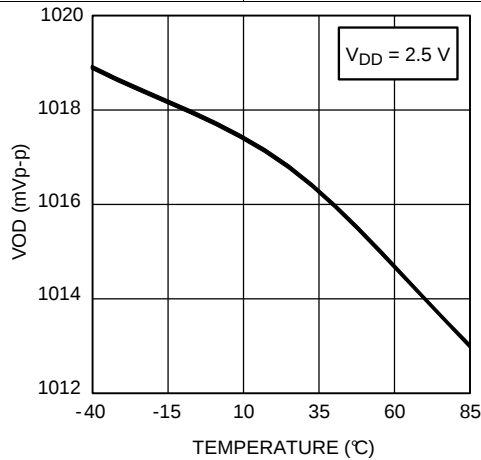
## 7.8 Typical Characteristics



**Figure 5. Power Dissipation (PD) vs Output Differential Voltage (VOD)**



**Figure 6. Output Differential Voltage (VOD = 1.0 Vp-p) vs Supply Voltage (VDD)**



**Figure 7. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Temperature**

## 8 Detailed Description

### 8.1 Overview

The DS125BR800 compensates for lossy printed-circuit board backplanes and balanced cables.

The DS125BR800 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register information from external EEPROM. Refer to [SMBUS Master Mode](#) for more information.

### 8.2 Functional Block Diagram

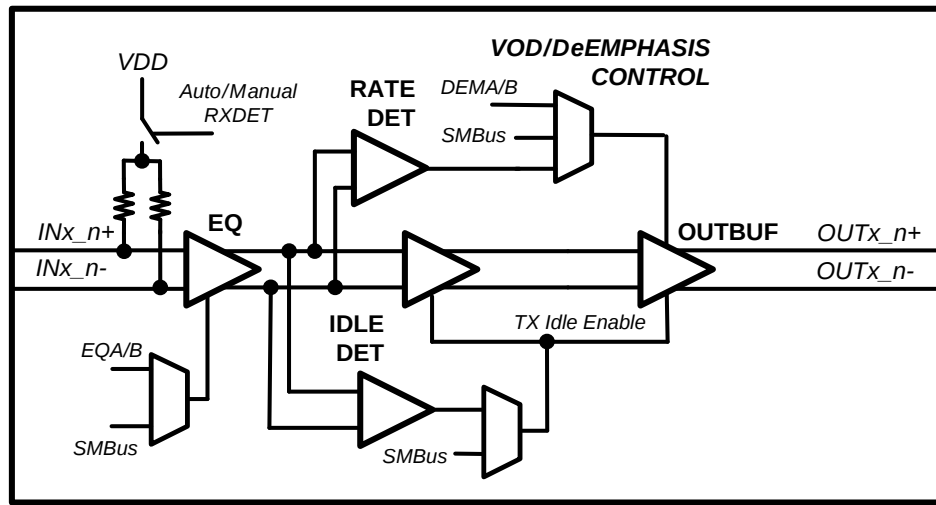


Figure 8. Block Diagram - Detail View of Channel (1 of 8)

### 8.3 Feature Description

#### 8.3.1 4-Level Input Configuration Guidelines

The 4-level input pins use a resistor divider to help set the 4 valid levels and provide a wider range of control settings when ENSMB=0. There is an internal 30-k $\Omega$  pullup and a 60-k $\Omega$  pulldown connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1-k $\Omega$  pullup, 1-k $\Omega$  pulldown, no connect, and 20-k $\Omega$  pulldown provide the optimal voltage levels for each of the four input states.

Table 1. 4-Level Input Voltage

| LEVEL | SETTING                      | 3.3-V MODE                | 2.5-V MODE                |
|-------|------------------------------|---------------------------|---------------------------|
| 0     | Tie 1 k $\Omega$ to GND      | 0.10 V                    | 0.08 V                    |
| R     | Tie 20 k $\Omega$ to GND     | $1/3 \times V_{IN}$       | $1/3 \times V_{DD}$       |
| Float | Float (leave pin open)       | $2/3 \times V_{IN}$       | $2/3 \times V_{DD}$       |
| 1     | Tie 1 k $\Omega$ to $V_{DD}$ | $V_{IN} - 0.05 \text{ V}$ | $V_{DD} - 0.04 \text{ V}$ |

- Level 1 - 2 =  $0.2 \times V_{IN}$  or  $V_{DD}$
- Level 2 - 3 =  $0.5 \times V_{IN}$  or  $V_{DD}$
- Level 3 - 4 =  $0.8 \times V_{IN}$  or  $V_{DD}$

To minimize the startup current associated with the integrated 2.5-V regulator the 1-k $\Omega$  pullup and pulldown resistors are recommended. If several 4-level inputs require the same setting, it is possible to combine two or more 1-k $\Omega$  resistors into a single lower value resistor. For example, combining two inputs with a single 500- $\Omega$  resistor is a good way to save board space.

### 8.3.2 PCIe Signal Integrity

When using the DS125BR800 in PCIe Gen-3 systems, there are specific signal integrity settings to ensure signal integrity margin. The settings were achieved with completing extensive testing. Contact your field representative for more information regarding the testing completed to achieve these settings.

For tuning the in the downstream direction (from CPU to EP).

- EQ: use the guidelines outlined in [Table 2](#).
- De-Emphasis: use the guidelines outlined in [Table 3](#).
- VOD: use the guidelines outlined in [Table 3](#).

For tuning in the upstream direction (from EP to CPU).

- EQ: use the guidelines outlined in [Table 2](#).
- De-Emphasis:
  - For trace lengths < 15" set to -3.5 dB
  - For trace lengths > 15" set to -6 dB
- VOD: set to 900 mV

**Table 2. Equalizer Settings**

| Level | EQA1<br>EQB1 | EQA0<br>EQB | EQ – 8 bits [7:0] | dB at<br>1.5 GHz | dB at<br>2.5 GHz | dB at<br>4 GHz | dB at<br>6 GHz | Suggested Use <sup>(1)</sup> |
|-------|--------------|-------------|-------------------|------------------|------------------|----------------|----------------|------------------------------|
| 1     | 0            | 0           | 0000 0000 = 0x00  | 2.5              | 3.5              | 3.8            | 3.1            | FR4 < 5 inch trace           |
| 2     | 0            | R           | 0000 0001 = 0x01  | 3.8              | 5.4              | 6.7            | 6.7            | FR4 5-10 inch trace          |
| 3     | 0            | Float       | 0000 0010 = 0x02  | 5.0              | 7.0              | 8.4            | 8.4            | FR4 10 inch trace            |
| 4     | 0            | 1           | 0000 0011 = 0x03  | 5.9              | 8.0              | 9.3            | 9.1            | FR4 15-20 inch trace         |
| 5     | R            | 0           | 0000 0111 = 0x07  | 7.4              | 10.3             | 12.8           | 13.7           | FR4 20-30 inch trace         |
| 6     | R            | R           | 0001 0101 = 0x15  | 6.9              | 10.2             | 13.9           | 16.2           | FR4 25-30 inch trace         |
| 7     | R            | Float       | 0000 1011 = 0x0B  | 9.0              | 12.4             | 15.3           | 15.9           | FR4 25-30 inch trace         |
| 8     | R            | 1           | 0000 1111 = 0x0F  | 10.2             | 13.8             | 16.7           | 17.0           | 8m, 30awg cable              |
| 9     | Float        | 0           | 0101 0101 = 0x55  | 8.5              | 12.6             | 17.5           | 20.7           | > 8m cable                   |
| 10    | Float        | R           | 0001 1111 = 0x1F  | 11.7             | 16.2             | 20.3           | 21.8           |                              |
| 11    | Float        | Float       | 0010 1111 = 0x2F  | 13.2             | 18.3             | 22.8           | 23.6           |                              |
| 12    | Float        | 1           | 0011 1111 = 0x3F  | 14.4             | 19.8             | 24.2           | 24.7           |                              |
| 13    | 1            | 0           | 1010 1010 = 0xAA  | 14.4             | 20.5             | 26.4           | 28.0           |                              |
| 14    | 1            | R           | 0111 1111 = 0x7F  | 16.0             | 22.2             | 27.8           | 29.2           |                              |
| 15    | 1            | Float       | 1011 1111 = 0xBF  | 17.6             | 24.4             | 30.2           | 30.9           |                              |
| 16    | 1            | 1           | 1111 1111 = 0xFF  | 18.7             | 25.8             | 31.6           | 31.9           |                              |

(1) Cable and FR4 lengths are for reference only. FR4 lengths based on a 100  $\Omega$  differential stripline with 5-mil traces and 8-mil trace separation. Optimal EQ setting should be determined via simulation and prototype verification.

**Table 3. Output Voltage and De-Emphasis Settings**

| Level | DEMA1<br>DEMB1 | DEMA0<br>DEMB0 | VOD Vp-p | DEM dB <sup>(1)</sup> | Inner Amplitude<br>Vp-p | Suggested Use <sup>(2)</sup> |
|-------|----------------|----------------|----------|-----------------------|-------------------------|------------------------------|
| 1     | 0              | 0              | 0.8      | 0                     | 0.8                     | FR4 < 5 inch 4-mil trace     |
| 2     | 0              | R              | 0.9      | 0                     | 0.9                     | FR4 < 5 inch 4-mil trace     |
| 3     | 0              | Float          | 0.9      | - 3.5                 | 0.6                     | FR4 10 inch 4-mil trace      |
| 4     | 0              | 1              | 1.0      | 0                     | 1.0                     | FR4 < 5 inch 4-mil trace     |
| 5     | R              | 0              | 1.0      | - 3.5                 | 0.7                     | FR4 10 inch 4-mil trace      |
| 6     | R              | R              | 1.0      | - 6                   | 0.5                     | FR4 15 inch 4-mil trace      |
| 7     | R              | Float          | 1.1      | 0                     | 1.1                     | FR4 < 5 inch 4-mil trace     |

(1) The VOD output amplitude and DEM de-emphasis levels are set with the DEMA/B[1:0] pins.

The de-emphasis levels are available in PCIe Gen-3 modes when MODE = 1 (tied to VIN)

(2) FR4 lengths are for reference only. FR4 lengths based on a 100  $\Omega$  differential stripline with 5-mil traces and 8-mil trace separation. Optimal DEM settings should be determined via simulation and prototype verification.

**Table 3. Output Voltage and De-Emphasis Settings (continued)**

| Level | DEMA1<br>DEMB1 | DEMA0<br>DEMB0 | VOD Vp-p | DEM dB <sup>(1)</sup> | Inner Amplitude<br>Vp-p | Suggested Use <sup>(2)</sup> |
|-------|----------------|----------------|----------|-----------------------|-------------------------|------------------------------|
| 8     | R              | 1              | 1.1      | - 3.5                 | 0.7                     | FR4 10 inch 4-mil trace      |
| 9     | Float          | 0              | 1.1      | - 6                   | 0.6                     | FR4 15 inch 4-mil trace      |
| 10    | Float          | R              | 1.2      | 0                     | 1.2                     | FR4 < 5 inch 4-mil trace     |
| 11    | Float          | Float          | 1.2      | - 3.5                 | 0.8                     | FR4 10 inch 4-mil trace      |
| 12    | Float          | 1              | 1.2      | - 6                   | 0.6                     | FR4 15 inch 4-mil trace      |
| 13    | 1              | 0              | 1.3      | 0                     | 1.3                     | FR4 < 5 inch 4-mil trace     |
| 14    | 1              | R              | 1.3      | - 3.5                 | 0.9                     | FR4 10 inch 4-mil trace      |
| 15    | 1              | Float          | 1.3      | - 6                   | 0.7                     | FR4 15 inch 4-mil trace      |
| 16    | 1              | 1              | 1.3      | - 9                   | 0.5                     | FR4 20 inch 4-mil trace      |

**Table 4. RX-Detect Settings**

| PWDN<br>(PIN 52) | RXDET<br>(PIN 22)   | SMBus REG<br>bit [3:2] | Input Termination                     | Recommended<br>Use | Comments                                                                                                                                                                                                               |
|------------------|---------------------|------------------------|---------------------------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                | 0                   | 00                     | Hi-Z                                  | X                  | Manual RX-Detect, input is high impedance mode                                                                                                                                                                         |
| 0                | Tie 20 kΩ<br>to GND | 01                     | Pre Detect: Hi-Z<br>Post Detect: 50 Ω | PCIe Only          | Auto RX-Detect, outputs test every 12 msec for 600 msec then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω.<br><br>Reset function by pulsing PWDN high for 5 μsec then low again |
| 0                | Float<br>(Default)  | 10                     | Pre Detect: Hi-Z<br>Post Detect: 50 Ω | PCIe Only          | Auto RX-Detect, outputs test every 12 msec until detection occurs; termination is Hi-Z until RX detection; once detected input termination is 50 Ω.                                                                    |
| 0                | 1                   | 11                     | 50 Ω                                  | All Others         | Manual RX-Detect, input is 50 Ω.                                                                                                                                                                                       |
| 1                | X                   |                        | High Impedance                        | X                  | Power down mode, input is Hi-Z, output drivers are disabled.<br><br>Used to reset RX-Detect State Machine when held high for 5 μsec.                                                                                   |

### 8.3.2.1 RX-Detect in SAS/SATA (up to 6 Gbps) Applications

Unlike PCIe systems, SAS/SATA (up to 6 Gbps) systems use a low speed Out-Of-Band or OOB communications sequence to detect and communicate between Controllers/Expanders and target drives. This communication eliminates the need to detect for endpoints like PCIe. For SAS/SATA systems, it is recommended to tie the RXDET pin high. This will ensure any OOB sequences sent from the Controller/Expander will reach the target drive without any additional latency due to the termination detection sequence defined by PCIe.

**Table 5. Signal Detect Threshold Level<sup>(1)</sup>**

| SD_TH<br>(PIN 26) | SMBus REG Bit<br>[3:2] and [1:0] | Assert Level (typ) | De-assert Level (typ) |
|-------------------|----------------------------------|--------------------|-----------------------|
| 0                 | 10                               | 210 mVp-p          | 150 mVp-p             |
| R                 | 01                               | 160 mVp-p          | 100 mVp-p             |
| F (default)       | 00                               | 180 mVp-p          | 110 mVp-p             |
| 1                 | 11                               | 190 mVp-p          | 130 mVp-p             |

(1) VDD = 2.5 V, 25°C and 0101 pattern at 8 Gbps

#### 8.3.2.1.1 Signal Detect Control for Datarates above 8 Gbps

Signal detect bandwidth limitations combined with high levels of signal attenuation can result in intermittent data loss above 8 Gbps. This data loss can be eliminated by disabling automatic detection and forcing the Signal Detect function to be always "on". This programming requires SMBus control over the DS125BR800 to be present. The Signal Detect function is controlled for each channel independently. The register programming sequence is shown below:

1. Write register 0x06 = 0x18 // Enable SMBus register programming

2. Write registers 0x0D[1] = 1'b, 0x14[1] = 1'b, 0x1B[1] = 1'b, 0x22[1] = 1'b /\* CH0 - CH3
3. Write registers 0x2A[1] = 1'b, 0x31[1] = 1'b, 0x38[1] = 1'b, 0x3F[1] = 1'b /\* CH4 - CH7

**Table 6. MODE Operation With Pin Control**

| MODE<br>(PIN 21) | Driver Characteristics | PCIe | SAS<br>SATA | 10G-KR | 10GbE | CPRI<br>OBSAI | SRIO<br>(R)XAU1 | Interlaken<br>Infiniband |
|------------------|------------------------|------|-------------|--------|-------|---------------|-----------------|--------------------------|
| 0                | Limiting               |      | X           |        | X     | X             | X               | X                        |
| R                | Transparent without DE |      |             |        |       |               |                 |                          |
| F (default)      | Automatic              | X    |             |        |       |               |                 |                          |
| 1                | Transparent with DE    |      |             | X      |       |               |                 |                          |

NOTE: Automatic operation allows input to sense the incoming data-rate and utilize a "Transparent" output driver for operation at or above 8 Gbps.

NOTE: SAS/SATA up to 6 Gbps.

### 8.3.2.2 MODE Operation with SMBus Registers

When in SMBus mode (Slave or Master), the MODE pin retains control of the output driver characteristics. In order to override this control function, Register 0x08[2] must be written with a "1". Writing this bit enables MODE control of each channel individually using the channel registers defined in [Table 10](#).

## 8.4 Device Functional Modes

### 8.4.1 Pin Control Mode

When in pin mode (ENSMB = 0), equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per [Table 3](#). For PCIe applications, the RXDET pins provides automatic and manual control for input termination (50  $\Omega$  or >50 k $\Omega$ ). MODE setting is also pin controllable with pin selections (PCIe Gen-1, PCIe Gen-2, auto detect, and PCIe Gen-3). The receiver electrical idle detect threshold is also adjustable via the SD\_TH pin.

### 8.4.2 SMBus Mode

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB, the EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins (MODE, RXDET and SD\_TH) remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If PWDN is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most high speed applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. [4-Level Input Configuration Guidelines](#) shows the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-Emphasis levels are set by registers.

## 8.5 Programming

### 8.5.1 SMBus Master Mode

The DS125BR800 devices support reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS125BR800 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines. For additional information, refer to [SNLA228](#).

- Set ENSMB = Float — enable the SMBUS master mode.
- The external EEPROM device address byte must be 0xA0 and capable of 520 kHz operation at 2.5 V and 3.3 V supply.

## Programming (continued)

- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is 0xB0.

When tying multiple DS125BR800 devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can load its configuration from the EEPROM. Example below is for 4 device.
  - U1: AD[3:0] = 0000 = 0xB0,
  - U2: AD[3:0] = 0001 = 0xB2,
  - U3: AD[3:0] = 0010 = 0xB4,
  - U4: AD[3:0] = 0011 = 0xB6
- Use a pull-up resistor on SDA and SCL; value = 2 kΩ
- Daisy-chain READ\_EN (pin 26) and ALL\_DONE (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  - Tie READ\_EN of the 1st device in the chain (U1) to GND
  - Tie ALL\_DONE of U1 to READ\_EN of U2
  - Tie ALL\_DONE of U2 to READ\_EN of U3
  - Tie ALL\_DONE of U3 to READ\_EN of U4
  - Optional: Tie ALL\_DONE output of U4 to a LED to show the devices have been loaded successfully

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS125BR800 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS125BR800 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS125BR800 device. For additional information on EEPROM programming, refer to [SNLA228](#).

```
:2000000000001000000407002FAD4002FAD4002FAD4002FAD401805F5A8005F5A8005F5AD8
:200020008005F5A800005454000000000000000000000000000000000000000000000000F6
:20006000000000000000000000000000000000000000000000000000000000000000000080
:20008000000000000000000000000000000000000000000000000000000000000000000060
:2000A000000000000000000000000000000000000000000000000000000000000000000040
:2000C000000000000000000000000000000000000000000000000000000000000000000020
:2000E000000000000000000000000000000000000000000000000000000000000000000000
:200040000000000000000000000000000000000000000000000000000000000000000000A0
```

### NOTE

The maximum EEPROM size supported is 8-kbits (1024 x 8 bits).

**Table 7. EEPROM Register Map - Single Device with Default Value**

| EEPROM Address Byte |      | Bit 7                    | Bit 6                    | Bit 5                    | Bit 4                    | Bit 3                    | Bit 2                    | Bit 1                    | Bit 0                    |
|---------------------|------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| Description         | 0x00 | CRC EN                   | Address Map Present      | EEPROM > 256 Bytes       | Reserved                 | DEVICE COUNT[3]          | DEVICE COUNT[2]          | DEVICE COUNT[1]          | DEVICE COUNT[0]          |
| Default Value       | 0x00 | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |
| Description         | 0x01 | Reserved                 | Reserved                 | Reserved                 | Reserved                 | Reserved                 | Reserved                 | Reserved                 | Reserved                 |
| Default Value       | 0x00 | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |
| Description         | 0x02 | Max EEPROM Burst size[7] | Max EEPROM Burst size[6] | Max EEPROM Burst size[5] | Max EEPROM Burst size[4] | Max EEPROM Burst size[3] | Max EEPROM Burst size[2] | Max EEPROM Burst size[1] | Max EEPROM Burst size[0] |
| Default Value       | 0x00 | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |
| Description         | 0x03 | PWDN_ch7                 | PWDN_ch6                 | PWDN_ch5                 | PWDN_ch4                 | PWDN_ch3                 | PWDN_ch2                 | PWDN_ch1                 | PWDN_ch0                 |
| SMBus Register      |      | 0x01 [7]                 | 0x01 [6]                 | 0x01 [5]                 | 0x01 [4]                 | 0x01 [3]                 | 0x01 [2]                 | 0x01 [1]                 | 0x01 [0]                 |
| Default Value       | 0x00 | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |
| Description         | 0x04 | lpbk_1                   | lpbk_0                   | PWDN_INPUTS              | PWDN_OSC                 | Ovrd_PWDN                | Reserved                 | Reserved                 | Reserved                 |
| SMBus Register      |      | 0x02 [5]                 | 0x02 [4]                 | 0x02 [3]                 | 0x02 [2]                 | 0x02 [0]                 | 0x04 [7]                 | 0x04 [6]                 | 0x04 [5]                 |
| Default Value       | 00   | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |
| Description         | 0x05 | Reserved                 | Reserved                 | Reserved                 | Reserved                 | Reserved                 | rxdet_bt看_en             | Ovrd_idle_th             | Ovrd_RES                 |
| SMBus Register      |      | 0x04 [4]                 | 0x04 [3]                 | 0x04 [2]                 | 0x04 [1]                 | 0x04 [0]                 | 0x06 [4]                 | 0x08 [6]                 | 0x08 [5]                 |
| Default Value       | 04   | 0                        | 0                        | 0                        | 0                        | 0                        | 1                        | 0                        | 0                        |
| Description         | 0x06 | Ovrd_IDLE                | Ovrd_RX_DET              | Ovrd_MODE                | Ovrd_RES                 | Ovrd_RES                 | rx_delay_sel_2           | rx_delay_sel_1           | rx_delay_sel_0           |
| SMBus Register      |      | 0x08 [4]                 | 0x08 [3]                 | 0x08 [2]                 | 0x08 [1]                 | 0x08 [0]                 | 0x0B [6]                 | 0x0B [5]                 | 0x0B [4]                 |
| Default Value       | 07   | 0                        | 0                        | 0                        | 0                        | 0                        | 1                        | 1                        | 1                        |
| Description         | 0x07 | RD_delay_sel_3           | RD_delay_sel_2           | RD_delay_sel_1           | RD_delay_sel_0           | ch0_Idle_auto            | ch0_Idle_sel             | ch0_RXDET_1              | ch0_RXDET_0              |
| SMBus Register      |      | 0x0B [3]                 | 0x0B [2]                 | 0x0B [1]                 | 0x0B [0]                 | 0x0E [5]                 | 0x0E [4]                 | 0x0E [3]                 | 0x0E [2]                 |
| Default Value       | 00   | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |
| Description         | 0x08 | ch0_BST_7                | ch0_BST_6                | ch0_BST_5                | ch0_BST_4                | ch0_BST_3                | ch0_BST_2                | ch0_BST_1                | ch0_BST_0                |
| SMBus Register      |      | 0x0F [7]                 | 0x0F [6]                 | 0x0F [5]                 | 0x0F [4]                 | 0x0F [3]                 | 0x0F [2]                 | 0x0F [1]                 | 0x0F [0]                 |
| Default Value       | 2F   | 0                        | 0                        | 1                        | 0                        | 1                        | 1                        | 1                        | 1                        |
| Description         | 0x09 | ch0_Sel_scp              | ch0_Sel_mode             | ch0_RES_2                | ch0_RES_1                | ch0_RES_0                | ch0_VOD_2                | ch0_VOD_1                | ch0_VOD_0                |
| SMBus Register      |      | 0x10 [7]                 | 0x10 [6]                 | 0x10 [5]                 | 0x10 [4]                 | 0x10 [3]                 | 0x10 [2]                 | 0x10 [1]                 | 0x10 [0]                 |
| Default Value       | AD   | 1                        | 0                        | 1                        | 0                        | 1                        | 1                        | 0                        | 1                        |
| Description         | 0x0A | ch0_DEM_2                | ch0_DEM_1                | ch0_DEM_0                | ch0_Slow                 | ch0_idle_tha_1           | ch0_idle_tha_0           | ch0_idle_thd_1           | ch0_idle_thd_0           |
| SMBus Register      |      | 0x11 [2]                 | 0x11 [1]                 | 0x11 [0]                 | 0x12 [7]                 | 0x12 [3]                 | 0x12 [2]                 | 0x12 [1]                 | 0x12 [0]                 |
| Default Value       | 40   | 0                        | 1                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |

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**Table 7. EEPROM Register Map - Single Device with Default Value (continued)**

| EEPROM Address Byte |      | Bit 7          | Bit 6          | Bit 5          | Bit 4          | Bit 3          | Bit 2             | Bit 1             | Bit 0          |
|---------------------|------|----------------|----------------|----------------|----------------|----------------|-------------------|-------------------|----------------|
| Description         | 0x0B | ch1_idle_auto  | ch1_idle_sel   | ch1_RXDET_1    | ch1_RXDET_0    | ch1_BST_7      | ch1_BST_6         | ch1_BST_5         | ch1_BST_4      |
| SMBus Register      |      | 0x15 [5]       | 0x15 [4]       | 0x15 [3]       | 0x15 [2]       | 0x16 [7]       | 0x16 [6]          | 0x16 [5]          | 0x16 [4]       |
| Default Value       |      | 0              | 0              | 0              | 0              | 0              | 0                 | 1                 | 0              |
| Description         | 0x0C | ch1_BST_3      | ch1_BST_2      | ch1_BST_1      | ch1_BST_0      | ch1_Sel_scp    | ch1_Sel_mode      | ch1_RES_2         | ch1_RES_1      |
| SMBus Register      |      | 0x16 [3]       | 0x16 [2]       | 0x16 [1]       | 0x16 [0]       | 0x17 [7]       | 0x17 [6]          | 0x17 [5]          | 0x17 [4]       |
| Default Value       |      | 1              | 1              | 1              | 1              | 1              | 0                 | 1                 | 0              |
| Description         | 0x0D | ch1_RES_0      | ch1_VOD_2      | ch1_VOD_1      | ch1_VOD_0      | ch1_DEM_2      | ch1_DEM_1         | ch1_DEM_0         | ch1_Slow       |
| SMBus Register      |      | 0x17 [3]       | 0x17 [2]       | 0x17 [1]       | 0x17 [0]       | 0x18 [2]       | 0x18 [1]          | 0x18 [0]          | 0x19 [7]       |
| Default Value       |      | 1              | 1              | 0              | 1              | 0              | 1                 | 0                 | 0              |
| Description         | 0x0E | ch1_idle_tha_1 | ch1_idle_tha_0 | ch1_idle_thd_1 | ch1_idle_thd_0 | ch2_Idle_auto  | ch2_Idle_sel      | ch2_RXDET_1       | ch2_RXDET_0    |
| SMBus Register      |      | 0x19 [3]       | 0x19 [2]       | 0x19 [1]       | 0x19 [0]       | 0x1C [5]       | 0x1C [4]          | 0x1C [3]          | 0x1C [2]       |
| Default Value       |      | 0              | 0              | 0              | 0              | 0              | 0                 | 0                 | 0              |
| Description         | 0x0F | ch2_BST_7      | ch2_BST_6      | ch2_BST_5      | ch2_BST_4      | ch2_BST_3      | ch2_BST_2         | ch2_BST_1         | ch2_BST_0      |
| SMBus Register      |      | 0x1D [7]       | 0x1D [6]       | 0x1D [5]       | 0x1D [4]       | 0x1D [3]       | 0x1D [2]          | 0x1D [1]          | 0x1D [0]       |
| Default Value       |      | 0              | 0              | 1              | 0              | 1              | 1                 | 1                 | 1              |
| Description         | 0x10 | ch2_Sel_scp    | ch2_Sel_mode   | ch2_RES_2      | ch2_RES_1      | ch2_RES_0      | ch2_VOD_2         | ch2_VOD_1         | ch2_VOD_0      |
| SMBus Register      |      | 0x1E [7]       | 0x1E [6]       | 0x1E [5]       | 0x1E [4]       | 0x1E [3]       | 0x1E [2]          | 0x1E [1]          | 0x1E [0]       |
| Default Value       |      | 1              | 0              | 1              | 0              | 1              | 1                 | 0                 | 1              |
| Description         | 0x11 | ch2_DEM_2      | ch2_DEM_1      | ch2_DEM_0      | ch2_Slow       | ch2_idle_tha_1 | ch2_idle_tha_0    | ch2_idle_thd_1    | ch2_idle_thd_0 |
| SMBus Register      |      | 0x1F [2]       | 0x1F [1]       | 0x1F [0]       | 0x20 [7]       | 0x20 [3]       | 0x20 [2]          | 0x20 [1]          | 0x20 [0]       |
| Default Value       |      | 0              | 1              | 0              | 0              | 0              | 0                 | 0                 | 0              |
| Description         | 0x12 | ch3_Idle_auto  | ch3_Idle_sel   | ch3_RXDET_1    | ch3_RXDET_0    | ch3_BST_7      | ch3_BST_6         | ch3_BST_5         | ch3_BST_4      |
| SMBus Register      |      | 0x23 [5]       | 0x23 [4]       | 0x23 [3]       | 0x23 [2]       | 0x24 [7]       | 0x24 [6]          | 0x24 [5]          | 0x24 [4]       |
| Default Value       |      | 0              | 0              | 0              | 0              | 0              | 0                 | 1                 | 0              |
| Description         | 0x13 | ch3_BST_3      | ch3_BST_2      | ch3_BST_1      | ch3_BST_0      | ch3_Sel_scp    | ch3_Sel_mode      | ch3_RES_2         | ch3_RES_1      |
| SMBus Register      |      | 0x24 [3]       | 0x24 [2]       | 0x24 [1]       | 0x24 [0]       | 0x25 [7]       | 0x25 [6]          | 0x25 [5]          | 0x25 [4]       |
| Default Value       |      | 1              | 1              | 1              | 1              | 1              | 0                 | 1                 | 0              |
| Description         | 0x14 | ch3_RES_0      | ch3_VOD_2      | ch3_VOD_1      | ch3_VOD_0      | ch3_DEM_2      | ch3_DEM_1         | ch3_DEM_0         | ch3_Slow       |
| SMBus Register      |      | 0x25 [3]       | 0x25 [2]       | 0x25 [1]       | 0x25 [0]       | 0x26 [2]       | 0x26 [1]          | 0x26 [0]          | 0x27 [7]       |
| Default Value       |      | 1              | 1              | 0              | 1              | 0              | 1                 | 0                 | 0              |
| Description         | 0x15 | ch3_idle_tha_1 | ch3_idle_tha_0 | ch3_idle_thd_1 | ch3_idle_thd_0 | ovrd_fast_idle | en_high_idle_th_n | en_high_idle_th_s | en_fast_idle_n |
| SMBus Register      |      | 0x27 [3]       | 0x27 [2]       | 0x27 [1]       | 0x27 [0]       | 0x28 [6]       | 0x28 [5]          | 0x28 [4]          | 0x28 [3]       |
| Default Value       |      | 0              | 0              | 0              | 0              | 0              | 0                 | 0                 | 1              |

Table 7. EEPROM Register Map - Single Device with Default Value (continued)

| EEPROM Address Byte |      | Bit 7          | Bit 6          | Bit 5          | Bit 4          | Bit 3          | Bit 2          | Bit 1          | Bit 0          |
|---------------------|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Description         | 0x16 | en_fast_idle_s | eqsd_mgain_n   | eqsd_mgain_s   | ch4_idle_auto  | ch4_idle_sel   | ch4_RXDET_1    | ch4_RXDET_0    | ch4_BST_7      |
| SMBus Register      |      | 0x28 [2]       | 0x28 [1]       | 0x28 [0]       | 0x2B [5]       | 0x2B [4]       | 0x2B [3]       | 0x2B [2]       | 0x2C [7]       |
| Default Value       | 80   | 1              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |
| Description         | 0x17 | ch4_BST_6      | ch4_BST_5      | ch4_BST_4      | ch4_BST_3      | ch4_BST_2      | ch4_BST_1      | ch4_BST_0      | ch4_Sel_scp    |
| SMBus Register      |      | 0x2C [6]       | 0x2C [5]       | 0x2C [4]       | 0x2C [3]       | 0x2C [2]       | 0x2C [1]       | 0x2C [0]       | 0x2D [7]       |
| Default Value       | 5F   | 0              | 1              | 0              | 1              | 1              | 1              | 1              | 1              |
| Description         | 0x18 | ch4_Sel_mode   | ch4_RES_2      | ch4_RES_1      | ch4_RES_0      | ch4_VOD_2      | ch4_VOD_1      | ch4_VOD_0      | ch4_DEM_2      |
| SMBus Register      |      | 0x2D [6]       | 0x2D [5]       | 0x2D [4]       | 0x2D [3]       | 0x2D [2]       | 0x2D [1]       | 0x2D [0]       | 0x2E [2]       |
| Default Value       | 5A   | 0              | 1              | 0              | 1              | 1              | 0              | 1              | 0              |
| Description         | 0x19 | ch4_DEM_1      | ch4_DEM_0      | ch4_Slow       | ch4_idle_tha_1 | ch4_idle_tha_0 | ch4_idle_thd_1 | ch4_idle_thd_0 | ch5_idle_auto  |
| SMBus Register      |      | 0x2E [1]       | 0x2E [0]       | 0x2F [7]       | 0x2F [3]       | 0x2F [2]       | 0x2F [1]       | 0x2F [0]       | 0x32 [5]       |
| Default Value       | 80   | 1              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |
| Description         | 0x1A | ch5_idle_sel   | ch5_RXDET_1    | ch5_RXDET_0    | ch5_BST_7      | ch5_BST_6      | ch5_BST_5      | ch5_BST_4      | ch5_BST_3      |
| SMBus Register      |      | 0x32 [4]       | 0x32 [3]       | 0x32 [2]       | 0x33 [7]       | 0x33 [6]       | 0x33 [5]       | 0x33 [4]       | 0x33 [3]       |
| Default Value       | 05   | 0              | 0              | 0              | 0              | 0              | 1              | 0              | 1              |
| Description         | 0x1B | ch5_BST_2      | ch5_BST_1      | ch5_BST_0      | ch5_Sel_scp    | ch5_Sel_mode   | ch5_RES_2      | ch5_RES_1      | ch5_RES_0      |
| SMBus Register      |      | 0x33 [2]       | 0x33 [1]       | 0x33 [0]       | 0x34 [7]       | 0x34 [6]       | 0x34 [5]       | 0x34 [4]       | 0x34 [3]       |
| Default Value       | F5   | 1              | 1              | 1              | 1              | 0              | 1              | 0              | 1              |
| Description         | 0x1C | ch5_VOD_2      | ch5_VOD_1      | ch5_VOD_0      | ch5_DEM_2      | ch5_DEM_1      | ch5_DEM_0      | ch5_Slow       | ch5_idle_tha_1 |
| SMBus Register      |      | 0x34 [2]       | 0x34 [1]       | 0x34 [0]       | 0x35 [2]       | 0x35 [1]       | 0x35 [0]       | 0x36 [7]       | 0x36 [3]       |
| Default Value       | A8   | 1              | 0              | 1              | 0              | 1              | 0              | 0              | 0              |
| Description         | 0x1D | ch5_idle_tha_0 | ch5_idle_thd_1 | ch5_idle_thd_0 | ch6_idle_auto  | ch6_idle_sel   | ch6_RXDET_1    | ch6_RXDET_0    | ch6_BST_7      |
| SMBus Register      |      | 0x36 [2]       | 0x36 [1]       | 0x36 [0]       | 0x39 [5]       | 0x39 [4]       | 0x39 [3]       | 0x39 [2]       | 0x3A [7]       |
| Default Value       | 00   | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |
| Description         | 0x1E | ch6_BST_6      | ch6_BST_5      | ch6_BST_4      | ch6_BST_3      | ch6_BST_2      | ch6_BST_1      | ch6_BST_0      | ch6_Sel_scp    |
| SMBus Register      |      | 0x3A [6]       | 0x3A [5]       | 0x3A [4]       | 0x3A [3]       | 0x3A [2]       | 0x3A [1]       | 0x3A [0]       | 0x3B [7]       |
| Default Value       | 5F   | 0              | 1              | 0              | 1              | 1              | 1              | 1              | 1              |
| Description         | 0x1F | ch6_Sel_mode   | ch6_RES_2      | ch6_RES_1      | ch6_RES_0      | ch6_VOD_2      | ch6_VOD_1      | ch6_VOD_0      | ch6_DEM_2      |
| SMBus Register      |      | 0x3B [6]       | 0x3B [5]       | 0x3B [4]       | 0x3B [3]       | 0x3B [2]       | 0x3B [1]       | 0x3B [0]       | 0x3C [2]       |
| Default Value       | 5A   | 0              | 1              | 0              | 1              | 1              | 0              | 1              | 0              |
| Description         | 0x20 | ch6_DEM_1      | ch6_DEM_0      | ch6_Slow       | ch6_idle_tha_1 | ch6_idle_tha_0 | ch6_idle_thd_1 | ch6_idle_thd_0 | ch7_idle_auto  |
| SMBus Register      |      | 0x3C [1]       | 0x3C [0]       | 0x3D [7]       | 0x3D [3]       | 0x3D [2]       | 0x3D [1]       | 0x3D [0]       | 0x40 [5]       |
| Default Value       | 80   | 1              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

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**Table 7. EEPROM Register Map - Single Device with Default Value (continued)**

| EEPROM Address Byte |      | Bit 7          | Bit 6          | Bit 5          | Bit 4       | Bit 3        | Bit 2     | Bit 1     | Bit 0          |
|---------------------|------|----------------|----------------|----------------|-------------|--------------|-----------|-----------|----------------|
| Description         | 0x21 | ch7_idle_sel   | ch7_RXDET_1    | ch7_RXDET_0    | ch7_BST_7   | ch7_BST_6    | ch7_BST_5 | ch7_BST_4 | ch7_BST_3      |
| SMBus Register      |      | 0x40 [4]       | 0x40 [3]       | 0x40 [2]       | 0x41 [7]    | 0x41 [6]     | 0x41 [5]  | 0x41 [4]  | 0x41 [3]       |
| Default Value       |      | 0              | 0              | 0              | 0           | 0            | 1         | 0         | 1              |
| Description         | 0x22 | ch7_BST_2      | ch7_BST_1      | ch7_BST_0      | ch7_Sel_scp | ch7_Sel_mode | ch7_RES_2 | ch7_RES_1 | ch7_RES_0      |
| SMBus Register      |      | 0x41 [2]       | 0x41 [1]       | 0x41 [0]       | 0x42 [7]    | 0x42 [6]     | 0x42 [5]  | 0x42 [4]  | 0x42 [3]       |
| Default Value       |      | 1              | 1              | 1              | 1           | 0            | 1         | 0         | 1              |
| Description         | 0x23 | ch7_VOD_2      | ch7_VOD_1      | ch7_VOD_0      | ch7_DEM_2   | ch7_DEM_1    | ch7_DEM_0 | ch7_Slow  | ch7_idle_tha_1 |
| SMBus Register      |      | 0x42 [2]       | 0x42 [1]       | 0x42 [0]       | 0x43 [2]    | 0x43 [1]     | 0x43 [0]  | 0x44 [7]  | 0x44 [3]       |
| Default Value       |      | 1              | 0              | 1              | 0           | 1            | 0         | 0         | 0              |
| Description         | 0x24 | ch7_idle_tha_0 | ch7_idle_thd_1 | ch7_idle_thd_0 | Reserved    | Reserved     | Reserved  | Reserved  | Reserved       |
| SMBus Register      |      | 0x44 [2]       | 0x44 [1]       | 0x44 [0]       | 0x47 [3]    | 0x47 [2]     | 0x47 [2]  | 0x47 [0]  | 0x48 [7]       |
| Default Value       |      | 0              | 0              | 0              | 0           | 0            | 0         | 0         | 0              |
| Description         | 0x25 | Reserved       | Reserved       | Reserved       | Reserved    | Reserved     | Reserved  | Reserved  | Reserved       |
| SMBus Register      |      | 0x48 [6]       | 0x4C [7]       | 0x4C [6]       | 0x4C [5]    | 0x4C [4]     | 0x4C [3]  | 0x4C [0]  | 0x59 [0]       |
| Default Value       |      | 0              | 0              | 0              | 0           | 0            | 0         | 0         | 0              |
| Description         | 0x26 | Reserved       | Reserved       | Reserved       | Reserved    | Reserved     | Reserved  | Reserved  | Reserved       |
| SMBus Register      |      | 0x5A [7]       | 0x5A [6]       | 0x5A [5]       | 0x5A [4]    | 0x5A [3]     | 0x5A [2]  | 0x5A [1]  | 0x5A [0]       |
| Default Value       |      | 0              | 1              | 0              | 1           | 0            | 1         | 0         | 0              |
| Description         | 0x27 | Reserved       | Reserved       | Reserved       | Reserved    | Reserved     | Reserved  | Reserved  | Reserved       |
| SMBus Register      |      | 0x5B [7]       | 0x5B [6]       | 0x5B [5]       | 0x5B [4]    | 0x5B [3]     | 0x5B [2]  | 0x5B [1]  | 0x5B [0]       |
| Default Value       |      | 0              | 1              | 0              | 1           | 0            | 1         | 0         | 0              |

**Table 8. Example of EEPROM for Four Devices Using Two Address Maps**

| EEPROM Address | Address (Hex) | EEPROM Data | Comments                                                           |
|----------------|---------------|-------------|--------------------------------------------------------------------|
| 0              | 00            | 0x43        | CRC_EN = 0, Address Map = 1, >256 bytes = 0, Device Count[3:0] = 3 |
| 1              | 01            | 0x00        |                                                                    |
| 2              | 02            | 0x08        | EEPROM Burst Size                                                  |
| 3              | 03            | 0x00        | CRC not used                                                       |
| 4              | 04            | 0x0B        | Device 0 Address Location                                          |
| 5              | 05            | 0x00        | CRC not used                                                       |
| 6              | 06            | 0x0B        | Device 1 Address Location                                          |
| 7              | 07            | 0x00        | CRC not used                                                       |
| 8              | 08            | 0x30        | Device 2 Address Location                                          |
| 9              | 09            | 0x00        | CRC not used                                                       |
| 10             | 0A            | 0x30        | Device 3 Address Location                                          |
| 11             | 0B            | 0x00        | Begin Device 0, 1 - Address Offset 3                               |
| 12             | 0C            | 0x00        |                                                                    |
| 13             | 0D            | 0x04        |                                                                    |
| 14             | 0E            | 0x07        |                                                                    |
| 15             | 0F            | 0x00        |                                                                    |
| 16             | 10            | 0x00        | EQ CHB0 = 00                                                       |
| 17             | 11            | 0xAB        | VOD CHB0 = 1.0 V                                                   |
| 18             | 12            | 0x00        | DEM CHB0 = 0 (0 dB)                                                |
| 19             | 13            | 0x00        | EQ CHB1 = 00                                                       |
| 20             | 14            | 0x0A        | VOD CHB1 = 1.0 V                                                   |
| 21             | 15            | 0xB0        | DEM CHB1 = 0 (0 dB)                                                |
| 22             | 16            | 0x00        |                                                                    |
| 23             | 17            | 0x00        | EQ CHB2 = 00                                                       |
| 24             | 18            | 0xAB        | VOD CHB2 = 1.0 V                                                   |
| 25             | 19            | 0x00        | DEM CHB2 = 0 (0 dB)                                                |
| 26             | 1A            | 0x00        | EQ CHB3 = 00                                                       |
| 27             | 1B            | 0x0A        | VOD CHB3 = 1.0 V                                                   |
| 28             | 1C            | 0xB0        | DEM CHB3 = 0 (0 dB)                                                |
| 29             | 1D            | 0x01        |                                                                    |
| 30             | 1E            | 0x80        |                                                                    |
| 31             | 1F            | 0x01        | EQ CHA0 = 00                                                       |
| 32             | 20            | 0x56        | VOD CHA0 = 1.0 V                                                   |
| 33             | 21            | 0x00        | DEM CHA0 = 0 (0 dB)                                                |
| 34             | 22            | 0x00        | EQ CHA1 = 00                                                       |
| 35             | 23            | 0x15        | VOD CHA1 = 1.0 V                                                   |
| 36             | 24            | 0x60        | DEM CHA1 = 0 (0 dB)                                                |
| 37             | 25            | 0x00        |                                                                    |
| 38             | 26            | 0x01        | EQ CHA2 = 00                                                       |
| 39             | 27            | 0x56        | VOD CHA2 = 1.0 V                                                   |
| 40             | 28            | 0x00        | DEM CHA2 = 0 (0 dB)                                                |
| 41             | 29            | 0x00        | EQ CHA3 = 00                                                       |
| 42             | 2A            | 0x15        | VOD CHA3 = 1.0 V                                                   |
| 43             | 2B            | 0x60        | DEM CHA3 = 0 (0 dB)                                                |
| 44             | 2C            | 0x00        |                                                                    |
| 45             | 2D            | 0x00        |                                                                    |
| 46             | 2E            | 0x54        |                                                                    |

**Table 8. Example of EEPROM for Four Devices Using Two Address Maps (continued)**

| EEPROM Address | Address (Hex) | EEPROM Data | Comments                             |
|----------------|---------------|-------------|--------------------------------------|
| 47             | 2F            | 0x54        | End Device 0, 1 - Address Offset 39  |
| 48             | 30            | 0x00        | Begin Device 2, 3 - Address Offset 3 |
| 49             | 31            | 0x00        |                                      |
| 50             | 32            | 0x04        |                                      |
| 51             | 33            | 0x07        |                                      |
| 52             | 34            | 0x00        |                                      |
| 53             | 35            | 0x00        | EQ CHB0 = 00                         |
| 54             | 36            | 0xAB        | VOD CHB0 = 1.0 V                     |
| 55             | 37            | 0x00        | DEM CHB0 = 0 (0 dB)                  |
| 56             | 38            | 0x00        | EQ CHB1 = 00                         |
| 57             | 39            | 0x0A        | VOD CHB1 = 1.0 V                     |
| 58             | 3A            | 0xB0        | DEM CHB1 = 0 (0 dB)                  |
| 59             | 3B            | 0x00        |                                      |
| 60             | 3C            | 0x00        | EQ CHB2 = 00                         |
| 61             | 3D            | 0xAB        | VOD CHB2 = 1.0 V                     |
| 62             | 3E            | 0x00        | DEM CHB2 = 0 (0 dB)                  |
| 63             | 3F            | 0x00        | EQ CHB3 = 00                         |
| 64             | 40            | 0x0A        | VOD CHB3 = 1.0 V                     |
| 65             | 41            | 0xB0        | DEM CHB3 = 0 (0 dB)                  |
| 66             | 42            | 0x01        |                                      |
| 67             | 43            | 0x80        |                                      |
| 68             | 44            | 0x01        | EQ CHA0 = 00                         |
| 69             | 45            | 0x56        | VOD CHA0 = 1.0 V                     |
| 70             | 46            | 0x00        | DEM CHA0 = 0 (0 dB)                  |
| 71             | 47            | 0x00        | EQ CHA1 = 00                         |
| 72             | 48            | 0x15        | VOD CHA1 = 1.0 V                     |
| 73             | 49            | 0x60        | DEM CHA1 = 0 (0 dB)                  |
| 74             | 4A            | 0x00        |                                      |
| 75             | 4B            | 0x01        | EQ CHA2 = 00                         |
| 76             | 4C            | 0x56        | VOD CHA2 = 1.0 V                     |
| 77             | 4D            | 0x00        | DEM CHA2 = 0 (0 dB)                  |
| 78             | 4E            | 0x00        | EQ CHA3 = 00                         |
| 79             | 4F            | 0x15        | VOD CHA3 = 1.0 V                     |
| 80             | 50            | 0x60        | DEM CHA3 = 0 (0 dB)                  |
| 81             | 51            | 0x00        |                                      |
| 82             | 52            | 0x00        |                                      |
| 83             | 53            | 0x54        |                                      |
| 84             | 54            | 0x54        | End Device 2, 3 - Address Offset 39  |

NOTE: CRC\_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. This example has all 8 channels set to EQ = 00 (min boost), VOD = 1.0 V, DEM = 0 (0 dB) and multiple device can point to the same address map. Maximum EEPROM size is 8kbits (1024 x 8-bits).

### 8.5.2 Transfer of Data Via the SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

**START:** A High-to-Low transition on SDA while SCL is High indicates a message START condition.

**STOP:** A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

**IDLE:** If SCL and SDA are both High for a time exceeding  $t_{BUF}$  from the last detected STOP condition or if they are High for a total exceeding the maximum specification for  $t_{HIGH}$  then the bus will transfer to the IDLE state.

### 8.5.3 System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB = 1 k $\Omega$  to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS125BR800 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is 0xB0. Based on the SMBus 2.0 specification, the DS125BR800 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. [Table 9](#) shows the 16 addresses.

**Table 9. Device Slave Address Bytes**

| AD[3:0] Settings | Address Bytes (HEX) |
|------------------|---------------------|
| 0000             | B0                  |
| 0001             | B2                  |
| 0010             | B4                  |
| 0011             | B6                  |
| 0100             | B8                  |
| 0101             | BA                  |
| 0110             | BC                  |
| 0111             | BE                  |
| 1000             | C0                  |
| 1001             | C2                  |
| 1010             | C4                  |
| 1011             | C6                  |
| 1100             | C8                  |
| 1101             | CA                  |
| 1110             | CC                  |
| 1111             | CE                  |

The SDA, SCL pins are 3.3 V tolerant, but are not 5 V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 k $\Omega$  to 5 k $\Omega$  depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

### 8.5.4 SMBus Transactions

The device supports WRITE and READ transactions. See [Table 10](#) for register address, type (Read/Write, Read Only), default value and function information.

### 8.5.5 Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit ("0").
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

### 8.5.6 Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
7. The Device drives an ACK bit "0".
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit "1" indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

## 8.6 Register Maps

**Table 10. SMBUS Slave Mode Register Map**

| Address | Register Name              | Bit | Field               | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                       |
|---------|----------------------------|-----|---------------------|------|---------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x00    | Device Address Observation | 7   | Reserved            | R/W  | 0x00    |            | Set bit to 0.                                                                                                                                                                                                                                                                     |
|         |                            | 6:3 | Address Bit AD[3:0] | R    |         |            | Observation of AD[3:0] bit<br>[6]: AD3<br>[5]: AD2<br>[4]: AD1<br>[3]: AD0                                                                                                                                                                                                        |
|         |                            | 2   | EEPROM Read Done    | R    |         |            | 1: Device completed the read from external EEPROM.                                                                                                                                                                                                                                |
|         |                            | 1:0 | Reserved            | R/W  |         |            | Set bits to 0.                                                                                                                                                                                                                                                                    |
| 0x01    | PWDN Channels              | 7:0 | PWDN CHx            | R/W  | 0x00    | Yes        | Power Down per Channel<br>[7]: CH7 – CHA_3<br>[6]: CH6 – CHA_2<br>[5]: CH5 – CHA_1<br>[4]: CH4 – CHA_0<br>[3]: CH3 – CHB_3<br>[2]: CH2 – CHB_2<br>[1]: CH1 – CHB_1<br>[0]: CH0 – CHB_0<br>0x00 = all channels enabled<br>0xFF = all channels disabled<br>Note: override PWDN pin. |
| 0x02    | Override PWDN Control      | 7:1 | Reserved            | R/W  | 0x00    | Yes        | Set bits to 0.                                                                                                                                                                                                                                                                    |
|         |                            | 0   | Override PWDN       |      |         |            | 1: Block PWDN pin control<br>0: Allow PWDN pin control                                                                                                                                                                                                                            |
| 0x03    | Reserved                   | 7:0 | Reserved            | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                                                                                                                                     |
| 0x04    | Reserved                   | 7:0 | Reserved            | R/W  | 0x00    | Yes        | Set bits to 0                                                                                                                                                                                                                                                                     |
| 0x05    | Reserved                   | 7:0 | Reserved            | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                                                                                                                                     |
| 0x05    | Reserved                   | 7:0 | Reserved            | R/W  | 0x00    |            | Reserved                                                                                                                                                                                                                                                                          |
| 0x06    | Slave Register Control     | 7:5 | Reserved            | R/W  | 0x10    |            | Set bits to 0.                                                                                                                                                                                                                                                                    |
|         |                            | 4   | Reserved            |      |         | Yes        | Set bit to 1.                                                                                                                                                                                                                                                                     |
|         |                            | 3   | Register Enable     |      |         |            | 1 = Enable SMBus Register Control<br>0 = Disable SMBus Register Control<br><b>Note: In order to change VOD, DEM, and EQ of the channels in slave mode, this bit must be set to 1.</b>                                                                                             |
|         |                            | 2:0 | Reserved            |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                    |
| 0x07    | Digital Reset and Control  | 7   | Reserved            | R/W  | 0x01    |            | Set bit to 0.                                                                                                                                                                                                                                                                     |
|         |                            | 6   | Reset Registers     |      |         |            | Self clearing bit, set to 1 to reset the register to default values                                                                                                                                                                                                               |
|         |                            | 5   | Reset SMBus Master  |      |         |            | Self clearing reset to SMBus master state machine                                                                                                                                                                                                                                 |
|         |                            | 4:0 | Reserved            |      |         |            | Set bits to 0 0001'b.                                                                                                                                                                                                                                                             |

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**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name            | Bit | Field          | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                         |
|---------|--------------------------|-----|----------------|------|---------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x08    | Override Pin Control     | 7   | Reserved       | R/W  | 0x00    |            | Set bit to 0.                                                                                                                                                                                                                                                                                                                                                       |
|         |                          | 6   | Override SD_TH |      |         | Yes        | 1: Block SD_TH pin control<br>0: Allow SD_TH pin control                                                                                                                                                                                                                                                                                                            |
|         |                          | 5   | Reserved       |      |         | Yes        | Set bit to 0.                                                                                                                                                                                                                                                                                                                                                       |
|         |                          | 4   | Override IDLE  |      |         | Yes        | 1: IDLE control by registers<br>0: IDLE control by signal detect                                                                                                                                                                                                                                                                                                    |
|         |                          | 3   | Override RXDET |      |         | Yes        | 1: Block RXDET pin control<br>0: Allow RXDET pin control                                                                                                                                                                                                                                                                                                            |
|         |                          | 2   | Override MODE  |      |         | Yes        | 1: Block MODE pin control<br>0: Allow MODE pin control                                                                                                                                                                                                                                                                                                              |
|         |                          | 1   | Reserved       |      |         |            | Set bit to 0.                                                                                                                                                                                                                                                                                                                                                       |
|         |                          | 0   | Reserved       |      |         |            | Set bit to 0.                                                                                                                                                                                                                                                                                                                                                       |
| 0x09    | Reserved                 | 7:0 | Reserved       | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                                                                                                                                                                                                                       |
| 0x0A    | Signal Detect Monitor    | 7:0 | SD_TH Status   | R    | 0x00    |            | CH7 - CH0 Internal Signal Detector Indicator<br>[7]: CH7 - CHA_3<br>[6]: CH6 - CHA_2<br>[5]: CH5 - CHA_1<br>[4]: CH4 - CHA_0<br>[3]: CH3 - CHB_3<br>[2]: CH2 - CHB_2<br>[1]: CH1 - CHB_1<br>[0]: CH0 - CHB_0<br>0 = Signal detected at input (active data)<br>1 = Signal not detected at input (idle state)<br>NOTE: These bits only function when RATE pin = FLOAT |
| 0x0B    | Reserved                 | 7   | Reserved       | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                                                                                                                                                                                                                       |
|         |                          | 6:0 | Reserved       | R/W  | 0x70    | Yes        | Set bits to 111 0000'b                                                                                                                                                                                                                                                                                                                                              |
| 0x0C    | Reserved                 | 7:0 | Reserved       | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                                                                                                                                                                                                                       |
| 0x0D    | CH0 - CHB0 Signal Detect | 7:3 | Reserved       | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                      |
|         |                          | 2   | SD Reset       |      |         |            | 1: Force signal detect "off"<br>0: Normal operation                                                                                                                                                                                                                                                                                                                 |
|         |                          | 1   | SD Preset      |      |         |            | 1: Force signal detect "on"<br>0: Normal operation                                                                                                                                                                                                                                                                                                                  |
|         |                          | 0   | Reserved       |      |         |            | Set bit to 0.                                                                                                                                                                                                                                                                                                                                                       |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name             | Bit | Field                    | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|---------------------------|-----|--------------------------|------|---------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x0E    | CH0 - CHB0<br>IDLE, RXDET | 7:6 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         |                           | 5   | IDLE_AUTO                |      |         | Yes        | 1 = Allow IDLE_SEL control in bit 4<br>0 = Automatic IDLE detect<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 4   | IDLE_SEL                 |      |         | Yes        | 1: Output is MUTED (electrical idle)<br>0: Output is ON<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                                  |
|         |                           | 3:2 | RXDET                    |      |         | Yes        | 00: Input is high-z impedance<br>01: Auto RX-Detect,<br>outputs test every 12 ms for 600 ms (50 times) then stops; termination<br>is high-z until detection; once detected input termination is 50 $\Omega$<br>10: Auto RX-Detect,<br>outputs test every 12 ms until detection occurs; termination is high-z<br>until detection; once detected input termination is 50 $\Omega$<br>11: Input is 50 $\Omega$<br>Note: override RXDET pin. |
|         |                           | 1:0 | Reserved                 |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0x0F    | CH0 - CHB0<br>EQ          | 7:0 | EQ Control               | R/W  | 0x2F    | Yes        | IB0 EQ Control - total of 256 levels.<br>See <a href="#">Table 2</a> .                                                                                                                                                                                                                                                                                                                                                                   |
| 0x10    | CH0 - CHB0<br>VOD         | 7   | Short Circuit Protection | R/W  | 0xAD    | Yes        | 1: Enable the short circuit protection<br>0: Disable the short circuit protection                                                                                                                                                                                                                                                                                                                                                        |
|         |                           | 6   | MODE_SEL                 |      |         | Yes        | 1: PCIe Gen-1 or PCIe Gen-2<br>0: PCIe Gen-3<br>Note: override the MODE pin.                                                                                                                                                                                                                                                                                                                                                             |
|         |                           | 5:3 | Reserved                 |      |         | Yes        | Set bits to default value - 101.                                                                                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 2:0 | VOD Control              |      |         | Yes        | OB0 VOD Control<br>000: 0.7 V<br>001: 0.8 V<br>010: 0.9 V<br>011: 1.0 V<br>100: 1.1 V<br>101: 1.2 V (default)<br>110: 1.3 V<br>111: 1.4 V                                                                                                                                                                                                                                                                                                |

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**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name                | Bit | Field           | Type | Default | EEPROM Bit | Description                                                                                                                                                        |
|---------|------------------------------|-----|-----------------|------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x11    | CH0 - CHB0<br>DEM            | 7   | RXDET STATUS    | R    | 0x02    |            | Observation bit for RXDET CH0 - CHB0.<br>1: RX = detected<br>0: RX = not detected                                                                                  |
|         |                              | 6:5 | MODE_DET STATUS | R    |         |            | Observation bit for MODE_DET CH0 - CHB0.<br>00: PCIe Gen-1 (2.5G)<br>01: PCIe Gen-2 (5G)<br>11: PCIe Gen-3 (8G+)<br>Note: Only functions when MODE Pin = Automatic |
|         |                              | 4:3 | Reserved        | R/W  |         |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2:0 | DEM Control     | R/W  |         | Yes        | OB0 DEM Control<br>000: 0 dB<br>001: -1.5 dB<br>010: -3.5 dB (default)<br>011: -5 dB<br>100: -6 dB<br>101: -8 dB<br>110: -9 dB<br>111: -12 dB                      |
| 0x12    | CH0 - CHB0<br>IDLE Threshold | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 3:2 | IDLE tha        |      |         | Yes        | Assert threshold<br>00 = 180 mVp-p (default)<br>01 = 160 mVp-p<br>10 = 210 mVp-p<br>11 = 190 mVp-p<br>Note: override the SD_TH pin.                                |
|         |                              | 1:0 | IDLE thd        |      |         | Yes        | De-Assert threshold<br>00 = 110 mVp-p (default)<br>01 = 100 mVp-p<br>10 = 150 mVp-p<br>11 = 130 mVp-p<br>Note: override the SD_TH pin.                             |
| 0x13    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x14    | CH1 - CHB1<br>Signal Detect  | 7:3 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2   | SD Reset        |      |         |            | 1: Force signal detect "off"<br>0: Normal operation                                                                                                                |
|         |                              | 1   | SD Preset       |      |         |            | 1: Force signal detect "on"<br>0: Normal operation                                                                                                                 |
|         |                              | 0   | Reserved        |      |         |            | Set bit to 0.                                                                                                                                                      |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name             | Bit | Field                    | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------|---------------------------|-----|--------------------------|------|---------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x15    | CH1 - CHB1<br>IDLE, RXDET | 7:6 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                      |
|         |                           | 5   | IDLE_AUTO                |      |         | Yes        | 1 = Allow IDLE_SEL control in bit 4<br>0 = Automatic IDLE detect<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                    |
|         |                           | 4   | IDLE_SEL                 |      |         | Yes        | 1: Output is MUTED (electrical idle)<br>0: Output is ON<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                             |
|         |                           | 3:2 | RXDET                    |      |         | Yes        | 00: Input is high-z impedance<br>01: Auto RX-Detect,<br>outputs test every 12 ms for 600 ms (50 times) then stops; termination<br>is high-z until detection; once detected input termination is 50 Ω<br>10: Auto RX-Detect,<br>outputs test every 12 ms until detection occurs; termination is high-z<br>until detection; once detected input termination is 50 Ω<br>11: Input is 50 Ω<br>Note: override RXDET pin. |
|         |                           | 1:0 | Reserved                 |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0x16    | CH1 - CHB1<br>EQ          | 7:0 | EQ Control               | R/W  | 0x2F    | Yes        | IB1 EQ Control - total of 256 levels.<br>See <a href="#">Table 2</a> .                                                                                                                                                                                                                                                                                                                                              |
| 0x17    | CH1 - CHB1<br>VOD         | 7   | Short Circuit Protection | R/W  | 0xAD    | Yes        | 1: Enable the short circuit protection<br>0: Disable the short circuit protection                                                                                                                                                                                                                                                                                                                                   |
|         |                           | 6   | MODE_SEL                 |      |         | Yes        | 1: PCIe Gen-1 or PCIe Gen-2<br>0: PCIe Gen-3<br>Note: override the MODE pin.                                                                                                                                                                                                                                                                                                                                        |
|         |                           | 5:3 | Reserved                 |      |         | Yes        | Set bits to default value - 101.                                                                                                                                                                                                                                                                                                                                                                                    |
|         |                           | 2:0 | VOD Control              |      |         | Yes        | OB1 VOD Control<br>000: 0.7 V<br>001: 0.8 V<br>010: 0.9 V<br>011: 1.0 V<br>100: 1.1 V<br>101: 1.2 V (default)<br>110: 1.3 V<br>111: 1.4 V                                                                                                                                                                                                                                                                           |

**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name                | Bit | Field           | Type | Default | EEPROM Bit | Description                                                                                                                                                        |
|---------|------------------------------|-----|-----------------|------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x18    | CH1 - CHB1<br>DEM            | 7   | RXDET STATUS    | R    | 0x02    |            | Observation bit for RXDET CH1 - CHB1.<br>1: RX = detected<br>0: RX = not detected                                                                                  |
|         |                              | 6:5 | MODE_DET STATUS | R    |         |            | Observation bit for MODE_DET CH1 - CHB1.<br>00: PCIe Gen-1 (2.5G)<br>01: PCIe Gen-2 (5G)<br>11: PCIe Gen-3 (8G+)<br>Note: Only functions when MODE Pin = Automatic |
|         |                              | 4:3 | Reserved        | R/W  |         |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2:0 | DEM Control     | R/W  |         | Yes        | OB1 DEM Control<br>000: 0 dB<br>001: -1.5 dB<br>010: -3.5 dB (default)<br>011: -5 dB<br>100: -6 dB<br>101: -8 dB<br>110: -9 dB<br>111: -12 dB                      |
| 0x19    | CH1 - CHB1<br>IDLE Threshold | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 3:2 | IDLE tha        |      |         | Yes        | Assert threshold<br>00 = 180 mVp-p (default)<br>01 = 160 mVp-p<br>10 = 210 mVp-p<br>11 = 190 mVp-p<br>Note: override the SD_TH pin.                                |
|         |                              | 1:0 | IDLE thd        |      |         | Yes        | De-Assert threshold<br>00 = 110 mVp-p (default)<br>01 = 100 mVp-p<br>10 = 150 mVp-p<br>11 = 130 mVp-p<br>Note: override the SD_TH pin.                             |
| 0x1A    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x1B    | CH2 - CHB2<br>Signal Detect  | 7:3 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2   | SD Reset        |      |         |            | 1: Force signal detect "off"<br>0: Normal operation                                                                                                                |
|         |                              | 1   | SD Preset       |      |         |            | 1: Force signal detect "on"<br>0: Normal operation                                                                                                                 |
|         |                              | 0   | Reserved        |      |         |            | Set bit to 0.                                                                                                                                                      |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name             | Bit | Field                    | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------|---------------------------|-----|--------------------------|------|---------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1C    | CH2 - CHB2<br>IDLE, RXDET | 7:6 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                      |
|         |                           | 5   | IDLE_AUTO                |      |         | Yes        | 1 = Allow IDLE_SEL control in bit 4<br>0 = Automatic IDLE detect<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                    |
|         |                           | 4   | IDLE_SEL                 |      |         | Yes        | 1: Output is MUTED (electrical idle)<br>0: Output is ON<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                             |
|         |                           | 3:2 | RXDET                    |      |         | Yes        | 00: Input is high-z impedance<br>01: Auto RX-Detect,<br>outputs test every 12 ms for 600 ms (50 times) then stops; termination<br>is high-z until detection; once detected input termination is 50 Ω<br>10: Auto RX-Detect,<br>outputs test every 12 ms until detection occurs; termination is high-z<br>until detection; once detected input termination is 50 Ω<br>11: Input is 50 Ω<br>Note: override RXDET pin. |
|         |                           | 1:0 | Reserved                 |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0x1D    | CH2 - CHB2<br>EQ          | 7:0 | EQ Control               | R/W  | 0x2F    | Yes        | IB2 EQ Control - total of 256 levels.<br>See <a href="#">Table 2</a> .                                                                                                                                                                                                                                                                                                                                              |
| 0x1E    | CH2 - CHB2<br>VOD         | 7   | Short Circuit Protection | R/W  | 0xAD    | Yes        | 1: Enable the short circuit protection<br>0: Disable the short circuit protection                                                                                                                                                                                                                                                                                                                                   |
|         |                           | 6   | MODE_SEL                 |      |         | Yes        | 1: PCIe Gen-1 or PCIe Gen-2<br>0: PCIe Gen-3<br>Note: override the MODE pin.                                                                                                                                                                                                                                                                                                                                        |
|         |                           | 5:3 | Reserved                 |      |         | Yes        | Set bits to default value - 101.                                                                                                                                                                                                                                                                                                                                                                                    |
|         |                           | 2:0 | VOD Control              |      |         | Yes        | OB2 VOD Control<br>000: 0.7 V<br>001: 0.8 V<br>010: 0.9 V<br>011: 1.0 V<br>100: 1.1 V<br>101: 1.2 V (default)<br>110: 1.3 V<br>111: 1.4 V                                                                                                                                                                                                                                                                           |

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**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name                | Bit | Field           | Type | Default | EEPROM Bit | Description                                                                                                                                                        |
|---------|------------------------------|-----|-----------------|------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x1F    | CH2 - CHB2<br>DEM            | 7   | RXDET STATUS    | R    | 0x02    |            | Observation bit for RXDET CH2 - CHB2.<br>1: RX = detected<br>0: RX = not detected                                                                                  |
|         |                              | 6:5 | MODE_DET STATUS | R    |         |            | Observation bit for MODE_DET CH2 - CHB2.<br>00: PCIe Gen-1 (2.5G)<br>01: PCIe Gen-2 (5G)<br>11: PCIe Gen-3 (8G+)<br>Note: Only functions when MODE Pin = Automatic |
|         |                              | 4:3 | Reserved        | R/W  |         |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2:0 | DEM Control     | R/W  |         | Yes        | OB2 DEM Control<br>000: 0 dB<br>001: –1.5 dB<br>010: –3.5 dB (default)<br>011: –5 dB<br>100: –6 dB<br>101: –8 dB<br>110: –9 dB<br>111: –12 dB                      |
| 0x20    | CH2 - CHB2<br>IDLE Threshold | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 3:2 | IDLE tha        |      |         | Yes        | Assert threshold<br>00 = 180 mVp-p (default)<br>01 = 160 mVp-p<br>10 = 210 mVp-p<br>11 = 190 mVp-p<br>Note: override the SD_TH pin.                                |
|         |                              | 1:0 | IDLE thd        |      |         | Yes        | De-Assert threshold<br>00 = 110 mVp-p (default)<br>01 = 100 mVp-p<br>10 = 150 mVp-p<br>11 = 130 mVp-p<br>Note: override the SD_TH pin.                             |
| 0x21    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x22    | CH3 - CHB3<br>Signal Detect  | 7:3 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2   | SD Reset        |      |         |            | 1: Force signal detect "off"<br>0: Normal operation                                                                                                                |
|         |                              | 1   | SD Preset       |      |         |            | 1: Force signal detect "on"<br>0: Normal operation                                                                                                                 |
|         |                              | 0   | Reserved        |      |         |            | Set bit to 0.                                                                                                                                                      |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name             | Bit | Field                    | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|---------------------------|-----|--------------------------|------|---------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x23    | CH3 - CHB3<br>IDLE, RXDET | 7:6 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         |                           | 5   | IDLE_AUTO                |      |         | Yes        | 1 = Allow IDLE_SEL control in bit 4<br>0 = Automatic IDLE detect<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 4   | IDLE_SEL                 |      |         | Yes        | 1: Output is MUTED (electrical idle)<br>0: Output is ON<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                                  |
|         |                           | 3:2 | RXDET                    |      |         | Yes        | 00: Input is high-z impedance<br>01: Auto RX-Detect,<br>outputs test every 12 ms for 600 ms (50 times) then stops; termination<br>is high-z until detection; once detected input termination is 50 $\Omega$<br>10: Auto RX-Detect,<br>outputs test every 12 ms until detection occurs; termination is high-z<br>until detection; once detected input termination is 50 $\Omega$<br>11: Input is 50 $\Omega$<br>Note: override RXDET pin. |
|         |                           | 1:0 | Reserved                 |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0x24    | CH3 - CHB3<br>EQ          | 7:0 | EQ Control               | R/W  | 0x2F    | Yes        | IB3 EQ Control - total of 256 levels.<br>See <a href="#">Table 2</a> .                                                                                                                                                                                                                                                                                                                                                                   |
| 0x25    | CH3 - CHB3<br>VOD         | 7   | Short Circuit Protection | R/W  | 0xAD    | Yes        | 1: Enable the short circuit protection<br>0: Disable the short circuit protection                                                                                                                                                                                                                                                                                                                                                        |
|         |                           | 6   | MODE_SEL                 |      |         | Yes        | 1: PCIe Gen-1 or PCIe Gen-2<br>0: PCIe Gen-3<br>Note: override the MODE pin.                                                                                                                                                                                                                                                                                                                                                             |
|         |                           | 5:3 | Reserved                 |      |         | Yes        | Set bits to default value - 101.                                                                                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 2:0 | VOD Control              |      |         | Yes        | OB0 VOD Control<br>000: 0.7 V<br>001: 0.8 V<br>010: 0.9 V<br>011: 1.0 V<br>100: 1.1 V<br>101: 1.2 V (default)<br>110: 1.3 V<br>111: 1.4 V                                                                                                                                                                                                                                                                                                |

**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name                | Bit | Field           | Type | Default | EEPROM Bit | Description                                                                                                                                                        |
|---------|------------------------------|-----|-----------------|------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x26    | CH3 - CHB3<br>DEM            | 7   | RXDET STATUS    | R    | 0x02    |            | Observation bit for RXDET CH3 - CHB3.<br>1: RX = detected<br>0: RX = not detected                                                                                  |
|         |                              | 6:5 | MODE_DET STATUS | R    |         |            | Observation bit for MODE_DET CH3 - CHB3.<br>00: PCIe Gen-1 (2.5G)<br>01: PCIe Gen-2 (5G)<br>11: PCIe Gen-3 (8G+)<br>Note: Only functions when MODE Pin = Automatic |
|         |                              | 4:3 | Reserved        | R/W  |         |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2:0 | DEM Control     | R/W  |         | Yes        | OB3 DEM Control<br>000: 0 dB<br>001: -1.5 dB<br>010: -3.5 dB (default)<br>011: -5 dB<br>100: -6 dB<br>101: -8 dB<br>110: -9 dB<br>111: -12 dB                      |
| 0x27    | CH3 - CHB3<br>IDLE Threshold | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 3:2 | IDLE tha        |      |         | Yes        | Assert threshold<br>00 = 180 mVp-p (default)<br>01 = 160 mVp-p<br>10 = 210 mVp-p<br>11 = 190 mVp-p<br>Note: override the SD_TH pin.                                |
|         |                              | 1:0 | IDLE thd        |      |         | Yes        | De-Assert threshold<br>00 = 110 mVp-p (default)<br>01 = 100 mVp-p<br>10 = 150 mVp-p<br>11 = 130 mVp-p<br>Note: override the SD_TH pin.                             |
| 0x28    | Signal Detect Control        | 7:6 | Reserved        | R/W  | 0x0C    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 5:4 | High IDLE       |      |         | Yes        | Enable higher range of Signal Detect Thresholds<br>[5]: CH0 - CH3<br>[4]: CH4 -CH7                                                                                 |
|         |                              | 3:2 | Fast IDLE       |      |         | Yes        | Enable Fast OOB response<br>[3]: CH0 - CH3<br>[2]: CH4 -CH7                                                                                                        |
|         |                              | 1:0 | Reduced SD Gain |      |         | Yes        | Enable reduced Signal Detect Gain<br>[1]: CH0 - CH3<br>[0]: CH4 -CH7                                                                                               |
| 0x29    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name               | Bit | Field                    | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|-----------------------------|-----|--------------------------|------|---------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x2A    | CH4 - CHA0<br>Signal Detect | 7:3 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         |                             | 2   | SD Reset                 |      |         |            | 1: Force signal detect "off"<br>0: Normal operation                                                                                                                                                                                                                                                                                                                                                                                      |
|         |                             | 1   | SD Preset                |      |         |            | 1: Force signal detect "on"<br>0: Normal operation                                                                                                                                                                                                                                                                                                                                                                                       |
|         |                             | 0   | Reserved                 |      |         |            | Set bit to 0.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 0x2B    | CH4 - CHA0<br>IDLE, RXDET   | 7:6 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         |                             | 5   | IDLE_AUTO                |      |         | Yes        | 1 = Allow IDLE_SEL control in bit 4<br>0 = Automatic IDLE detect<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                         |
|         |                             | 4   | IDLE_SEL                 |      |         | Yes        | 1: Output is MUTED (electrical idle)<br>0: Output is ON<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                                  |
|         |                             | 3:2 | RXDET                    |      |         | Yes        | 00: Input is high-z impedance<br>01: Auto RX-Detect,<br>outputs test every 12 ms for 600 ms (50 times) then stops; termination<br>is high-z until detection; once detected input termination is 50 $\Omega$<br>10: Auto RX-Detect,<br>outputs test every 12 ms until detection occurs; termination is high-z<br>until detection; once detected input termination is 50 $\Omega$<br>11: Input is 50 $\Omega$<br>Note: override RXDET pin. |
|         |                             | 1:0 | Reserved                 |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0x2C    | CH4 - CHA0<br>EQ            | 7:0 | EQ Control               | R/W  | 0x2F    | Yes        | IA0 EQ Control - total of 256 levels.<br>See <a href="#">Table 2</a> .                                                                                                                                                                                                                                                                                                                                                                   |
| 0x2D    | CH4 - CHA0<br>VOD           | 7   | Short Circuit Protection | R/W  | 0xAD    | Yes        | 1: Enable the short circuit protection<br>0: Disable the short circuit protection                                                                                                                                                                                                                                                                                                                                                        |
|         |                             | 6   | MODE_SEL                 |      |         | Yes        | 1: PCIe Gen-1 or PCIe Gen-2<br>0: PCIe Gen-3<br>Note: override the MODE pin.                                                                                                                                                                                                                                                                                                                                                             |
|         |                             | 5:3 | Reserved                 |      |         | Yes        | Set bits to default value - 101.                                                                                                                                                                                                                                                                                                                                                                                                         |
|         |                             | 2:0 | VOD Control              |      |         | Yes        | OA0 VOD Control<br>000: 0.7 V<br>001: 0.8 V<br>010: 0.9 V<br>011: 1.0 V<br>100: 1.1 V<br>101: 1.2 V (default)<br>110: 1.3 V<br>111: 1.4 V                                                                                                                                                                                                                                                                                                |

**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name                | Bit | Field           | Type | Default | EEPROM Bit | Description                                                                                                                                                        |
|---------|------------------------------|-----|-----------------|------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x2E    | CH4 - CHA0<br>DEM            | 7   | RXDET STATUS    | R    | 0x02    |            | Observation bit for RXDET CH4 - CHA0.<br>1: RX = detected<br>0: RX = not detected                                                                                  |
|         |                              | 6:5 | MODE_DET STATUS | R    |         |            | Observation bit for MODE_DET CH4 - CHA0.<br>00: PCIe Gen-1 (2.5G)<br>01: PCIe Gen-2 (5G)<br>11: PCIe Gen-3 (8G+)<br>Note: Only functions when MODE Pin = Automatic |
|         |                              | 4:3 | Reserved        | R/W  |         |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2:0 | DEM Control     | R/W  |         | Yes        | OA0 DEM Control<br>000: 0 dB<br>001: –1.5 dB<br>010: –3.5 dB (default)<br>011: –5 dB<br>100: –6 dB<br>101: –8 dB<br>110: –9 dB<br>111: –12 dB                      |
| 0x2F    | CH4 - CHA0<br>IDLE Threshold | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 3:2 | IDLE tha        |      |         | Yes        | Assert threshold<br>00 = 180 mVp-p (default)<br>01 = 160 mVp-p<br>10 = 210 mVp-p<br>11 = 190 mVp-p<br>Note: override the SD_TH pin.                                |
|         |                              | 1:0 | IDLE thd        |      |         | Yes        | De-Assert threshold<br>00 = 110 mVp-p (default)<br>01 = 100 mVp-p<br>10 = 150 mVp-p<br>11 = 130 mVp-p<br>Note: override the SD_TH pin.                             |
| 0x30    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x31    | CH5 - CHA1<br>Signal Detect  | 7:3 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2   | SD Reset        |      |         |            | 1: Force signal detect "off"<br>0: Normal operation                                                                                                                |
|         |                              | 1   | SD Preset       |      |         |            | 1: Force signal detect "on"<br>0: Normal operation                                                                                                                 |
|         |                              | 0   | Reserved        |      |         |            | Set bit to 0.                                                                                                                                                      |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name             | Bit | Field                    | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|---------------------------|-----|--------------------------|------|---------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x32    | CH5 - CHA1<br>IDLE, RXDET | 7:6 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         |                           | 5   | IDLE_AUTO                |      |         | Yes        | 1 = Allow IDLE_SEL control in bit 4<br>0 = Automatic IDLE detect<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 4   | IDLE_SEL                 |      |         | Yes        | 1: Output is MUTED (electrical idle)<br>0: Output is ON<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                                  |
|         |                           | 3:2 | RXDET                    |      |         | Yes        | 00: Input is high-z impedance<br>01: Auto RX-Detect,<br>outputs test every 12 ms for 600 ms (50 times) then stops; termination<br>is high-z until detection; once detected input termination is 50 $\Omega$<br>10: Auto RX-Detect,<br>outputs test every 12 ms until detection occurs; termination is high-z<br>until detection; once detected input termination is 50 $\Omega$<br>11: Input is 50 $\Omega$<br>Note: override RXDET pin. |
|         |                           | 1:0 | Reserved                 |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0x33    | CH5 - CHA1<br>EQ          | 7:0 | EQ Control               | R/W  | 0x2F    | Yes        | IA1 EQ Control - total of 256 levels.<br>See <a href="#">Table 2</a> .                                                                                                                                                                                                                                                                                                                                                                   |
| 0x34    | CH5 - CHA1<br>VOD         | 7   | Short Circuit Protection | R/W  | 0xAD    | Yes        | 1: Enable the short circuit protection<br>0: Disable the short circuit protection                                                                                                                                                                                                                                                                                                                                                        |
|         |                           | 6   | MODE_SEL                 |      |         | Yes        | 1: PCIe Gen-1 or PCIe Gen-2<br>0: PCIe Gen-3<br>Note: override the MODE pin.                                                                                                                                                                                                                                                                                                                                                             |
|         |                           | 5:3 | Reserved                 |      |         | Yes        | Set bits to default value - 101.                                                                                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 2:0 | VOD Control              |      |         | Yes        | OA1 VOD Control<br>000: 0.7 V<br>001: 0.8 V<br>010: 0.9 V<br>011: 1.0 V<br>100: 1.1 V<br>101: 1.2 V (default)<br>110: 1.3 V<br>111: 1.4 V                                                                                                                                                                                                                                                                                                |

**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name                | Bit | Field           | Type | Default | EEPROM Bit | Description                                                                                                                                                        |
|---------|------------------------------|-----|-----------------|------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x35    | CH5 - CHA1<br>DEM            | 7   | RXDET STATUS    | R    | 0x02    |            | Observation bit for RXDET CH5 - CHA1.<br>1: RX = detected<br>0: RX = not detected                                                                                  |
|         |                              | 6:5 | MODE_DET STATUS | R    |         |            | Observation bit for MODE_DET CH5 - CHA1.<br>00: PCIe Gen-1 (2.5G)<br>01: PCIe Gen-2 (5G)<br>11: PCIe Gen-3 (8G+)<br>Note: Only functions when MODE Pin = Automatic |
|         |                              | 4:3 | Reserved        | R/W  |         |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2:0 | DEM Control     | R/W  |         | Yes        | OA1 DEM Control<br>000: 0 dB<br>001: -1.5 dB<br>010: -3.5 dB (default)<br>011: -5 dB<br>100: -6 dB<br>101: -8 dB<br>110: -9 dB<br>111: -12 dB                      |
| 0x36    | CH5 - CHA1<br>IDLE Threshold | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 3:2 | IDLE tha        |      |         | Yes        | Assert threshold<br>00 = 180 mVp-p (default)<br>01 = 160 mVp-p<br>10 = 210 mVp-p<br>11 = 190 mVp-p<br>Note: override the SD_TH pin.                                |
|         |                              | 1:0 | IDLE thd        |      |         | Yes        | De-Assert threshold<br>00 = 110 mVp-p (default)<br>01 = 100 mVp-p<br>10 = 150 mVp-p<br>11 = 130 mVp-p<br>Note: override the SD_TH pin.                             |
| 0x37    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x38    | CH6 - CHA2<br>Signal Detect  | 7:3 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2   | SD Reset        |      |         |            | 1: Force signal detect "off"<br>0: Normal operation                                                                                                                |
|         |                              | 1   | SD Preset       |      |         |            | 1: Force signal detect "on"<br>0: Normal operation                                                                                                                 |
|         |                              | 0   | Reserved        |      |         |            | Set bit to 0.                                                                                                                                                      |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name             | Bit | Field                    | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|---------------------------|-----|--------------------------|------|---------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x39    | CH6 - CHA2<br>IDLE, RXDET | 7:6 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         |                           | 5   | IDLE_AUTO                |      |         | Yes        | 1 = Allow IDLE_SEL control in bit 4<br>0 = Automatic IDLE detect<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 4   | IDLE_SEL                 |      |         | Yes        | 1: Output is MUTED (electrical idle)<br>0: Output is ON<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                                  |
|         |                           | 3:2 | RXDET                    |      |         | Yes        | 00: Input is high-z impedance<br>01: Auto RX-Detect,<br>outputs test every 12 ms for 600 ms (50 times) then stops; termination<br>is high-z until detection; once detected input termination is 50 $\Omega$<br>10: Auto RX-Detect,<br>outputs test every 12 ms until detection occurs; termination is high-z<br>until detection; once detected input termination is 50 $\Omega$<br>11: Input is 50 $\Omega$<br>Note: override RXDET pin. |
|         |                           | 1:0 | Reserved                 |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0x3A    | CH6 - CHA2<br>EQ          | 7:0 | EQ Control               | R/W  | 0x2F    | Yes        | IA2 EQ Control - total of 256 levels.<br>See <a href="#">Table 2</a> .                                                                                                                                                                                                                                                                                                                                                                   |
| 0x3B    | CH6 - CHA2<br>VOD         | 7   | Short Circuit Protection | R/W  | 0xAD    | Yes        | 1: Enable the short circuit protection<br>0: Disable the short circuit protection                                                                                                                                                                                                                                                                                                                                                        |
|         |                           | 6   | MODE_SEL                 |      |         | Yes        | 1: PCIe Gen-1 or PCIe Gen-2<br>0: PCIe Gen-3<br>Note: override the MODE pin.                                                                                                                                                                                                                                                                                                                                                             |
|         |                           | 5:3 | Reserved                 |      |         | Yes        | Set bits to default value - 101.                                                                                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 2:0 | VOD Control              |      |         | Yes        | OA2 VOD Control<br>000: 0.7 V<br>001: 0.8 V<br>010: 0.9 V<br>011: 1.0 V<br>100: 1.1 V<br>101: 1.2 V (default)<br>110: 1.3 V<br>111: 1.4 V                                                                                                                                                                                                                                                                                                |

**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name                | Bit | Field           | Type | Default | EEPROM Bit | Description                                                                                                                                                        |
|---------|------------------------------|-----|-----------------|------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x3C    | CH6 - CHA2<br>DEM            | 7   | RXDET STATUS    | R    | 0x02    |            | Observation bit for RXDET CH6 - CHA2.<br>1: RX = detected<br>0: RX = not detected                                                                                  |
|         |                              | 6:5 | MODE_DET STATUS | R    |         |            | Observation bit for MODE_DET CH6 - CHA2.<br>00: PCIe Gen-1 (2.5G)<br>01: PCIe Gen-2 (5G)<br>11: PCIe Gen-3 (8G+)<br>Note: Only functions when MODE Pin = Automatic |
|         |                              | 4:3 | Reserved        | R/W  |         |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2:0 | DEM Control     | R/W  |         | Yes        | OA2 DEM Control<br>000: 0 dB<br>001: -1.5 dB<br>010: -3.5 dB (default)<br>011: -5 dB<br>100: -6 dB<br>101: -8 dB<br>110: -9 dB<br>111: -12 dB                      |
| 0x3D    | CH6 - CHA2<br>IDLE Threshold | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 3:2 | IDLE tha        |      |         | Yes        | Assert threshold<br>00 = 180 mVp-p (default)<br>01 = 160 mVp-p<br>10 = 210 mVp-p<br>11 = 190 mVp-p<br>Note: override the SD_TH pin.                                |
|         |                              | 1:0 | IDLE thd        |      |         | Yes        | De-Assert threshold<br>00 = 110 mVp-p (default)<br>01 = 100 mVp-p<br>10 = 150 mVp-p<br>11 = 130 mVp-p<br>Note: override the SD_TH pin.                             |
| 0x3E    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x3F    | CH0 - CHB0<br>Signal Detect  | 7:3 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2   | SD Reset        |      |         |            | 1: Force signal detect "off"<br>0: Normal operation                                                                                                                |
|         |                              | 1   | SD Preset       |      |         |            | 1: Force signal detect "on"<br>0: Normal operation                                                                                                                 |
|         |                              | 0   | Reserved        |      |         |            | Set bit to 0.                                                                                                                                                      |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name             | Bit | Field                    | Type | Default | EEPROM Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|---------------------------|-----|--------------------------|------|---------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x40    | CH7 - CHA3<br>IDLE, RXDET | 7:6 | Reserved                 | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         |                           | 5   | IDLE_AUTO                |      |         | Yes        | 1 = Allow IDLE_SEL control in bit 4<br>0 = Automatic IDLE detect<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 4   | IDLE_SEL                 |      |         | Yes        | 1: Output is MUTED (electrical idle)<br>0: Output is ON<br>Note: override IDLE control.                                                                                                                                                                                                                                                                                                                                                  |
|         |                           | 3:2 | RXDET                    |      |         | Yes        | 00: Input is high-z impedance<br>01: Auto RX-Detect,<br>outputs test every 12 ms for 600 ms (50 times) then stops; termination<br>is high-z until detection; once detected input termination is 50 $\Omega$<br>10: Auto RX-Detect,<br>outputs test every 12 ms until detection occurs; termination is high-z<br>until detection; once detected input termination is 50 $\Omega$<br>11: Input is 50 $\Omega$<br>Note: override RXDET pin. |
|         |                           | 1:0 | Reserved                 |      |         |            | Set bits to 0.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0x41    | CH7 - CHA3<br>EQ          | 7:0 | EQ Control               | R/W  | 0x2F    | Yes        | IA3 EQ Control - total of 256 levels.<br>See <a href="#">Table 2</a> .                                                                                                                                                                                                                                                                                                                                                                   |
| 0x42    | CH7 - CHA3<br>VOD         | 7   | Short Circuit Protection | R/W  | 0xAD    | Yes        | 1: Enable the short circuit protection<br>0: Disable the short circuit protection                                                                                                                                                                                                                                                                                                                                                        |
|         |                           | 6   | MODE_SEL                 |      |         | Yes        | 1: PCIe Gen-1 or PCIe Gen-2<br>0: PCIe Gen-3<br>Note: override the MODE pin.                                                                                                                                                                                                                                                                                                                                                             |
|         |                           | 5:3 | Reserved                 |      |         | Yes        | Set bits to default value - 101.                                                                                                                                                                                                                                                                                                                                                                                                         |
|         |                           | 2:0 | VOD Control              |      |         | Yes        | OA3 VOD Control<br>000: 0.7 V<br>001: 0.8 V<br>010: 0.9 V<br>011: 1.0 V<br>100: 1.1 V<br>101: 1.2 V (default)<br>110: 1.3 V<br>111: 1.4 V                                                                                                                                                                                                                                                                                                |

**Register Maps (continued)**
**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name                | Bit | Field           | Type | Default | EEPROM Bit | Description                                                                                                                                                        |
|---------|------------------------------|-----|-----------------|------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x43    | CH7 - CHA3<br>DEM            | 7   | RXDET STATUS    | R    | 0x02    |            | Observation bit for RXDET CH7 - CHA3.<br>1: RX = detected<br>0: RX = not detected                                                                                  |
|         |                              | 6:5 | MODE_DET STATUS | R    |         |            | Observation bit for MODE_DET CH7 - CHA3.<br>00: PCIe Gen-1 (2.5G)<br>01: PCIe Gen-2 (5G)<br>11: PCIe Gen-3 (8G+)<br>Note: Only functions when MODE Pin = Automatic |
|         |                              | 4:3 | Reserved        | R/W  |         |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 2:0 | DEM Control     | R/W  |         | Yes        | OA3 DEM Control<br>000: 0 dB<br>001: -1.5 dB<br>010: -3.5 dB (default)<br>011: -5 dB<br>100: -6 dB<br>101: -8 dB<br>110: -9 dB<br>111: -12 dB                      |
| 0x44    | CH7 - CHA3<br>IDLE Threshold | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0.                                                                                                                                                     |
|         |                              | 3:2 | IDLE tha        |      |         | Yes        | Assert threshold<br>00 = 180 mVp-p (default)<br>01 = 160 mVp-p<br>10 = 210 mVp-p<br>11 = 190 mVp-p<br>Note: override the SD_TH pin.                                |
|         |                              | 1:0 | IDLE thd        |      |         | Yes        | De-Assert threshold<br>00 = 110 mVp-p (default)<br>01 = 100 mVp-p<br>10 = 150 mVp-p<br>11 = 130 mVp-p<br>Note: override the SD_TH pin.                             |
| 0x45    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x46    | Reserved                     | 7:0 | Reserved        | R/W  | 0x38    |            | Set bits to 0x38                                                                                                                                                   |
| 0x47    | Reserved                     | 7:4 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
|         |                              | 3:0 | Reserved        | R/W  |         | Yes        | Set bits to 0                                                                                                                                                      |
| 0x48    | Reserved                     | 7:6 | Reserved        | R/W  | 0x05    | Yes        | Set bits to 0                                                                                                                                                      |
|         |                              | 5:0 | Reserved        | R/W  |         |            | Set bits to 00 0101'b                                                                                                                                              |
| 0x49    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x4A    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |
| 0x4B    | Reserved                     | 7:0 | Reserved        | R/W  | 0x00    |            | Set bits to 0                                                                                                                                                      |

## Register Maps (continued)

**Table 10. SMBUS Slave Mode Register Map (continued)**

| Address | Register Name | Bit | Field    | Type | Default | EEPROM Bit | Description      |
|---------|---------------|-----|----------|------|---------|------------|------------------|
| 0x4C    | Reserved      | 7:3 | Reserved | R/W  | 0x00    | Yes        | Set bits to 0    |
|         |               | 2:1 | Reserved | R/W  |         |            | Set bits to 0    |
|         |               | 0   | Reserved | R/W  |         | Yes        | Set bits to 0    |
| 0x4D    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x4E    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x4F    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x50    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x51    | Device ID     | 7:5 | VERSION  | R    | 0x45    |            | 010'b            |
|         |               | 4:0 | ID       |      |         |            | 00101'b          |
| 0x52    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x53    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x54    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x55    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x56    | Reserved      | 7:0 | Reserved | R/W  | 0x10    |            | Set bits to 0x10 |
| 0x57    | Reserved      | 7:0 | Reserved | R/W  | 0x64    |            | Set bits to 0x64 |
| 0x58    | Reserved      | 7:0 | Reserved | R/W  | 0x21    |            | Set bits to 0x21 |
| 0x59    | Reserved      | 7:1 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
|         |               | 0   | Reserved |      |         | Yes        | Set bit to 0     |
| 0x5A    | Reserved      | 7:0 | Reserved | R/W  | 0x54    | Yes        | Set bits to 0x54 |
| 0x5B    | Reserved      | 7:0 | Reserved | R/W  | 0x54    | Yes        | Set bits to 0x54 |
| 0x5C    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x5D    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x5E    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x5F    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x60    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |
| 0x61    | Reserved      | 7:0 | Reserved | R/W  | 0x00    |            | Set bits to 0    |

## 9 Application and Implementation

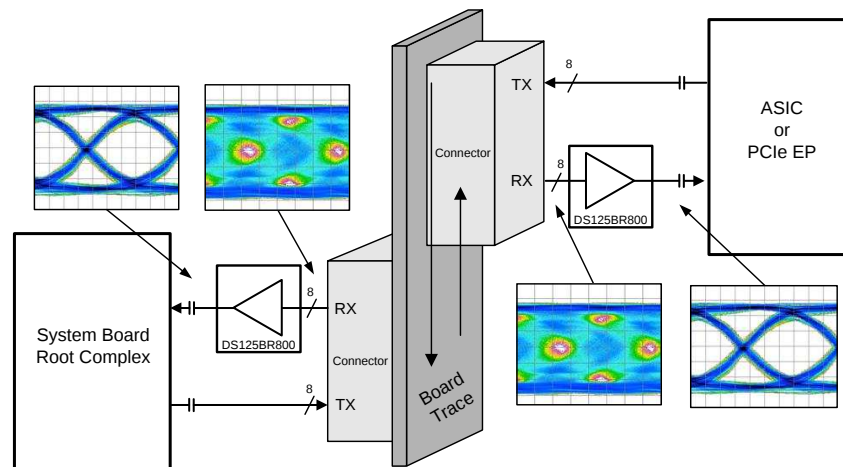
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The DS125BR800 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to [Layout Guidelines](#) and the *LVDS Owner's Manual*, [SNLA187](#), for more detailed information on high speed design tips to address signal integrity design issues.

### 9.2 Typical Application



**Figure 9. Typical Application**

#### 9.2.1 Design Requirements

As with any high speed design, there are many factors which influence the overall performance. Below are a list of critical areas for consideration and study during design.

- Use 100  $\Omega$  impedance traces. Generally these are very loosely coupled to ease routing length differences.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- The maximum body size for AC-coupling capacitors is 0402.
- Back-drill connector vias and signal vias to minimize stub length.
- Use Reference plane vias to ensure a low inductance path for the return current.

#### 9.2.2 Detailed Design Procedure

The DS125BR800 is designed to be placed at a location where the input CTLE can help to compensate for a portion of the overall channel attenuation. In order to optimize performance, the repeater requires tuning to extend the reach of the cable or trace length while also recovering a solid eye opening. To tune the repeater, the settings mentioned in [Table 2](#) and [Table 3](#) (for Pin Mode) are recommended as a default starting point for most applications. Once these settings are configured, additional tuning of the EQ and, to a lesser extent, VOD may be required to optimize the repeater performance for each specific application environment. Examples of the repeater performance as a generic high speed datapath repeater are illustrated in the performance curves in the next section.

## Typical Application (continued)

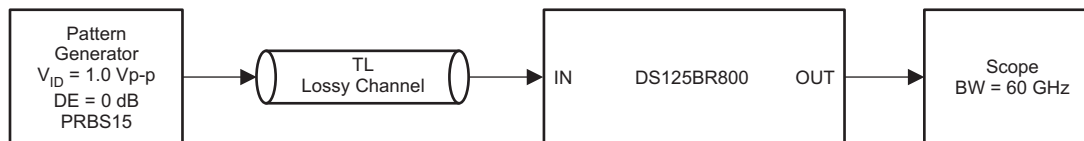
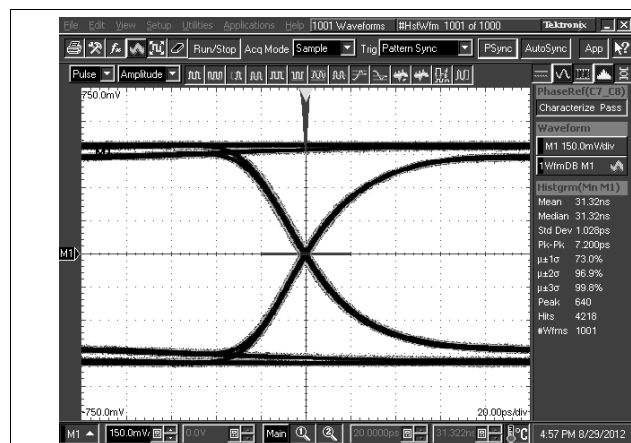


Figure 10. Test Setup Connections Diagram

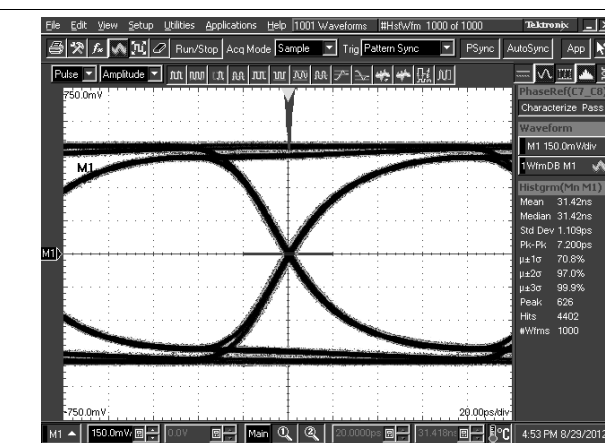


Figure 11. Test Setup Connections Diagram

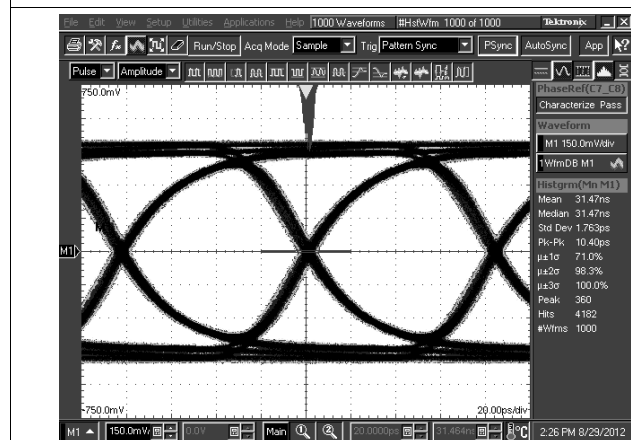
## 9.2.3 Application Curves



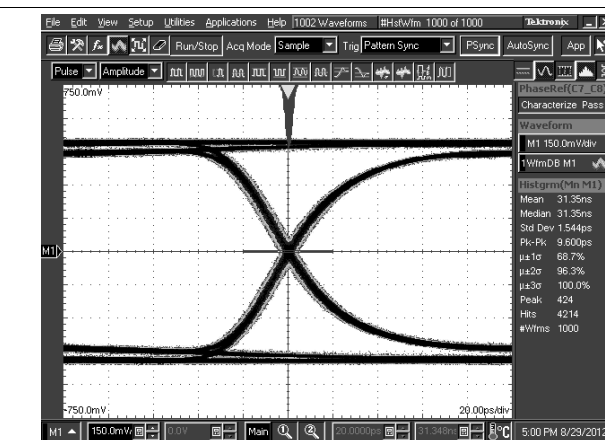
DS125BR800 settings: EQ[1:0] = 0, F = 0x02, DEM[1:0] = 0, 1  
Figure 12. TL = 10 inch 5-mil FR4 trace, 5 Gbps



DS125BR800 settings: EQ[1:0] = 0, F = 0x02, DEM[1:0] = 0, 1  
Figure 13. TL = 10 inch 5-mil FR4 trace, 8 Gbps



DS125BR800 settings: EQ[1:0] = 0, R = 0x01, DEM[1:0] = 0, 1  
Figure 14. TL = 10 inch 5-mil FR4 trace, 12 Gbps



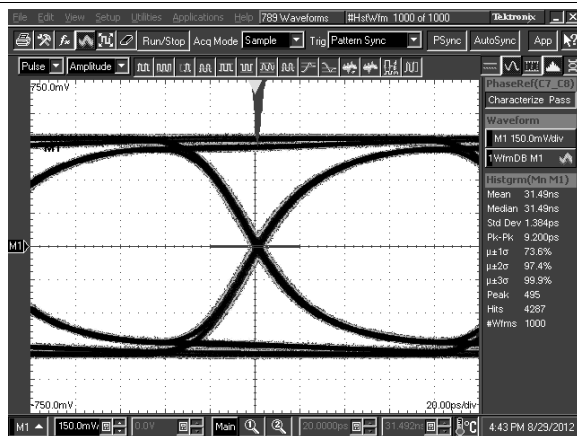
DS125BR800 settings: EQ[1:0] = 0, 1 = 0x03, DEM[1:0] = 0, 1  
Figure 15. TL = 20 inch 5-mil FR4 trace, 5 Gbps

## DS125BR800

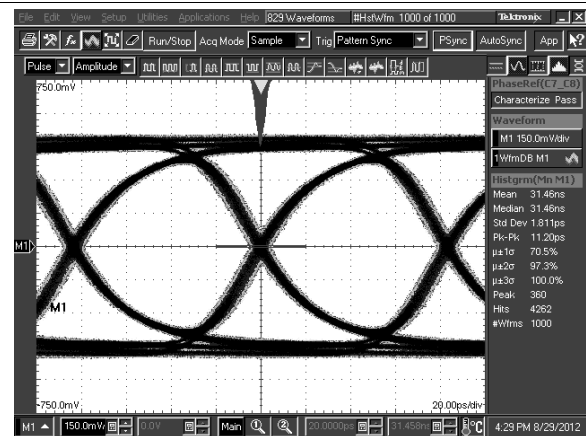
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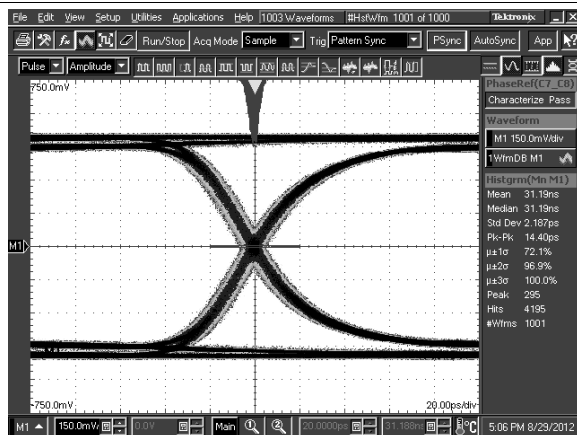
### Typical Application (continued)



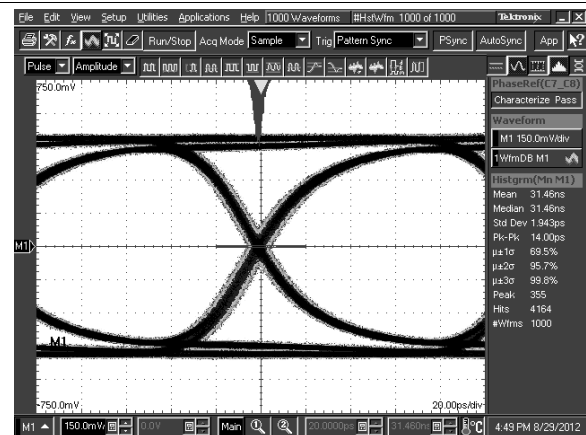
DS125BR800 settings: EQ[1:0] = 0, 1 = 0x03, DEM[1:0] = 0, 1  
Figure 16. TL = 20 inch 5-mil FR4 trace, 8 Gbps



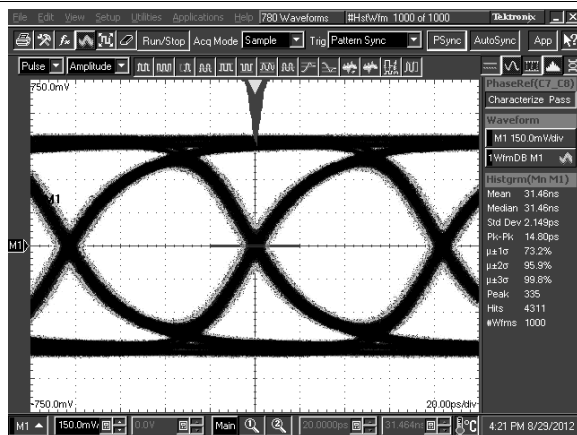
DS125BR800 settings: EQ[1:0] = 0, 1 = 0x03, DEM[1:0] = 0, 1  
Figure 17. TL = 20 inch 5-mil FR4 trace, 12 Gbps



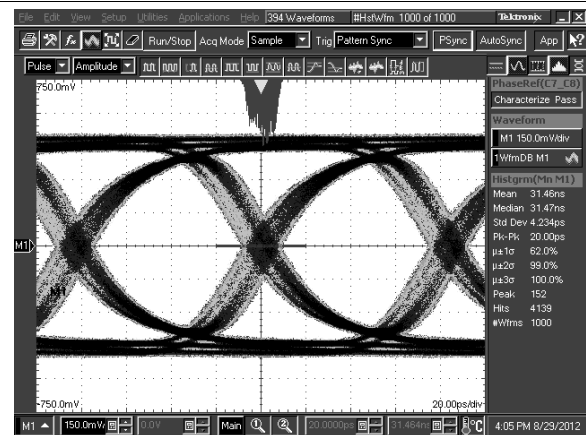
DS125BR800 settings: EQ[1:0] = R, 0 = 0x07, DEM[1:0] = 0, 1  
Figure 18. TL = 30 inch 5-mil FR4 trace, 5 Gbps



DS125BR800 settings: EQ[1:0] = R, 0 = 0x07, DEM[1:0] = 0, 1  
Figure 19. TL = 30 inch 5-mil FR4 trace, 8 Gbps

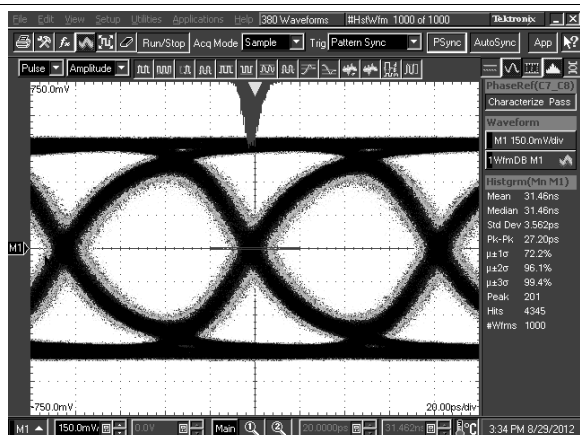


DS125BR800 settings: EQ[1:0] = R, 0 = 0x07, DEM[1:0] = 0, 1  
Figure 20. TL = 30 inch 5-mil FR4 trace, 12 Gbps

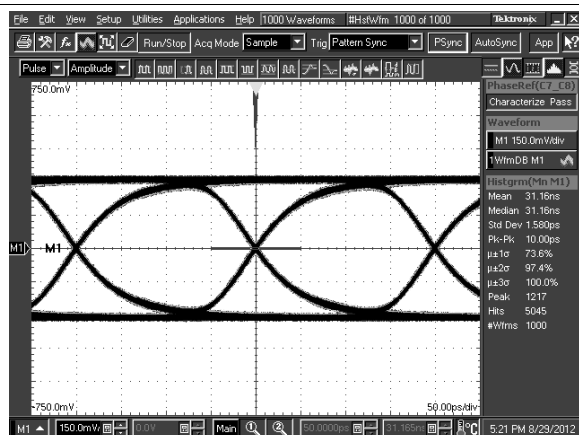


DS125BR800 settings: EQ[1:0] = R, 0 = 0x07, DEM[1:0] = 0, 1  
Figure 21. TL1 = 5-meter 30-AWG 100 Ω Twin-axial Cable, 12 Gbps

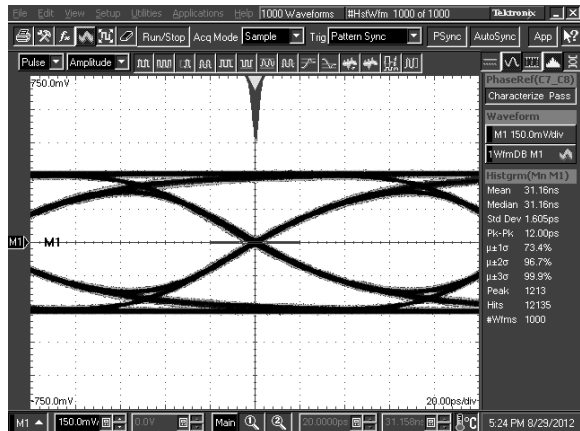
## Typical Application (continued)



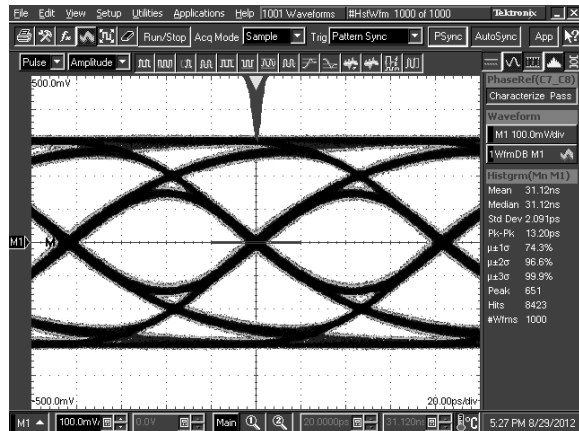
DS125BR800 settings: EQ[1:0] = R, 1 = 0x0F, DEM[1:0] = 0, 1  
Figure 22. TL1 = 8-meter 30-AWG 100  $\Omega$  Twin-axial Cable, 12 Gbps



DS125BR800 settings: EQ[1:0] = 0, 1 = 0x03, DEM[1:0] = R, 0  
Figure 23. TL1 = 20 inch 5-mil FR4 trace, TL2 = 10 inch 5-mil FR4 trace, 5 Gbps



DS125BR800 settings: EQ[1:0] = R, 1 = 0x0F, DEM[1:0] = R, 0  
Figure 24. TL1 = 20 inch 5-mil FR4 trace, TL2 = 10 inch 5-mil FR4 trace, 8 Gbps



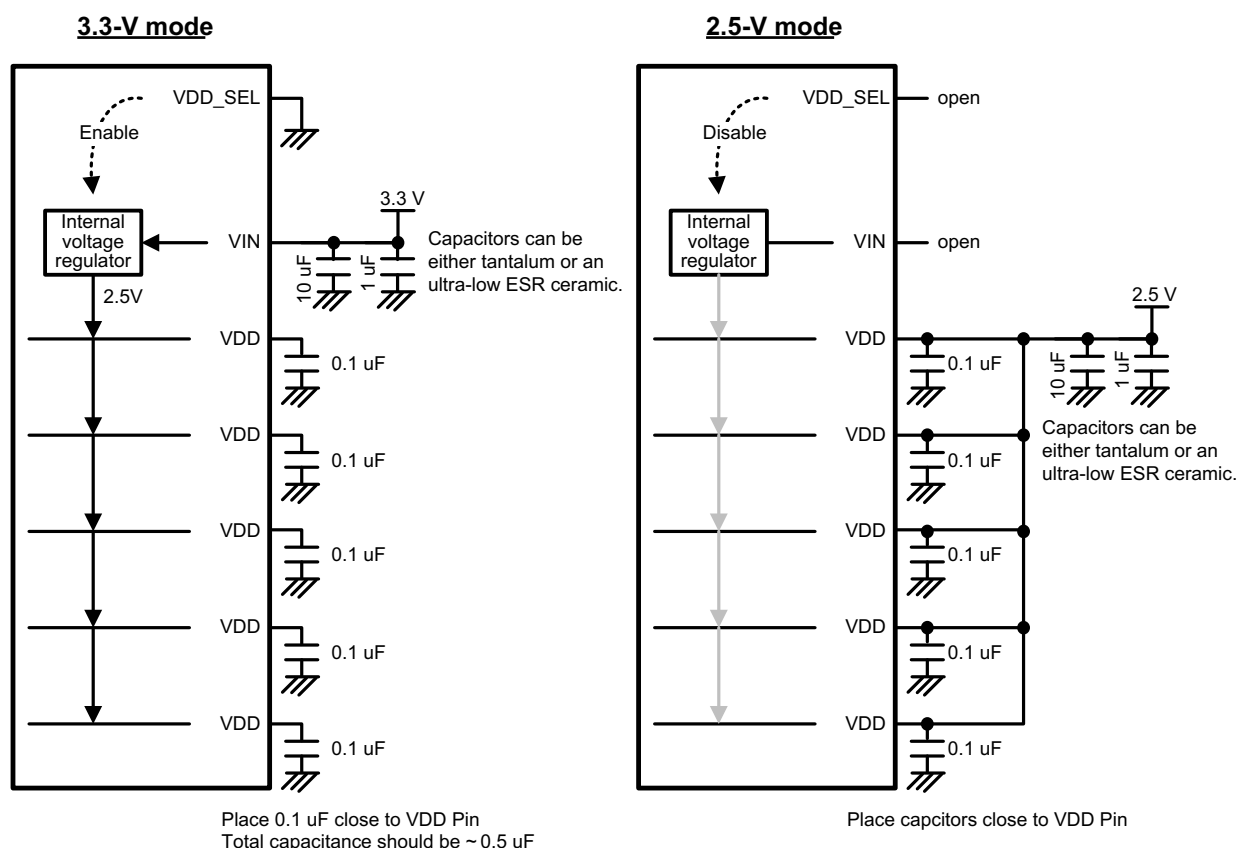
DS125BR800 settings: EQ[1:0] = R, 1 = 0x0F, DEM[1:0] = R, 0  
Figure 25. TL1 = 20 inch 5-mil FR4 trace, TL2 = 10 inch 5-mil FR4 trace, 12 Gbps

## 10 Power Supply Recommendations

### 10.1 3.3-V or 2.5-V Supply Mode Operation

The DS125BR800 has an optional internal voltage regulator to provide the 2.5-V supply to the device. In 3.3-V mode operation, the VIN pin = 3.3 V is used to supply power to the device. The internal regulator will provide the 2.5 V to the VDD pins of the device and a 0.1- $\mu$ F cap is needed at each of the 5 VDD pins for power supply decoupling (total capacitance should be  $\leq 0.5 \mu\text{F}$ ), and the VDD\_SEL pin must be tied to GND to enable the internal regulator. In 2.5-V mode operation, the VIN pin should be left open and 2.5-V supply must be applied to the 5 VDD pins to power the device. The VDD\_SEL pin must be left open (no connect) to disable the internal regulator.

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**Figure 26. 3.3-V or 2.5-V Supply Connection Diagram**

## 10.2 Power Supply Bypassing

Two approaches are recommended to ensure that the DS125BR800 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1- $\mu$ F bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the DS125BR800. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1  $\mu$ F to 10  $\mu$ F should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

## 11 Layout

### 11.1 Layout Guidelines

The CML inputs and LPDS outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100  $\Omega$ . It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

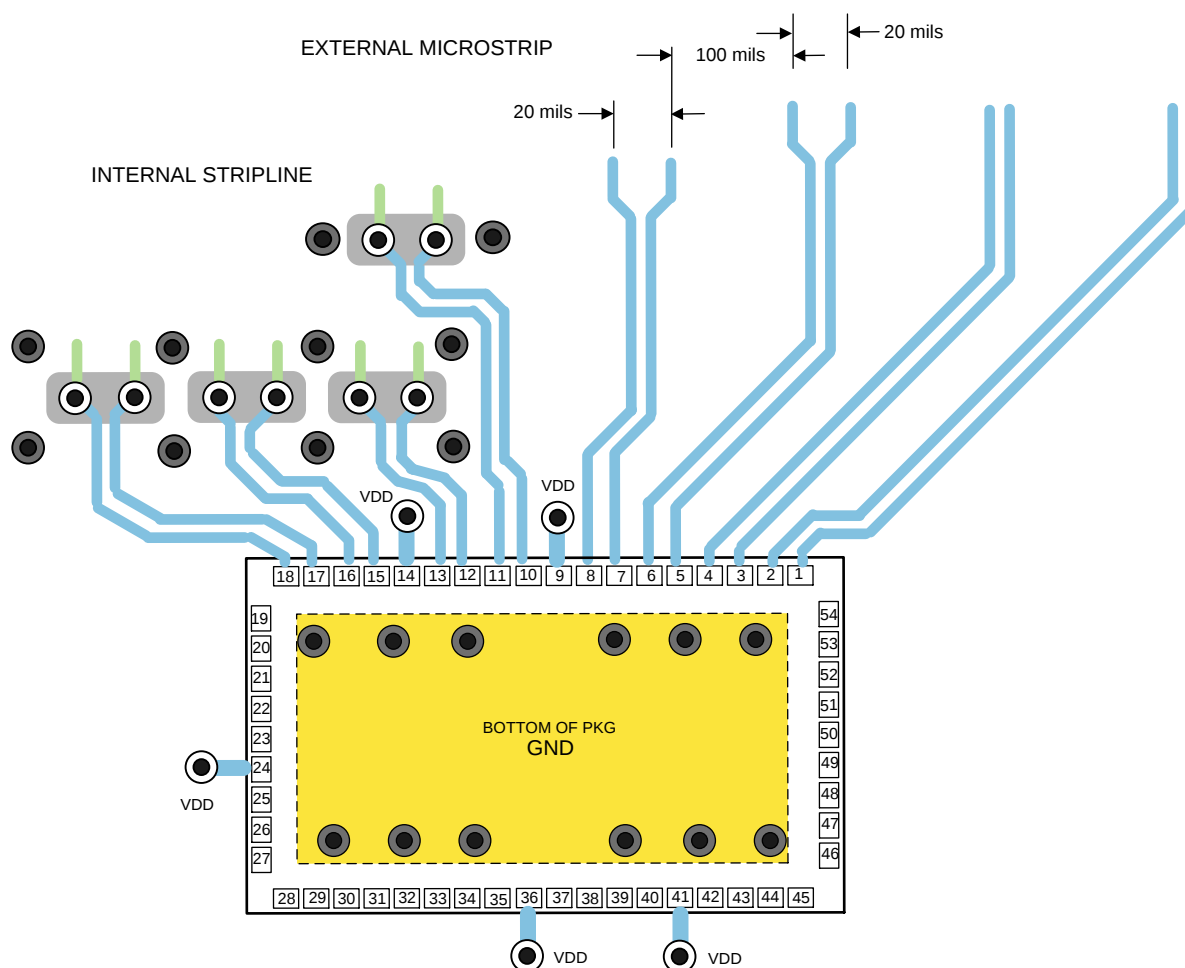
[Figure 27](#) depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high frequency effects of stubs on the signal path.

## DS125BR800

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www.ti.com.cn

### 11.2 Layout Example



**Figure 27. Typical Routing Options**

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

- 《焊接的绝对最大额定值》(SNOA549)
- 《LVDS 用户手册》(SNLA187)
- 《了解高速中继器和复用缓冲器的 *EEPROM* 编程》(SNLA228)

### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.3 商标

All trademarks are the property of their respective owners.

### 12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.5 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DS125BR800SQ/NOPB</a>  | Active        | Production           | WQFN (NJY)   54 | 2000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | DS125BR800SQ        |
| DS125BR800SQ/NOPB.A                | Active        | Production           | WQFN (NJY)   54 | 2000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | DS125BR800SQ        |
| DS125BR800SQ/NOPB.B                | Active        | Production           | WQFN (NJY)   54 | 2000   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | DS125BR800SQ        |
| <a href="#">DS125BR800SQE/NOPB</a> | Active        | Production           | WQFN (NJY)   54 | 250   SMALL T&R       | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | DS125BR800SQ        |
| DS125BR800SQE/NOPB.A               | Active        | Production           | WQFN (NJY)   54 | 250   SMALL T&R       | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | DS125BR800SQ        |
| DS125BR800SQE/NOPB.B               | Active        | Production           | WQFN (NJY)   54 | 250   SMALL T&R       | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 85    | DS125BR800SQ        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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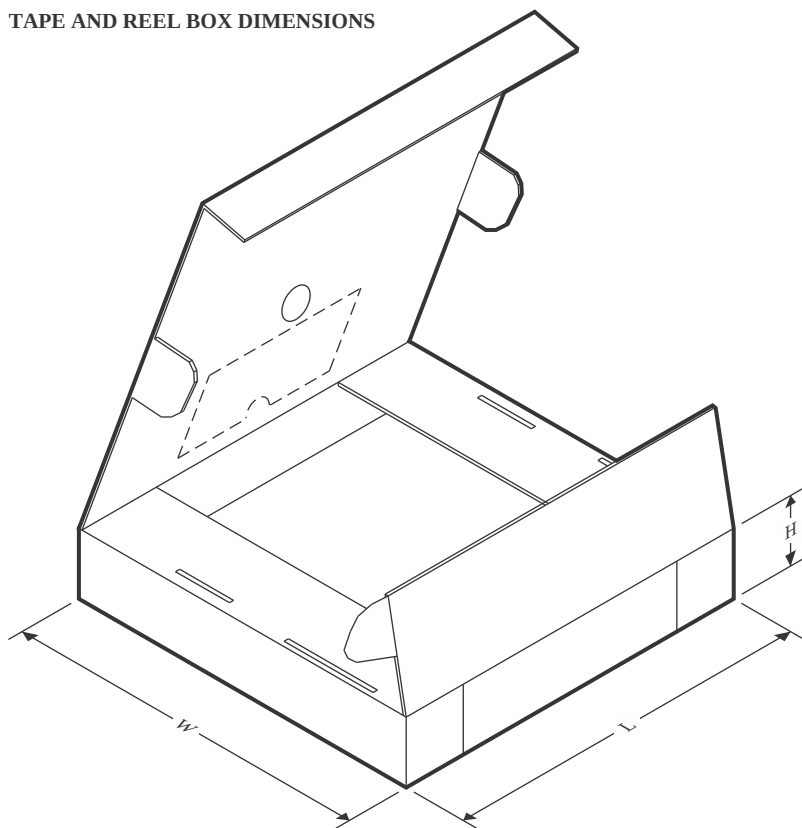
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS125BR800SQ/NOPB  | WQFN         | NJY             | 54   | 2000 | 330.0              | 16.4               | 5.8     | 10.3    | 1.0     | 12.0    | 16.0   | Q1            |
| DS125BR800SQE/NOPB | WQFN         | NJY             | 54   | 250  | 178.0              | 16.4               | 5.8     | 10.3    | 1.0     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



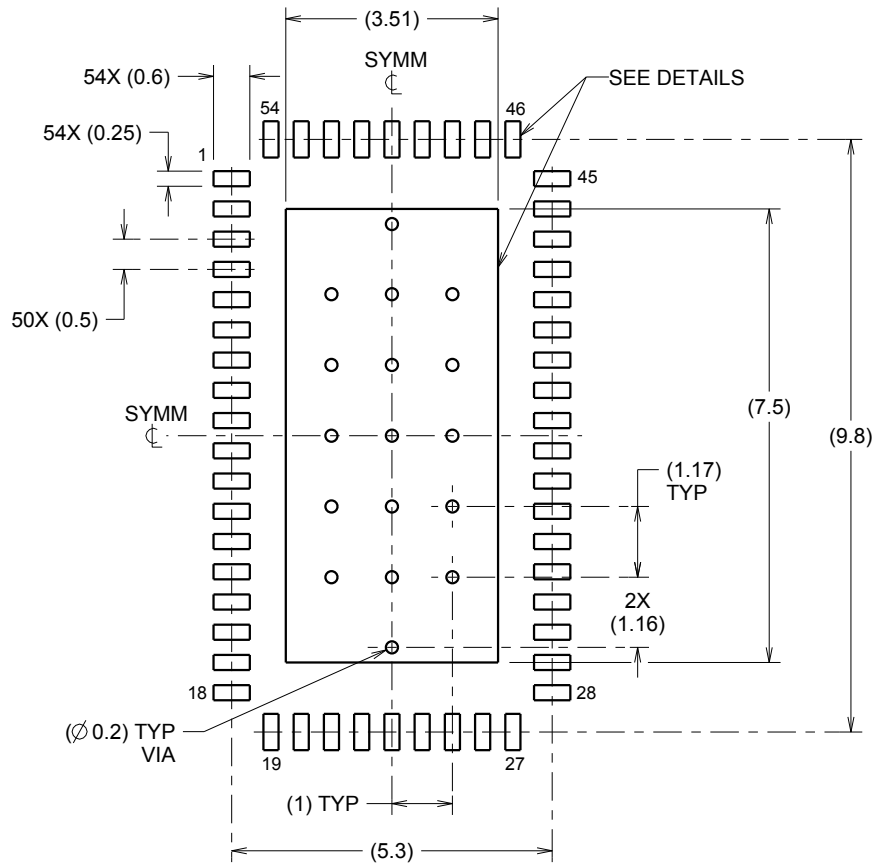
\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS125BR800SQ/NOPB  | WQFN         | NJY             | 54   | 2000 | 356.0       | 356.0      | 36.0        |
| DS125BR800SQE/NOPB | WQFN         | NJY             | 54   | 250  | 208.0       | 191.0      | 35.0        |

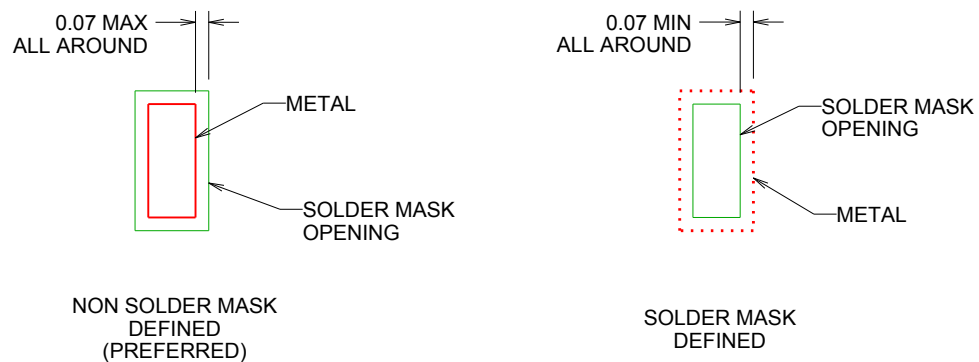
WQFN

[illegible]

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.  
2. This drawing is subject to change without notice.  
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE  
SCALE:8X

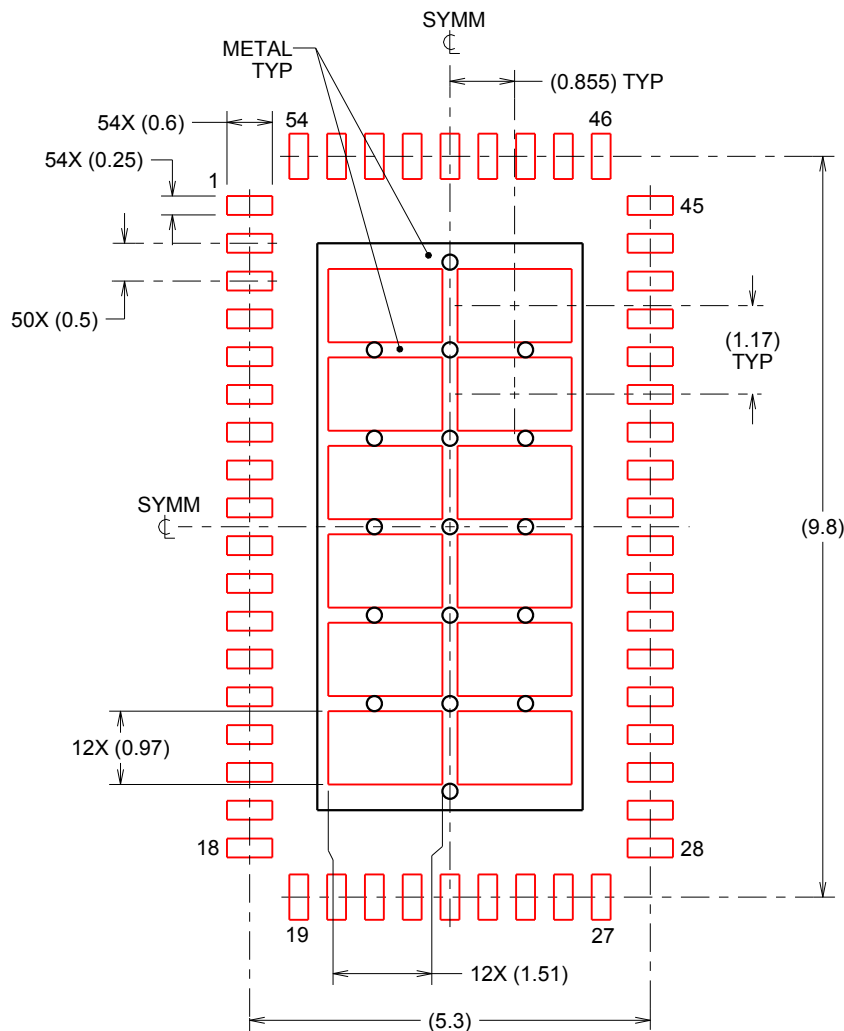


SOLDER MASK DETAILS

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NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).



**SOLDERPASTE EXAMPLE**  
 BASED ON 0.125mm THICK STENCIL

EXPOSED PAD  
 67% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:10X

4214993/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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