DRV8816 DMOS 双路 1/2 H 桥电机驱动器

1 特性

- 独立的 H 桥电机驱动器
  - 驱动一个直流电机或其它负载
  - 低 $R_{DS(on)}$ MOSFET（典型值 0.4Ω）
- 低功耗睡眠模式
- 支持 100% PWM
- 工作电源电压范围为 8V 至 38V
- 耐热增强型表面贴装封装
- 可配置过流限制
- 保护特性：
  - VBB 欠压闭锁 (UVLO)
  - 电荷泵电压 (CPUV)
  - 过流保护 (OCP)
  - 短接至电源保护 (STS)
  - 短接至地保护 (STG)
  - 过热警告 (OTW)
  - 过热关断 (OTS)
  - 故障条件指示引脚 (nFAULT)

2 应用范围

- 打印机
- 工业自动化
- 机器人
- 电动工具

3 说明

本示例中使用的 DRV8816 提供一个具有两个独立 ½H 桥驱动器的多用途电源驱动器解决方案。 此器件能够驱动一个有刷直流电机或者步进电机的一个绕组，以及其它诸如螺线管等的器件。 一个简单的 INx/ENx 接口可实现与控制器电路的轻松对接。

输出级使用配置为 ½H 桥的 N 通道功率 MOSFET。DRV8816 能够提供高达 ±2.8A 的峰值输出电流，承受最高 38V 的工作电压。一个内部电荷泵可用来生成所需的栅极驱动电压。

低功耗睡眠模式可将部分内部电路关断，从而实现极低的静态电流和功耗。 这种睡眠模式可通过专用的 nSLEEP 引脚来设定。

内部保护功能包括欠压闭锁、电荷泵故障、过流保护、电源短路保护、接地短路保护、过热警告和过热关断。故障条件通过 nFAULT 引脚指示

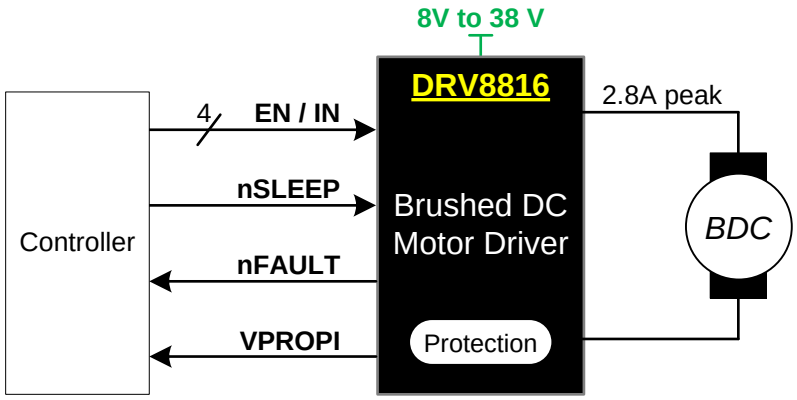
DRV8816 采用带有 PowerPAD™ 的 16 引脚散热薄型小外形尺寸 (HTSSOP) 封装（环保型：符合 RoHS 标准且不含锑/溴）

器件信息(1)

部件号	封装	封装尺寸（标称值）
DRV8816	HTSSOP (16)	4.40mm × 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



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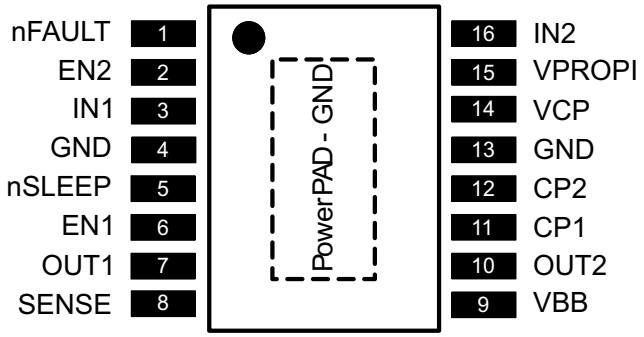
5 修订历史记录

Changes from Original (September 2013) to Revision A **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4
- Updated Figure 5 ... 12

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	NO.			
POWER AND GROUND				
CP1	11	PWR	Charge pump switching node	Connect a 0.1-µF X7R capacitor rated for VBB between CP1 and CP2
CP2	12	—		
GND	4, 13, PPAD	PWR	Device ground	Connect to system ground
VBB	9	PWR	Power supply input	Connect to main power supply. Bypass to GND with a 0.1-µF ceramic capacitor and a larger bulk capacitor rated for at least the VBB voltage
VCP	14	PWR	Charge pump output	Connect a 0.1-µF 16-V ceramic capacitor between VCP and VBB
CONTROL				
EN1	6	I	½-H bridge enable	Logic high enables ½-H bridge output; logic low puts the FETs in HI-Z; internal pulldown
EN2	2			
IN1	3	I	½-H bridge control	Logic high enables the high-side ½-H bridge FET; logic low enables the low side FET; internal pulldown
IN2	16			
nFAULT	1	O	Fault indication pin	Pulled logic low with fault condition; open-drain output requires an external pullup
nSLEEP	5	I	Device sleep mode	Pull logic low to put device into a low-power sleep mode; internal pulldown
OUTPUT				
OUT1	7	O	½-H bridge output	
OUT2	10	O	½-H bridge output	
SENSE	8	O	H-bridge low-side connect	Connect directly to GND or through a sense resistor to set OCP
VPROPI				
VPROPI	15	O	Current-proportional output	

Table 1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VBB}	VBB	GND	0.1-µF ceramic capacitor and a larger bulk capacitor rated for at least the VBB voltage
C_{VCP}	VCP	VBB	0.1-µF 16-V ceramic capacitor
R_{nFAULT}	VCC(1)	nFAULT	>1 kΩ resistor
R_{nSLEEP}	VCC(1)	nSLEEP	If nSLEEP isn't actively controlled, use a pull-up resistor of less than 20 kΩ
R_{SENSE}	SENSE	GND	Optional low-value resistor. If not used, connect SENSE pin directly to GND.
R_{VPROPI}	VPROPI	GND	If VPROPI is used, add a 100kΩ resistor to GND

(1) VCC is not a pin on the DRV8816, but a VCC supply voltage pullup is required.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VBB	Power supply voltage	–0.6	40	V
	Charge pump positive switching pin (CP2)	–0.6	VBB + 7	V
	Charge pump negative switching pin (CP1)	–0.6	VBB	V
	Digital pin voltage range (IN1, IN2, EN1, EN2, nSLEEP, nFAULT)	–0.3	7	V
	VBB to OUTx	–0.6	40	V
	OUTx to SENSE	–0.6	40	V
$V_{(SENSE)}$	Sense voltage (SENSE) (2)	–0.5	1.0	V
	H-bridge output current (OUT1, OUT2, SENSE)	0	2.8	A
	VPROPI pin voltage range (VPROPI)	–0.3	3.6	V
T_A	Operating ambient temperature	–40	85	°C
T_J	Operating junction temperature	–40	190	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–40	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)

		MIN	MAX	UNIT
VBB	Power supply voltage range	8	38	V
V_I	Input pin voltage range	0	5.5	V
f_{PWM}	Applied PWM signal (IN1, IN2, EN1, EN2)		100	kHz
I_{OUT}	H-bridge output current		2.8	A
T_A	Ambient temperature	–40	85	°C

(1) Power dissipation and thermal limits must be observed.

7.4 Thermal Information

THERMAL METRIC[1]		DRV8816 PWP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	43.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[3]	30.8	
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	25.3	
ψ_{JT}	Junction-to-top characterization parameter[5]	1.1	
ψ_{JB}	Junction-to-board characterization parameter[6]	25	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[7]	5.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ JT , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ JA , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ JB , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ JA , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (VBB)							
VBB	VBB operating voltage			8		38	V
I_{VBB}	VBB operating supply current	f_{PWM} < 50 kHz			6		mA
		Charge pump on, Outputs disabled			3.2		mA
I_{VBBQ}	VBB sleep-mode supply current	nSLEEP = 0, T_J = 25°C				10	µA
CONTROL INPUTS (IN1, IN2, EN1, EN2, nSLEEP)							
V_{IL}	Input logic low voltage	IN1, IN2, EN1, EN2		0		0.8	V
V_{IH}	Input logic high voltage			2		5.5	
V_{IL}	Input logic low voltage	nSLEEP		0		0.8	V
V_{IH}	Input logic high voltage			2.2		5.5	V
I_{IL}	Input logic low current	IN1, IN2, EN2, nSLEEP	V_{IN} = 0 V		0		µA
I_{IH}	Input logic high current		V_{IN} = 5 V		25		
I_{IL}	Input logic low current	EN1	V_{IN} = 0 V		0		µA
I_{IH}	Input logic high current		V_{IN} = 5 V		100		
R_{PD}	Pulldown resistance	IN1, IN2, EN2, nSLEEP			200		kΩ
		EN1			50		
SERIAL AND CONTROL OUTPUT (nFAULT)							
V_{OL}	Output logic low voltage	I_{sink} = 1 mA				0.4	V
DMOS DRIVERS (OUT1, OUT2, SENSE)							
$R_{DS(on)}$	Output ON resistance	Source driver, I_{OUT} = –2.8 A, T_J = 25°C			0.48		Ω
		Source driver, I_{OUT} = –2.8 A, T_J = 125°C			0.74	0.85	
		Sink driver, I_{OUT} = –2.8 A, T_J = 25°C			0.35		
		Sink driver, I_{OUT} = –2.8 A, T_J = 125°C			0.52	0.7	
V_{TRIP}	SENSE trip voltage	R_{SENSE} between SENSE and GND			500		mV

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_f	Body diode forward voltage	Source diode, I_f = –2.8 A			1.4	V
		Sink diode, I_f = 2.8 A			1.4	
t_{pd}	OUTx propagation delay	From High-Z to High		70		ns
		From High-Z to Low		700 (1)		
		From High to High-Z		120		
		From High to Low		700		
		From Low to High-Z		350		
		From Low to High		350		
t_{COD}	Crossover delay			500		ns
DAGain	VPROPI amplifier gain	Sense = 0.1 to 0.4 V		5		V/V
PROTECTION CIRCUITS						
V_{UVLO}	VBB UVLO	VBB rising		6.5	7.5	V
V_{CPUV}	VCP UVLO (2)	VBB rising; CPUV recovery		12	13.8	V
I_{OCP}	Overcurrent protection trip level		3			A
t_{DEG}	Overcurrent deglitch time			3.0		µs
t_{OCP}	Overcurrent retry time			1.6		ms
T_{OTW}	Thermal warning temperature	Die temperature T_j		160		°C
$T_{OTW\ HYS}$	Thermal warning hysteresis	Die temperature T_j		15		°C
T_{OTS}	Thermal shutdown temperature	Die temperature T_j		175		°C
$T_{OTS\ HYS}$	Thermal shutdown hysteresis	Die temperature T_j		15		°C

(1) If OUT2 is High, the typical time for OUT1 to go from High-Z to Low is 1700 ns.
(2) Whenever VCP is less than VM + 10 V, a CPUV event occurs. This fault will be asserted whenever VBB is below 12 V. Note that the H-bridges will remain enabled until VBB = V_{UVLO} even through nFAULT is pulled low.

7.6 Typical Characteristics

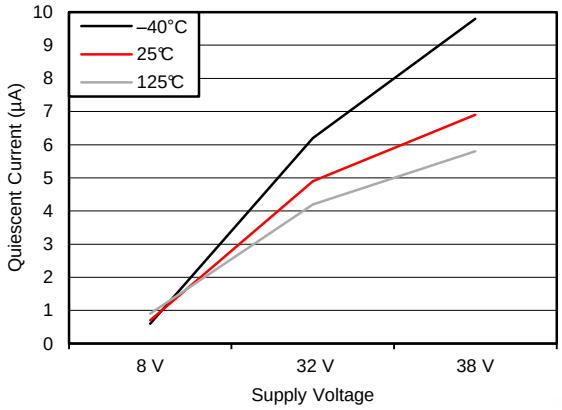


Figure 1. I_{VBBQ} vs VBB

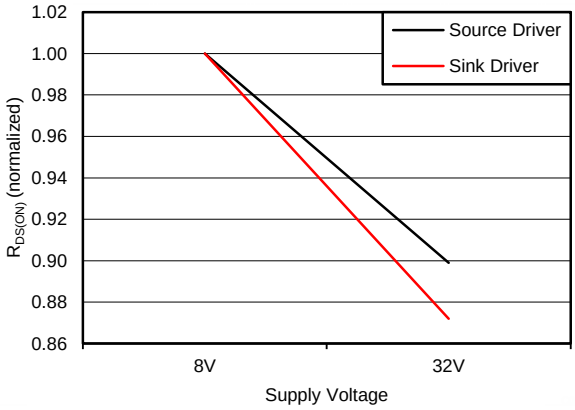


Figure 2. $R_{DS(ON)}$ vs VBB (normalized to VBB = 8V)

Typical Characteristics (continued)

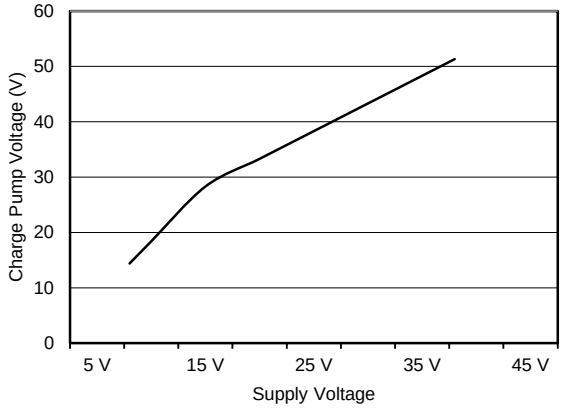


Figure 3. VCP vs VBB

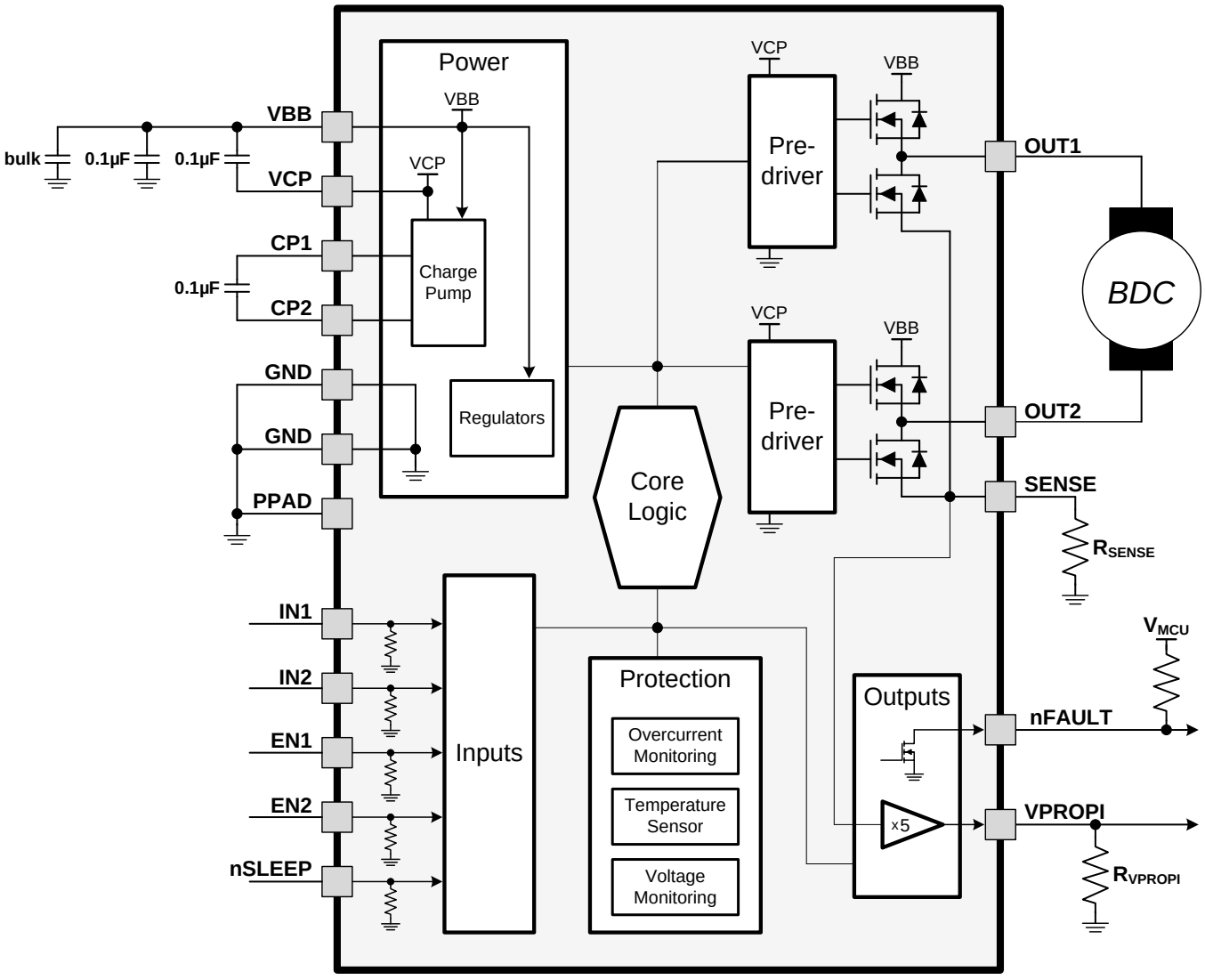
8 Detailed Description

8.1 Overview

The DRV8816 uses 4 CMOS inputs to control 2 high-voltage high-current outputs, while integrating protection features, fault reporting, a sleep mode, and current sensing. EN1 and IN1 control OUT1, and EN2 and IN2 control OUT2, according to Table 2. The device is designed to drive two independent loads or one brushed DC motor, as shown in Figure 4 and Table 3.

When an R_{SENSE} resistor is used, the DRV8816 will automatically disable itself if V_{SENSE} exceeds 500mV—this provides a user-programmable overcurrent threshold. The VPROPI output equals the sense voltage amplified by a factor of 5, and it can be used by a microcontroller to know the motor current, in order to Pulse-Width Modulate the DRV8816 inputs and regulate motor current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bridge Control

The DRV8816 is controlled using separate enable and input pins for each ½-H-bridge.

Feature Description (continued)

Table 2 shows the logic for the DRV8816.

Table 2. DRV8816 Logic

ENx	INx	OUTx
0	X	Z
1	0	L
1	1	H

If a single DC motor is connected to the DRV8816, it is connected between the OUT1 and OUT2 pins as shown in Figure 4. Two DC motors may also be connected to the DRV8816. In this mode, it is not possible to reverse the direction of the motors; the motors will turn only in one direction. The connections are shown in Figure 4.

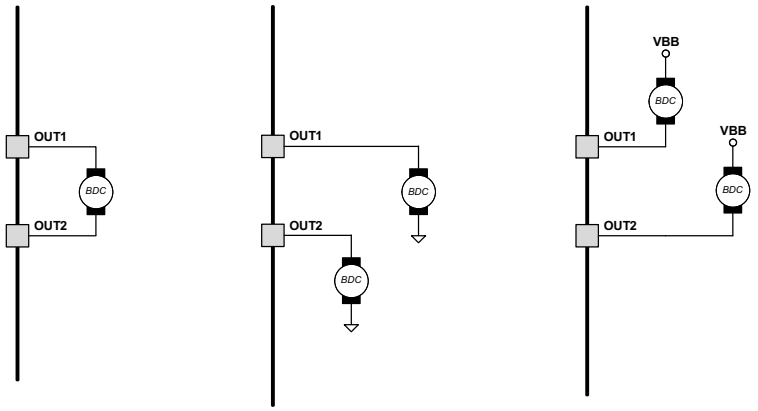


Figure 4. Bridge Control

Table 3 shows how motor operation for a single-brushed DC motor is controlled.

Table 3. Motor Operation for a Single-Brushed DC Motor

EN1	EN2	IN1	IN2	OUT1	OUT2	Operation
0	X	X	X	Z	X(1)	Off (coast)
X	0	X	X	X(1)	Z	Off (coast)
1	1	0	0	L	L	Brake
1	1	0	1	L	H	Reverse
1	1	1	0	H	L	Forward
1	1	1	1	H	H	Brake

(1) The Half-H bridges are independent; output state depends on ENx and INx.

Table 4 shows how motor operation for dual-brushed DC motors is controlled.

Table 4. Motor Operation for a Dual-Brushed DC Motor

	ENx	INx	OUTx	Operation
Motor connected to GND	0	X	Z	Off (coast)
	1	0	L	Brake
	1	1	H	Forward
	ENx	**INx**	**OUTx**	**Operation**
Motor connected to VBB	0	X	Z	Off (coast)
	1	0	L	Forward
	1	1	H	Brake

8.3.2 Charge Pump

The charge pump is used to generate a supply above VBB to drive the source-side DMOS gates. A 0.1-µF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1-µF ceramic monolithic capacitor should be connected between VCP and VBB to act as a reservoir to run the high-side DMOS devices. The VCP voltage level is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

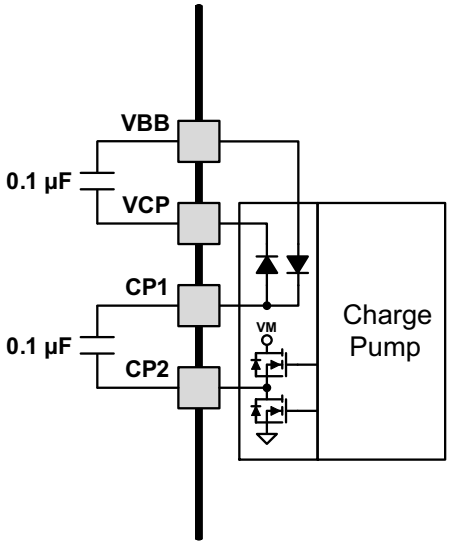


Figure 5. Charge Pump

8.3.3 VPROPI

The VPROPI output is equal to approximately 5× the voltage present on the SENSE pin. VPROPI is meaningful only if there is a resistor connected to the SENSE pin; If SENSE is connected to ground, VPROPI measures 0 V. Also note that during slow decay (brake), VPROPI measures 0 V. VPROPI can output a maximum of 2.5 V, because at 500 mV on SENSE, the H-bridge is disabled.

8.3.4 Protection Circuits

The DRV8816 is fully protected against VBB undervoltage, charge pump undervoltage, overcurrent, and overtemperature events.

8.3.4.1 VBB UVLO

If at any time the voltage on the VBB pin falls below the UVLO threshold voltage, all FETs in the H-bridge will be disabled and the charge pump will be disabled. Operation will resume when VBB rises above the UVLO threshold. Note that nFAULT does not indicate a UVLO because the CPUV fault is always asserted below VBB = 12 V.

8.3.4.2 VCP UVLO (CPUV)

During a CPUV event, the VCP voltage is measured to be below VCP + 10 V. If at any time the voltage on the VCP pin falls below the UVLO threshold voltage, the nFAULT pin is driven low. The nFAULT pin is released after operation has resumed. Note that this fault does not disable the output FETs and allows the device to continue operating. When VBB is below 12 V, this fault condition is always asserted and nFAULT is pulled low.

8.3.4.3 OCP

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, all FETs in the H-bridge are disabled, nFAULT is driven low, and a t_{OCP} fault timer is started. After this period, t_{OCP}, the device is then allowed to follow the input commands and another turn-on is attempted (nFAULT becomes high again during this attempt). If there is still a fault condition, the cycle repeats. If after t_{OCP} expires it is determined the short condition is not present, normal operation resumes and nFAULT is released.

8.3.4.4 OTW

If the die temperature increases past the thermal warning threshold, the nFAULT pin is driven low. After the die temperature has fallen below the hysteresis level, the nFAULT pin is released. If the die temperature continues to increase, the device enters overtemperature shutdown as described in *OTS* .

8.3.4.5 OTS

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the charge pump is shut down. After the die temperature has fallen to a safe level, operation automatically resumes.

8.4 Device Functional Modes

8.4.1 SENSE

A low-value resistor can be placed between the SENSE pin and ground for current-sensing purposes. The PCB should be designed with wide metal paths on each side of the resistor, to minimize IR drop that would decrease sense accuracy. Likewise, the distance from the sense resistor to the DRV8816 and bulk capacitor should be minimized.

To set a manual overcurrent trip threshold, place a resistor between the SENSE pin and GND. When the SENSE pin rises above 500 mV, the H-bridge output is disabled (High-Z). The device will automatically retry with a period of t_{OCP}. The overcurrent trip threshold can be calculated using I_{TRIP} = 500 mV/Ω. The overcurrent trip level selected cannot be greater than I_{OCP}.

If a sense resistor is not used, tie the SENSE pin directly to GND; in that case, the I_{OCP} detection of current through the internal FETs still functions.

Device Functional Modes (continued)

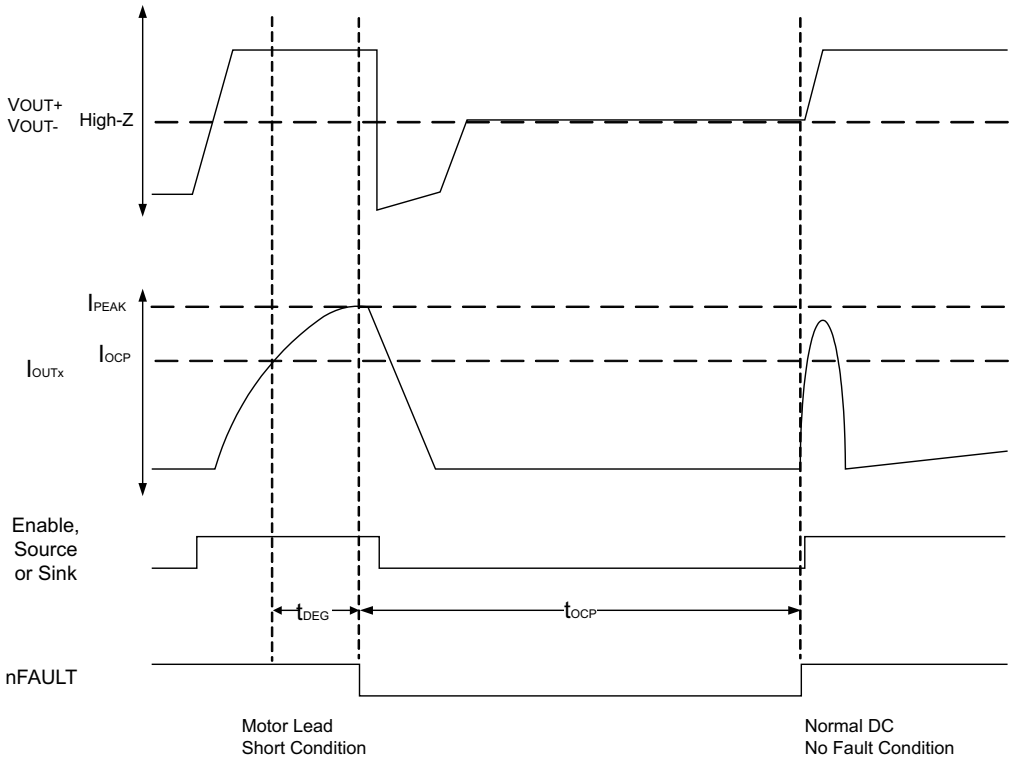


Figure 6. Overcurrent Threshold

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8816 is typically used to drive a brushed DC motor.

9.2 Typical Application

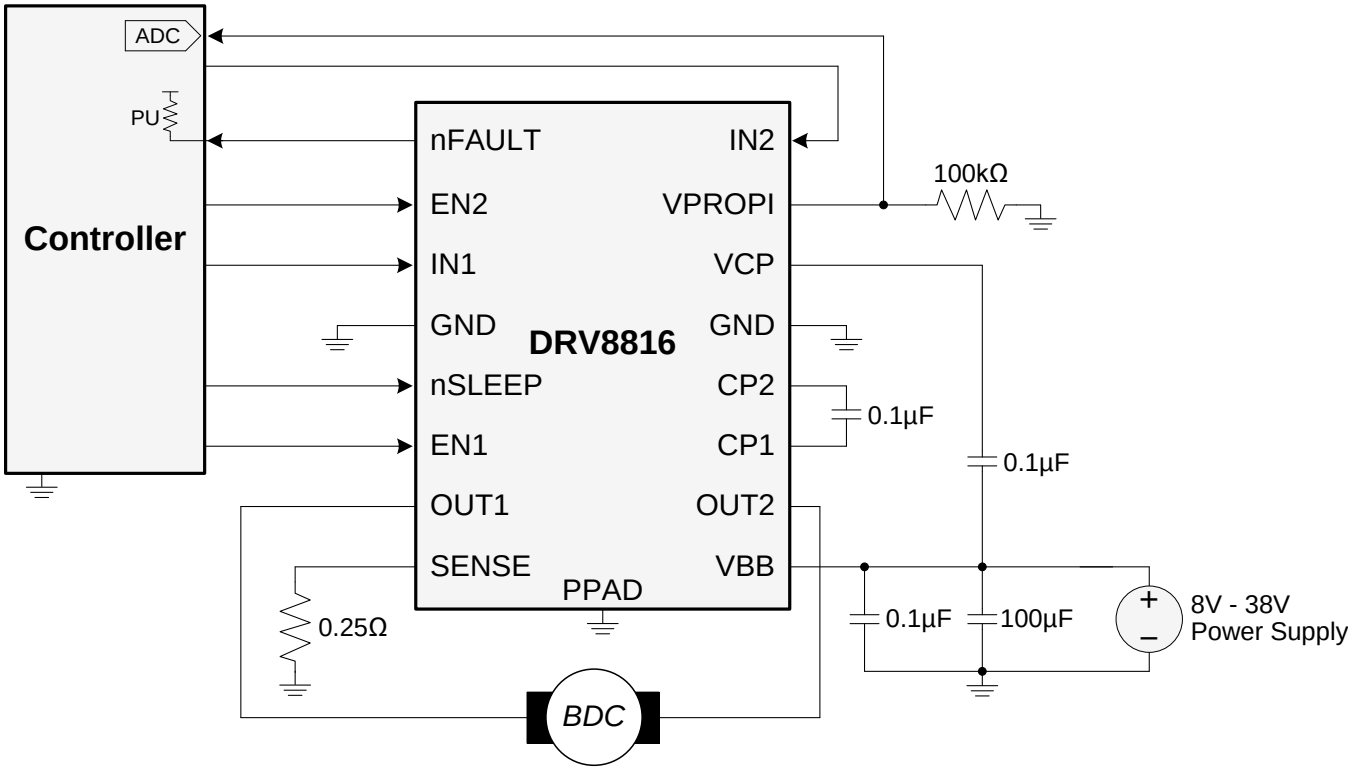


Figure 7. Typical Application

9.2.1 Design Requirements

Table 5 shows parameters to consider when designing.

Table 5. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_{BB}	24V
Motor RMS current	I_{RMS}	0.8A
Motor startup current	I_{START}	2A
Motor current trip point	I_{TRIP}	2.5A

9.2.2 Detailed Design Procedure

9.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

9.2.2.2 Power Dissipation

The power dissipation of the DRV8816 is a function of RMS motor current and the each output's FET resistance ($R_{DS(ON)}$).

$$\text{Power} \approx I_{RMS}^2 \times (\text{High-Side } R_{DS(ON)} + \text{Low-Side } R_{DS(ON)}) \quad (1)$$

For this example, the ambient temperature is 35°C, and the junction temperature reaches 65°C. At 65°C, the sum of $R_{DS(ON)}$ is about 1Ω. With an example motor current of 0.8A, the dissipated power in the form of heat will be $0.8A^2$ x 1Ω = 0.64W.

The temperature that the DRV8816 reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, in order dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8816 had an effective thermal resistance $R_{\theta JA}$ of 47°C/W, and:

$$T_J = T_A + (P_D \times R_{\theta JA}) = 35°C + (0.64W \times 47°C/W) = 65°C \quad (2)$$

9.2.2.3 Motor Current Trip Point

When the voltage on pin SENSE exceeds V_{TRIP} (0.5V), overcurrent is detected. The R_{SENSE} resistor should be sized to set the desired I_{TRIP} level.

$$R_{SENSE} = 0.5V / I_{TRIP} \quad (3)$$

To set I_{TRIP} to 2A, R_{SENSE} = 0.5V / 2A = 0.25Ω.

To prevent false trips, I_{TRIP} must be higher than regular operating current. Motor current during startup is typically much higher than steady-state spinning, because the initial load torque is higher, and the absence of back-EMF causes a higher voltage and extra current across the motor windings.

It can be beneficial to limit startup current by using series inductors on the DRV8816 output, as that allows I_{TRIP} to be lower, and it may decrease the system's required bulk capacitance. Startup current can also be limited by ramping the forward drive duty cycle.

9.2.2.4 Sense Resistor Selection

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals I_{RMS}^2 x R. For example, if peak motor current is 3A, RMS motor current is 2A, and a 0.05Ω sense resistor is used, the resistor will dissipate $2A^2$ x 0.05Ω = 0.2W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

9.2.3 Application Curves

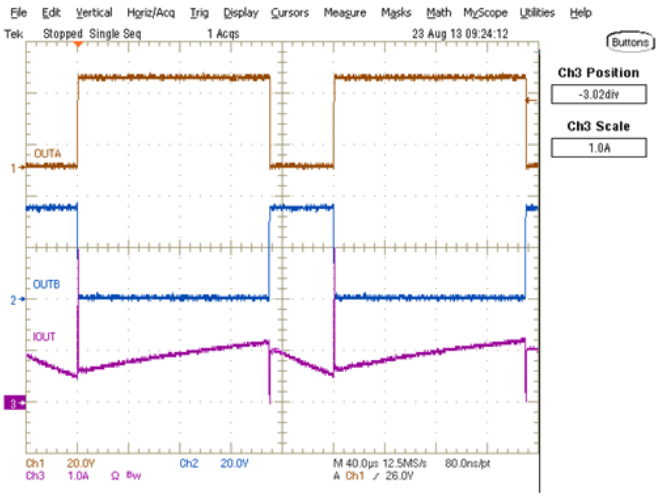


Figure 8. Forward Drive, Fast Decay

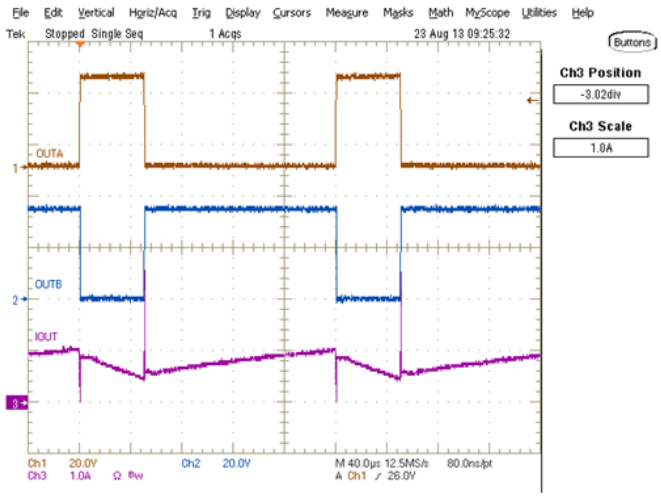


Figure 9. Reverse Drive, Fast Decay

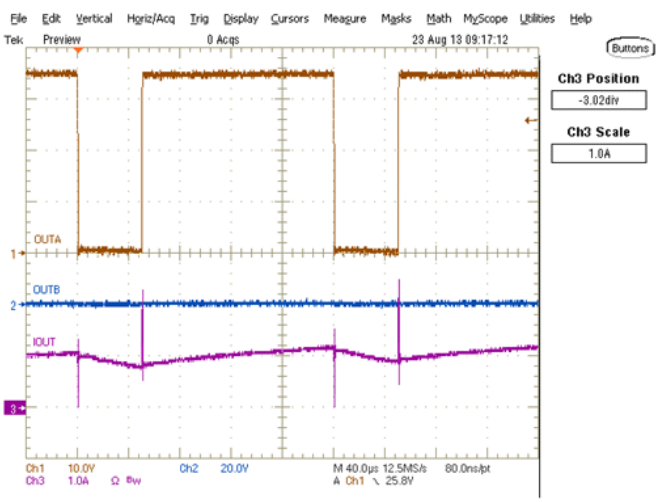


Figure 10. Forward Drive, Slow Decay

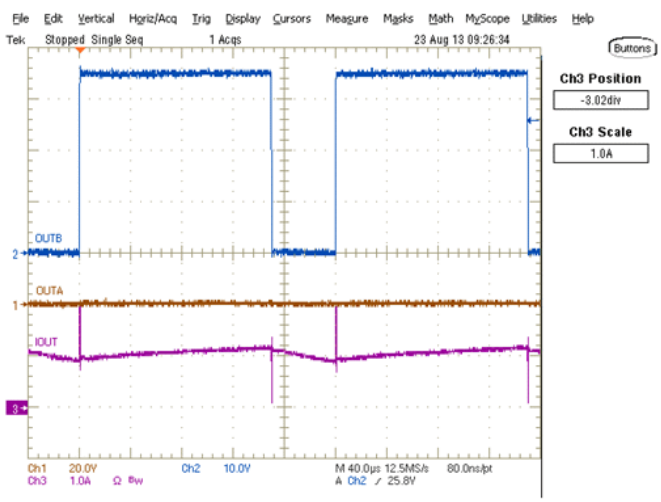


Figure 11. Reverse Drive, Slow Decay

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor systems.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

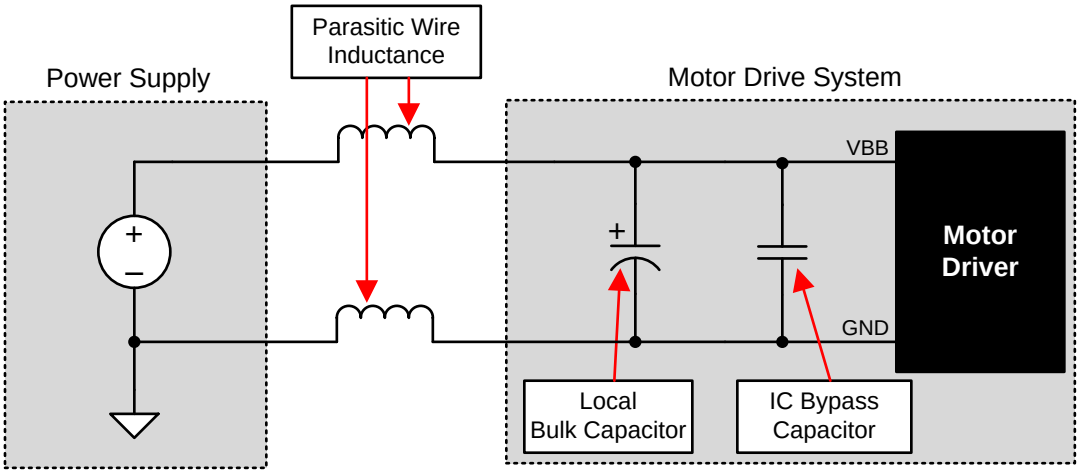


Figure 12. Example Setup of Motor Drive System with External Power Supply

10.2 Power Supervisor

Control input nSLEEP is used to minimize power consumption when the DRV8816 is not in use. This disables much of the internal circuitry, including the internal voltage rails and charge pump. nSLEEP is asserted low. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

11 Layout

11.1 Layout Guidelines

The printed circuit board (PCB) should use a heavy ground plane. For optimum electrical and thermal performance, the DRV8816 must be soldered directly onto the board. On the underside of the DRV8816 is a thermal pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically 100 µF) in parallel with a ceramic capacitor placed as close as possible to the device. The ceramic capacitors between VCP and VBB, connected to VREG, and between CP1 and CP2 should be as close to the pins of the device as possible, in order to minimize lead inductance.

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (4)$$

where

- P_{TOT} is the total power dissipation.
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETS.
- $I_{OUT(RMS)}$ is the RMS output current being applied to each winding.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

$I_{OUT(RMS)}$ is equal to approximately 0.7× the full-scale output current setting.

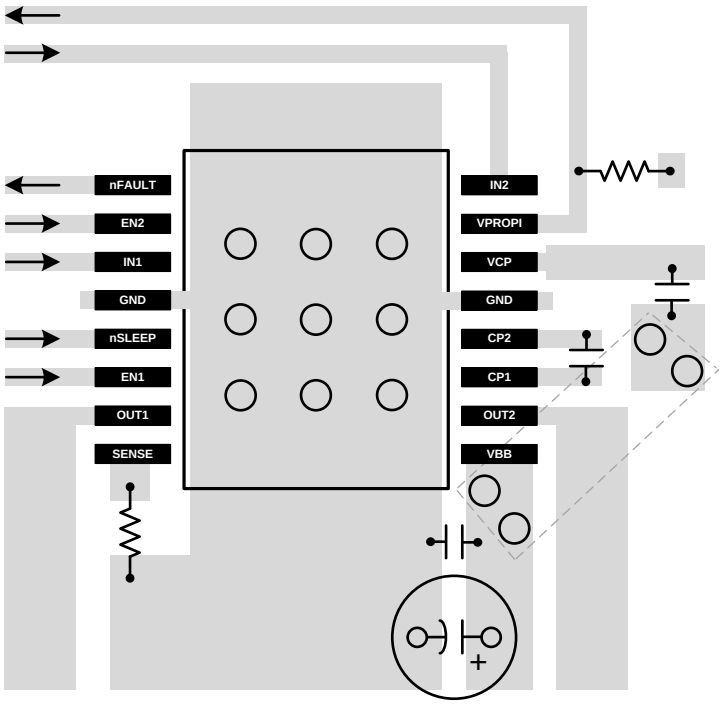
The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

11.1.1 Ground

A ground power plane should be located as close to DRV8816 as possible. The copper ground plane directly under the thermal pad makes a good location. This pad can then be connected to ground for this purpose.

11.2 Layout Example



11.3 Thermal Protection

If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level. Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

12 器件和文档支持

12.1 商标

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8816PWP	Obsolete	Production	HTSSOP (PWP) | 16	-	-	Call TI	Call TI	-40 to 85	DRV8816
DRV8816PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8816
DRV8816PWPR.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8816

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

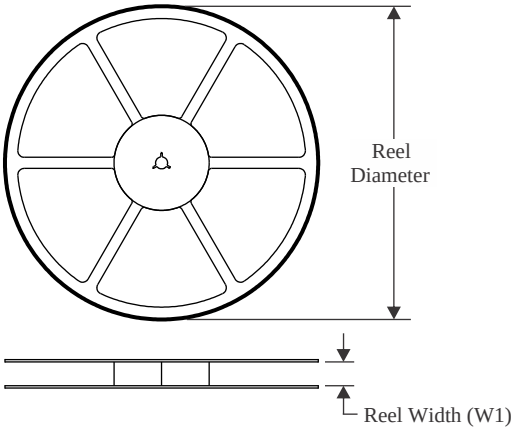
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

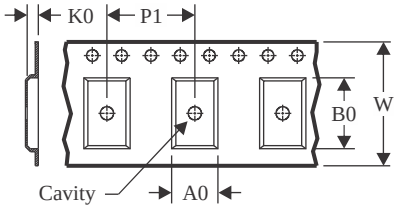
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

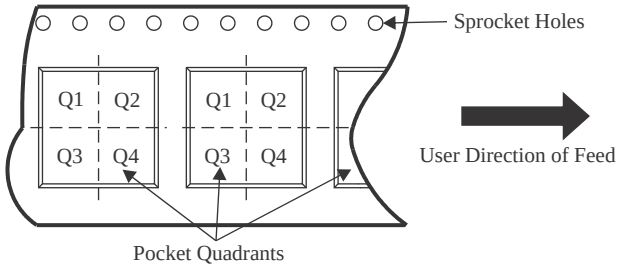


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

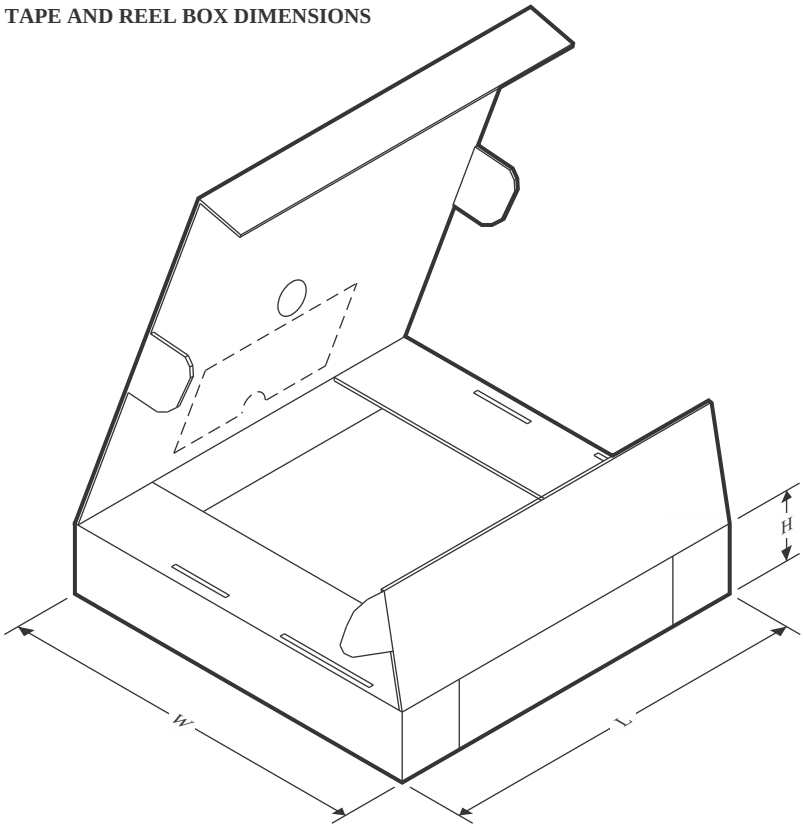
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8816PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

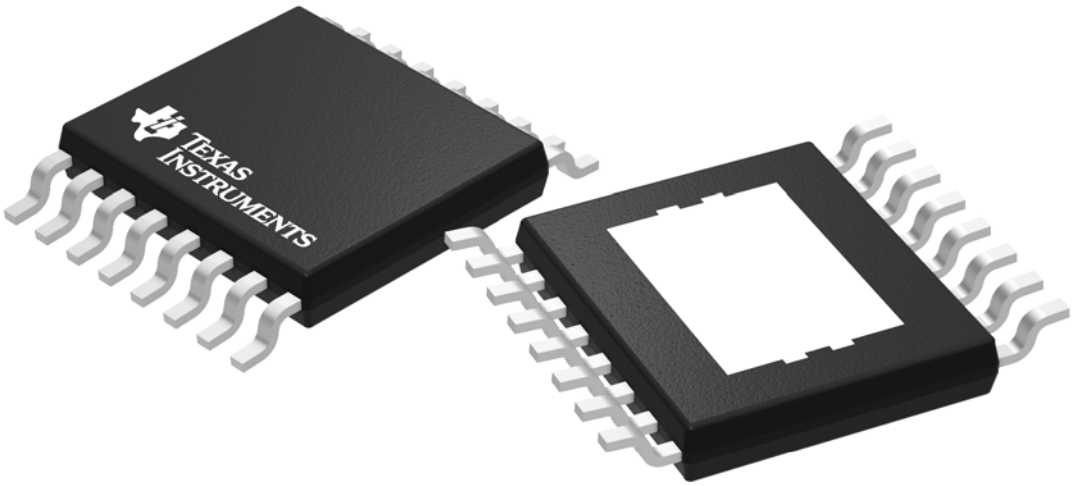


*All dimensions are nominal

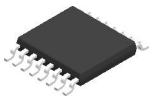
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8816PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

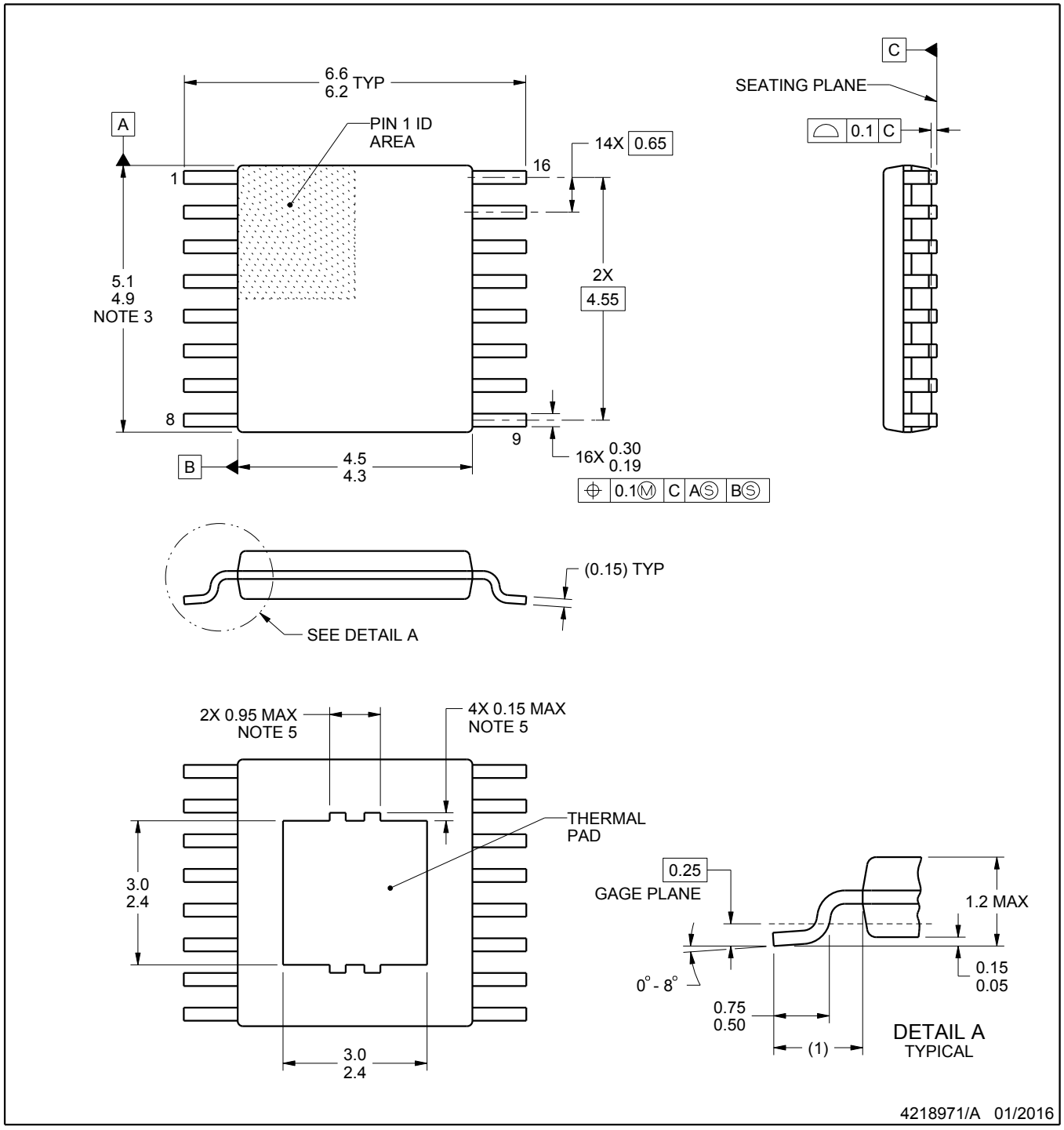


PACKAGE OUTLINE

PWP0016B

PowerPAD™ TSSOP - 1.2 mm max height

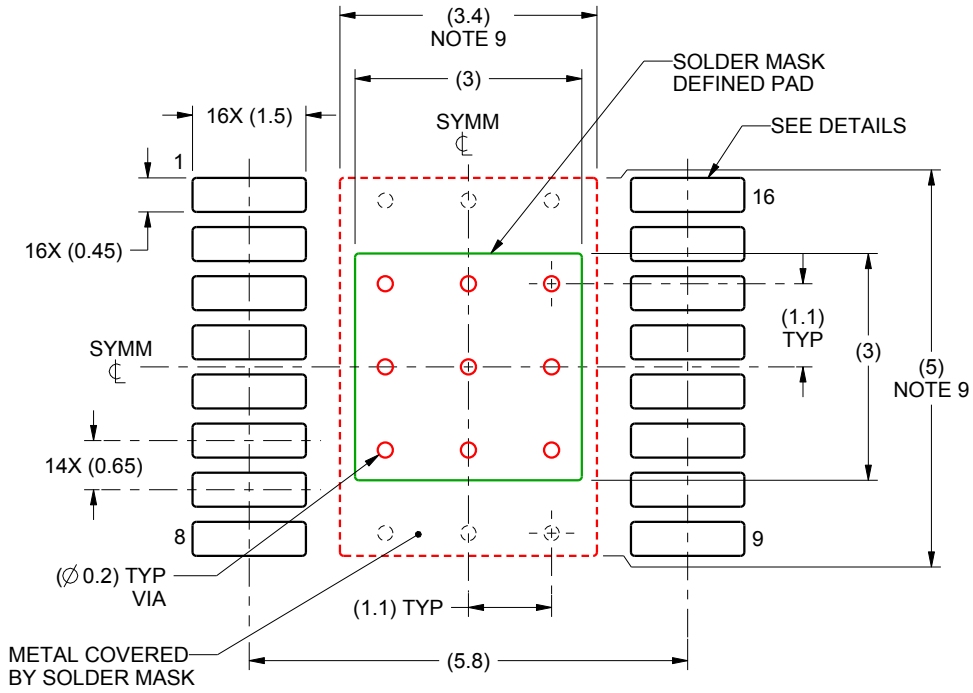
PLASTIC SMALL OUTLINE



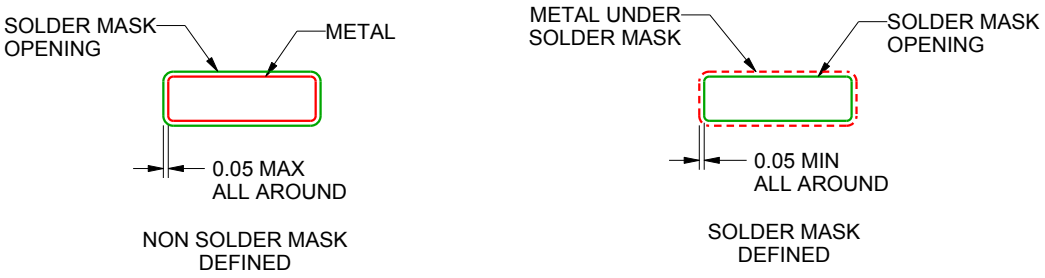
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

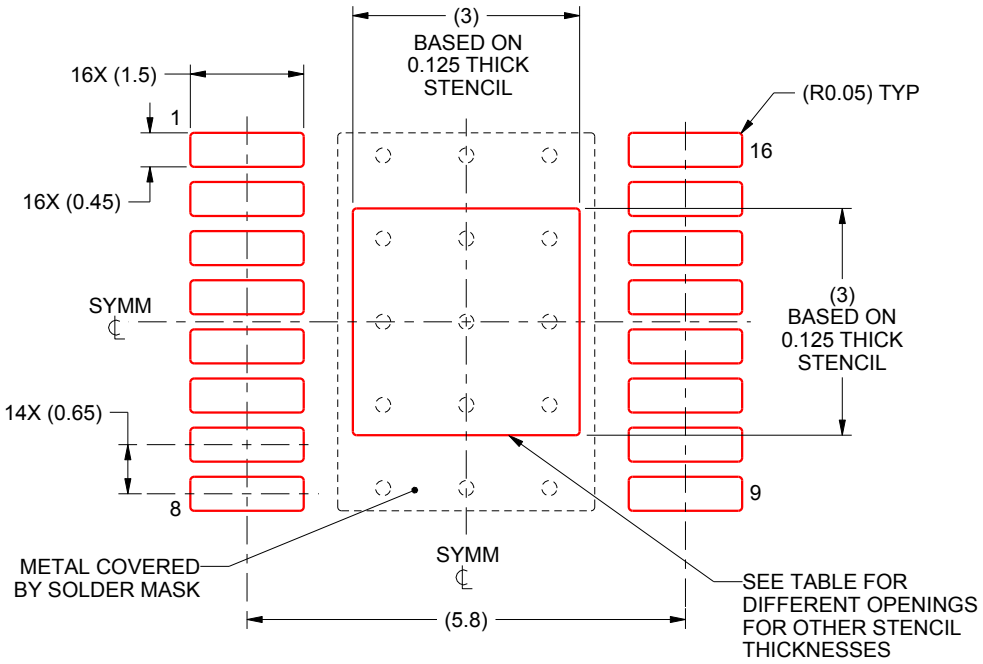


SOLDER MASK DETAILS
PADS 1-16

4218971/A 01/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.35 X 3.35
0.125	3 X 3 (SHOWN)
0.15	2.74 X 2.74
0.175	2.54 X 2.54

4218971/A 01/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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