



## DRV425 磁通门磁场传感器

### 1 特性

- 高精度、集成磁通门传感器：
  - 偏移：±8μT（最大值）
  - 偏移漂移：±5nT/°C（典型值）
  - 增益误差：0.04%（典型值）
  - 增益漂移：±7ppm/°C（典型值）
  - 线性度：±0.1%
  - 噪声：1.5nT/√Hz（典型值）
- 传感器范围：±2mT（最大值）
  - 范围和增益可通过外部电阻进行调节
- 可选带宽：47kHz 或 32kHz
- 精密基准：
  - 精度：2%（最大值），漂移：50ppm/°C（最大值）
  - 引脚可选电压：2.5V 或 1.65V
  - 可选比例模式：VDD/2
- 诊断 特性：超限和错误标志
- 电源电压范围：3.0V 至 5.5V

### 2 应用

- 线性位置感测
- 母线电流感测
- 走线电流感测
- 通用磁场传感器
- 过流检测
- 电机可靠性诊断
- 频率和电压逆变器
- 太阳能逆变器

### 3 说明

DRV425 专为单轴磁场感测 需要快速切换频率的应用，而设计，可实现电气隔离式高灵敏度精密直流和交流磁场测量。该器件可提供独特且专有的集成磁通门传感器 (IFG)。该传感器内置一个补偿线圈，支持 ±2mT 的高精度感测范围，测量带宽最高可达 47kHz。该传感器的低偏移、低漂移、低噪声特性与内部补偿线圈的精确增益、低增益漂移和极低非线性度相结合，可提供无与伦比的磁场测量精度。DRV425 输出与感测到的场强成正比的模拟信号。

DRV425 提供了一组完整 采用，包括内部差分放大器、片上精密基准以及诊断功能，能够最大限度地减少组件数量并削减系统级成本。

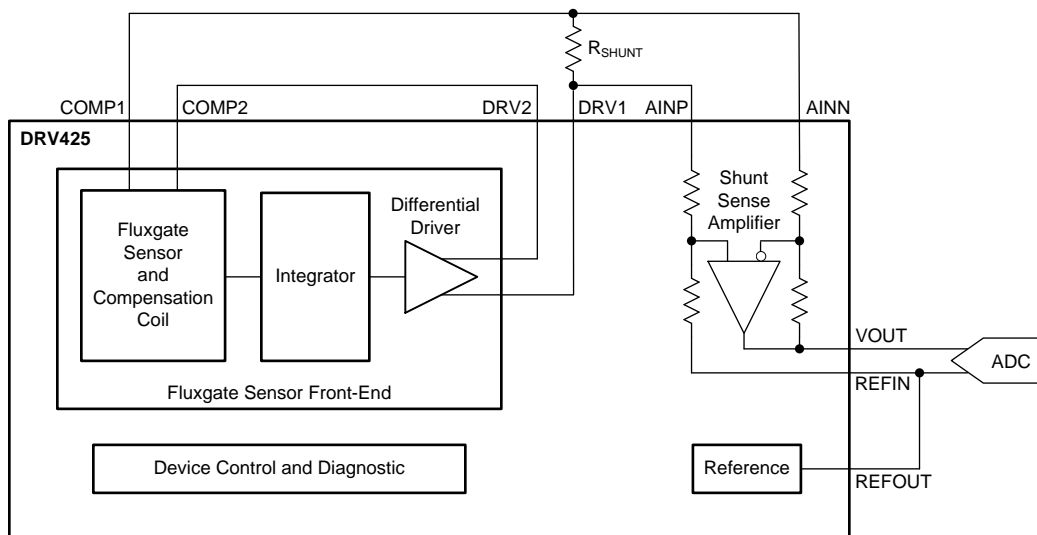
DRV425 采用带有 PowerPAD™ 的耐热增强型、无磁性、超薄四方扁平无引线 (WQFN) 封装来实现优化散热，并且在 -40°C 至 +125°C 的扩展工业温度范围内额定运行。

器件信息 (1)

部件号	封装	封装尺寸（标称值）
DRV425	WQFN (20)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



## 目录

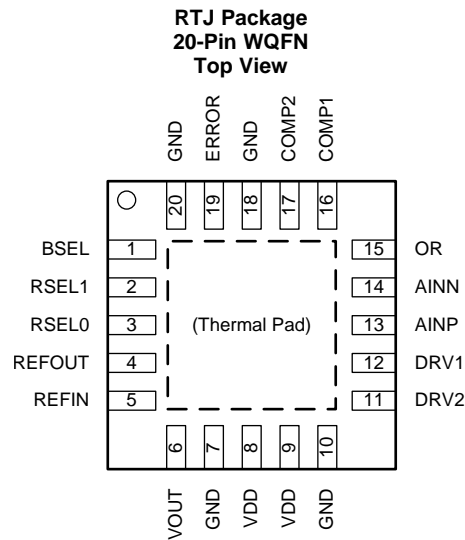
<b>1</b>	<b>特性</b> .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>24</b>
<b>2</b>	<b>应用</b> .....	<b>1</b>	8.1	Application Information.....	24
<b>3</b>	<b>说明</b> .....	<b>1</b>	8.2	Typical Applications .....	24
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	<b>9</b>	<b>Power-Supply Recommendations</b> .....	<b>29</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	9.1	Power-Supply Decoupling.....	29
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	9.2	Power-On Start-Up and Brownout .....	29
6.1	Absolute Maximum Ratings .....	4	9.3	Power Dissipation .....	29
6.2	ESD Ratings.....	4	<b>10</b>	<b>Layout</b> .....	<b>30</b>
6.3	Recommended Operating Conditions.....	4	10.1	Layout Guidelines .....	30
6.4	Thermal Information .....	4	10.2	Layout Example .....	31
6.5	Electrical Characteristics.....	5	<b>11</b>	<b>器件和文档支持</b> .....	<b>32</b>
6.6	Typical Characteristics .....	7	11.1	文档支持 .....	32
<b>7</b>	<b>Detailed Description</b> .....	<b>17</b>	11.2	社区资源 .....	32
7.1	Overview .....	17	11.3	商标 .....	32
7.2	Functional Block Diagram .....	17	11.4	静电放电警告 .....	32
7.3	Feature Description.....	18	11.5	Glossary .....	32
7.4	Device Functional Modes.....	23	<b>12</b>	<b>机械、封装和可订购信息</b> .....	<b>32</b>

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Original (October 2015) to Revision A</b>	<b>Page</b>
• 已修复损坏的链接 .....	<b>1</b>
• 已添加最后四个 应用 要点的措辞 .....	<b>1</b>
• Changed device name in 图 63 .....	<b>21</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AINN	14	I	Inverting input of the shunt-sense amplifier
AINP	13	I	Noninverting input of the shunt-sense amplifier
BSEL	1	I	Filter bandwidth select input
COMP1	16	I	Internal compensation coil input 1
COMP2	17	I	Internal compensation coil input 2
DRV1	12	O	Compensation coil driver output 1
DRV2	11	O	Compensation coil driver output 2
ERROR	19	O	Error flag: open-drain, active-low output
GND	7, 10, 18, 20	—	Ground reference
OR	15	O	Shunt-sense amplifier overrange indicator: open-drain, active-low output
PowerPAD		—	Connect the thermal pad to GND
REFIN	5	I	Common-mode reference input for the shunt-sense amplifier
REFOUT	4	O	Voltage reference output
RSEL0	3	I	Voltage reference mode selection input 0
RSEL1	2	I	Voltage reference mode selection input 1
VDD	8, 9	—	Supply voltage, 3.0 V to 5.5 V. Decouple both pins using 1-μF ceramic capacitors placed as close as possible to the device. See the <a href="#">Power-Supply Decoupling</a> and <a href="#">Layout</a> sections for further details.
VOUT	6	O	Shunt-sense amplifier output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply voltage (VDD to GND)	−0.3	6.5	V
	Input voltage, except AINP and AINN pins <sup>(2)</sup>	GND − 0.5	VDD + 0.5	
	Shunt-sense amplifier inputs (AINP and AINN pins) <sup>(3)</sup>	GND − 6.0	VDD + 6.0	
Current	DRV1 and DRV2 pins (short-circuit current, I <sub>OS</sub> ) <sup>(4)</sup>	−300	300	mA
	Shunt-sense amplifier input pins AINP and AINN	−5	5	
	All remaining pins	−25	25	
Temperature	Junction, T <sub>J</sub> max	−50	150	°C
	Storage, T <sub>stg</sub>	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited, except for the differential amplifier input pins.
- (3) These inputs are not diode-clamped to the power-supply rails.
- (4) Power-limited; observe maximum junction temperature.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage range (VDD to GND)	3.0	5.0	5.5	V
T <sub>A</sub>	Specified ambient temperature range	−40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DRV425	UNIT
		RTJ (WQFN)	
		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	34.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	33.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	11	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	11	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

All minimum and maximum specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  to  $5.5\text{ V}$ , and  $I_{DRV1} = I_{DRV2} = 0\text{ mA}$ , unless otherwise noted. Typical values are at  $V_{DD} = 5.0\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>FLUXGATE SENSOR FRONT-END</b>						
	Offset	No magnetic field	–8	±2	8	μT
	Offset drift	No magnetic field		±5		nT/°C
G	Gain	Current at DRV1 and DRV2 outputs		12.2		mA/mT
	Gain error			±0.04%		
	Gain drift	Best-fit line method		±7		ppm/°C
	Linearity error			0.1%		
	Hysteresis	Magnetic field sweep from –10 mT to 10 mT		1.4		μT
	Noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		17		nTrms
	Noise density	$f = 1\text{ kHz}$		1.5		nT/√Hz
	Compensation range		–2		2	mT
	Saturation trip level for the ERROR pin <sup>(1)</sup>	Open-loop, uncompensated field		1.6		mT
	ERROR delay	Open-loop at $B > 1.6\text{ mT}$		4 to 6		μs
BW	Bandwidth	BSEL = 0, $R_{SHUNT} = 22\ \Omega$		32		kHz
		BSEL = 1, $R_{SHUNT} = 22\ \Omega$		47		
$I_{OS}$	Short-circuit current	$V_{DD} = 5\text{ V}$		250		mA
		$V_{DD} = 3.3\text{ V}$		150		
	Common-mode output voltage at the DRV1 and DRV2 pins			$V_{REFOUT}$		V
	Compensation coil resistance			100		Ω
<b>SHUNT-SENSE AMPLIFIER</b>						
$V_{OO}$	Output offset voltage	$V_{AINP} = V_{AINN} = V_{REFIN}$ , $V_{DD} = 3.0\text{ V}$	–0.075	±0.01	0.075	mV
	Output offset voltage drift		–2	±0.4	2	μV/°C
CMRR	Common-mode rejection ratio, RTO <sup>(2)</sup>	$V_{CM} = -1\text{ V}$ to $V_{DD} + 1\text{ V}$ , $V_{REFIN} = V_{DD} / 2$	–250	±50	250	μV/V
PSRR <sub>AMP</sub>	Power-supply rejection ratio, RTO <sup>(2)</sup>	$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$ , $V_{CM} = V_{REFIN}$	–50	±4	50	μV/V
$V_{ICR}$	Common-mode input voltage range		–1		$V_{DD} + 1$	V
$Z_{id}$	Differential input impedance		16.5	20	23.5	kΩ
$Z_{ic}$	Common-mode input impedance		40	50	60	kΩ
$G_{nom}$	Nominal gain	$V_{VOUT} / (V_{AINP} - V_{AINN})$		4		V/V
$E_G$	Gain error		–0.3%	±0.02%	0.3%	
	Gain error drift		–5	±1	5	ppm/°C
	Linearity error			12		ppm
	Voltage output swing from negative rail (OR pin trip level) <sup>(1)</sup>	$V_{DD} = 5.5\text{ V}$ , $I_{VOUT} = 2.5\text{ mA}$		48	85	mV
		$V_{DD} = 3.0\text{ V}$ , $I_{VOUT} = 2.5\text{ mA}$		56	100	
	Voltage output swing from positive rail (OR pin trip level) <sup>(1)</sup>	$V_{DD} = 5.5\text{ V}$ , $I_{VOUT} = -2.5\text{ mA}$	$V_{DD} - 85$	$V_{DD} - 48$		mV
		$V_{DD} = 3.0\text{ V}$ , $I_{VOUT} = -2.5\text{ mA}$	$V_{DD} - 100$	$V_{DD} - 56$		
	Signal overrange indication delay (OR pin) <sup>(1)</sup>	$V_{IN} = 1\text{-V}$ step		2.5 to 3.5		μs
$I_{OS}$	Short-circuit current	VOUT connected to GND		–18		mA
		VOUT connected to VDD		20		
$BW_{-3dB}$	Bandwidth			2		MHz
SR	Slew rate			6.5		V/μs
$t_{sa}$	Settling time	Large signal $\Delta V = \pm 2\text{ V}$ to 1%, no external filter		0.9		μs
		Small signal $\Delta V = \pm 0.4\text{ V}$ to 0.01%		8		
$e_n$	Output voltage noise density	$f = 1\text{ kHz}$ , compensation loop disabled		170		nV/√Hz
$V_{REFIN}$	Input voltage range at pin REFIN	Input voltage range at REFIN pin	GND		VDD	V

(1) See the [Magnetic Field Range, Overage Indicator, and Error Flag](#) section for details on the behavior of the ERROR and OR outputs.

(2) Parameter value is referred-to-output (RTO).

## Electrical Characteristics (continued)

All minimum and maximum specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ , and  $I_{DRV1} = I_{DRV2} = 0\text{ mA}$ , unless otherwise noted. Typical values are at  $V_{DD} = 5.0\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE						
V <sub>REFOUT</sub>	Reference output voltage at the REFOUT pin	RSEL[1:0] = 00, no load	2.45	2.5	2.55	V
		RSEL[1:0] = 01, no load	1.6	1.65	1.7	
		RSEL[1:0] = 1x, no load	45	50	55	% of VDD
	Reference output voltage drift	RSEL[1:0] = 0x	−50	±10	50	ppm/°C
	Voltage divider gain error drift	RSEL[1:0] = 1x	−50	±10	50	ppm/°C
PSRR <sub>REF</sub>	Power-supply rejection ratio	RSEL[1:0] = 0x	−300	±15	300	μV/V
ΔV <sub>O(ΔIO)</sub>	Load regulation	RSEL[1:0] = 0x, load to GND or VDD, ΔI <sub>LOAD</sub> = 0 mA to 5 mA, T <sub>A</sub> = −40°C to +125°C		0.15	0.35	mV/mA
		RSEL[1:0] = 1x, load to GND or VDD, ΔI <sub>LOAD</sub> = 0 mA to 5 mA, T <sub>A</sub> = −40°C to +125°C		0.3	0.8	
I <sub>OS</sub>	Short-circuit current	REFOUT connected to VDD		20		mA
		REFOUT connected to GND		−18		mA
DIGITAL INPUTS/OUTPUTS (CMOS)						
I <sub>IL</sub>	Input leakage current			0.01		μA
V <sub>IH</sub>	High-level input voltage	T <sub>A</sub> = −40°C to +125°C	0.7 × VDD		VDD + 0.3	V
V <sub>IL</sub>	Low-level input voltage	T <sub>A</sub> = −40°C to +125°C	−0.3		0.3 × VDD	V
V <sub>OH</sub>	High-level output voltage	Open-drain output	Set by external pullup resistor			V
V <sub>OL</sub>	Low-level output voltage	4-mA sink current		0.3		V
POWER SUPPLY						
I <sub>Q</sub>	Quiescent current	I <sub>DRV1/2</sub> = 0 mA, 3.0 V ≤ VDD ≤ 3.6 V, T <sub>A</sub> = −40°C to +125°C		6	8	mA
		I <sub>DRV1/2</sub> = 0 mA, 4.5 V ≤ VDD ≤ 5.5 V, T <sub>A</sub> = −40°C to +125°C		7	10	
V <sub>POR</sub>	Power-on reset threshold			2.4		V

## 6.6 Typical Characteristics

at VDD = 5 V and T<sub>A</sub> = 25°C (unless otherwise noted)

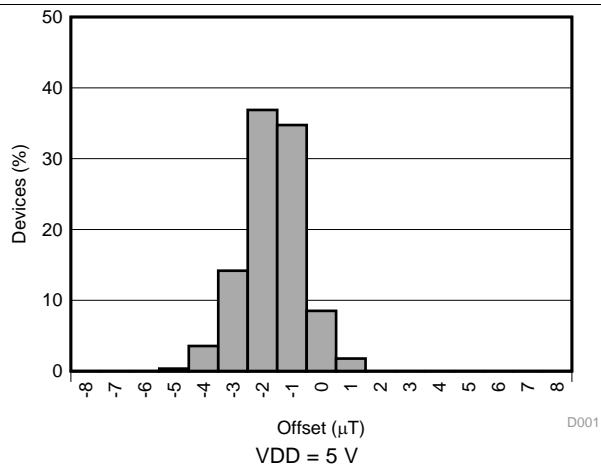


图 1. Fluxgate Sensor Front-End Offset Histogram

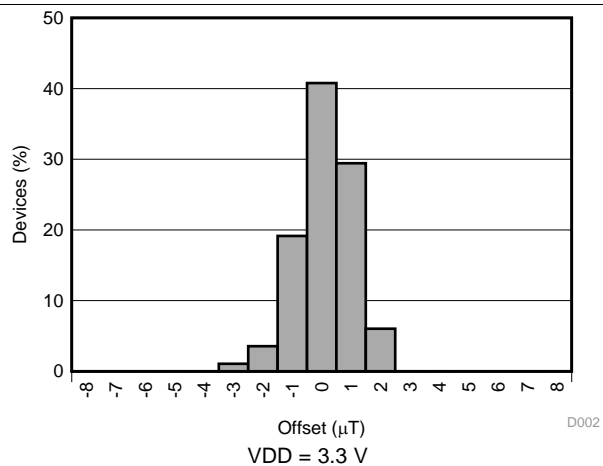


图 2. Fluxgate Sensor Front-End Offset Histogram

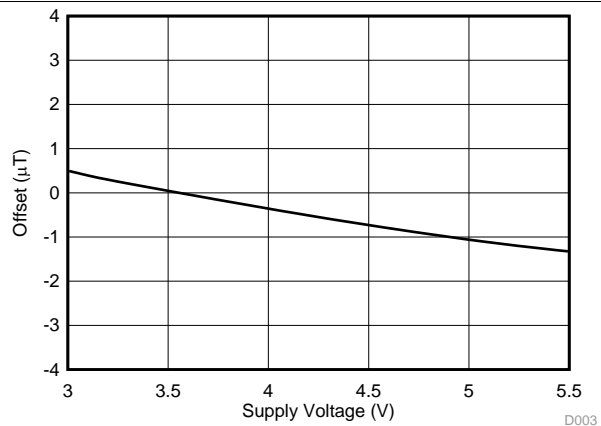


图 3. Fluxgate Sensor Front-End Offset vs Supply Voltage

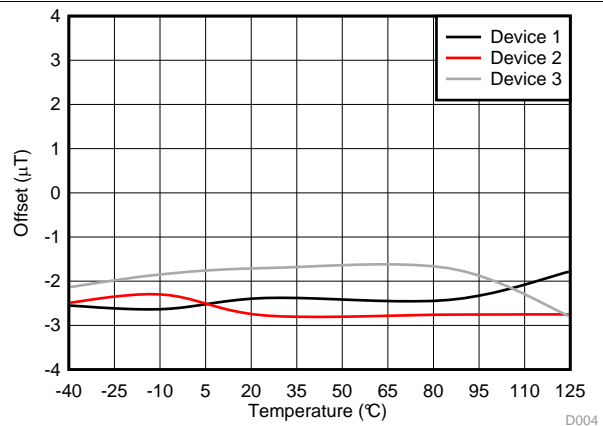


图 4. Fluxgate Sensor Front-End Offset vs Temperature

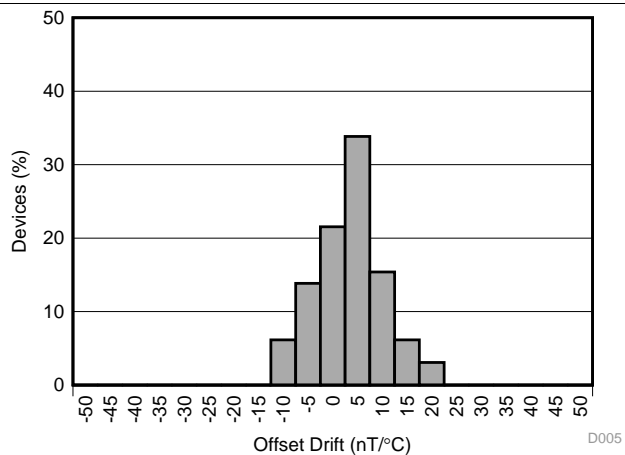


图 5. Fluxgate Sensor Front-End Offset Drift Histogram

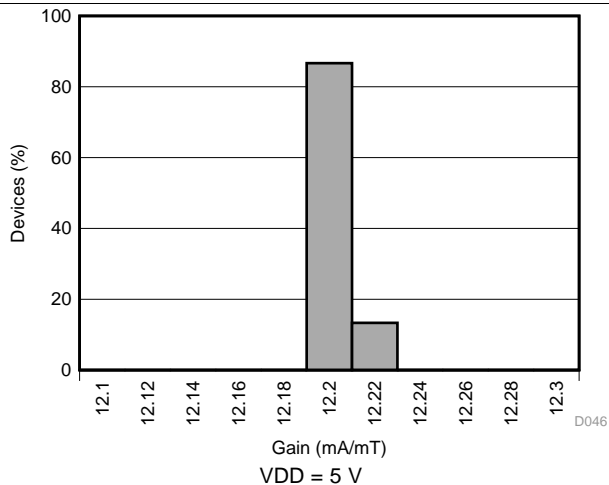


图 6. Fluxgate Sensor Front-End Gain Histogram

## Typical Characteristics (接下页)

at VDD = 5 V and T<sub>A</sub> = 25°C (unless otherwise noted)

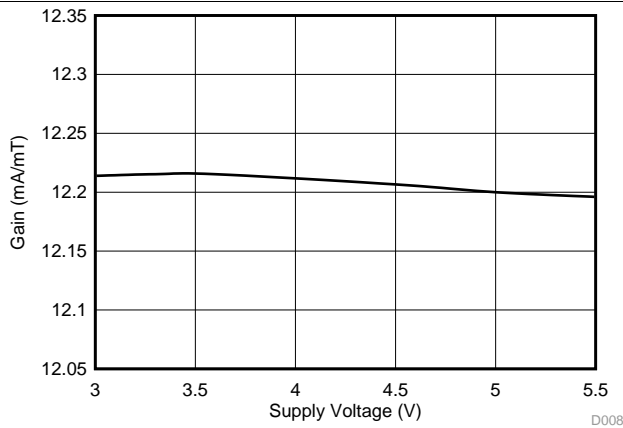


图 7. Fluxgate Sensor Front-End Gain vs Supply Voltage

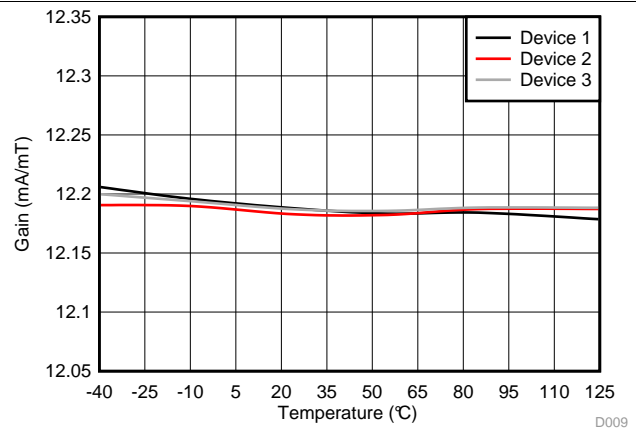


图 8. Fluxgate Sensor Front-End Gain vs Temperature

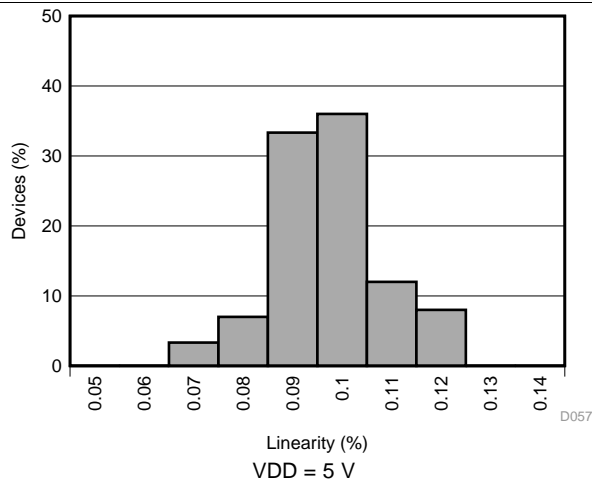


图 9. Fluxgate Sensor Front-End Linearity Histogram

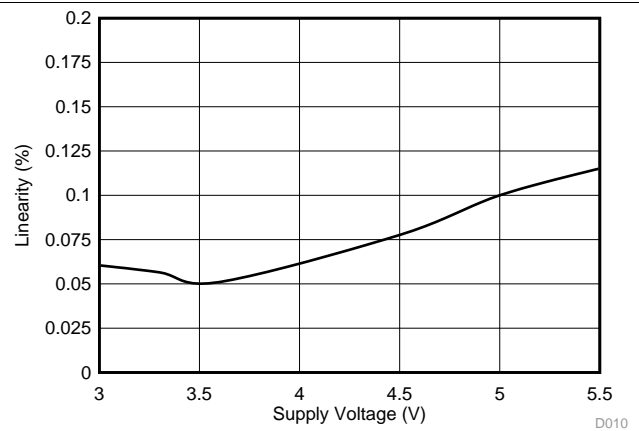


图 10. Fluxgate Sensor Front-End Linearity vs Supply Voltage

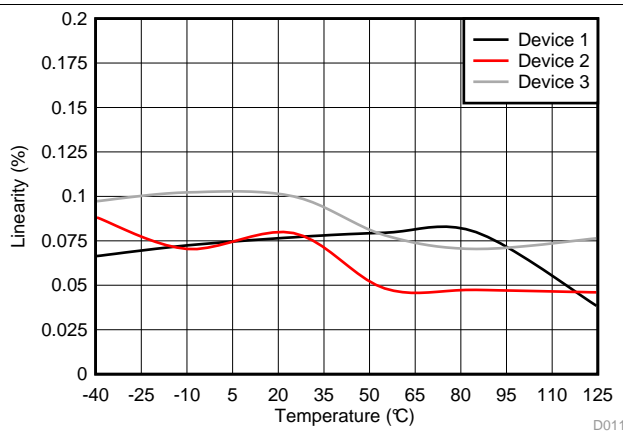


图 11. Fluxgate Sensor Front-End Linearity vs Temperature

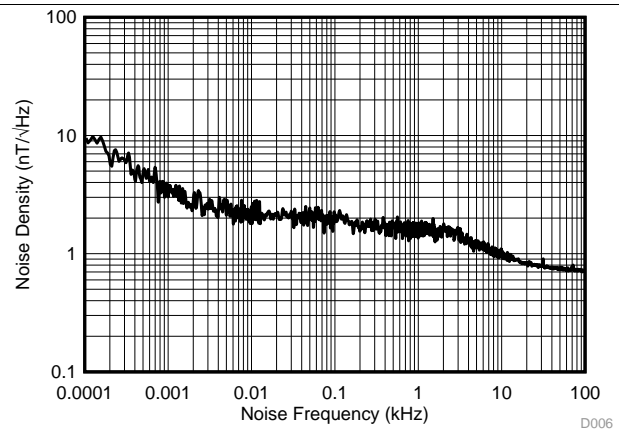
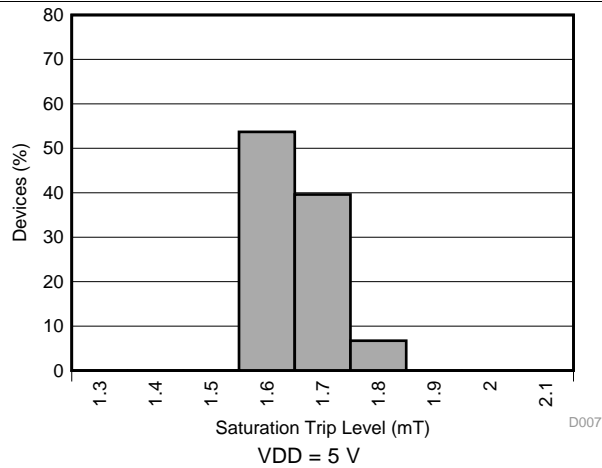


图 12. Fluxgate Sensor Front-End Noise Density vs Noise Frequency

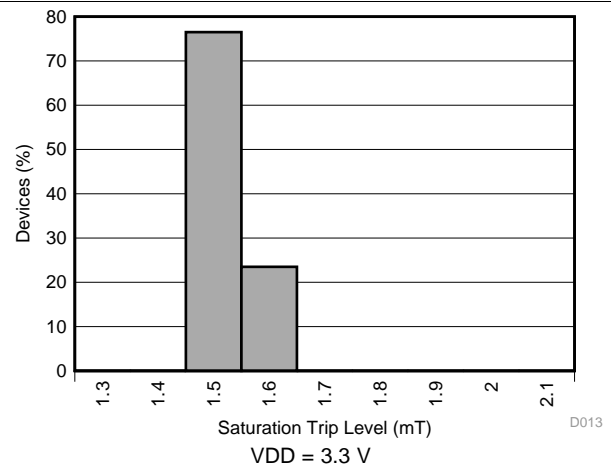


## Typical Characteristics (接下页)

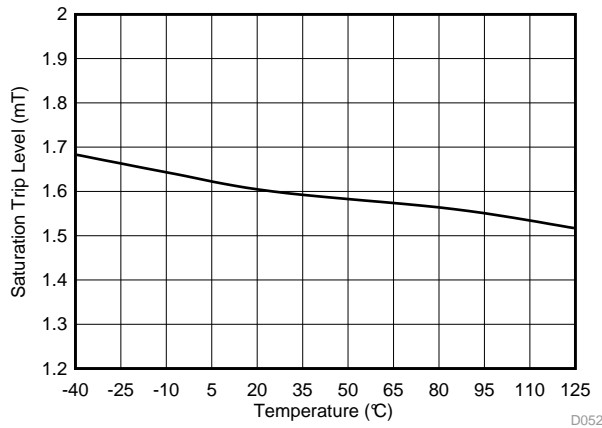
at VDD = 5 V and T<sub>A</sub> = 25°C (unless otherwise noted)



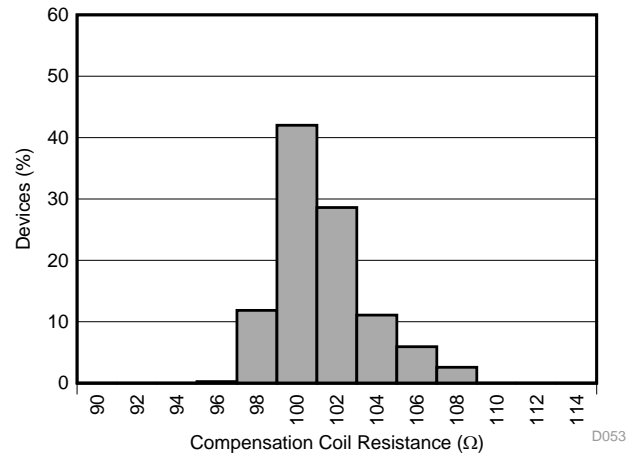
**图 13. Fluxgate Sensor Saturation (ERROR Pin) Trip Level Histogram**



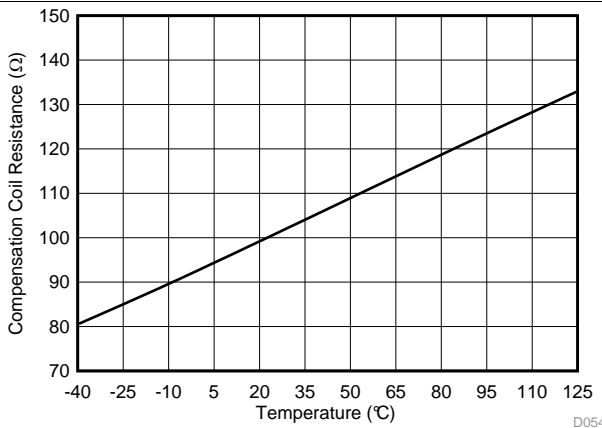
**图 14. Fluxgate Sensor Saturation (ERROR Pin) Trip Level Histogram**



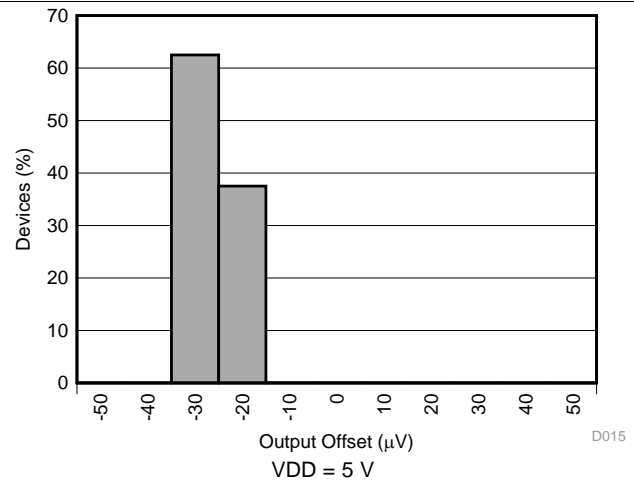
**图 15. Fluxgate Sensor Saturation (ERROR Pin) Trip Level vs Temperature**



**图 16. Compensation Coil Resistance Histogram**



**图 17. Compensation Coil Resistance vs Temperature**



**图 18. Shunt-Sense Amplifier Output Offset Histogram**

## Typical Characteristics (接下页)

at  $V_{DD} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

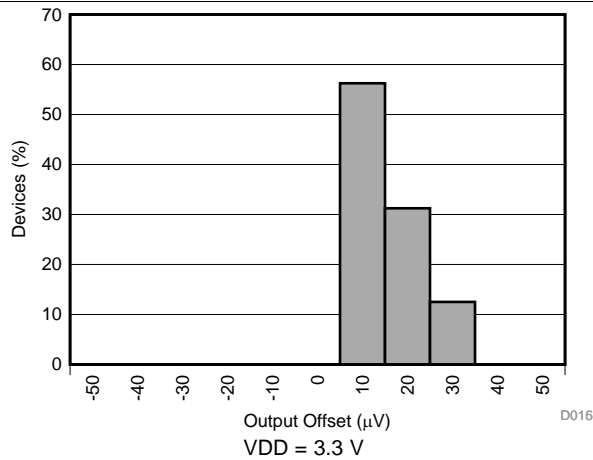


图 19. Shunt-Sense Amplifier Output Offset Histogram

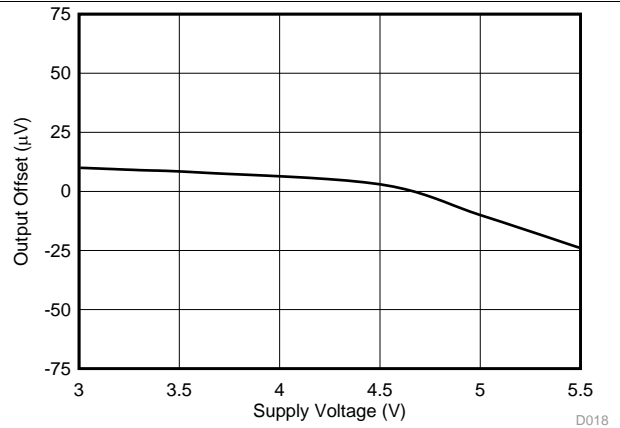


图 20. Shunt-Sense Amplifier Output Offset vs Supply Voltage

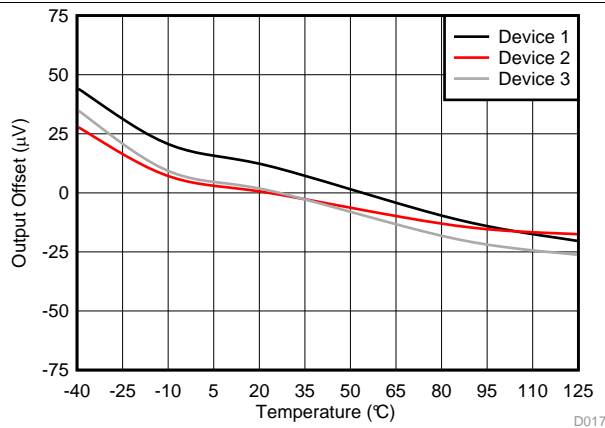


图 21. Shunt-Sense Amplifier Output Offset vs Temperature

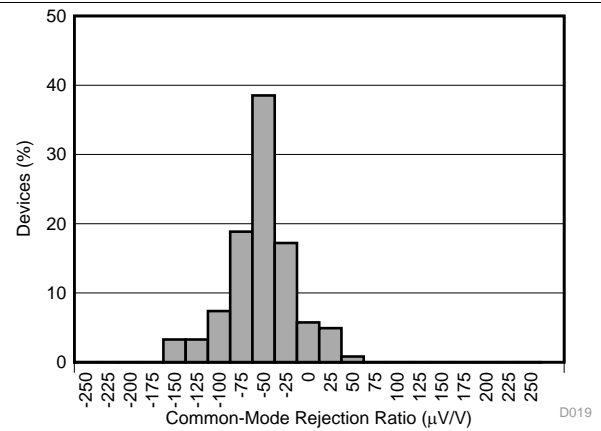


图 22. Shunt-Sense Amplifier CMRR Histogram

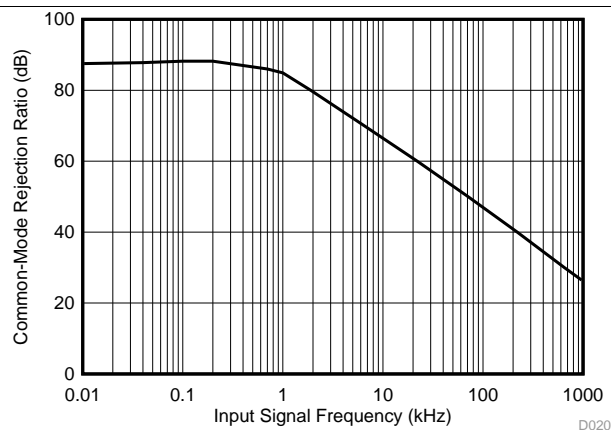


图 23. Shunt-Sense Amplifier CMRR vs Input Signal Frequency

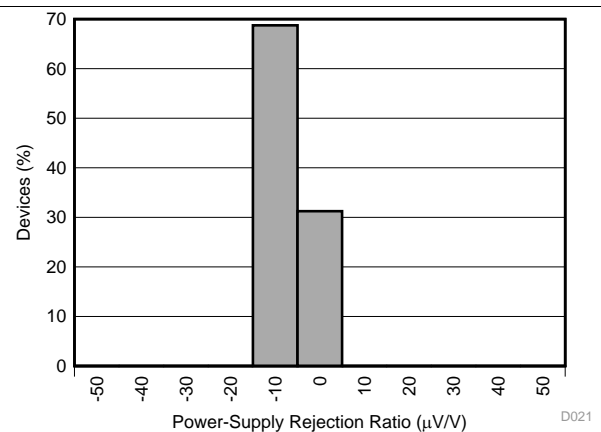


图 24. Shunt-Sense Amplifier PSRR Histogram

## Typical Characteristics (接下页)

at VDD = 5 V and T<sub>A</sub> = 25°C (unless otherwise noted)

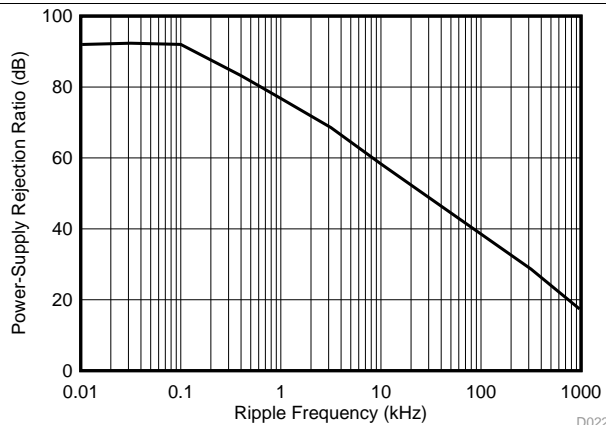


图 25. Shunt-Sense Amplifier PSRR vs Ripple Frequency

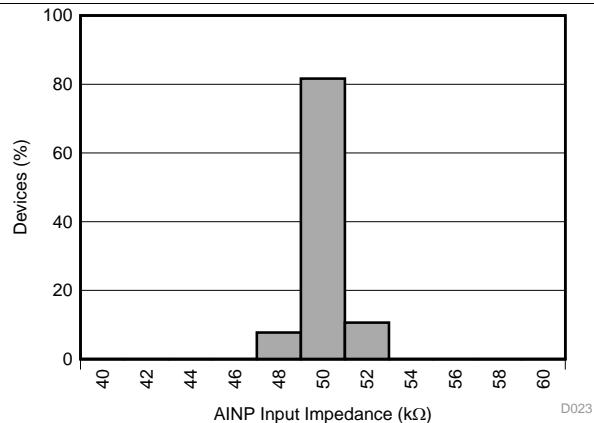


图 26. Shunt-Sense Amplifier AINP Input Impedance Histogram

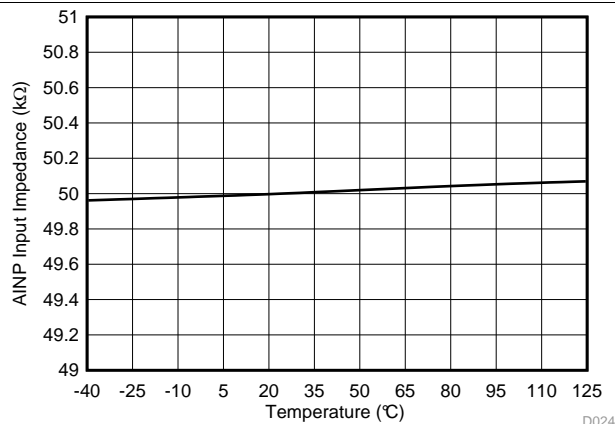


图 27. Shunt-Sense Amplifier AINP Input Impedance vs Temperature

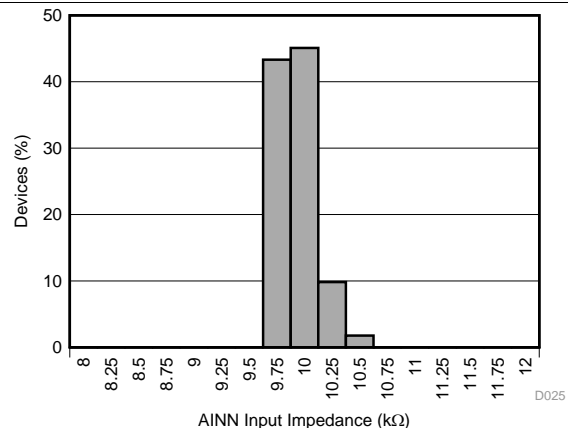


图 28. Shunt-Sense Amplifier AINN Input Impedance Histogram

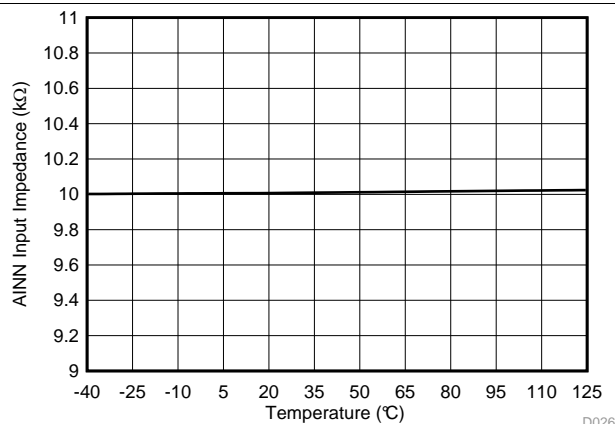


图 29. Shunt-Sense Amplifier AINN Input Impedance vs Temperature

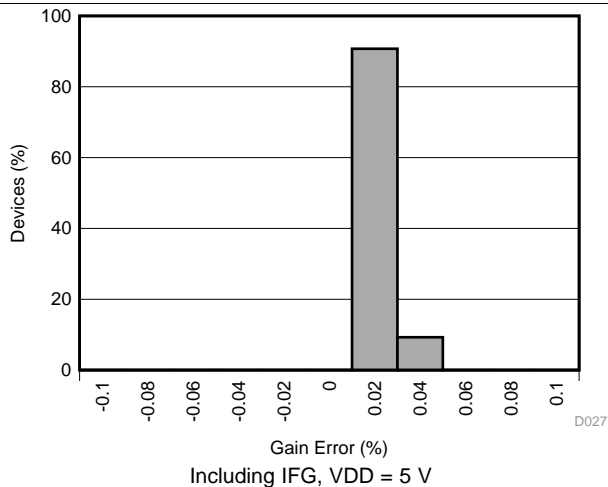


图 30. Shunt-Sense Amplifier Gain Error Histogram

## Typical Characteristics (接下页)

at VDD = 5 V and T<sub>A</sub> = 25°C (unless otherwise noted)

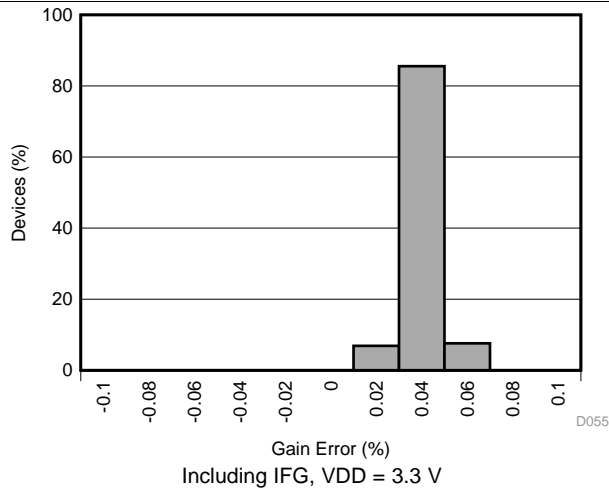


图 31. Shunt-Sense Amplifier Gain Error Histogram

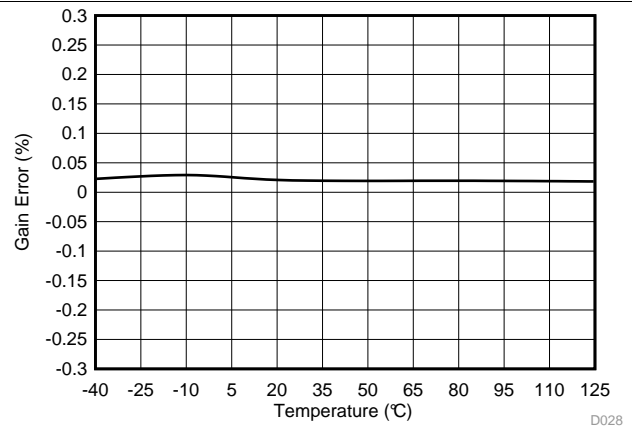


图 32. Shunt-Sense Amplifier Gain Error vs Temperature

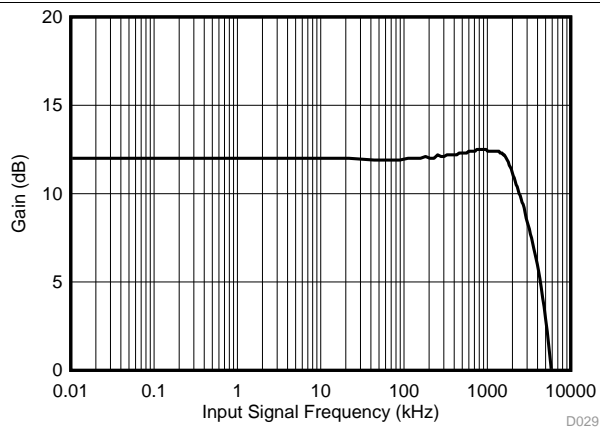


图 33. Shunt-Sense Amplifier Gain vs Input Signal Frequency

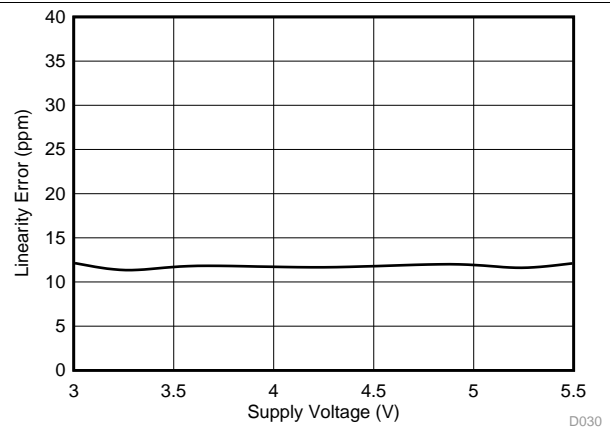


图 34. Shunt-Sense Amplifier Linearity Error vs Supply Voltage

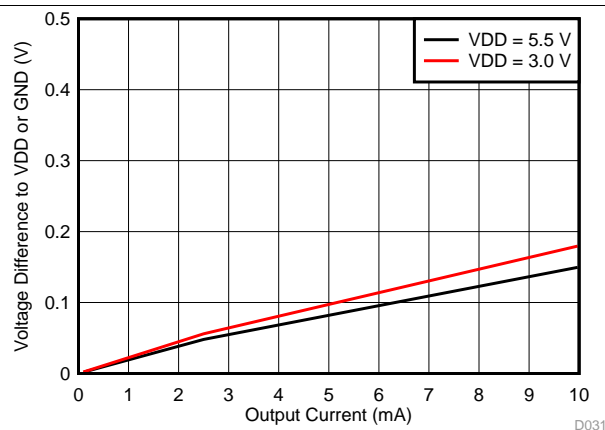


图 35. OR Pin Trip Level vs Output Current

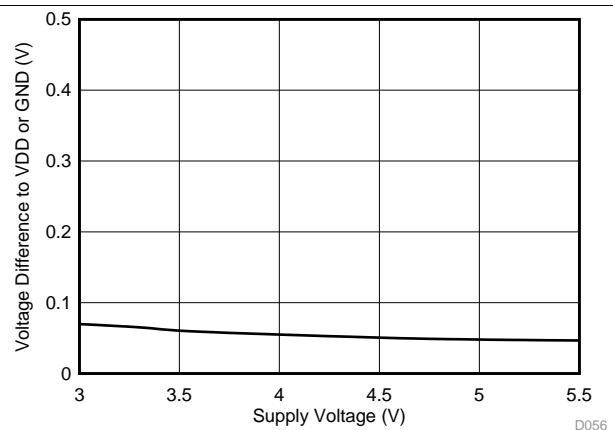


图 36. OR Pin Trip Level vs Supply Voltage

## Typical Characteristics (接下页)

at  $V_{DD} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

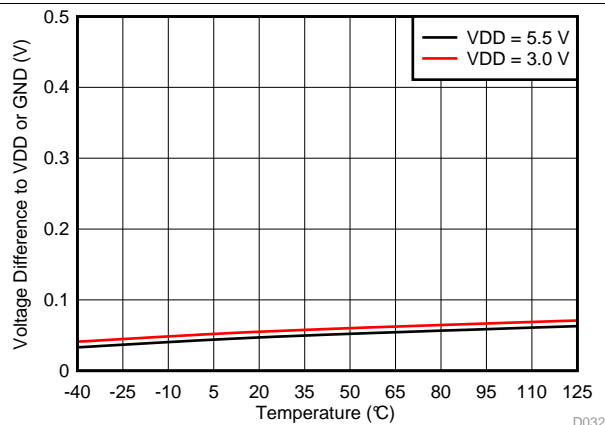


图 37. OR Pin Trip Level vs Temperature

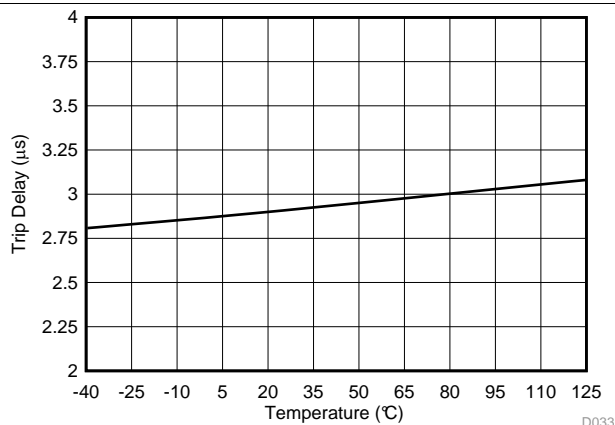


图 38. OR Pin Trip Delay vs Temperature

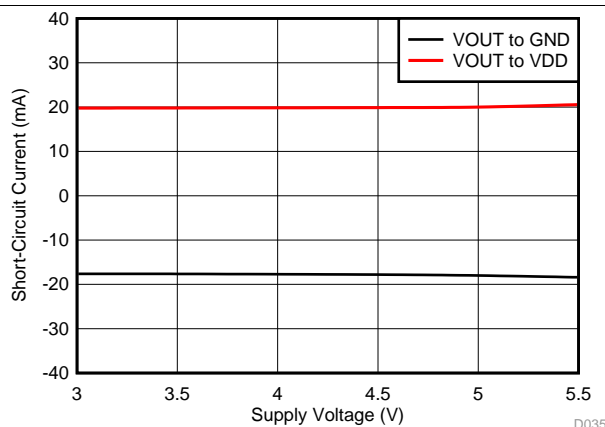


图 39. Shunt-Sense Amplifier Output Short-Circuit Current vs Supply Voltage

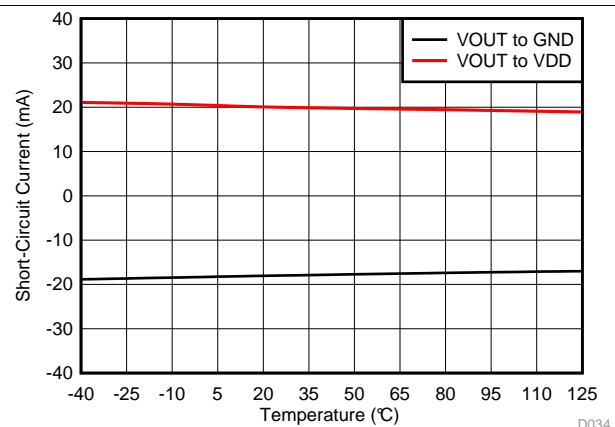


图 40. Shunt-Sense Amplifier Output Short-Circuit Current vs Temperature

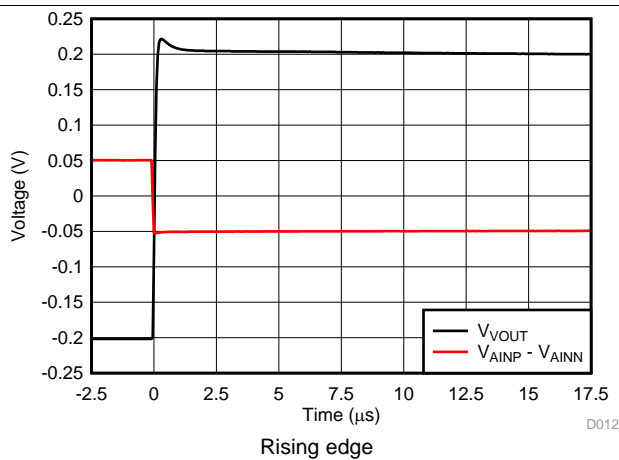


图 41. Shunt-Sense Amplifier Small-Signal Settling Time

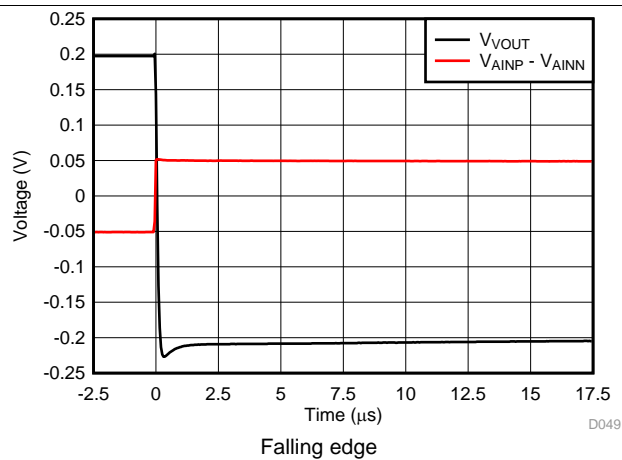


图 42. Shunt-Sense Amplifier Small-Signal Settling Time

## Typical Characteristics (接下页)

at  $V_{DD} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

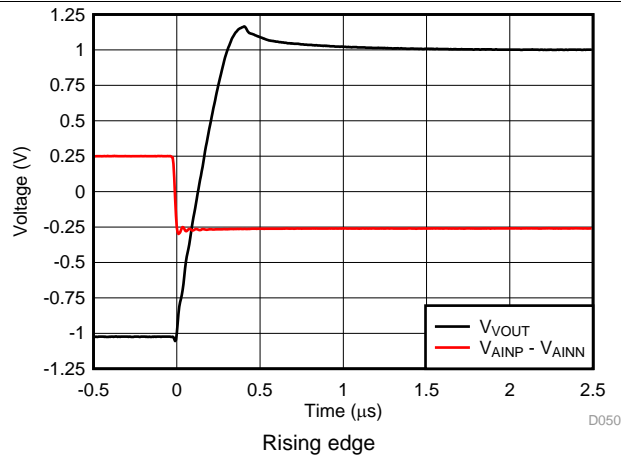


图 43. Shunt-Sense Amplifier Large-Signal Settling Time

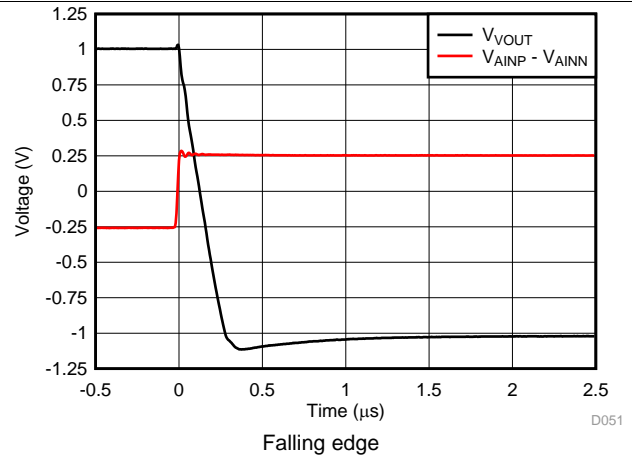


图 44. Shunt-Sense Amplifier Large-Signal Settling Time

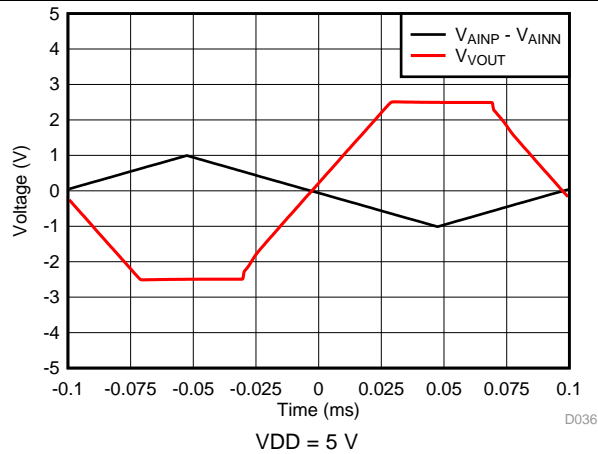


图 45. Shunt-Sense Amplifier Overload Recovery Response

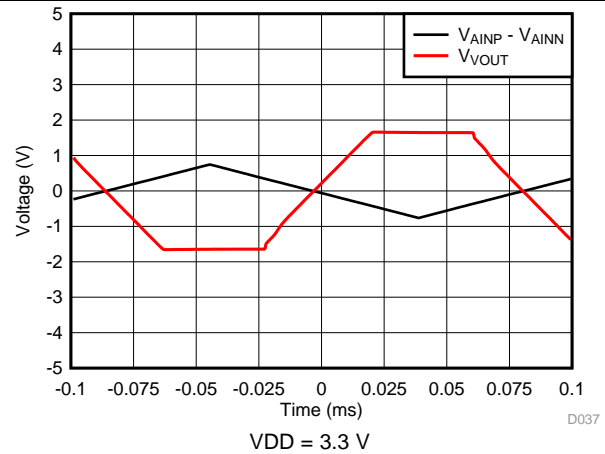


图 46. Shunt-Sense Amplifier Overload Recovery Response

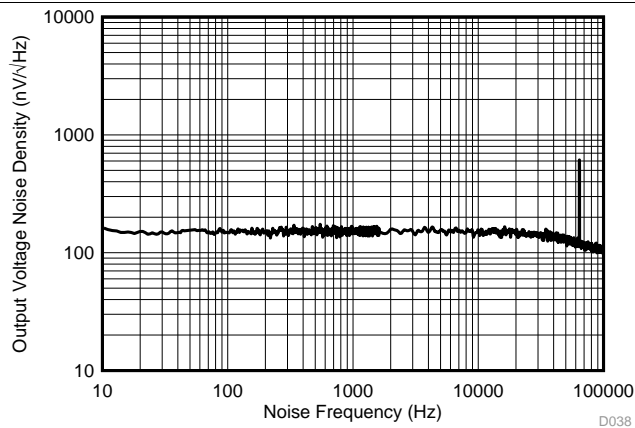


图 47. Shunt-Sense Amplifier Output Voltage Noise Density vs Noise Frequency

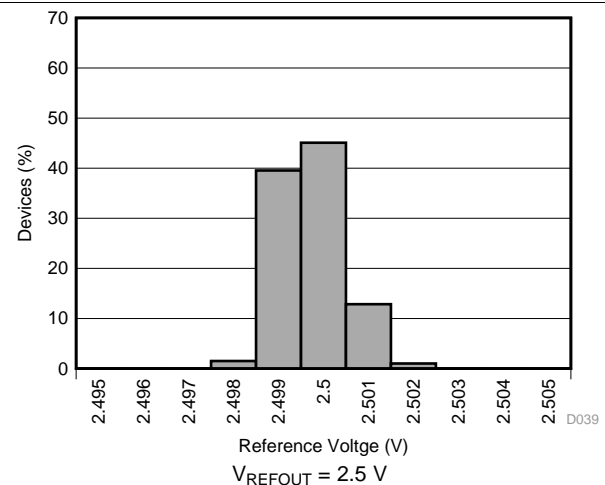


图 48. Reference Voltage Histogram

## Typical Characteristics (接下页)

at VDD = 5 V and T<sub>A</sub> = 25°C (unless otherwise noted)

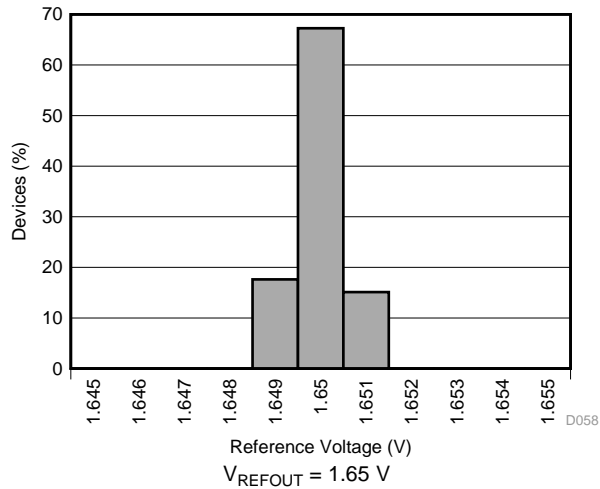


图 49. Reference Voltage Histogram

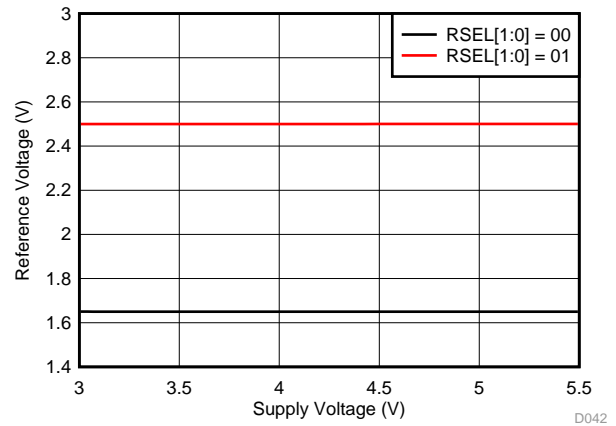


图 50. Reference Voltage vs Supply Voltage

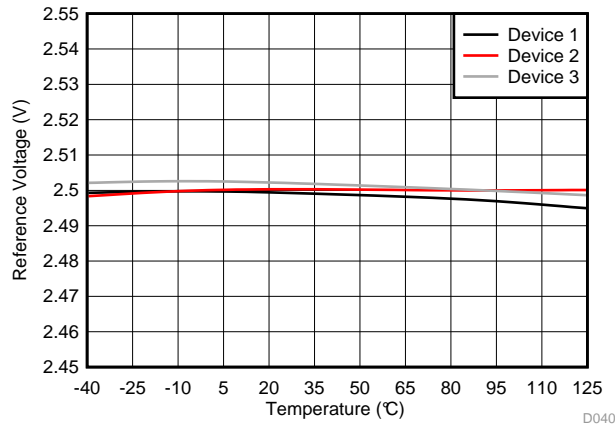


图 51. Reference Voltage vs Temperature

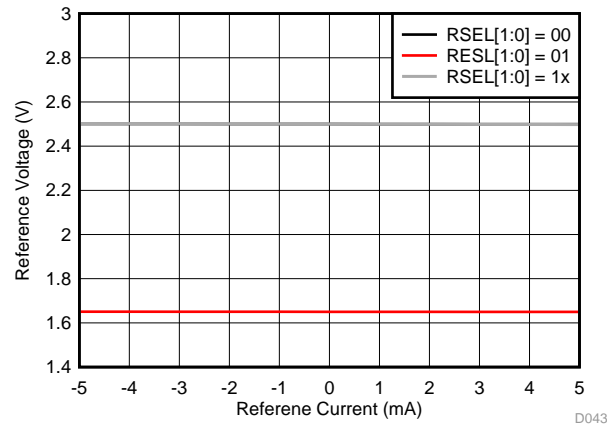


图 52. Reference Voltage vs Reference Output Current

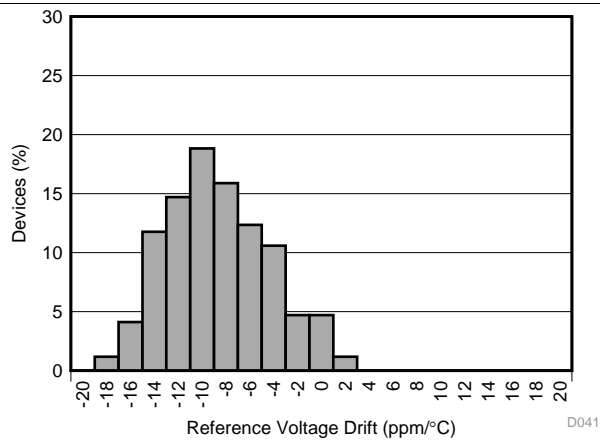


图 53. Reference Voltage Drift Histogram

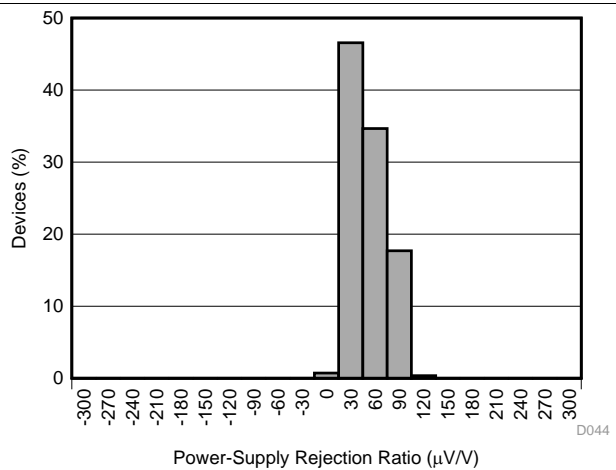


图 54. Reference Voltage PSRR Histogram

## Typical Characteristics (接下页)

at VDD = 5 V and T<sub>A</sub> = 25°C (unless otherwise noted)

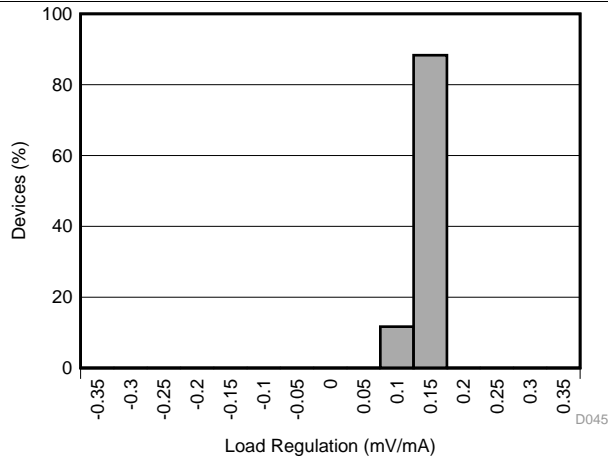


图 55. Reference Voltage Load Regulation Histogram

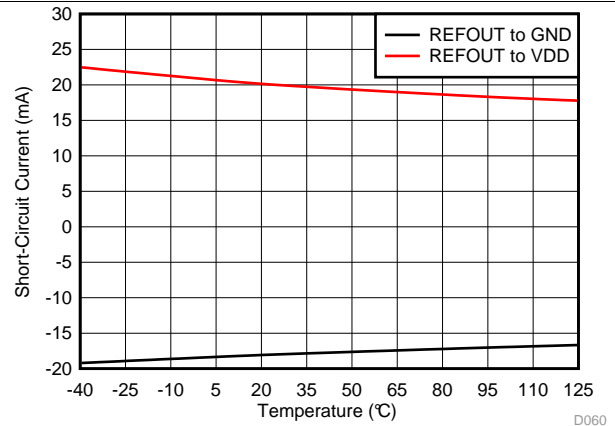


图 56. Reference Short-Circuit Current vs Temperature

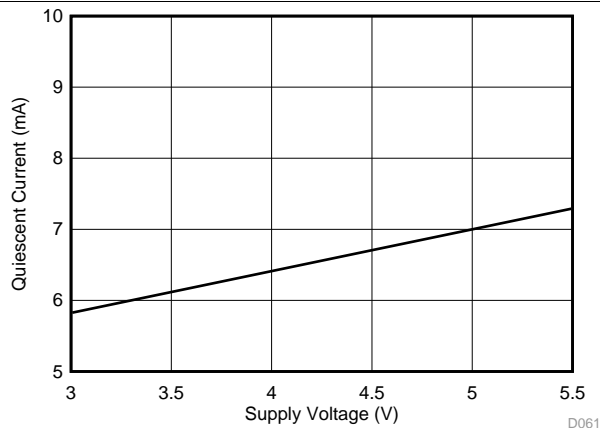


图 57. Quiescent Current vs Supply Voltage

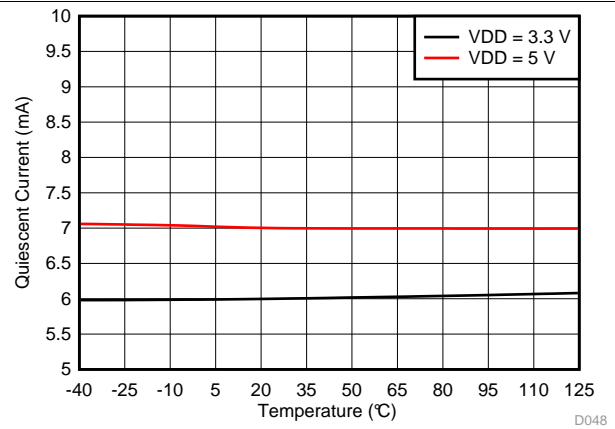


图 58. Quiescent Current vs Temperature

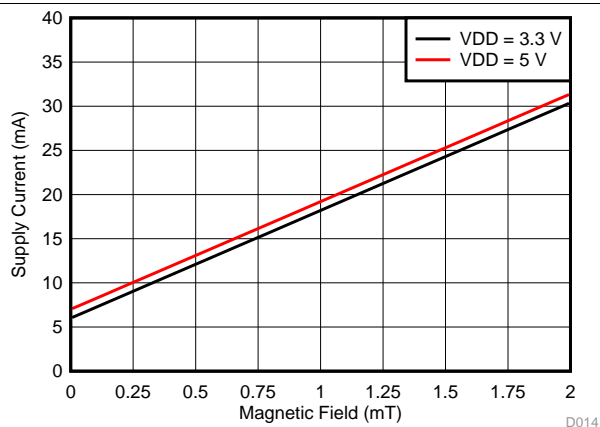


图 59. Supply Current vs Magnetic Field

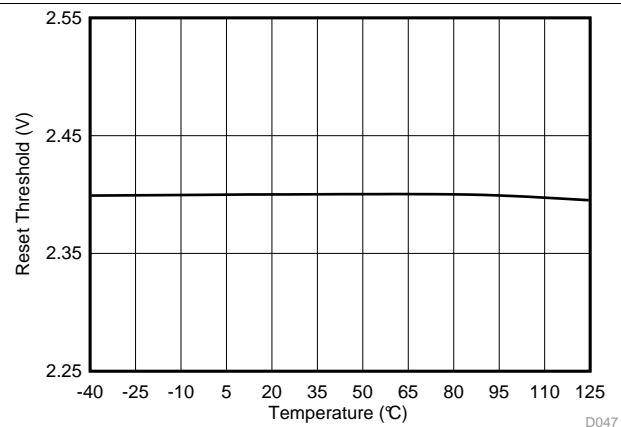


图 60. Power-On Reset Threshold vs Temperature





## 7.3 Feature Description

### 7.3.1 Fluxgate Sensor Front-End

The following sections describe the functional blocks and features of the integrated fluxgate sensor front-end.

#### 7.3.1.1 Fluxgate Sensor

The fluxgate sensor of the DRV425 is uniquely suited for high-performance magnetic-field sensors because of the high sensitivity, low noise, and low offset of the sensor. The fluxgate principle relies on repeatedly driving the sensor in and out of saturation; therefore, the sensor is free of any significant magnetic hysteresis. The feedback loop accurately drives a compensation current through the integrated compensation coil and drives the magnetic field at the sensor back to zero. This approach supports excellent gain stability and high linearity of the measurement.

The DRV425 package is free of any ferromagnetic materials in order to prevent magnetization by external fields and to obtain accurate and hysteresis-free operation. Select non-magnetizable materials for the printed circuit board (PCB) and passive components in the direct vicinity of the DRV425; see the [Layout Guidelines](#) section for more details.

The orientation and the sensitivity axis of the fluxgate sensor is indicated by a dashed line on the top of the package, as shown in [图 61](#). [图 61](#) also shows the location of the sensor inside the package.

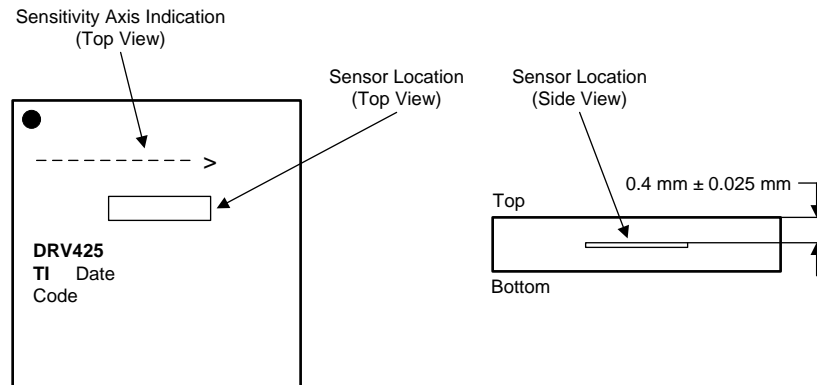


图 61. Magnetic Sensitivity Direction of the Integrated Fluxgate Sensor

The sensitivity of the fluxgate sensor is a vector function of its sensitivity axis and the magnetic field orientation. [图 62](#) shows the output of the DRV425 in dependency of the orientation of the device to a constant magnetic field.

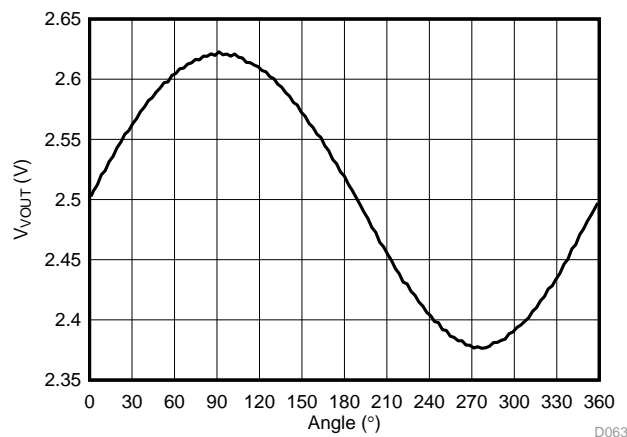


图 62. DRV425 Output vs Magnetic Field Orientation

## Feature Description (接下页)

### 7.3.1.2 Bandwidth

The small-signal bandwidth of the DRV425 is determined by the behavior of the compensation loop versus frequency. The implemented integrator limits the bandwidth of the loop to provide stable response. Use the digital input pin BSEL to select the bandwidth. For a shunt resistor of 22 Ω and BSEL = 0, the bandwidth is 32 kHz; for BSEL = 1, the bandwidth is 47 kHz.

Bandwidth can be reduced by increasing the value of the shunt resistor because the shunt resistor and the compensation coil resistance form a voltage divider. The reduced bandwidth (BW) can be calculated using [公式 2](#):

$$BW = \frac{R_{COIL} + 22\ \Omega}{R_{COIL} + R_{SHUNT}} \times BW_{22\ \Omega} = \frac{122\ \Omega}{100\ \Omega + R_{SHUNT}} \times BW_{22\ \Omega}$$

where

- $R_{COIL}$  = internal compensation coil resistance (100 Ω),
- $R_{SHUNT}$  = external shunt resistance, and
- $BW_{22\Omega}$  = sensor bandwidth with  $R_{SHUNT} = 22\ \Omega$  (depending on the BSEL setting) (2)

The bandwidth for a given shunt resistor value can also be calculated using the *DRV425 System Parameter Calculator*, [SLOC331](#). For large magnetic fields ( $B > 500\ \mu T$ ), the effective bandwidth of the sensor is limited by fluxgate saturation effects. For a magnetic signal with a 2-mT amplitude, the large-signal bandwidth is 10 kHz with BSEL = 0 or 15 kHz with BSEL = 1.

Although the analog output responds slowly to large fields, a magnetic field with a magnitude of 1.6 mT (or higher) beyond the measurement range of the DRV425 triggers the ERROR pin within 4 μs to 6 μs. See the [Magnetic Field Range, Overrange Indicator, and Error Flag](#) section for more details.

### 7.3.1.3 Differential Driver for the Internal Compensation Coil

The differential compensation coil driver provides the current for the internal compensation coil at the DRV1 and DRV2 pins. The driver is capable of sourcing up to ±250 mA with a 5-V supply or up to ±150 mA in 3.3-V mode. The current capability is not internally limited. The actual value of the compensation coil current depends on the magnetic field strength and is limited by the sum of the resistance of the internal compensation coil and the external shunt resistor value. The internal compensation coil resistance depends on temperature (see [图 17](#)) and must be taken into account when dimensioning the system. Select the value of the shunt resistor to avoid OR pin trip levels in normal operation.

The common-mode voltage of the compensation coil driver outputs is set by the RSEL pins (see the [Voltage Reference](#) section). Thus, the common-mode voltage of the shunt-sense amplifier is matched if the internal reference is used.

Consider the polarity of the compensation coil connection to the output of the compensation coil driver. If the polarity is incorrect, then the driver output drives to the power-supply rails, even at low primary-current levels. In this case, interchange the connection of the DRV1 and DRV2 pins to the compensation coil.

## Feature Description (接下页)

### 7.3.1.4 Magnetic Field Range, Overrange Indicator, and Error Flag

The measurement range of the DRV425 is determined by the amount of current driven into the compensation coil and the output voltage range of the shunt-sense amplifier. The maximum compensation current is limited by the supply voltage and the series resistance of the compensation coil and the shunt.

The magnetic field range is adjusted with the external shunt resistor. The *DRV425 System Parameter Calculator*, [SLOC331](#) provides the maximum shunt resistor values depending on the supply voltage (VDD) and the selected reference voltage (V<sub>REFIN</sub>) for various magnetic field ranges.

For proper operation at a maximum field (B<sub>MAX</sub>), choose a shunt resistor (R<sub>SHUNT</sub>) using [公式 3](#)

$$R_{SHUNT} \leq \frac{\min((VDD - V_{REFIN}), V_{REFIN}) - 0.085 \text{ V}}{B_{MAX} \times 12.2 \text{ A/T} \times 4 \text{ V/V}}$$

where

- VDD = minimum supply voltage of the DRV425 (V),
- V<sub>REFIN</sub> = common-mode voltage of the shunt-sense amplifier (V), and
- B<sub>MAX</sub> = desired magnetic field range (T)

(3)

Alternatively, to adjust the output voltage of the DRV425 for a desired maximum voltage (V<sub>VOUTMAX</sub>), use [公式 4](#):

$$R_{SHUNT} \leq \frac{V_{VOUTMAX} - V_{REFIN}}{B_{MAX} \times 12.2 \text{ A/T} \times 4 \text{ V/V}}$$

where

- V<sub>VOUTMAX</sub> = desired maximum output voltage at VOUT pin (V), and
- B<sub>MAX</sub> = desired magnetic field range (T)

(4)

To avoid railing of the compensation coil driver, assure that [公式 5](#) is fulfilled:

$$\frac{B_{MAX} \times (R_{COIL} + R_{SHUNT}) \times 12.2 \text{ A/T}}{2} + 0.1 \text{ V} \leq \min((VDD - V_{REFIN}), V_{REFIN})$$

where

- B<sub>MAX</sub> = desired magnetic field range (T),
- R<sub>COIL</sub> = compensation coil resistance (Ω),
- VDD = minimum supply voltage of the DRV425 (V), and
- V<sub>REFIN</sub> = selected internal reference voltage value (V)

(5)

The *DRV425 System Parameter Calculator*, [SLOC331](#) is designed to assist with selecting the system parameters.

The DRV425 offers two diagnostic output pins to detect large fields that exceed the measurement range of the sensor: the overrange indicator (OR) and the ERROR flag.

In normal operation, the DRV425 sensor feedback loop compensates the magnetic field inside the fluxgate to zero. Therefore, a large field inside the fluxgate indicates that the feedback loop is not properly working and the sensor output is invalid. To detect this condition, the ERROR pin is pulled low if the internal field exceeds 1.6 mT. The ERROR output is suppressed for 4 μs to 6 μs to prevent an undesired reaction to transients or noise. For static and slowly varying ambient fields, the ERROR pin triggers when the ambient field exceeds the sensor measurement range by more than 1.6 mT. For dynamic magnetic fields that exceed the sensor bandwidth as specified in the [Specifications](#) section, the feedback loop response is too slow to accurately compensate the internal field to zero. Therefore, high-frequency fields can trigger the ERROR pin, even if the ambient field does not exceed the measurement range by 1.6 mT.

In addition, the low-active overrange pin (OR) indicates railing of the output of the shunt-sense amplifier. The OR output is suppressed for 2.5 μs to 3.5 μs to prevent an undesired reaction to transients or noise. The OR pin trip level refers to the output voltage value of the shunt-sense amplifier as specified in the [Specifications](#) section. Use [公式 3](#) and [公式 4](#) to adjust the OR pin behavior to the specific system-level requirements.

Both the ERROR and OR pins are open-drain outputs that require an external pullup resistor. Connect both pins together with a single pullup resistor to provide a single diagnostic flag, if desired.

## Feature Description (接下页)

Based on the *DRV425 System Parameter Calculator*, [SLOC331](#), for a design for a  $\pm 2$ -mT magnetic field input range with a supply of 5 V ( $\pm 5\%$ ), a shunt resistor value of  $22\ \Omega$  is selected and [图 63](#) shows the status of the diagnostic flags in the resulting three operation ranges.

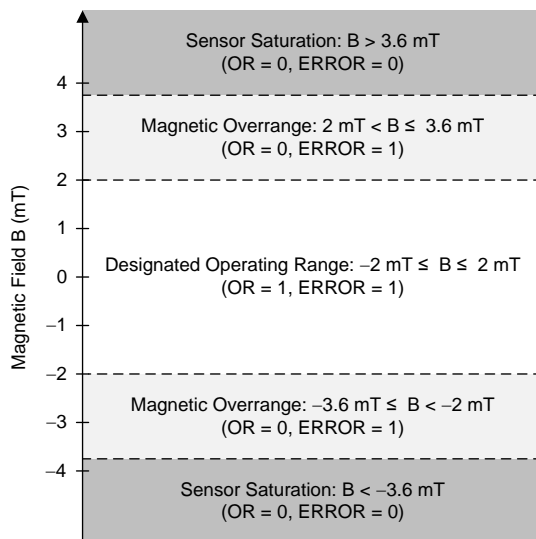


图 63. Magnetic Field Range of the DRV425 (VDD = 5 V and  $R_{SHUNT} = 22\ \Omega$ )

With the proper  $R_{SHUNT}$  value, the differential amplifier output rails and activates the overrange flag (OR = 0) when the magnetic field exceeds the designated operating range. For fields that exceed the measurement range of the DRV425 by  $\geq 1.6$  mT, the fluxgate is permanently saturated and the ERROR pin is pulled low. In this condition, the fluxgate sensor does not provide a valid output value and, therefore, the output VOUT of the DRV425 must be ignored. In applications where the ERROR pin cannot be separately monitored, combining the VOUT and ERROR outputs is recommended (as shown in [图 64](#)) to indicate a magnetic field outside of the sensor range by pulling the output of the DRV425 to ground.

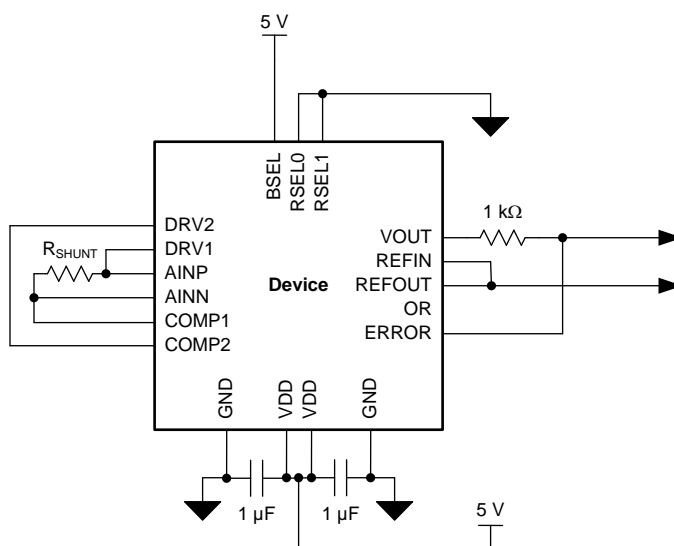


图 64. Field Overrange Detection Using a Combined VOUT and ERROR Pin

## Feature Description (接下页)

### 7.3.2 Shunt-Sense Amplifier

The compensation coil current creates a voltage drop across the external shunt resistor,  $R_{SHUNT}$ . The internal differential amplifier senses this voltage drop. This differential amplifier offers wide bandwidth and a high slew rate. Excellent dc stability and accuracy result from a chopping technique. The voltage gain is 4 V/V, set by precisely-matched and thermally-stable internal resistors.

Both the AINN and AINP differential amplifier inputs are connected to the external shunt resistor. This shunt resistor, in series with the internal 10-k $\Omega$  input resistors of the shunt sense amplifier, causes an additional gain error. Therefore, for best common-mode rejection performance, place a dummy shunt resistor ( $R_5$ ) with a value higher than the shunt resistor in series with the REFIN pin to restore the matching of both resistor dividers, as shown in 图 65.

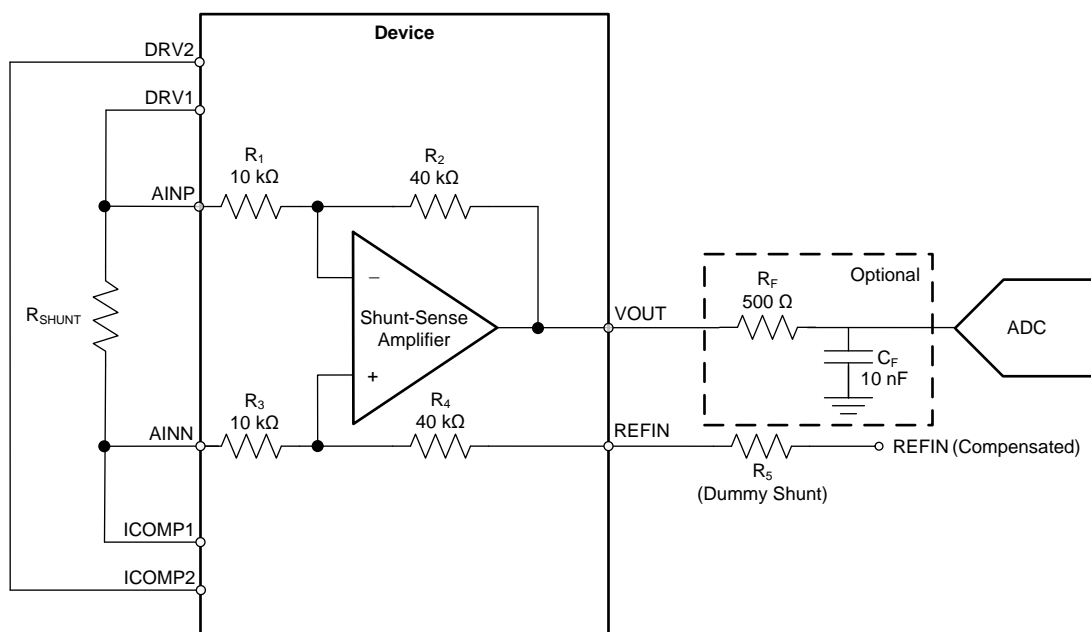


图 65. Internal Difference Amplifier with an Example of a Decoupling Filter

For an overall gain of 4 V/V, calculate the value of  $R_5$  using 公式 6:

$$4 = \frac{R_2}{R_1} = \frac{R_4 + R_5}{R_{SHUNT} + R_3}$$

where:

- $R_2 / R_1 = R_4 / R_3 = 4$ ,
- $R_5 = R_{SHUNT} \times 4$

(6)

If the input signal is large, the amplifier output drives close to the supply rails. The amplifier output is able to drive the input of a successive approximation register (SAR) analog-to-digital converter (ADC). For best performance, add an RC low-pass filter stage between the shunt-sense amplifier output and the ADC input. This filter limits the noise bandwidth and decouples the high-frequency sampling noise of the ADC input from the amplifier output. For filter resistor  $R_F$  and filter capacitor  $C_F$  values, see the specific converter recommendations in the respective product data sheet.

The shunt-sense amplifier output drives 100 pF directly and shows a 50% overshoot with a 1-nF capacitance. Filter resistor  $R_F$  extends the capacitive load range. Note that with an  $R_F$  of only 20  $\Omega$ , the load capacitor must be either less than 1 nF or more than 33 nF to avoid overshoot; with an  $R_F$  of 50  $\Omega$ , this transient area is avoided.

## Feature Description (接下页)

Reference input REFIN is the common-mode voltage node for the output signal VOUT. Use the internal voltage reference of the DRV425 by connecting the REFIN pin to the reference output REFOUT. To avoid mismatch errors, use the same reference voltage for REFIN and the ADC. Alternatively, use an ADC with a pseudo-differential input, with the positive input of the ADC connected to VOUT and the negative input connected to REFIN of the DRV425.

### 7.3.3 Voltage Reference

The internal precision voltage reference circuit offers low-drift performance at the REFOUT output pin and is used for internal biasing. The reference output is intended to be the common-mode voltage of the output (the VOUT pin) to provide a bipolar signal swing. This low-impedance output tolerates sink and source currents of  $\pm 5$  mA. However, fast load transients can generate ringing on this line. A small series resistor of a few ohms improves the response, particularly for capacitive loads equal to or greater than 1  $\mu$ F.

Adjust the value of the voltage reference output to the power supply of the DRV425 using mode selection pins RSEL0 and RSEL1, as shown in 表 1.

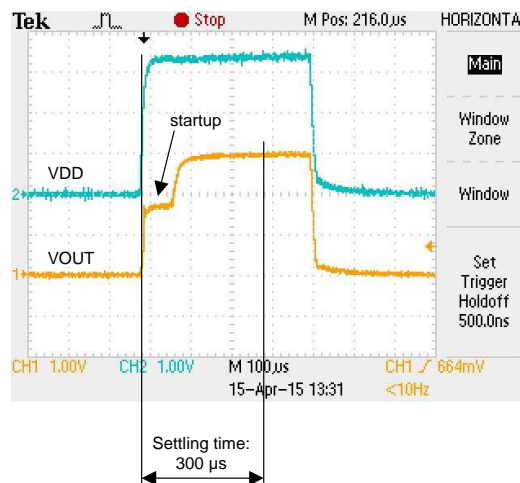
**表 1. Reference Output Voltage Selection**

MODE	RSEL1	RSEL0	DESCRIPTION
$V_{REFOUT} = 2.5$ V	0	0	Use with a sensor module supply of 5 V
$V_{REFOUT} = 1.65$ V	0	1	Use with a sensor module supply of 3.3 V
Ratiometric output	1	x	Provides an output centered on $VDD / 2$

In ratiometric output mode, an internal resistor divider divides the power-supply voltage by a factor of two.

### 7.3.4 Low-Power Operation of the DRV425

In applications with low-bandwidth or low sample-rate requirements, the average power dissipation of the DRV425 can be significantly reduced by powering the device down between measurements. The DRV425 requires 300  $\mu$ s to fully settle the analog output VOUT, as shown in 图 66. To minimize power dissipation, the device can be powered down immediately after acquiring the sample by the ADC.



**图 66. Settling Time of the DRV425 Output VOUT**

## 7.4 Device Functional Modes

The DRV425 is operational when the power supply VDD is applied, as specified in the [Specifications](#) section. The DRV425 has no additional functional modes.

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The DRV425 is a high-sensitivity and high-performance magnetic-field sensor. The analog output of the DRV425 can be processed by a 12- to 16-bit analog to digital converter (ADC). The following sections show examples of DRV425-based applications.

### 8.2 Typical Applications

#### 8.2.1 Linear Position Sensing

The high sensitivity of the fluxgate sensor, combined with the high linearity of the compensation loop and low noise of the DRV425, make the device suitable for high-performance linear-position sense applications. A typical schematic of such a 5-V application using an internal 2.5-V reference is shown in 图 67.

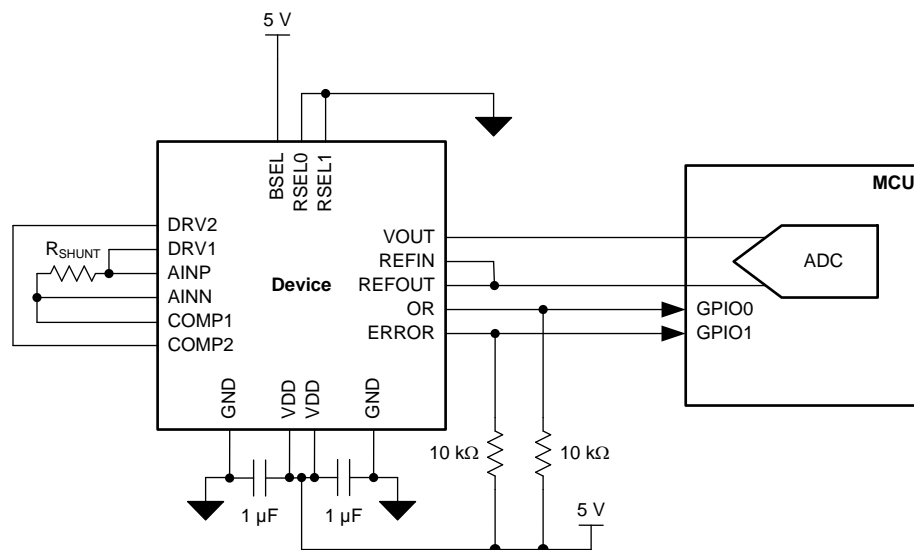


图 67. Simplified Schematic of a DRV425-Based Linear-Position Sensing Application

#### 8.2.1.1 Design Requirements

For the example shown in 图 67, use the parameters listed in 表 2 as a starting point of the design.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Magnetic field range	VDD = 5 V: $\pm 2$ mT (max) VDD = 3.3 V: $\pm 1.3$ mT (max)
Supply voltage, VDD	3.0 V to 5.5 V
Reference voltage, $V_{REFIN}$	Range: GND to VDD If an internal reference is used: 2.5 V, 1.65 V, or VDD / 2
Shunt resistor, $R_{SHUNT}$	Depends on the desired magnetic field range, reference, and supply voltage; see the <i>DRV425 System Parameter Calculator</i> , <a href="#">SLOC331</a> for details.



### 8.2.1.2 Detailed Design Procedure

Use the following procedure to design a solution for a linear-position sensor based on the DRV425:

- Select the proper supply voltage VDD to support the desired magnetic field range (see 表 2 for reference).
- Select the proper reference voltage  $V_{REFIN}$  to support the desired magnetic field range and to match the input voltage specifications of the desired ADC.
- Use the *DRV425 System Parameter Calculator*, [SLOC331](#) (*RangeCalculator* tab) to select the proper shunt resistor value of  $R_{SHUNT}$ .
- The sensitivity drift performance of a DRV425-based linear position sensor is dominated by the temperature coefficient of the external shunt resistor. Select a low-drift shunt resistor for best sensor performance.
- Use the *DRV425 System Parameter Calculator*, [SLOC331](#) (*Problems Detected Table in DRV425 System Parameters* tab) to verify the system response.

The amplitude of the magnetic field is a function of distance to and the shape of the magnet, as shown in 图 69. If the magnetic field to be measured exceeds 3.6 mT, see the datasheet of the magnet to calculate the appropriate minimum distance to the DRV425 to avoid saturating the fluxgate sensor.

The high sensitivity of the DRV425 may require shielding of the sensing area to avoid influence of undesired magnetic field sources (such as the earth magnetic field). Alternatively, an additional DRV425 can be used to perform difference measurement to cancel the influence of a static magnetic field source, as shown in 图 68. 图 70 shows the differential voltage generated by two DRV425 devices in such a circuit.

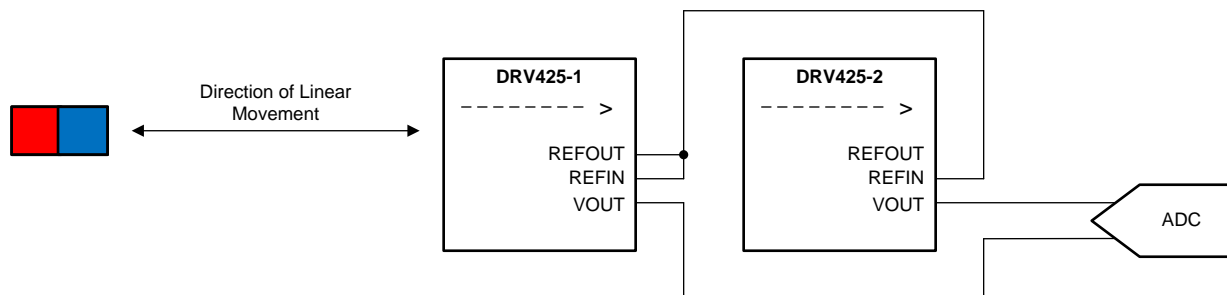


图 68. Differential Linear-Position Sensing Using Two DRV425 Devices

### 8.2.1.3 Application Curves

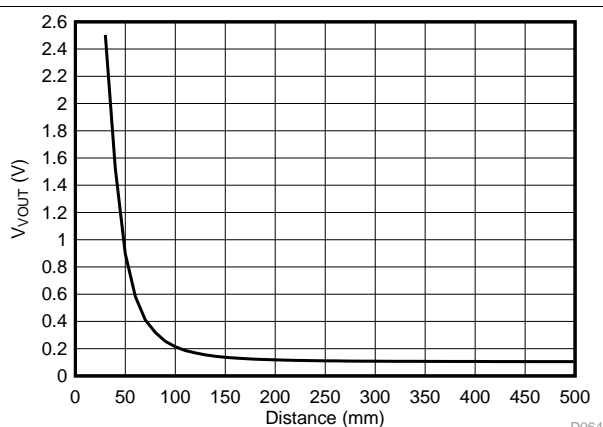


图 69. Analog Output Voltage of the DRV425 vs Distance to the Magnet

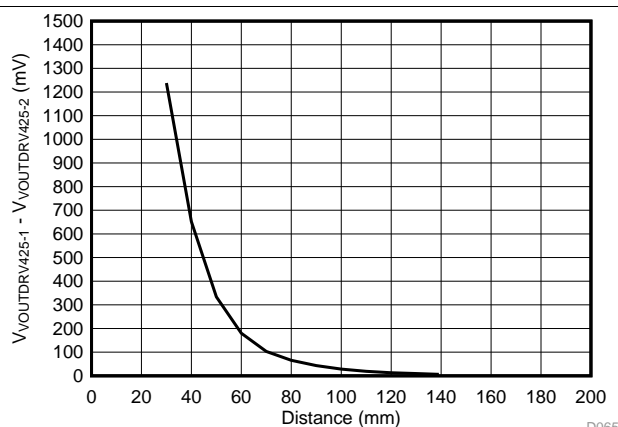


图 70. Difference Between Two DRV425 Outputs vs Distance to the Magnet

## 8.2.2 Current Sensing in Busbars

In existing applications that use busbars for power distribution, closed-loop current modules are usually used to accurately measure and control the current. These modules are usually bulky because of the required large magnetic core. Additionally, because the compensation current generated inside the module is proportional to the usually high busbar current, the power dissipation of this solution is usually as high as several watts.

图 71 shows an alternative approach with two DRV425 devices. If a hole is drilled in the middle of the busbar, the current is split in two equal parts that generate magnetic field gradients with opposite directions inside the hole. These magnetic fields are termed  $B_R$  and  $B_L$  in 图 72. The opposite fields cancel each other out in the middle of the hole. The high sensitivity and linearity of two DRV425 devices positioned at the same distance from the middle of the hole allow the small opposite fields to be sensed and the current measured with high-accuracy levels. The differential measurement rejects outside fields that generate a common-mode error that is subtracted at the output.

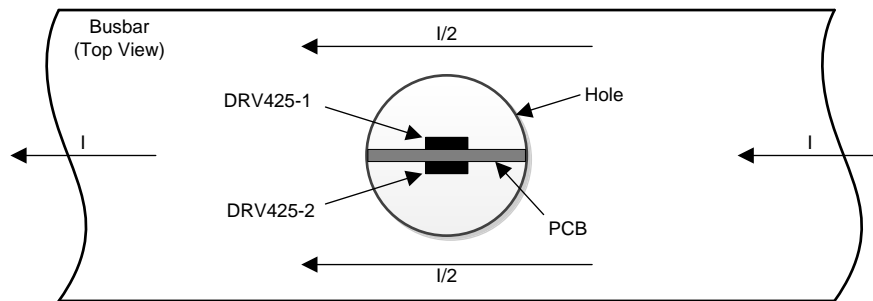


图 71. DRV425-Based Busbar Current Sensing

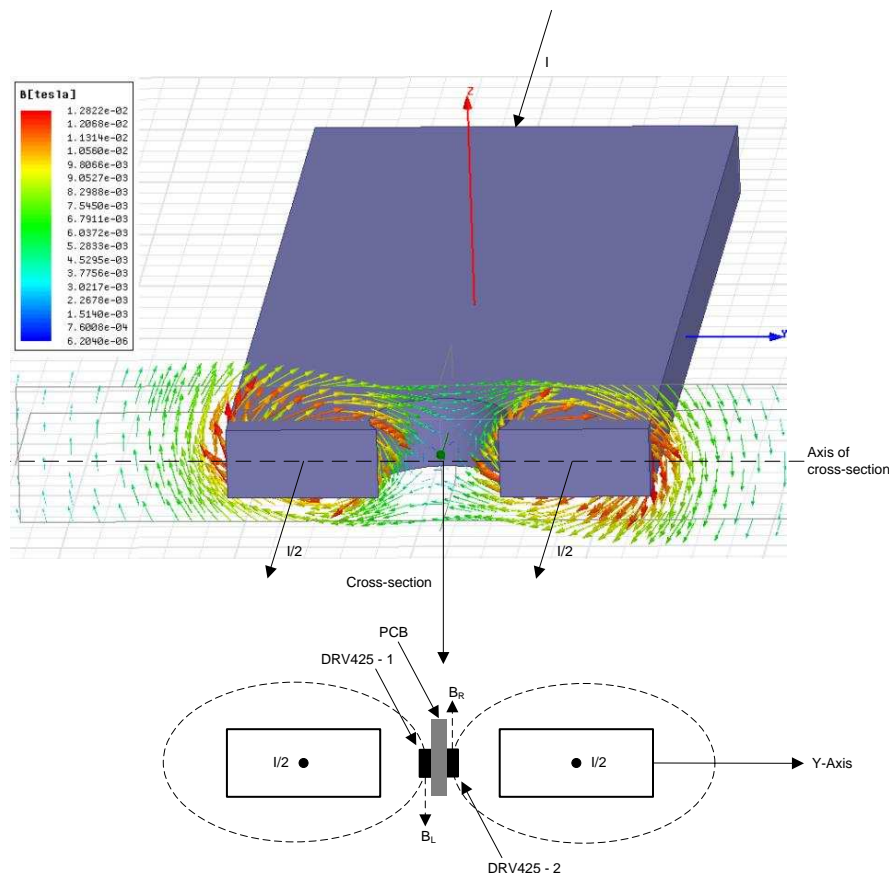


图 72. Magnetic Field Distribution Inside a Busbar Hole



In 图 73, the feedback loops of both DRV425 sensors are combined to directly produce a differential output  $V_{DIFF}$  that is proportional to the sensed magnetic field difference inside the busbar hole. Both compensation coils are connected in series and are driven from a single side of the compensation coil driver (the DRV1 pins of each DRV425). Therefore, both driver stages ensure that a current proportional to the magnetic fields  $B_R$  and  $B_L$  is driven through the respective compensation coil. The difference in current through both compensation coils, and thus the difference field between the sensors, flows through resistor  $R_3$  and is sensed by the shunt-sense amplifier of U2. The current proportional to the common-mode field inside the busbar hole flows through  $R_1$  and  $R_2$  and is sensed by the shunt-sense amplifier of U1.

Use the output  $V_{CM}$  to verify that the sensors are correctly positioned in the busbar hole with the following steps:

1. Measure  $V_{CM}$  with no current flow through the busbar and the PCB in the middle of the busbar hole. This value is the offset voltage  $V_{OFFSET}$ . The value of  $V_{OFFSET}$  only depends on stray fields and varies little with the absolute position of the sensors.
2. Apply current through the busbar and move the PCB along the y-axis in the busbar hole, as shown in 图 72. The PCB is in the center of the hole if  $V_{CM} = V_{OFFSET}$ .

The sensitivity drift performance of the circuit shown in 图 73 is dominated by the temperature coefficient of the external resistors  $R_1$ ,  $R_2$ , and  $R_3$ . Select low-drift resistors for best sensor performance. For overall system error calculation, also consider the affect of thermal expansion on the PCB and busbar.

The internal voltage reference of the DRV425 cannot be used in this application because of its limited driver capability. The OPA320 (U3) is a low-noise operational amplifier with a short-circuit current capability of  $\pm 65$  mA and is used to support the required compensation current.

The advantage of this solution is its simplicity: the currents are subtracted by the two DRV425 devices without additional components. The series connection of the compensation coils halves the voltage swing and reduces the measurement range of the sensors also by 50%. If a larger sensing range is required, operate the two sensors independently and use a differential amplifier or ADC to subtract both voltage outputs (VOUT).

Use the ERROR outputs for fast overcurrent detection on the system level.

### 8.2.2.3 Application Curves

图 74 and 图 75 show the measurement results on a 16-mm wide and 6-mm thick copper busbar with a 12-mm hole diameter using the circuit shown in 图 73. The two DRV425 devices are placed at a distance of 1 mm from each other on opposite sides of the PCB. The measurement range is  $\pm 500$  A; measurement results are limited by test setup. Independent operation of the two DRV425 sensors increases the measurement range to  $\pm 1000$  A with the same busbar geometry.

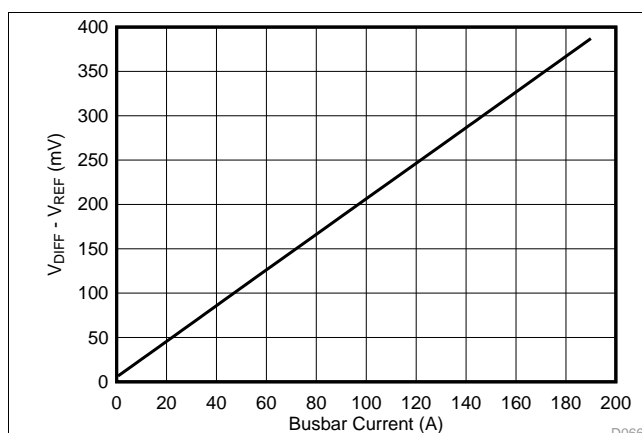


图 74. Analog Output Voltage vs Busbar Current

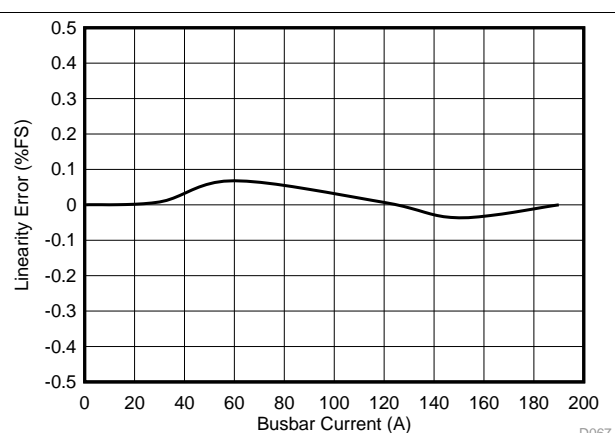


图 75. Linearity Error vs Busbar Current

## 9 Power-Supply Recommendations

### 9.1 Power-Supply Decoupling

Decouple both VDD pins of the DRV425 with 1-μF, X7R-type ceramic capacitors to the adjacent GND pin as illustrated in 图 76. For best performance, place both decoupling capacitors as close to the related power-supply pins as possible. Connect these capacitors to the power-supply source in a way that allows the current to flow through the pads of the decoupling capacitors.

### 9.2 Power-On Start-Up and Brownout

Power-on is detected when the supply voltage exceeds 2.4 V at the VDD pin. At this point, the DRV425 initiates the following start-up sequence:

1. Digital logic starts up and waits for 26 μs for the supply to settle.
2. The fluxgate sensor powers up.
3. The compensation loop is active 70 μs after the supply voltage exceeds 2.4 V.

During this startup sequence, the DRV1 and DRV2 outputs are pulled low to prevent undesired signals on the compensation coil and the ERROR pin is asserted low.

The DRV425 tests for low supply voltages with a brownout voltage level of 2.4 V. Use a power-supply source capable of supporting large current pulses driven by the DRV425, and low-ESR bypass capacitors for a stable supply voltage in the system. A supply drop below 2.4 V that lasts longer than 20 μs generates a power-on reset; the device ignores shorter voltage drops. A voltage drop on the VDD pin to below 1.8 V immediately initiates a power-on reset. After the power supply returns to 2.4 V, the device initiates a start-up cycle.

### 9.3 Power Dissipation

The thermally-enhanced, PowerPAD, WQFN package reduces the thermal impedance from junction to case. This package has a downset lead frame that the die is mounted to. The lead frame has an exposed thermal pad (PowerPAD) on the underside of the package, and provides a good thermal path for heat dissipation.

The power dissipation on both linear outputs DRV1 and DRV2 is calculated with 公式 7:

$$P_{D(DRV)} = I_{DRV} \times (V_{DRV} - V_{SUPPLY})$$

where

- $I_{DRV}$  = supply current as shown in 图 59,
- $V_{DRV}$  = voltage potential on the DRV1 or DRV2 output pin, and
- $V_{SUPPLY}$  = voltage potential closer to  $V_{DRV}$ : VDD or GND

(7)

#### 9.3.1 Thermal Pad

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences the overall heat dissipation. Technical details are described in application report *PowerPad Thermally Enhanced Package*, SLMA002, available for download at [www.ti.com](http://www.ti.com).

## 10 Layout

### 10.1 Layout Guidelines

The unique, integrated fluxgate of the DRV425 has a very high sensitivity to enable designing a closed-loop magnetic-field sensor with best-in-class precision and linearity. Observe proper PCB layout techniques because any current-conducting wire in the direct vicinity of the DRV425 generates a magnetic field that can distort measurements. Common passive components and some PCB plating materials contain ferromagnetic materials that are magnetizable. For best performance, use the following layout guidelines:

- Route current-conducting wires in pairs: route a wire with an incoming supply current next to, or on top of, its return current path. The opposite magnetic field polarity of these connections cancel each other. To facilitate this layout approach, the DRV425 positive and negative supply pins are located next to each other.
- Route the compensation coil connections close to each other as a pair to reduce coupling effects.
- Minimize the length of the compensation coil connections between the DRV1/2 and COMP1/2 pins.
- Route currents parallel to the fluxgate sensor sensitivity axis as illustrated in [Figure 76](#). As a result, magnetic fields are perpendicular to the fluxgate sensitivity and have limited affect.
- Vertical current flow (for example, through vias) generates a field in the fluxgate-sensitive direction. Minimize the number of vias in the vicinity of the DRV425.
- Use nonmagnetic passive components (for example, decoupling capacitors and the shunt resistor) to prevent magnetizing effects near the DRV425.
- Do not use PCB trace finishes with nickel-gold plating because of the potential for magnetization.
- Connect all GND pins to a local ground plane.

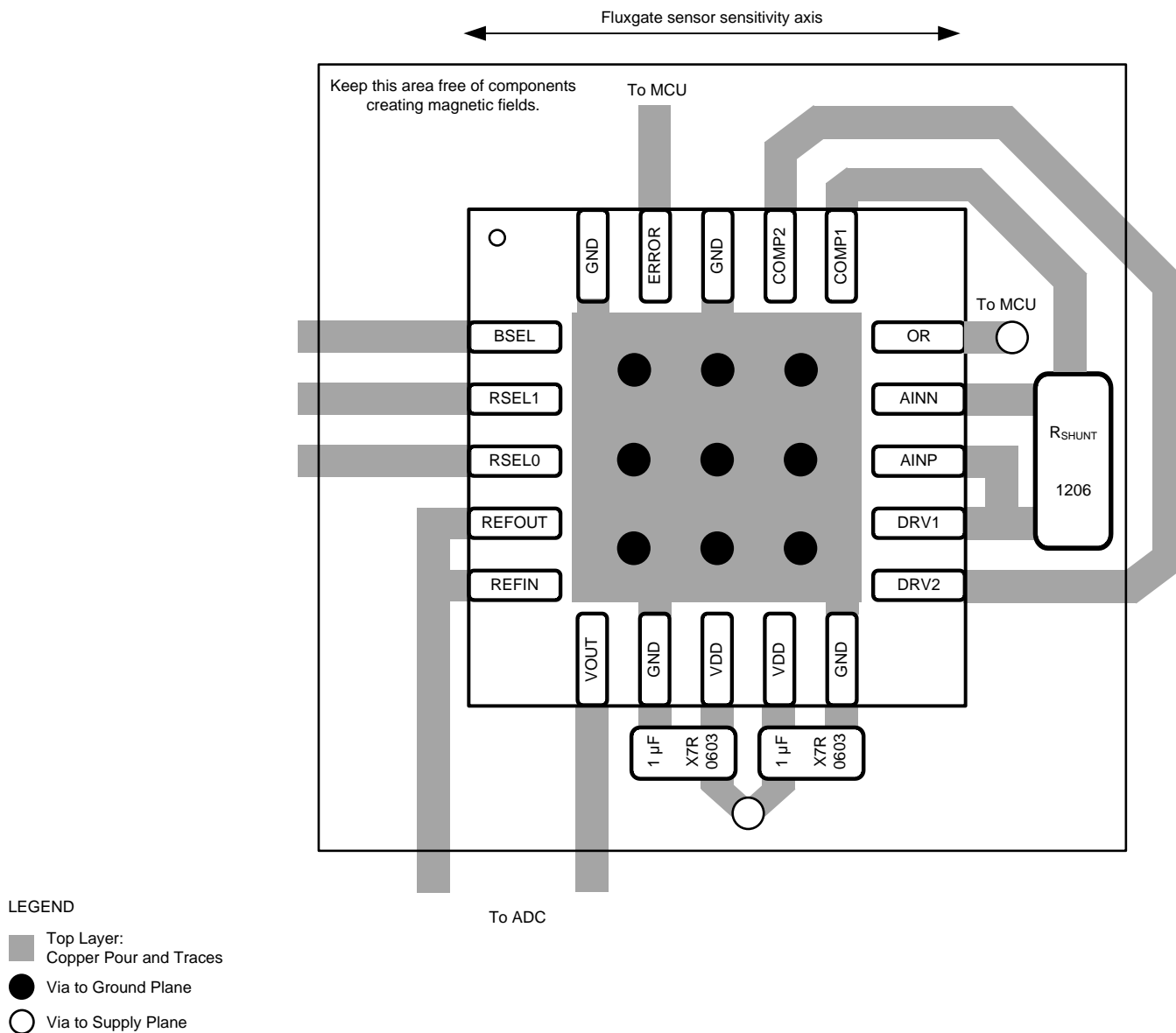
Ferrite beads in series to the power-supply connection reduce interaction with other circuits powered from the same supply voltage source. However, to prevent influence of the magnetic fields if ferrite beads are used, do not place them next to the DRV425.

The reference output (the REFOUT pin) refers to GND. Use a low-impedance and star-type connection to reduce the driver current and the fluxgate sensor current modulating the voltage drop on the ground track. The REFOUT and VOUT outputs are able to drive some capacitive load, but avoid large direct capacitive loading because of increased internal pulse currents. Given the wide bandwidth of the shunt-sense amplifier, isolate large capacitive loads with a small series resistor.

Solder the exposed PowerPAD on the bottom of the package to the ground layer because the PowerPAD is internally connected to the substrate that must be connected to the most-negative potential.

[Figure 76](#) illustrates a generic layout example that highlights the placement of components that are critical to the DRV425 performance. For specific layout examples, see the *DRV425EVM Users Guide*, [SLOU410](#).

## 10.2 Layout Example



**图 76. Generic Layout Example (Top View)**

## 11 器件和文档支持

### 11.1 文档支持

#### 11.1.1 相关文档

《OPA320 数据表》， [SBOS513](#)

《DRV425EVM 用户指南》， [SLOU410](#)

《DRV425 系统参数计算器》， [SLOC331](#)

《PowerPAD 耐热增强型封装》， [SLMA002](#)

### 11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DRV425RTJR</a>	Active	Production	QFN (RTJ)   20	3000   LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	-----> DRV425
DRV425RTJR.A	Active	Production	QFN (RTJ)   20	3000   LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	-----> DRV425
DRV425RTJR.B	Active	Production	QFN (RTJ)   20	3000   LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	-----> DRV425
<a href="#">DRV425RTJT</a>	Last Time Buy	Production	QFN (RTJ)   20	250   SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	-----> DRV425
DRV425RTJT.B	NRND	Production	QFN (RTJ)   20	250   SMALL T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	-----> DRV425

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF DRV425 :**

- Automotive : [DRV425-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## GENERIC PACKAGE VIEW

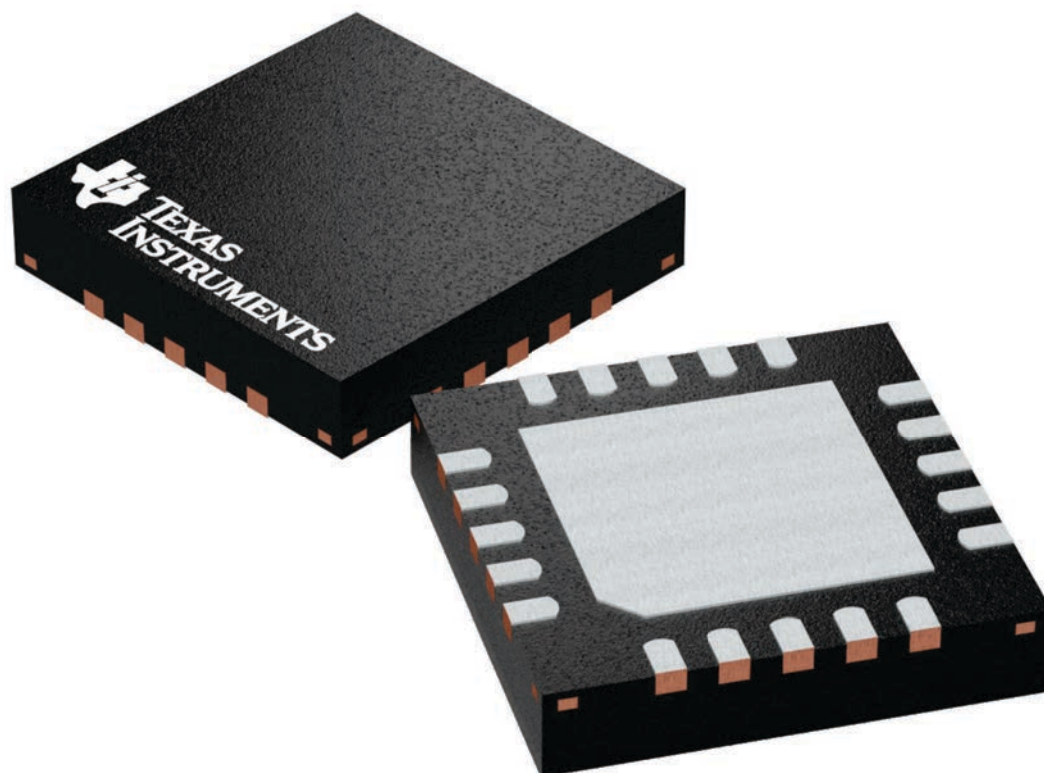
**RTJ 20**

**WQFN - 0.8 mm max height**

4 x 4, 0.5 mm pitch

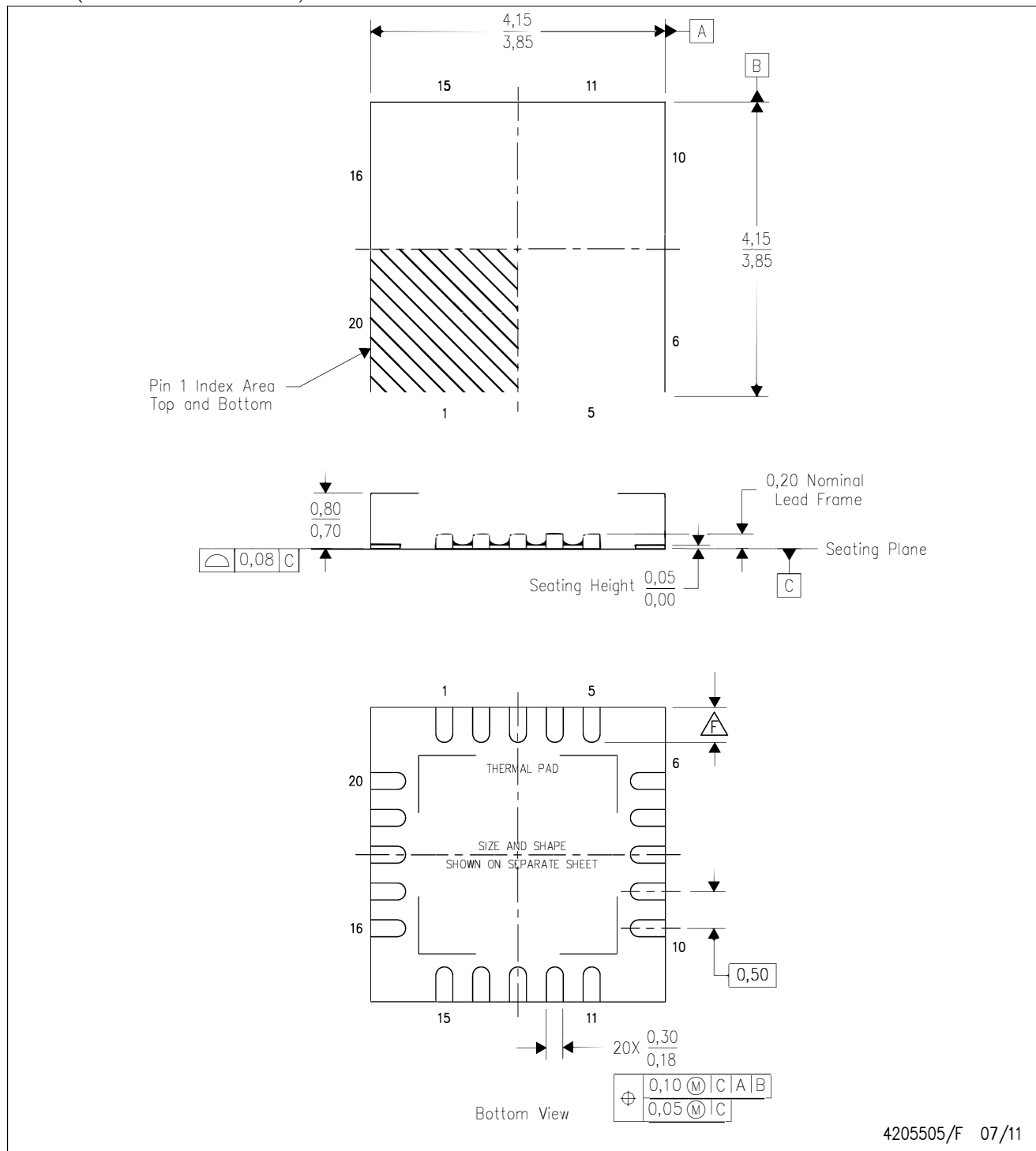
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



RTJ (S-PWQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- ⚠ Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

RTJ (S-PWQFN-N20)

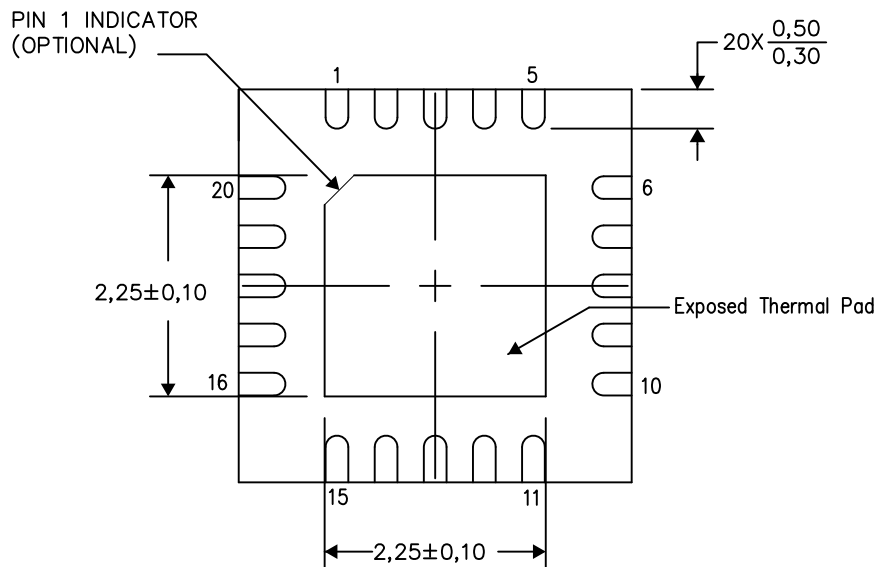
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206256-8/V 05/15

NOTE: All linear dimensions are in millimeters

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
版权所有 © 2025，德州仪器 (TI) 公司