DP83848-HT PHYTER™ 军用级温度单端口 10/100Mbps 以太网物理层收发器

1 特性

- 低功耗 3.3V，0.18µm CMOS 技术
- 低功耗：小于 270mW（典型值）
- 3.3V MAC 接口
- 针对 10/100Mb/s 的自动 MDIX
- 能量检测模式
- 25MHz 时钟输出
- SNI 接口（可配置）
- RMII 修订版本 1.2 接口（可配置）
- MII 串行管理接口（MDC 和 MDIO）
- IEEE 802.3u MII
- IEEE 802.3u 自动协商和并行检测
- IEEE 802.3u ENDEC，10BASE-T 收发器和滤波器
- IEEE 802.3u PCS，100BASE-TX 收发器和滤波器
- IEEE 1149.1 JTAG
- 集成了符合 ANSI X3.263 标准的双绞线物理介质相关 (TP-PMD) 物理子层，该子层具有自适应均衡和基线漂移补偿
- 长达 150 米的无故障运行
- 可编程 LED 支持链路，10/100Mb/s 模式，活动和冲突检测
- 针对完整 PHY 状态的单寄存器访问
- 10/100Mbps 数据包 BIST（内置自检）
- 支持国防、航天和医疗应用
  – 受控基线
  – 同一组装和测试场所
  – 同一制造场所
  – 扩展级温度范围（–55°C 至 150°C）
  – 延长的产品生命周期
  – 延长的产品变更通知
  – 产品可追溯性

2 应用范围

- 汽车和运输
- 工业控制和工厂自动化
- 通用嵌入式应用

3 描述

要求以太网连接的应用的数量持续增加。 随着此类需求的增加，增加的市场需求是应用要求的一个变化。DP83848 被设计用于在恶劣环境中实现以太网连接。这款器件非常适合应用于恶劣环境，例如无线远程基站、汽车、运输和工业控制类应用。

DP83848 是一款高度可靠且功能丰富的稳健耐用型器件，其包含有增强型静电放电 (ESD) 保护、介质无关接口 (MII) 和简化的介质无关接口 (RMII)，可在选择 MPU 方面提供极大的灵活性。

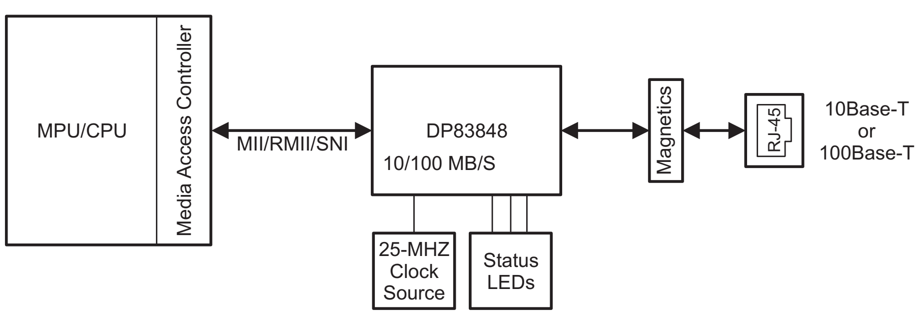
DP83848 特有集成的子层来支持 10BASE-T 和 100BASE-TX 以太网协议，这样确保了与所有其他基于标准的以太网解决方案的兼容性和互操作性。

器件信息[(1)]

器件型号	芯片	芯片尺寸（标称值）
DP83848-HT	KGD (49)	1592µm × 1532µm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 典型系统图



Typical Application

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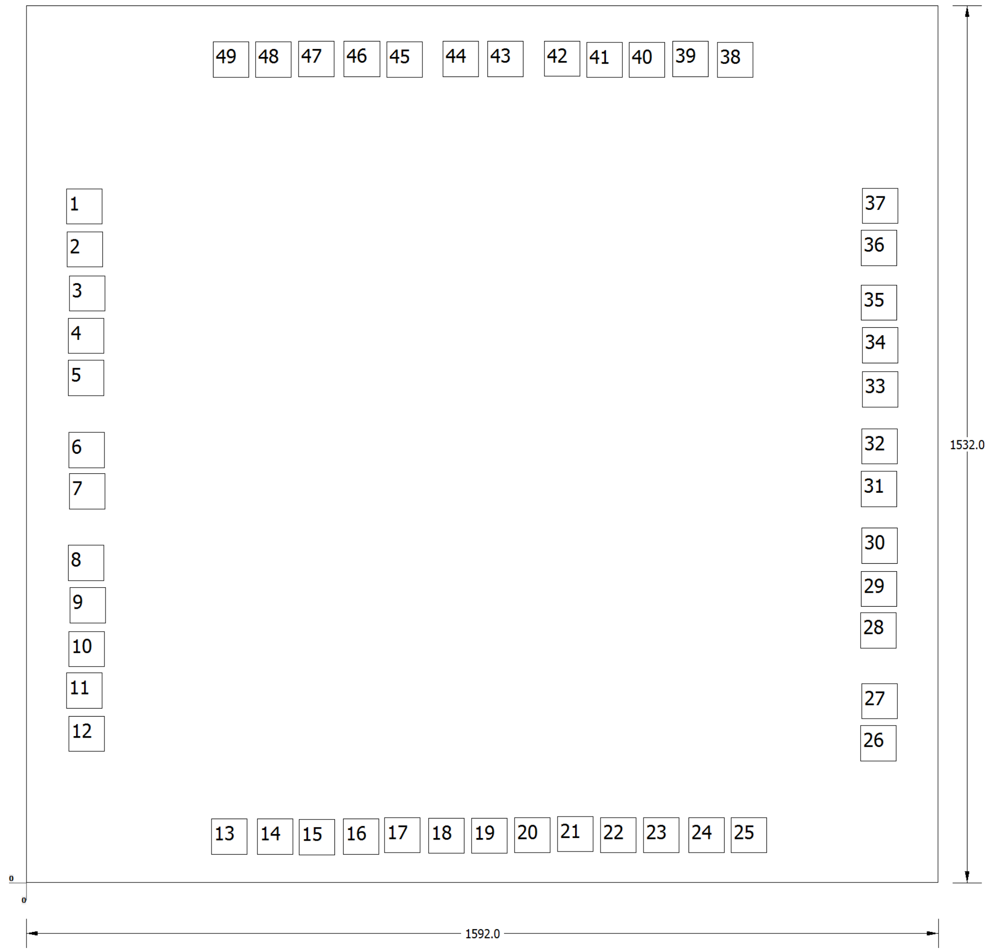
5 修订历史记录

日期	修订版本	注释
2015 年 2 月	*	最初发布版本

6 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils	Silicon with backgrind	Ground	AlCu.5%	0.9 µm



Bond Pin Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
TX_CLK	1	70.339	1149.962	133.368	1212.499
TX_EN	2	71.466	1074.524	134.495	1137.061
TXD_0	3	74.847	997.96	137.875	1060.497
TXD_1	4	72.593	923.648	135.621	986.185
TXD_2	5	72.593	850.461	135.621	912.998
TXD_3/SNI_MODE	6	73.72	724.356	136.748	786.893
PWR_DOWN/INT	7	74.847	652.295	137.875	714.832
TCK	8	72.812	527.247	135.841	589.783
TDO	9	75.657	453.341	138.686	515.878
TMS	10	74.235	376.592	137.263	439.129
TRST	11	69.967	304.108	132.996	366.645
TDI	12	74.235	228.781	137.263	291.318
RD-	13	322.955	49.09	385.984	111.627
RD+	14	402.74	49.09	465.768	111.627
AGND	15	476.319	48.204	539.348	110.741
AGND	16	553.445	49.09	616.473	111.627
TD-	17	625.251	51.748	688.279	114.285
TD+	18	702.376	50.862	765.405	113.399
PFBIN1	19	776.842	50.862	839.87	113.399
AGND	20	852.194	51.748	915.223	114.285
RESERVED	21	927.068	53.532	990.096	116.069
RESERVED	22	1001.534	51.76	1064.562	114.297
AVDD33	23	1076.886	51.76	1139.914	114.297
PFBOUT	24	1155.784	51.76	1218.813	114.297
RBIAS	25	1230.25	51.76	1293.279	114.297
25MHz_OUT	26	1455.826	212.106	1518.855	274.643
LED_ACT/COL/AN_EN	27	1457.926	285.53	1520.954	348.067
LED_SPEED/AN1	28	1455.826	409.302	1518.855	471.839
LED_LINK/AN0	29	1457.291	481.851	1520.319	544.388
RESET_N	30	1457.99	557.373	1521.019	619.91
MDIO	31	1456.591	655.971	1519.619	718.508
MDC	32	1457.99	730.794	1521.019	793.331
IOVDD33	33	1458.752	830.293	1521.781	892.83
X2	34	1458.752	907.287	1521.781	969.824
X1	35	1457.18	981.924	1520.208	1044.461
IOGND	36	1457.18	1076.987	1520.208	1139.524
DGND	37	1458.769	1150.513	1521.797	1213.05
PFBIN2	38	1205.966	1405.764	1268.995	1468.301
RX_CLK	39	1127.754	1407.005	1190.782	1469.542
RX_DV/MII_MODE	40	1052.024	1405.764	1115.053	1468.301
CRS/CRS_DV/LED_CFG	41	978.157	1405.764	1041.185	1468.301
RX_ER/MDIX_EN	42	903.668	1407.625	966.697	1470.162
COL/PHYAD0	43	804.841	1407.148	867.869	1469.685
RXD_0/PHYAD1	44	727.429	1407.148	790.457	1469.685
RXD_1/PHYAD2	45	629.094	1406.451	692.123	1468.988
RXD_2/PHYAD3	46	554.472	1407.148	617.5	1469.685
RXD_3/PHYAD4	47	474.967	1407.148	537.996	1469.685

Bond Pin Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
IOGND	48	399.647	1406.451	462.676	1468.988
IOVDD33	49	326.42	1406.451	389.448	1468.988

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	4.2	V
V_{IN}	DC input voltage	–0.5	V_{CC} + 0.5	V
V_{OUT}	DC output voltage	–0.5	V_{CC} + 0.5	V
T_J	Operating junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	ESD rating (R_{ZAP} = 1.5 kΩ, C_{ZAP} = 100 pF)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		3.6	V
T_A	Operating free-air temperature[2]	–55		150	°C
P_D	Power dissipation		267		mW

(1) Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.
(2) Provided that Thermal Pad is soldered down.

7.4 Thermal Information

THERMAL METRIC[1]		DP83848 PHP 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.74	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	19.5	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	19.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage	Nominal V_{CC}	2			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{CC}$			10	µA
I_{IL}	Input Low Current	V_{IN} = GND			10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA	V_{CC} – 0.5			V
I_{OZ}	TRI-STATE Leakage	$V_{OUT} = V_{CC}$, V_{OUT} = GND			±10	µA
V_{TPTD_100}	100M Transmit Voltage		0.89	1	1.15	V
$V_{TPTDsym}$	100M Transmit Voltage Symmetry				±2%	
VT_{PTD_10}	10M Transmit Voltage		2.17	2.5	2.8	V
C_{IN1}	CMOS Input Capacitance			5		pF
C_{OUT1}	CMOS Output Capacitance			5		pF
SD_{THon}	100BASE-TX Signal detect turnon threshold				1000	mV diff pk-pk
SD_{THoff}	100BASE-TX Signal detect turnoff threshold		200			mV diff pk-pk
V_{TH1}	10BASE-T Receive Threshold				585	mV
I_{dd100}	100BASE-TX (Full Duplex)			81		mA
I_{dd10}	10BASE-T (Full Duplex)			92		mA
I_{dd}	Power Down Mode			14		mA

7.6 AC Timing Specifications

Table 1. Power-Up Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.1.1	Post power-up stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization X1 Clock must be stable for a minimum of 167 ms at power up.	167			ms
T2.1.2	Hardware configuration latching time from power up	Hardware Configuration Pins are described in the Pin Description section X1 Clock must be stable for a minimum of 167 ms at power up.	167			ms
T2.1.3	Hardware configuration pins transition to output drivers			50		ns

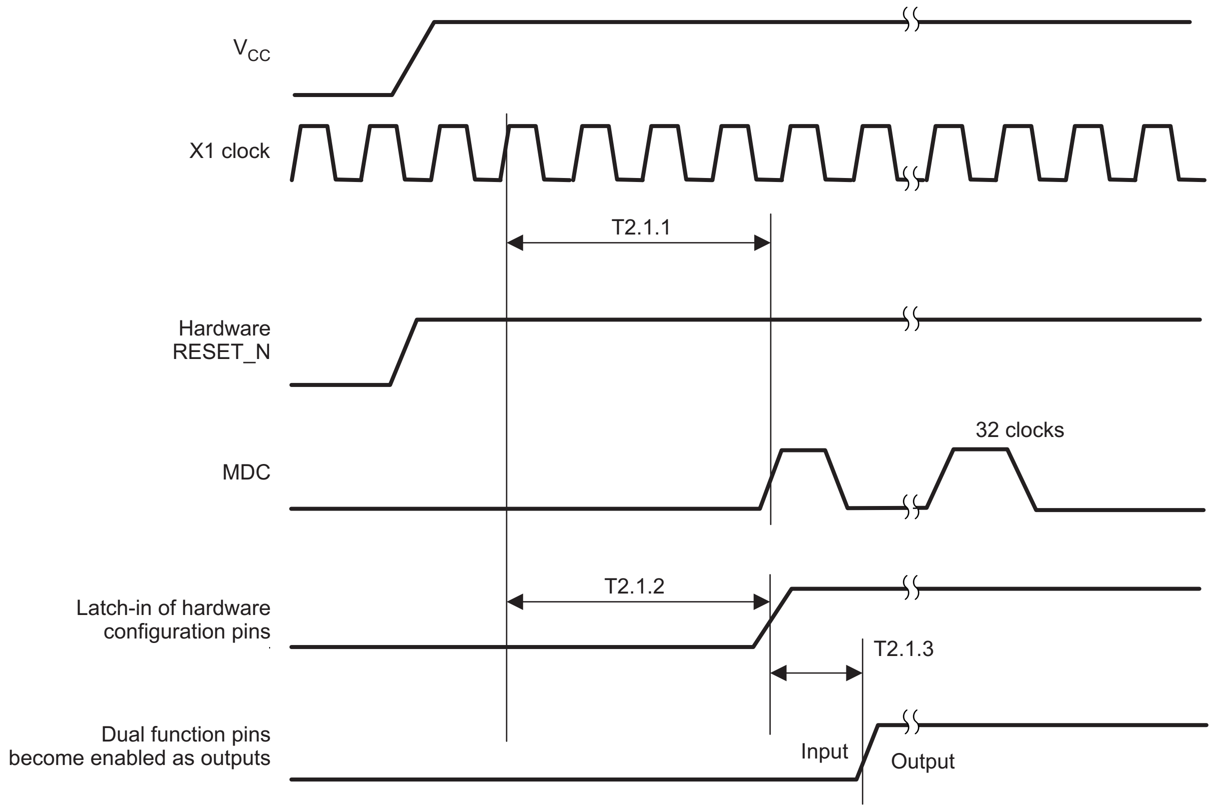


Figure 1. Power-Up Timing

Table 2. Reset Timing

PARAMETER		NOTES(1)	MIN	TYP	MAX	UNIT
T2.2.1	Post RESET Stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization		3		µs
T2.2.2	Hardware configuration latching time from the deassertion of RESET (either soft or hard)			3		µs
T2.2.3	Hardware configuration pins transition to output drivers			50		ns
T2.2.4	RESET pulse width	X1 Clock must be stable for at minimum of 1 µs during RESET pulse low time	1			µs

(1) It is important to choose pull-up and/or pull-down resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch-in the proper value prior to the pin transitioning to an output driver.

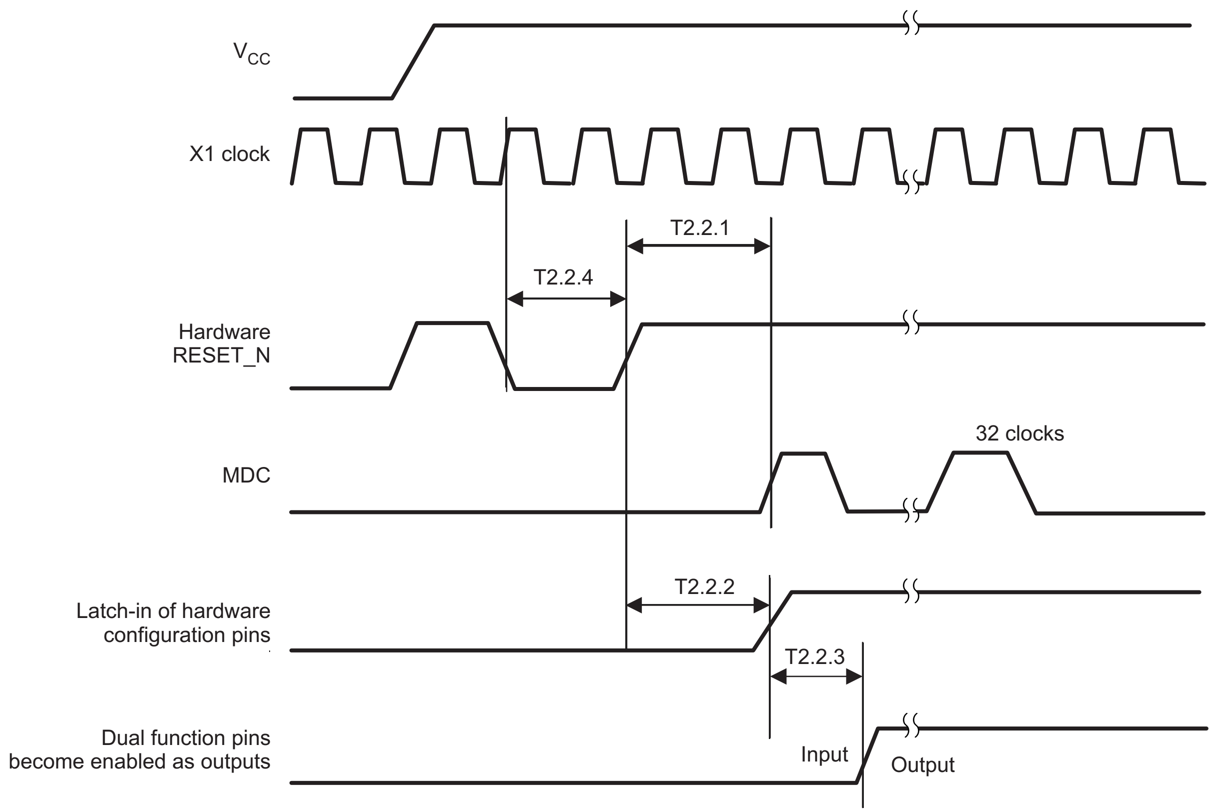


Figure 2. Reset Timing

Table 3. MII Serial Management Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.3.1	MDC to MDIO (output) delay time		0		30	ns
T2.3.2	MDIO (input) to MDC setup time		10			ns
T2.3.3	MDIO (input) to MDC hold time		10			ns
T2.3.4	MDC frequency			2.5	25	MHz

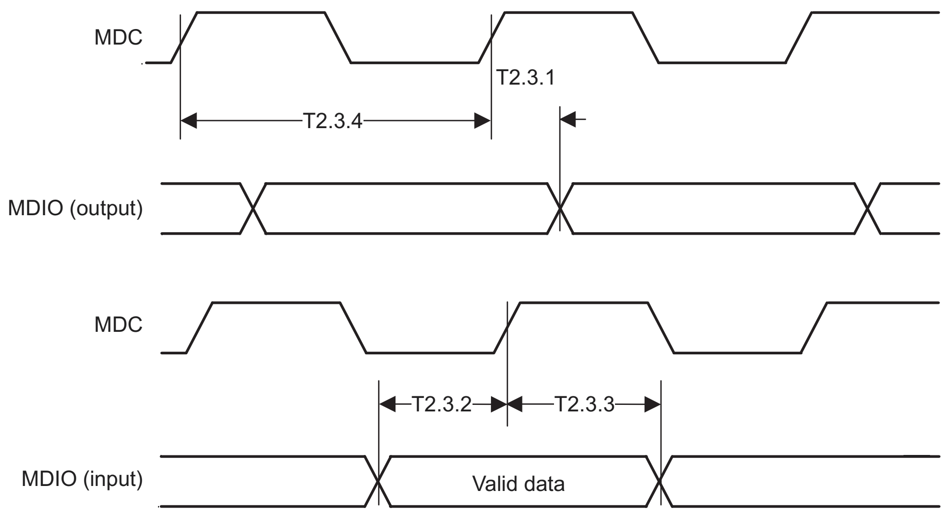


Figure 3. MII Serial Management Timing

Table 4. 100 Mb/s MII Transmit Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.4.1	TX_CLK high/low time	100 Mb/s normal mode	16	20	24	ns
T2.4.2	TXD[3:0], TX_EN data setup to TX_CLK	100 Mb/s normal mode	9.70			ns
T2.4.3	TXD[3:0], TX_EN data hold from TX_CLK	100 Mb/s normal mode	0			ns

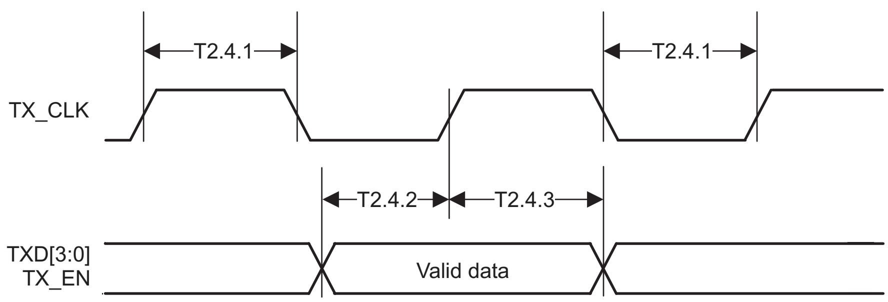


Figure 4. 100 Mb/s MII Transmit Timing

Table 5. 100 Mb/s MII Receive Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.5.1	RX_CLK high/low time	100 Mb/s normal mode	13	20	24	ns
T2.5.2	RX_CLK to RXD[3:0], RX_DV, RX_ER delay	100 Mb/s normal mode		20		ns

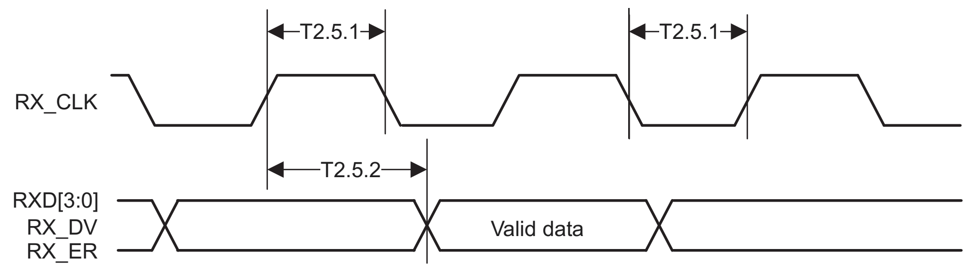


Figure 5. 100 Mb/s MII Receive Timing

Table 6. 100BASE-TX Transmit Packet Latency Timing

PARAMETER		NOTES(1)	MIN	TYP	MAX	UNIT
T2.6.1	TX_CLK to PMD output pair latency	100 Mb/s normal mode		6		bits

(1) For Normal mode, latency is determined by measuring the time from the first rising edge of TX_CLK occurring after the assertion of TX_EN to the first bit of the “J” code group as output from the PMD Output Pair. 1 bit time = 10 ns in 100 Mb/s mode.

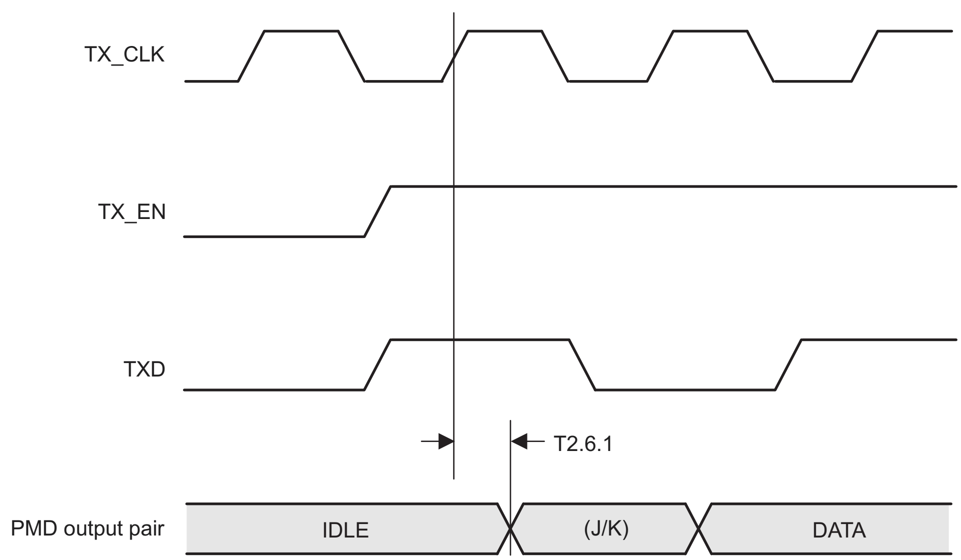


Figure 6. 100BASE-TX Transmit Packet Latency Timing

Table 7. 100BASE-TX Transmit Packet Deassertion Timing

PARAMETER		NOTES(1)	MIN	TYP	MAX	UNIT
T2.7.1	TX_CLK to PMD output pair deassertion	100 Mb/s normal mode		6		bits

(1) For Normal mode, latency is determined by measuring the time from the first rising edge of TX_CLK occurring after the assertion of TX_EN to the first bit of the “J” code group as output from the PMD Output Pair. 1 bit time = 10 ns in 100 Mb/s mode.

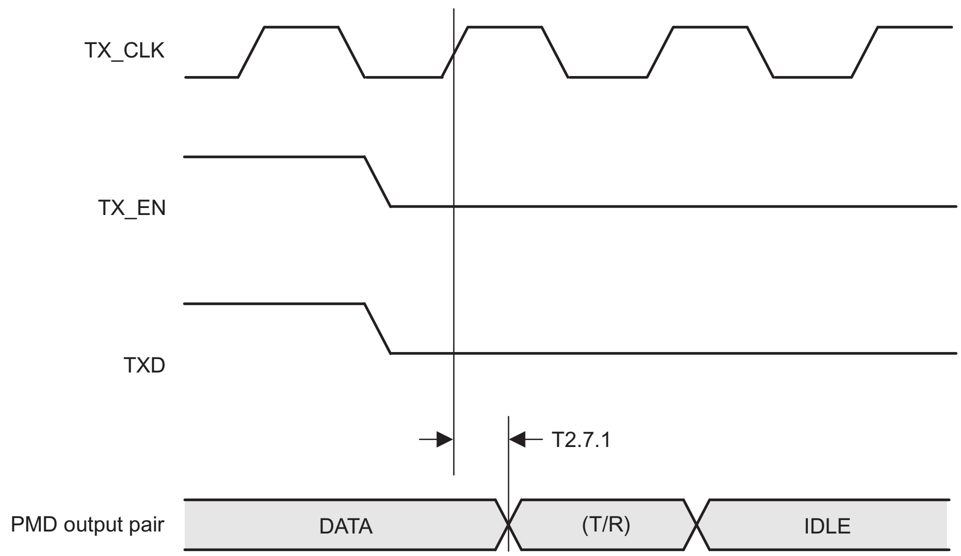


Figure 7. 100BASE-TX Transmit Packet Deassertion Timing

Table 8. 100BASE-TX Transmit Timing ($t_{R/F}$ & Jitter)

PARAMETER		NOTES[1][2]	MIN	TYP	MAX	UNIT
T2.8.1	100 Mb/s PMD output pair t_R and t_F		2.6	4	5.5	ns
	100 Mb/s t_R and t_F mismatch				710	ps
T2.8.2[3]	100 Mb/s PMD output pair transmit jitter				1.4	ns

(1) Normal Mismatch is the difference between the maximum and minimum of all rise and fall times.
(2) Rise and fall times taken at 10% and 90% of the +1 or –1 amplitude.
(3) Specified from –40°C to 125°C.

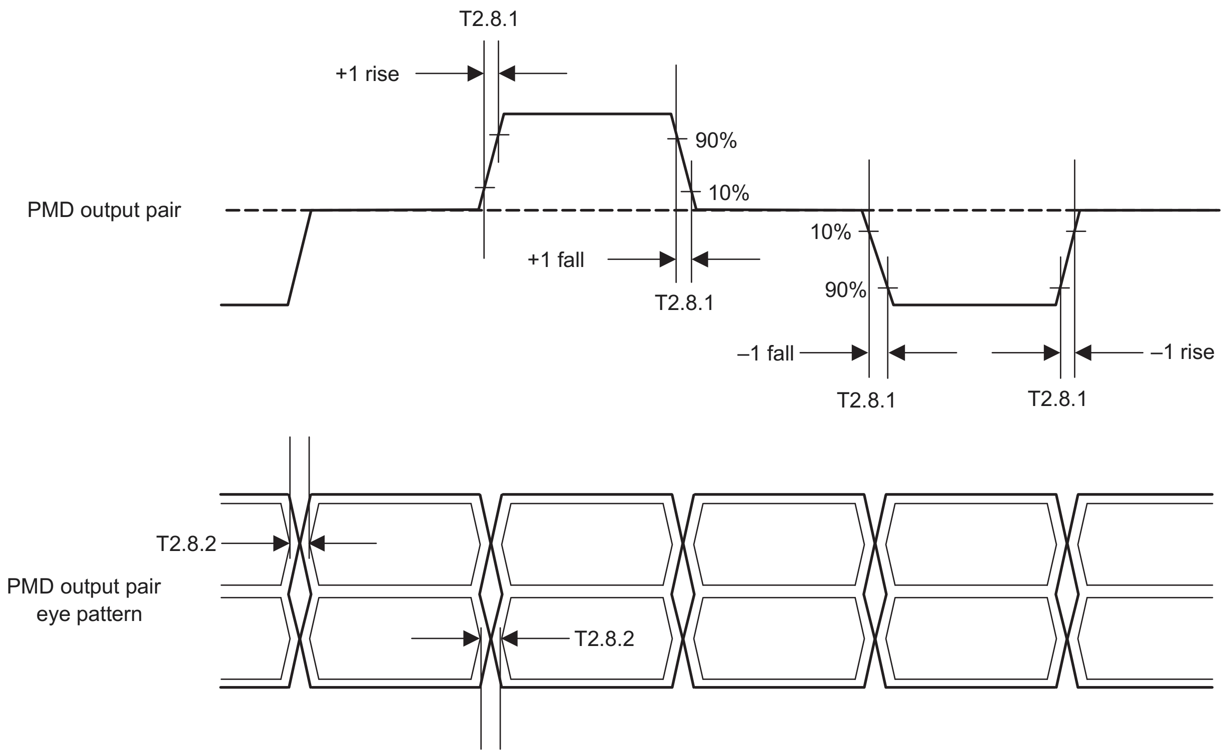


Figure 8. 100BASE-TX Transmit Timing ($t_{R/F}$ and Jitter)

Table 9. 100BASE-TX Receive Packet Latency Timing

PARAMETER[1]		NOTES[2][3]	MIN	TYP	MAX	UNIT
T2.9.1	Carrier sense ON delay	100 Mb/s normal mode		20		bits
T2.9.2	Receive data latency	100 Mb/s normal mode		24		bits

(1) Carrier sense ON delay is determined by measuring the time from the first bit of the “J” code group to the assertion of Carrier Sense.
(2) 1 bit time = 10 ns in 100 Mb/s mode.
(3) PMD input pair voltage amplitude is greater than the signal detect turn-on threshold value.

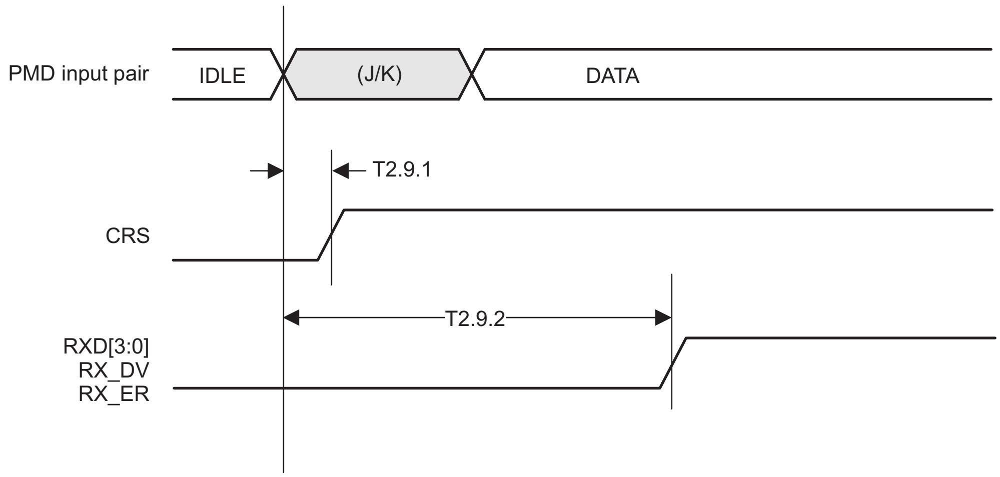


Figure 9. 100BASE-TX Receive Packet Latency Timing

Table 10. 100BASE-TX Receive Packet Deassertion Timing

PARAMETER		NOTES[1][2]	MIN	TYP	MAX	UNIT
T2.10.1	Carrier sense OFF delay	100 Mb/s normal mode		24		bits

(1) Carrier sense off delay is determined by measuring the time from the first bit of the “T” code group to the deassertion of carrier sense.
(2) 1 bit time = 10 ns in 100 Mb/s mode

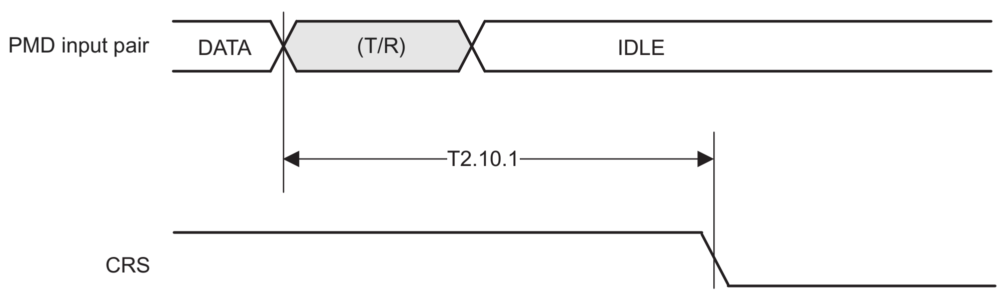


Figure 10. 100BASE-TX Receive Packet Deassertion Timing

Table 11. 10 Mb/s MII Transmit Timing

PARAMETER		NOTES[(1)]	MIN	TYP	MAX	UNIT
T2.11.1	TX_CLK high/low time	10 Mb/s MII mode	160	200	240	ns
T2.11.2	TXD[3:0], TX_EN data setup to TX_CLK fall	10 Mb/s MII mode	24.70			ns
T2.11.3	TXD[3:0], TX_EN data hold from TX_CLK rise	10 Mb/s MII mode	0			ns

(1) An attached Mac should drive the transmit signals using the positive edge of TX_CLK. As shown above, the MII signals are sampled on the falling edge of TX_CLK.

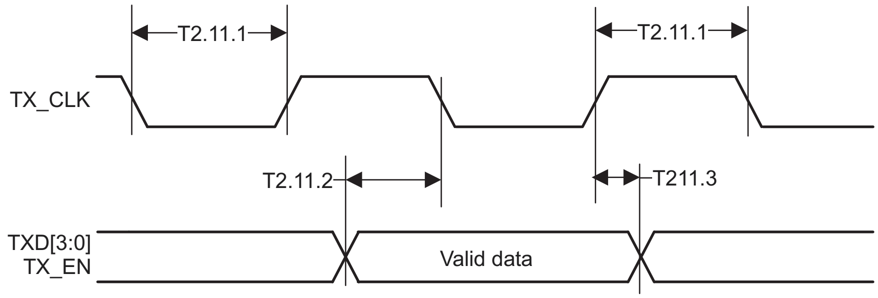


Figure 11. 10 Mb/s MII Transmit Timing

Table 12. 10 Mb/s MII Receive Timing

PARAMETER		NOTES[(1)]	MIN	TYP	MAX	UNIT
T2.12.1	RX_CLK high/low time		130	200	240	ns
T2.12.2	RX_CLK to RXD[3:0], RX_DV delay	10 Mb/s MII mode	100			ns
T2.12.3	RX_CLK rising edge delay from RXD[3:0], RX_DV valid	10 Mb/s MII mode		245		ns

(1) RX_CLK may be held low for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.

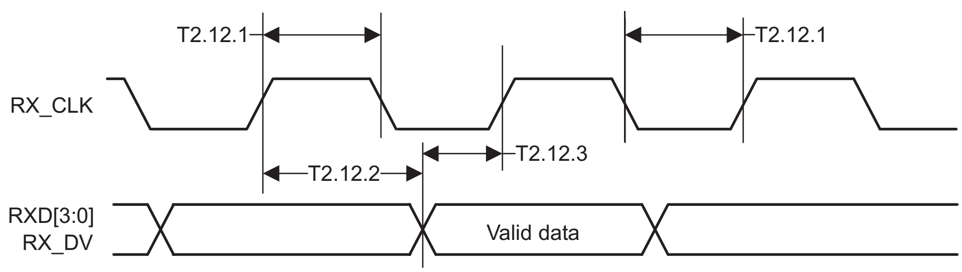


Figure 12. 10 Mb/s MII Receive Timing

Table 13. 10 Mb/s Serial Mode Transmit Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.13.1	TX_CLK high time	10 Mb/s serial mode		25		ns
T2.13.2	TX_CLK low time	10 Mb/s serial mode		75		ns
T2.13.3	TXD_0, TX_EN data setup to TX_CLK rise	10 Mb/s serial mode		24.70		ns
T2.13.4	TXD_0, TX_EN data hold from TX_CLK rise	10 Mb/s serial mode		6		ns

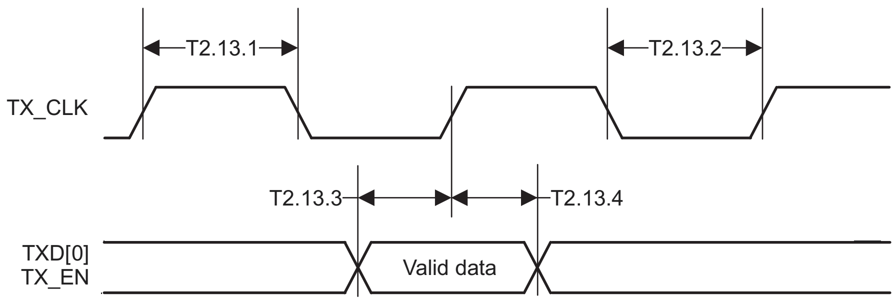


Figure 13. 10 Mb/s Serial Mode Transmit Timing

Table 14. 10 Mb/s Serial Mode Receive Timing

PARAMETER		NOTES(1)	MIN	TYP	MAX	UNIT
T2.14.1	RX_CLK high/low time			50		ns
T2.14.2	RX_CLK fall to RXD_0, RX_DV delay	10 Mb/s serial mode		0		ns

(1) RX_CLK may be held high for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.

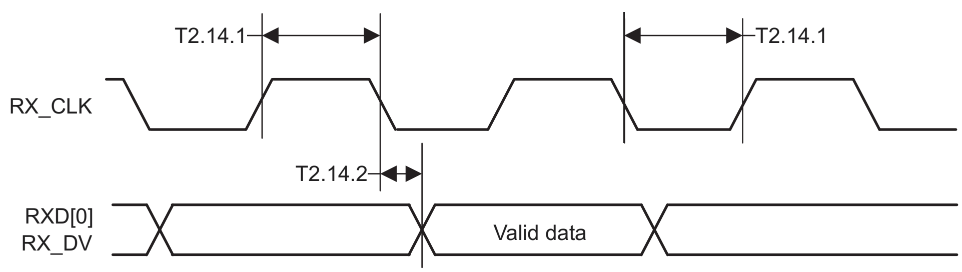


Figure 14. 10 Mb/s Serial Mode Receive Timing

Table 15. 10BASE-T Transmit Timing (Start of Packet)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.15.1	Transmit output delay from the falling edge of TX_CLK	10 Mb/s MII mode		3.5		bits
T2.15.2	Transmit output delay from the rising edge of TX_CLK	10 Mb/s Serial mode		3.5		bits

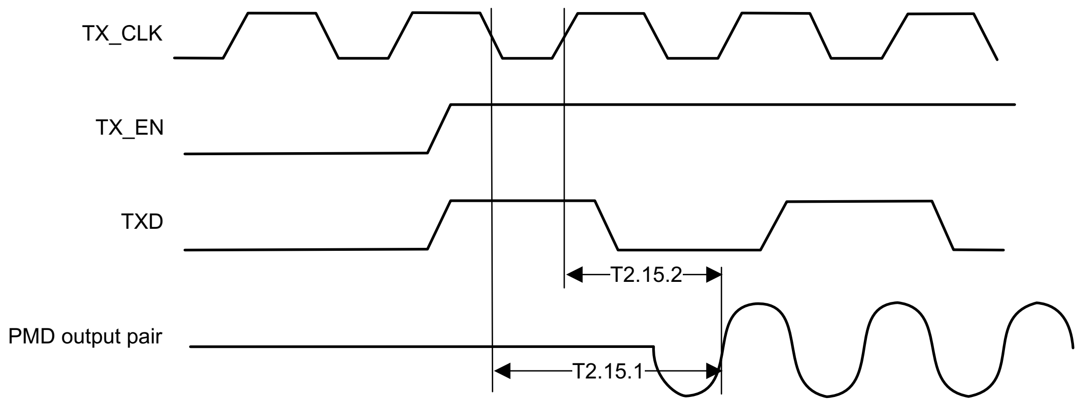


Figure 15. 10BASE-T Transmit Timing (Start of Packet)

Table 16. 10BASE-T Transmit Timing (End of Packet)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.16.1	End of packet high time (with ‘0’ ending bit)			300		ns
T2.16.2	End of packet high time (with ‘1’ ending bit)			300		ns

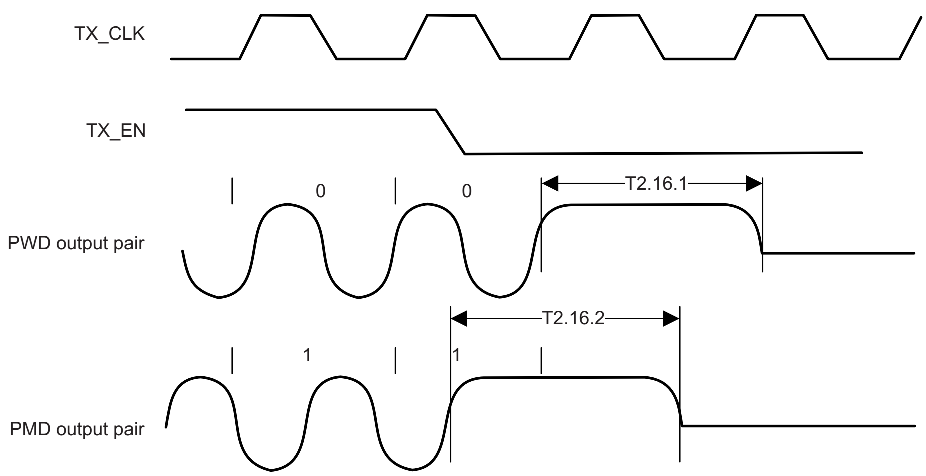


Figure 16. 10BASE-T Transmit Timing (End of Packet)

Table 17. 10BASE-T Receive Timing (Start of Packet)

PARAMETER		NOTES[(1)(2)]	MIN	TYP	MAX	UNIT
T2.17.1	Carrier sense turn on delay (PMD input pair to CRS)			630	1000	ns
T2.17.2	RX_DV latency			10		bits
T2.17.3	Receive data latency	Measurement shown from SFD		8		bits

(1) 10BASE-T RX_DV Latency is measured from first bit of preamble on the wire to the assertion of RX_DV
(2) 1 bit time = 100 ns in 10 Mb/s mode.

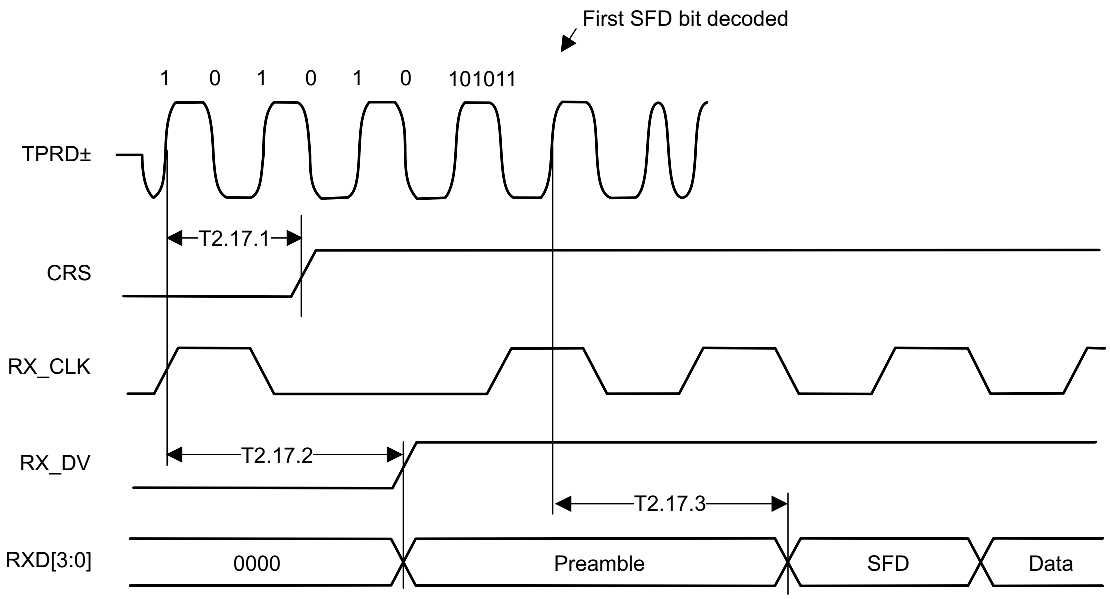


Figure 17. 10BASE-T Receive Timing (Start of Packet)

Table 18. 10BASE-T Receive Timing (End of Packet)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.18.1	Carrier sense turn off delay				1	µs

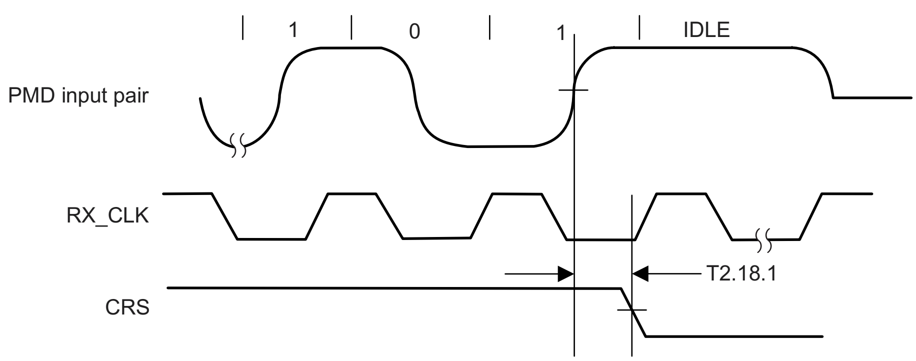


Figure 18. 10BASE-T Receive Timing (End of Packet)

Table 19. 10 Mb/s Heartbeat Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.19.1	CD heartbeat delay	All 10 Mb/s modes		1200		ns
T2.19.2	CD heartbeat duration	All 10 Mb/s modes		1000		ns

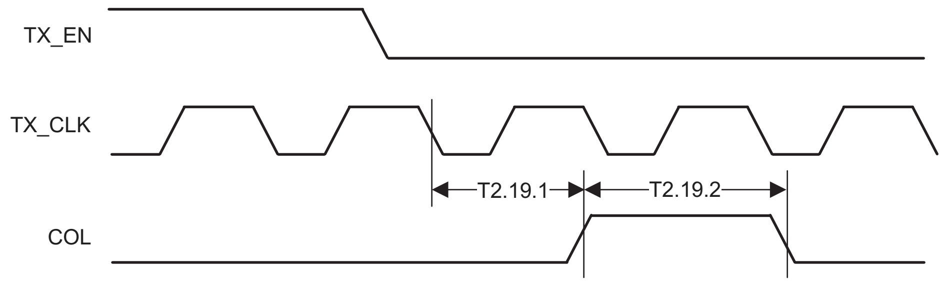


Figure 19. 10 Mb/s Heartbeat Timing

Table 20. 10 Mb/s Jabber Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.20.1	Jabber activation time			85		ms
T2.20.2	Jabber deactivation time			500		ms

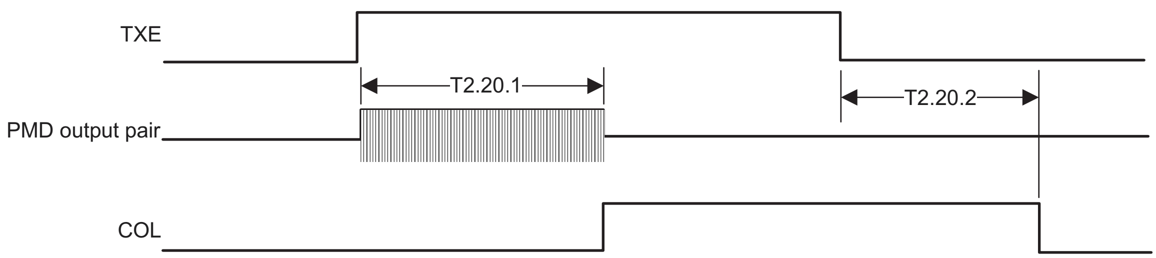


Figure 20. 10 Mb/s Jabber Timing

Table 21. 10BASE-T Normal Link Pulse Timing

PARAMETER		NOTES[(1)]	MIN	TYP	MAX	UNIT
T2.21.1	Pulse width			100		ns
T2.21.2	Pulse period			16		ms

(1) These specifications represent transmit timings.

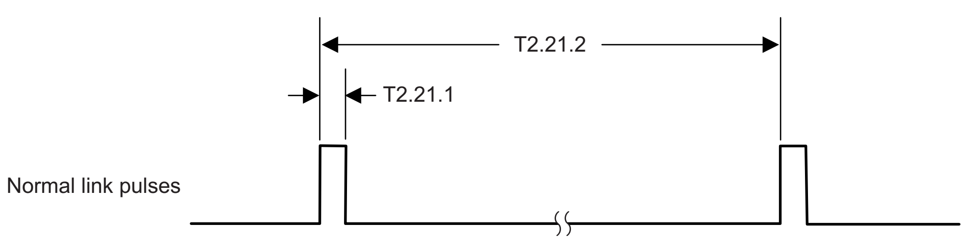


Figure 21. 10BASE-T Normal Link Pulse Timing

Table 22. Auto-Negotiation Fast Link Pulse (FLP) Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.22.1	Clock, data pulse width			100		ns
T2.22.2	Clock pulse to clock pulse period			125		μs

Table 22. Auto-Negotiation Fast Link Pulse (FLP) Timing (continued)

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.22.3	Clock pulse to data pulse period	Data = 1		62		µs
T2.22.4	Burst width			2		ms
T2.22.5	FLP burst to FLP burst period			16		ms

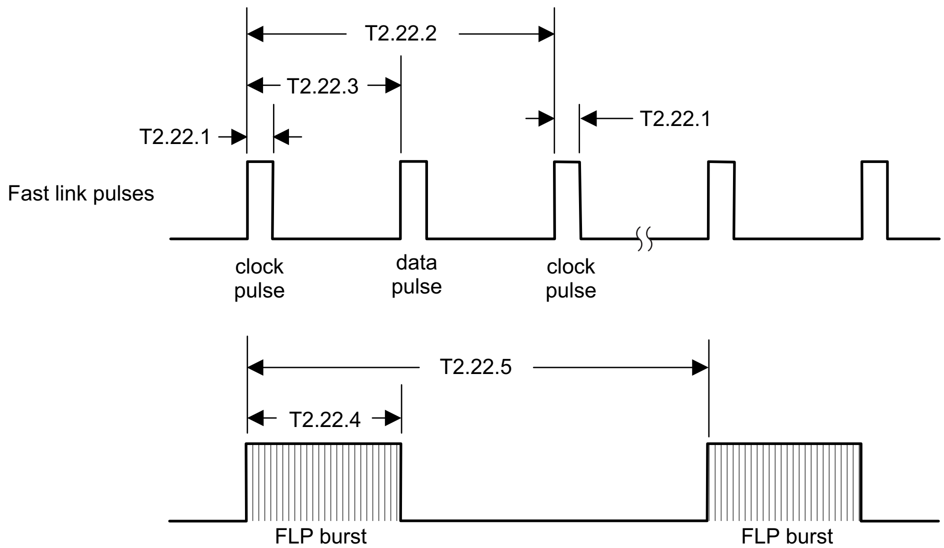


Figure 22. Auto-Negotiation Fast Link Pulse (FLP) Timing

Table 23. 100BASE-TX Signal Detect Timing

PARAMETER		NOTES(1)	MIN	TYP	MAX	UNIT
T2.23.1	SD internal turn-on time			1		ms
T2.23.2	SD internal turn-off time			350		µs

(1) The signal amplitude on PMD Input Pair must be TP-PMD compliant.

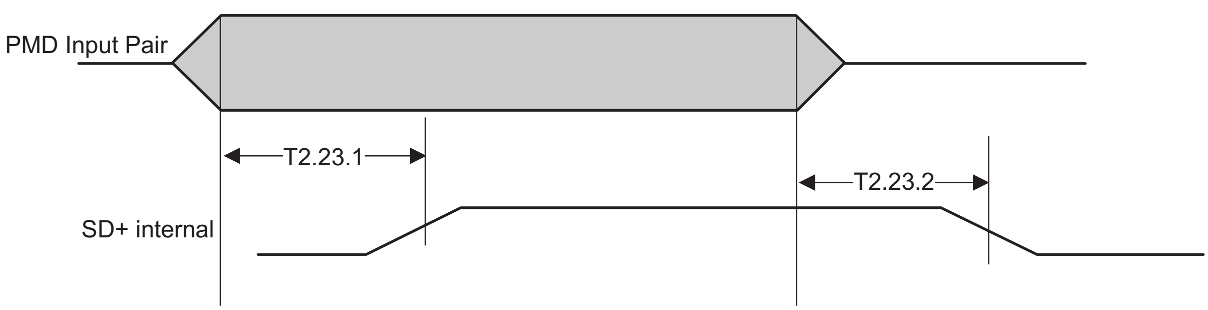


Figure 23. 100BASE-TX Signal Detect Timing

Table 24. 100 Mb/s Internal Loopback Timing

PARAMETER		NOTES[(1)(2)]	MIN	TYP	MAX	UNIT
T2.24.1	TX_EN to RX_DV loopback	100 Mb/s internal loopback mode		240		ns

(1) Due to the nature of the descrambler function, all 100BASE-TX Loopback modes will cause an initial “dead-time” of up to 550 μs during which time no data will be present at the receive MII outputs. The 100BASE-TX timing specified is based on device delays after the initial 550μs “dead-time”.
(2) Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.

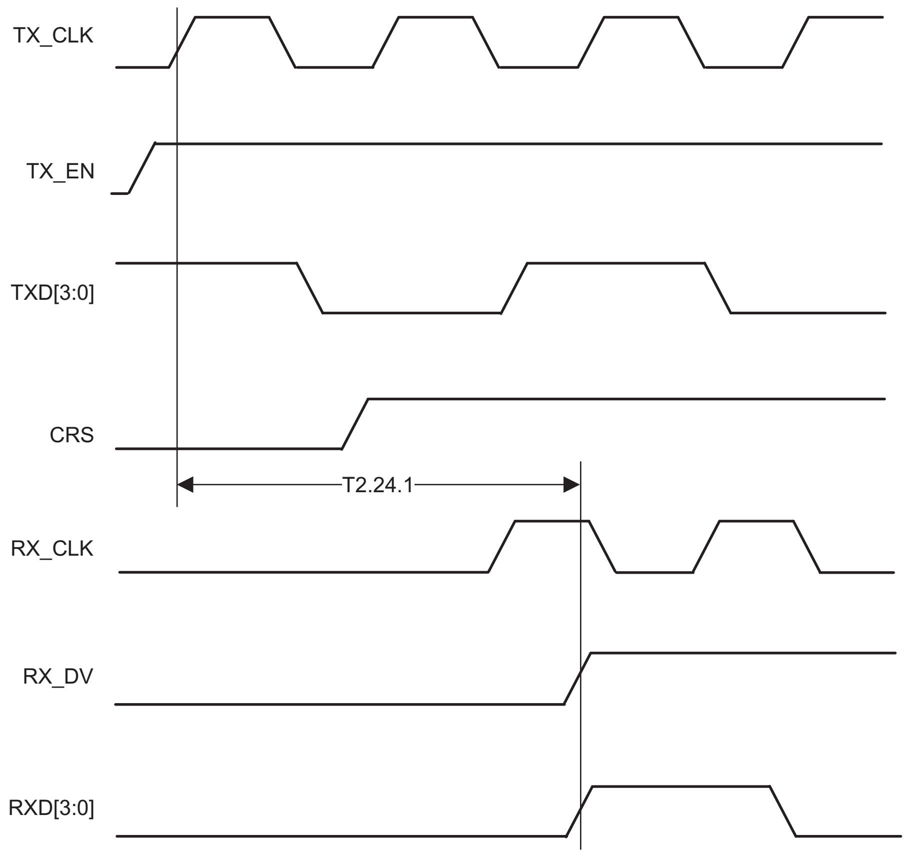


Figure 24. 100 Mb/s Internal Loopback Timing

Table 25. 10 Mb/s Internal Loopback Timing

PARAMETER		NOTES[(1)]	MIN	TYP	MAX	UNIT
T2.25.1	TX_EN to RX_DV loopback	10 Mb/s internal loopback mode			2.4	µs

(1) Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.

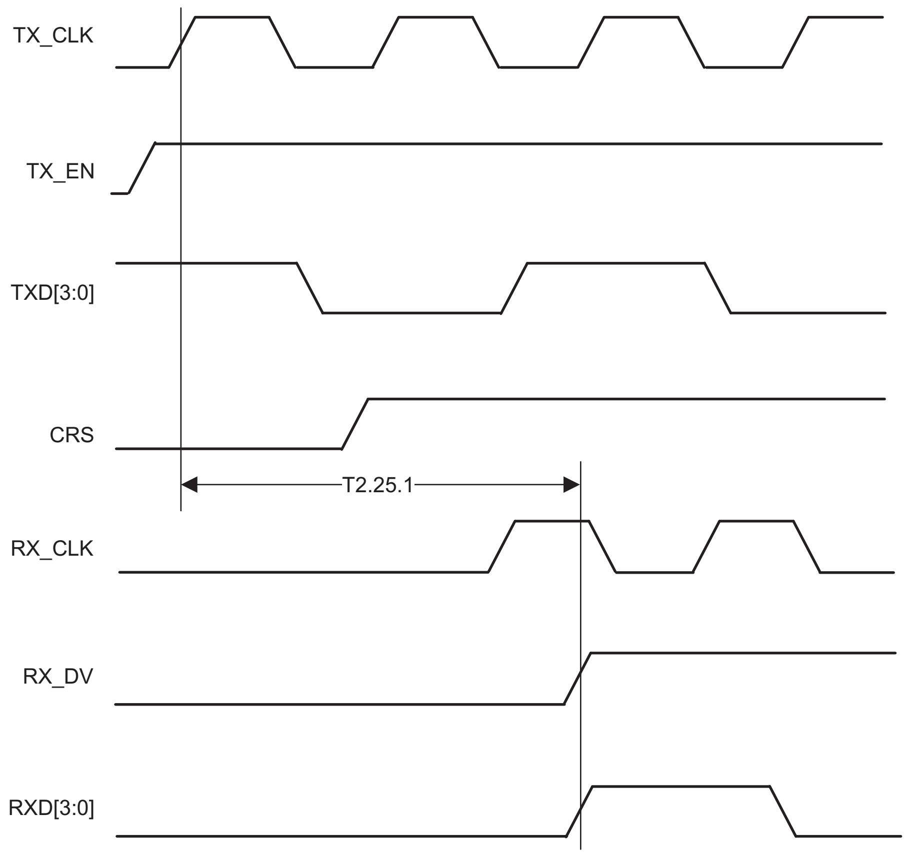


Figure 25. 10 Mb/s Internal Loopback Timing

Table 26. RMII Transmit Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.26.1	X1 clock period	50-MHz reference clock		20		ns
T2.26.2	TXD[1:0], TX_EN, data setup to X1 rising			3.70		ns
T2.26.3	TXD[1:0], TX_EN, data hold from X1 rising			1.70		ns
T2.26.4	X1 clock to PMD output pair latency	From X1 rising edge to first bit of symbol		17		bits

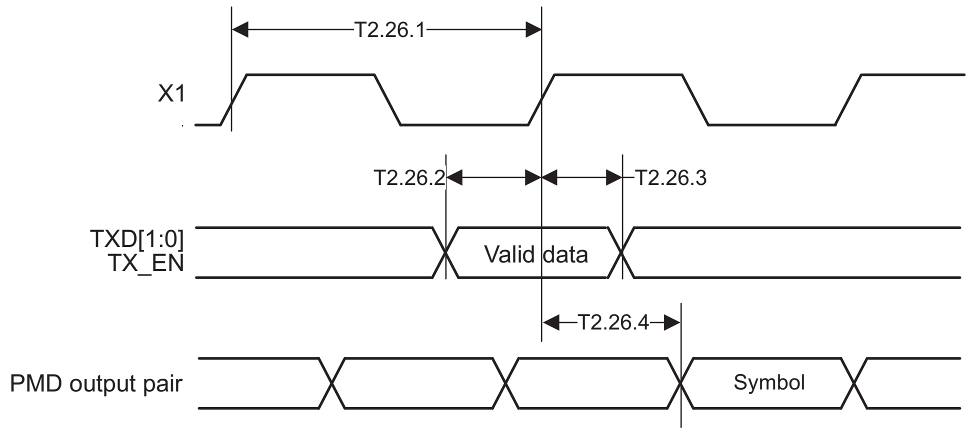


Figure 26. RMII Transmit Timing

Table 27. RMII Receive Timing

PARAMETER		NOTES (1) (2) (3)	MIN	TYP	MAX	UNIT
T2.27.1	X1 clock period	50 MHz Reference Clock		20		ns
T2.27.2	RXD[1:0], CRS_DV, RX_DV and RX_ER output delay from X1 rising			6		ns
T2.27.3	CRS ON delay	From JK symbol on PMD receive pair to initial assertion of CRS_DV		18.5		bits
T2.27.4	CRS OFF delay	From TR symbol on PMD receive pair to initial deassertion of CRS_DV		27		bits
T2.27.5	RXD[1:0] and RX_ER latency	From symbol on receive pair. Elasticity buffer set to default value (01).		38		bits

(1) Per the RMII Specification, output delays assume a 25-pF load.
(2) CRS_DV is asserted asynchronously in order to minimize latency of control signals through the why. CRS_DV may toggle synchronously at the end of the packet to indicate CRS deassertion.
(3) RX_DV is synchronous to X1. While not part of the RMII specification, this signal is provided to simplify recovery of receive data.

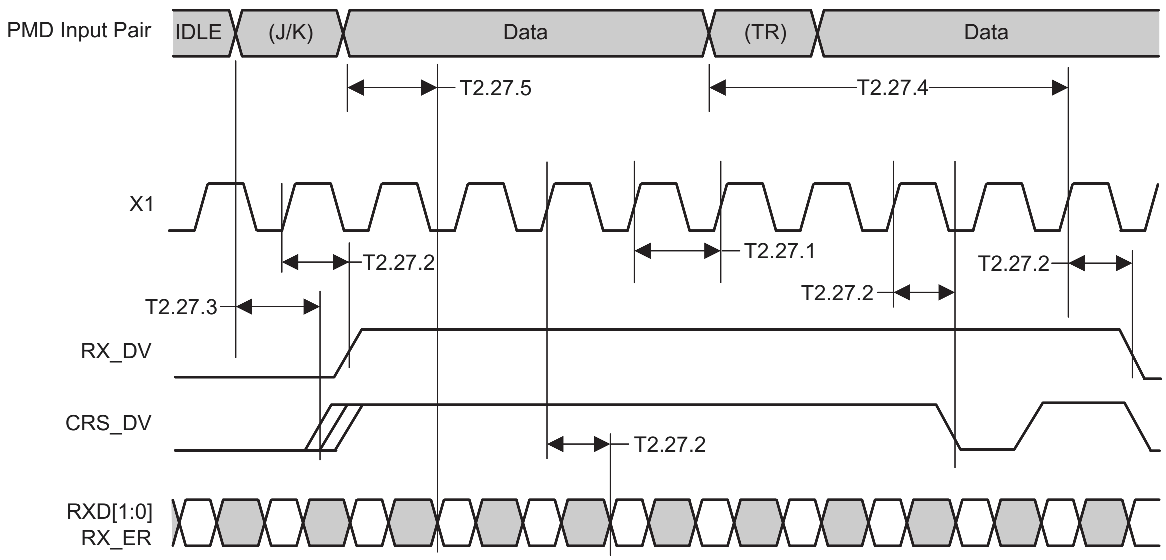


Figure 27. RMII Receive Timing

Table 28. Isolation Timing

PARAMETER		NOTES	MIN	TYP	MAX	UNIT
T2.28.1	From software clear of bit 10 in the BMCR register to the transition from Isolate to Normal Mode			100		µs
T2.28.2	From deassertion of software or hardware reset to transition from isolate to normal mode			500		µs

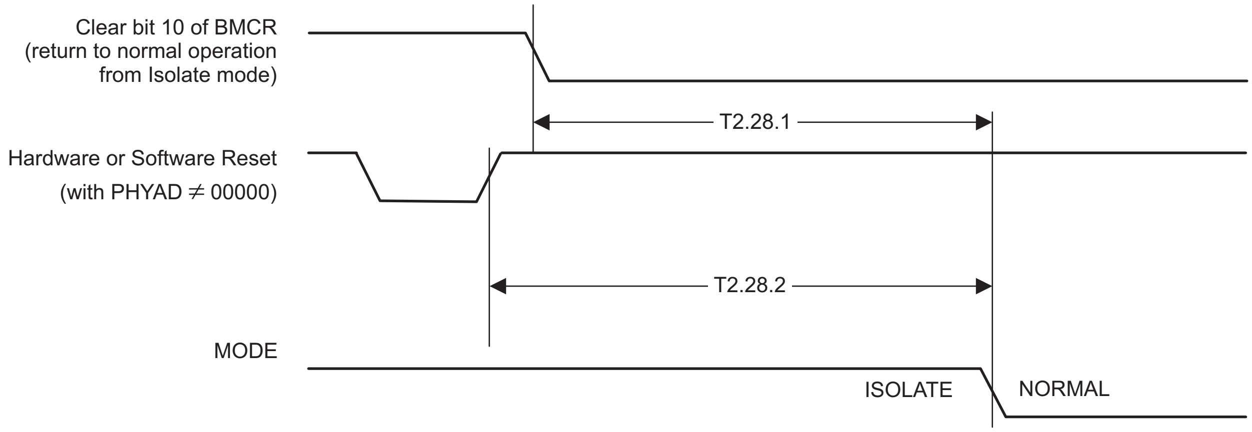


Figure 28. Isolation Timing

Table 29. 25 MHz_OUT Timing

PARAMETER		NOTES(1)	MIN	TYP	MAX	UNIT
T2.29.1	25 MHz_OUT high/low time	MII mode		20		ns
		RMII mode		10		
T2.29.2	25 MHz_OUT propagation delay	Relative to X1			8	ns

(1) 25 MHz_OUT characteristics are dependent upon the X1 input characteristics.

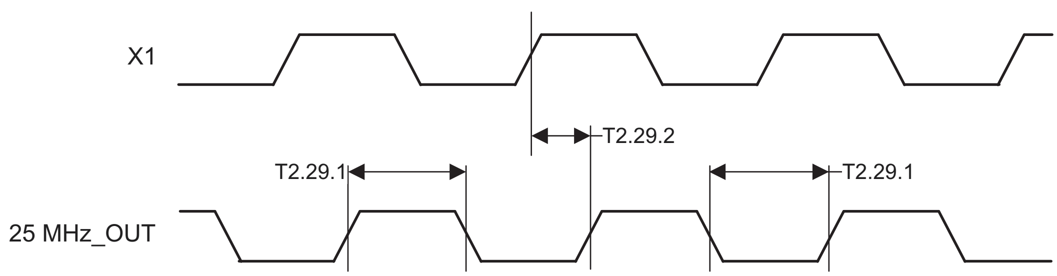
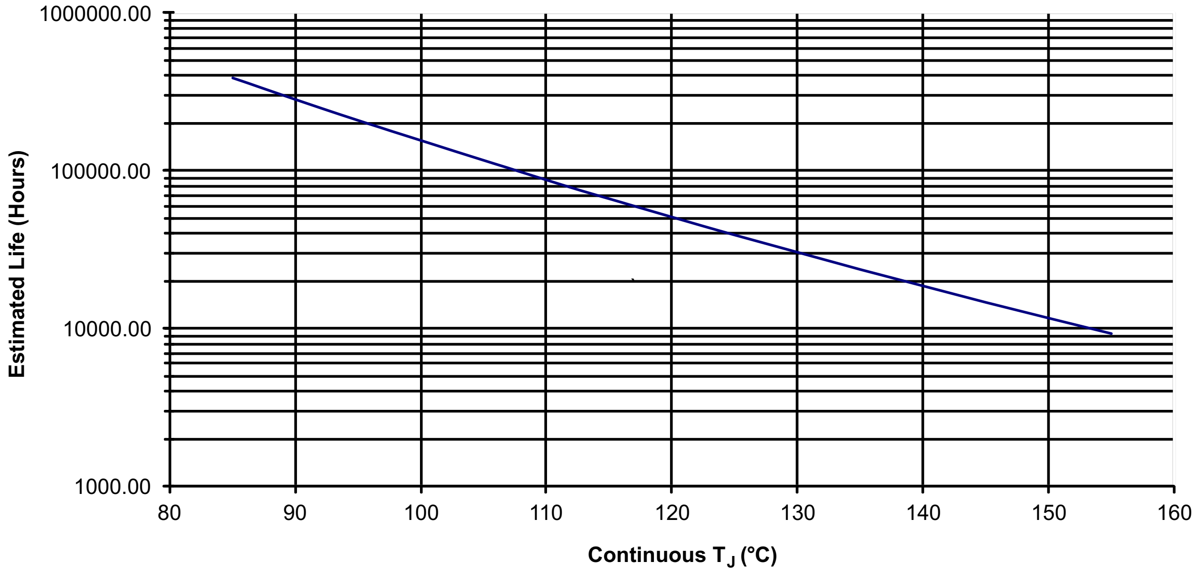


Figure 29. 25 MHz_OUT Timing

7.7 Typical Characteristics



1. See data sheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
3. Enhanced plastic product disclaimer applies.

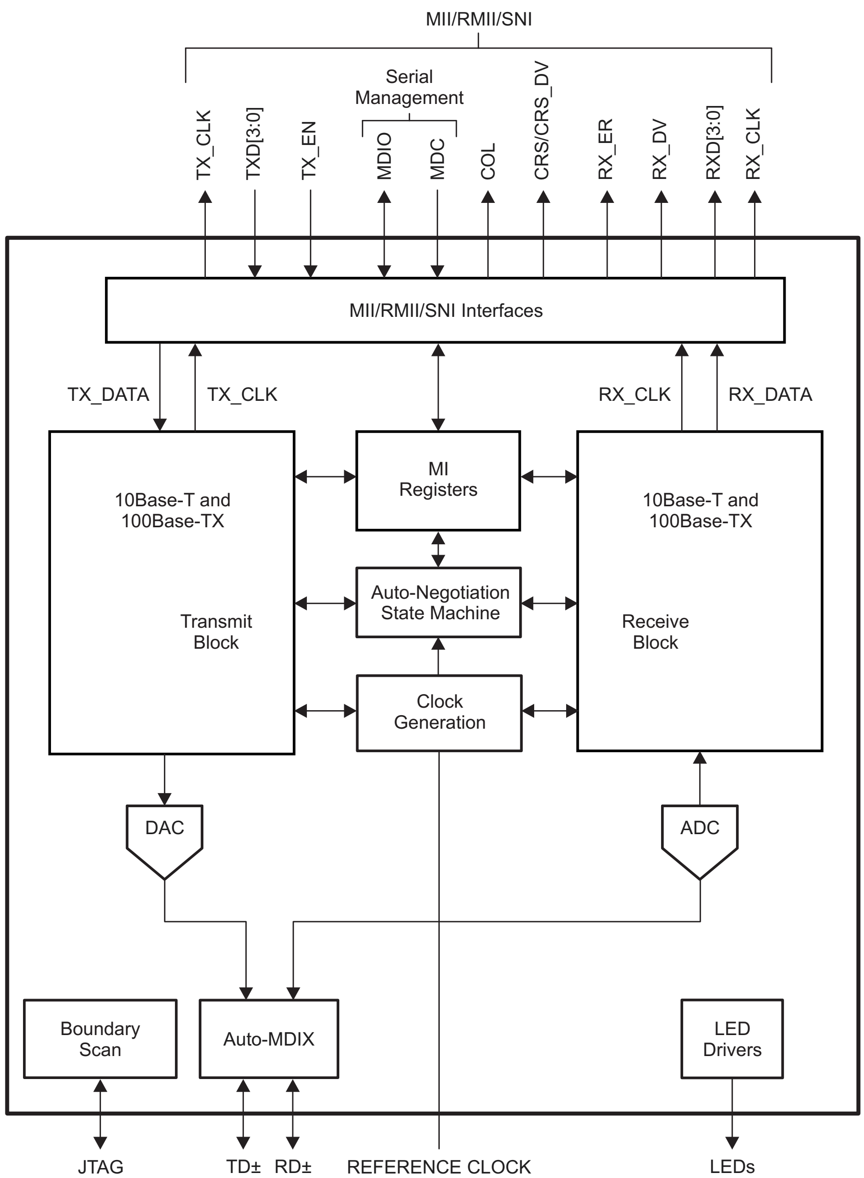
Figure 30. DP83848-HIREL Operating Life Derating Chart

8 Detailed Description

8.1 Overview

DP83848 is a highly reliable, feature rich robust device which includes enhanced ESD protection, MII and RMII for maximum flexibility in MPU selection. The DP83848 features integrated sublayers to support both 10BASE-T and 100BASE-TX Ethernet protocols, which ensures compatibility and interoperability with all other standards based Ethernet solutions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125 Mb/s serial data stream. Because the 100BASE-TX TP-PMD is integrated, the differential output pins, PMD output pair, can be directly routed to the magnetics.

Feature Description (continued)

The block diagram in Figure 31 provides an overview of each functional block within the 100BASE-TX transmit section.

The transmitter section consists of the following functional blocks:

- Code-group encoder and injection block
- Scrambler block (bypass option)
- NRZ to NRZI encoder block
- Binary to MLT-3 converter or common driver

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83848 implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3u Standard, Clause 24.

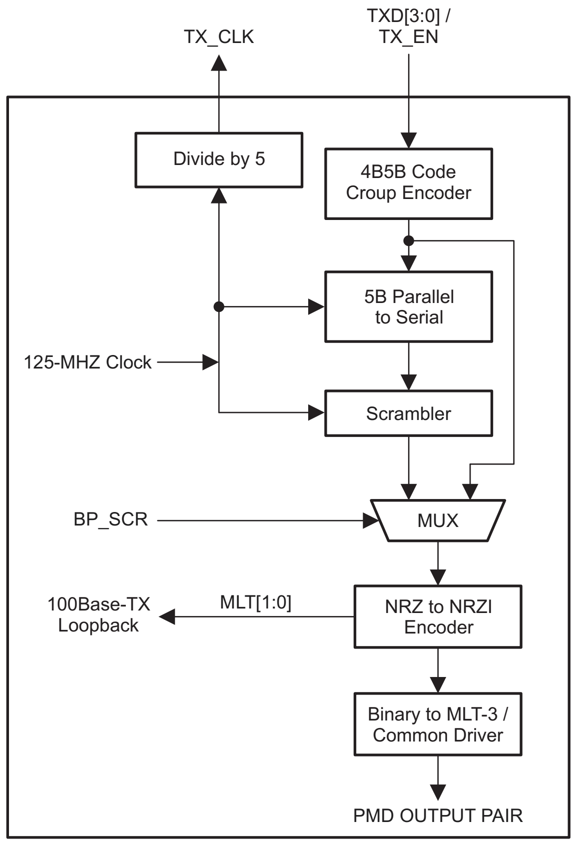


Figure 31. 100BASE-TX Transmit Block Diagram

Feature Description (continued)

Table 30. 4B5B Code-Group Encoding or Decoding

DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000 (1)
J	11000	First Start of Packet - 0101 (1)
K	10001	Second Start of Packet - 0101 (1)
T	01101	First End of Packet - 0000 (1)
R	00111	Second End of Packet - 0000 (1)
INVALID CODES		
V	00000	
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	

(1) Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.

8.3.1.1 Code-Group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of transmit enable signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of transmit enable).

8.3.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted pair cable (for 100BASE-TX applications). By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the PMD and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (i.e., continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB. The DP83848 uses the PHY_ID (pins PHYAD [4:0]) to set a unique seed value.

8.3.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI encoded in order to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 Unshielded twisted pair cable.

8.3.1.4 Binary to MLT-3 Convertor

The binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD output pair common driver is slew rate controlled. This should be considered when selecting AC coupling magnetics to ensure TP-PMD standard compliant transition times (3 ns < Tr < 5 ns).

The 100BASE-TX transmit TP-PMD function within the DP83848 is capable of sourcing only MLT-3 encoded data. Binary output from the PMD output pair is not possible in 100 Mb/s mode.

8.3.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125 Mb/s serial data stream to synchronous 4-bit nibble data that is provided to the MII. Because the 100BASE-TX TP-PMD is integrated, the differential input pins, RD±, can be directly routed from the AC coupling magnetics.

See Figure 32 for a block diagram of the 100BASE-TX receive function. This provides an overview of each functional block within the 100BASE-TX receive section.

The receive section consists of the following functional blocks:

- Analog front end
- Digital signal processor
- Signal detect
- MLT-3 to binary decoder
- NRZI to NRZ decoder
- Serial to parallel
- Descrambler
- Code group alignment
- 4B/5B decoder
- Link integrity monitor
- Bad SSD detection

8.3.2.1 Analog Front End

In addition to the digital equalization and gain control, the DP83848 includes analog equalization and gain control in the analog front end. The analog equalization reduces the amount of digital equalization required in the DSP.

8.3.2.2 Digital Signal Processor

The digital signal processor includes adaptive equalization with gain control and base line wander compensation.

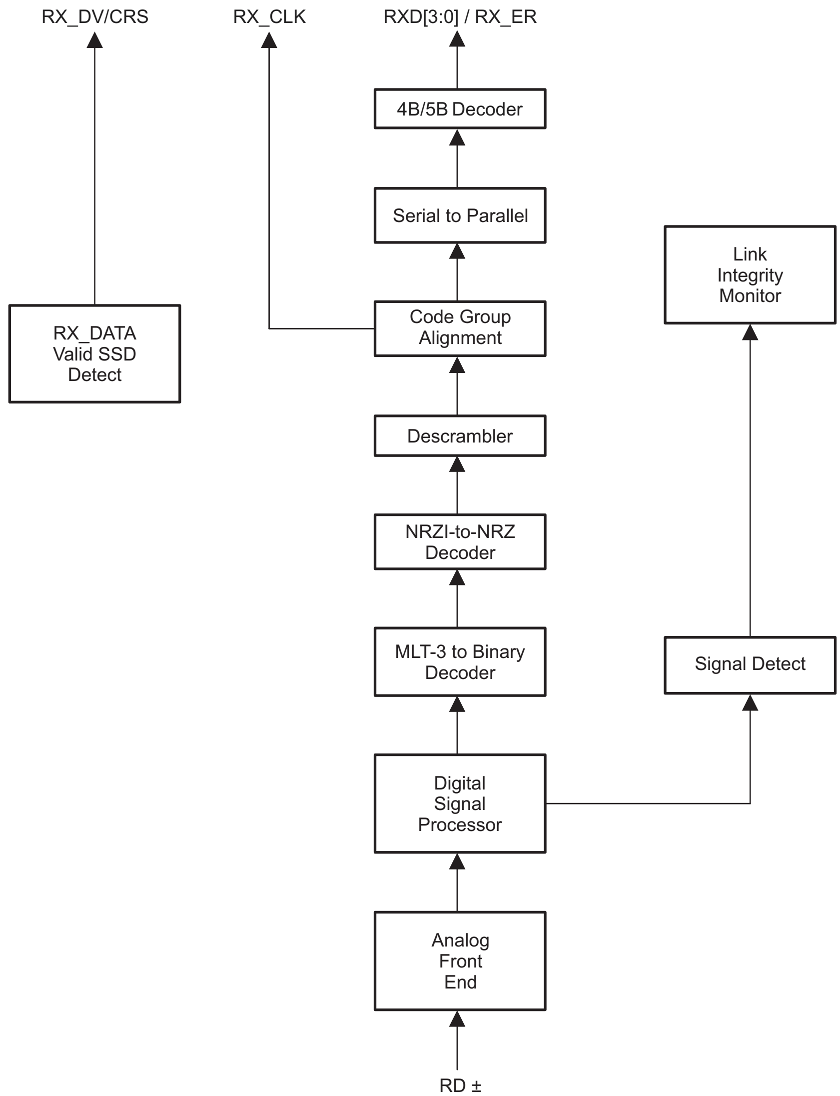


Figure 32. 100BASE-TX Receive Block Diagram

8.3.2.2.1 Digital Adaptive Equalization and Gain Control

When transmitting data at high speeds over copper twisted pair cable, frequency dependent attenuation becomes a concern. In high-speed twisted pair signalling, the frequency content of the transmitted signal can vary greatly during normal operation based primarily on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated to ensure the integrity of the transmission.

In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will over-compensate for shorter, less attenuating lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. The compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

The DP83848 utilizes an extremely robust equalization scheme referred as ‘digital adaptive equalization’.

The digital equalizer removes inter symbol interference (ISI) from the receive data stream by continuously adapting to provide a filter with the inverse frequency response of the channel. Equalization is combined with an adaptive gain control stage. This enables the receive 'eye pattern' to be opened sufficiently to allow very reliable data recovery.

The curves given in Figure 33 illustrate attenuation at certain frequencies for given cable lengths. This is derived from the worst case frequency vs. attenuation figures as specified in the EIA/TIA Bulletin TSB-36. These curves indicate the significant variations in signal attenuation that must be compensated for by the receive adaptive equalization circuit.

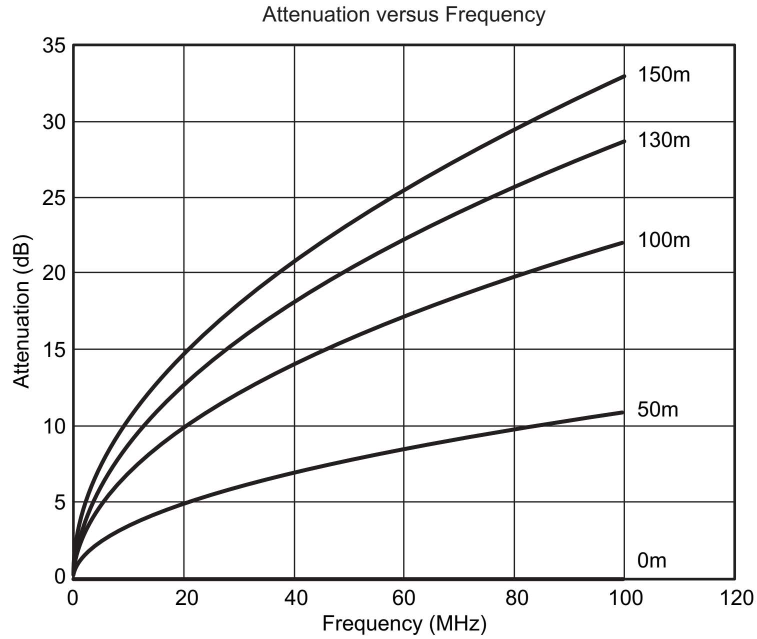


Figure 33. EIA/TIA Attenuation vs. Frequency for 0, 50, 100, 130 and 150 meters of CAT 5 cable

8.3.2.2.2 Base Line Wander Compensation

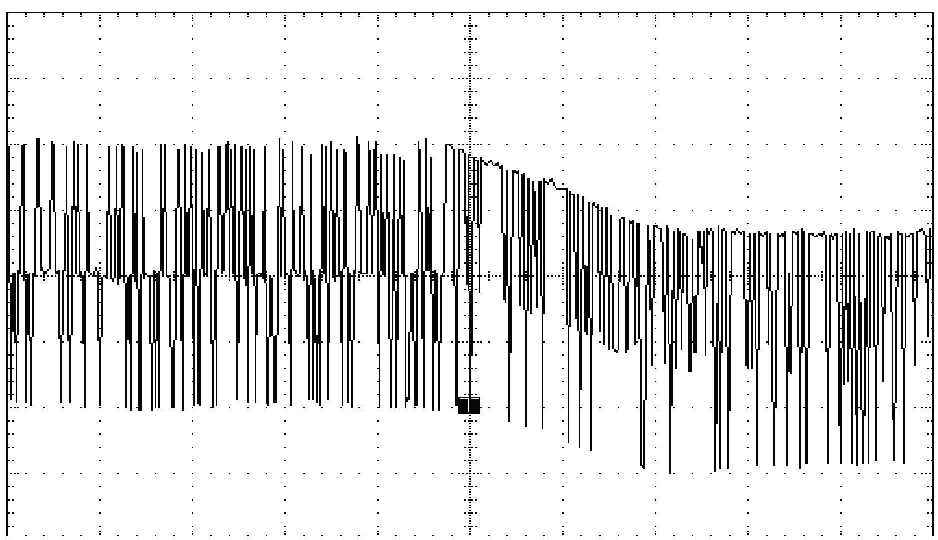


Figure 34. 100BASE-TX BLW Event

The DP83848 is completely ANSI TP-PMD compliant and includes base line wander (BLW) compensation. The BLW compensation block can successfully recover the TPPMD defined “killer” pattern.

BLW can generally be defined as the change in the average DC content, relatively short period over time, of an AC coupled digital transmission over a given transmission medium. (i.e., copper wire).

BLW results from the interaction between the low frequency components of a transmitted bit stream and the frequency response of the AC coupling components within the transmission system. If the low frequency content of the digital bit stream goes below the low frequency pole of the AC coupling transformers then the droop characteristics of the transformers will dominate resulting in potentially serious BLW.

The digital oscilloscope plot provided in Figure 34 illustrates the severity of the BLW event that can theoretically be generated during 100BASE-TX packet transmission. This event consists of approximately 800 mV of DC offset for a period of 120 µs. Left uncompensated, events such as this can cause packet loss.

8.3.2.3 Signal Detect

The signal detect function of the DP83848 is incorporated to meet the specifications mandated by the ANSI FDDI TP-PMD Standard as well as the IEEE 802.3 100BASE-TX Standard for both voltage thresholds and timing parameters.

Note that the reception of normal 10BASE-T link pulses and fast link pulses per IEEE 802.3u auto-negotiation by the 100BASE-TX receiver do not cause the DP83848 to assert signal detect.

8.3.2.4 MLT-3 to NRZI Decoder

The DP83848 decodes the MLT-3 information from the Digital Adaptive Equalizer block to binary NRZI data.

8.3.2.5 NRZI to NRZ

In a typical application, the NRZI to NRZ decoder is required in order to present NRZ formatted data to the descrambler.

8.3.2.6 Serial to Parallel

The 100BASE-TX receiver includes a serial to parallel converter which supplies 5-bit wide data symbols to the PCS Rx state machine.

8.3.2.7 Descrambler

A serial descrambler is used to de-scramble the received NRZ data. The descrambler has to generate an identical data scrambling sequence (N) in order to recover the original unscrambled data (UD) from the scrambled data (SD) as represented in the equations:

$$SD = (UD \oplus N) \tag{1}$$

$$UD = (SD \oplus N) \tag{2}$$

Synchronization of the descrambler to the original scrambling sequence (N) is achieved based on the knowledge that the incoming scrambled data stream consists of scrambled IDLE data. After the descrambler has recognized 12 consecutive IDLE code-groups, where an unscrambled IDLE code-group in 5B NRZ is equal to five consecutive ones (11111), it will synchronize to the receive data stream and generate unscrambled data in the form of unaligned 5B code-groups.

In order to maintain synchronization, the descrambler must continuously monitor the validity of the unscrambled data that it generates. To ensure this, a line state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler the hold timer starts a 722 µs countdown. Upon detection of sufficient IDLE code-groups (58 bit times) within the 722 µs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the line state monitor does not recognize sufficient unscrambled IDLE code-groups within the 722 µs period, the entire descrambler will be forced out of the current state of synchronization and reset in order to reacquire synchronization.

8.3.2.8 Code-Group Alignment

The code-group alignment module operates on unaligned 5-bit data from the descrambler (or, if the descrambler is bypassed, directly from the NRZI/NRZ decoder) and converts it into 5B code-group data (5 bits). Code-group alignment occurs after the J/K code-group pair is detected. Once the J/K code-group pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

8.3.2.9 4B/5B Decoder

The code-group decoder functions as a look up table that translates incoming 5B code-groups into 4B nibbles. The code-group decoder first detects the J/K code-group pair preceded by IDLE code-groups and replaces the J/K with MAC preamble. Specifically, the J/K 10-bit code-group pair is replaced by the nibble pair (0101 0101). All subsequent 5B code-groups are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the T/R code-group pair denoting the end of stream delimiter (ESD) or with the reception of a minimum of two IDLE code-groups.

8.3.2.10 100BASE-TX Link Integrity Monitor

The 100 Base TX Link monitor ensures that a valid and stable link is established before enabling both the transmit and receive PCS layer.

Signal detect must be valid for 395 µs to allow the link monitor to enter the link up state, and enable the transmit and receive functions.

8.3.2.11 Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is any transition from consecutive idle code-groups to non-idle code-groups which is not prefixed by the code-group pair /J/K.

If this condition is detected, the DP83848 will assert RX_ER and present RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code groups are detected. In addition, the false carrier sense counter register (FCSCR) will be incremented by one.

Once at least two IDLE code groups are detected, RX_ER and CRS become de-asserted.

8.3.3 10BASE-T Transceiver Module

The 10BASE-T transceiver module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard. An external filter is not required on the 10BASE-T interface since this is integrated inside the DP83848. This section focuses on the general 10BASET system level operation.

8.3.3.1 Operational Modes

8.3.3.1.1 Half Duplex Mode

In half duplex mode the DP83848 functions as a standard IEEE 802.3 10BASE-T transceiver supporting the CSMA/CD protocol.

8.3.3.1.2 Full Duplex Mode

In full duplex mode the DP83848 is capable of simultaneously transmitting and receiving without asserting the collision signal. The DP83848's 10 Mb/s ENDEC is designed to encode and decode simultaneously.

8.3.3.2 Smart Squelch

The smart squelch is responsible for determining when valid data is present on the differential receive inputs. The DP83848 implements an intelligent receive squelch to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. Smart squelch operation is independent of the 10BASE-T operational mode.

The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BSE-T standard) to determine the validity of data on the twisted pair inputs (refer to Figure 35).

The signal at the start of a packet is checked by the smart squelch and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150 ns. Finally the signal must again exceed the original squelch level within a 150 ns to ensure that the input waveform will not be rejected. This checking procedure results in the loss of typically three preamble bits at the beginning of each packet.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present. At this time, the smart squelch circuitry is reset.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 150 ns, indicating the end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise causing premature end of packet detection.

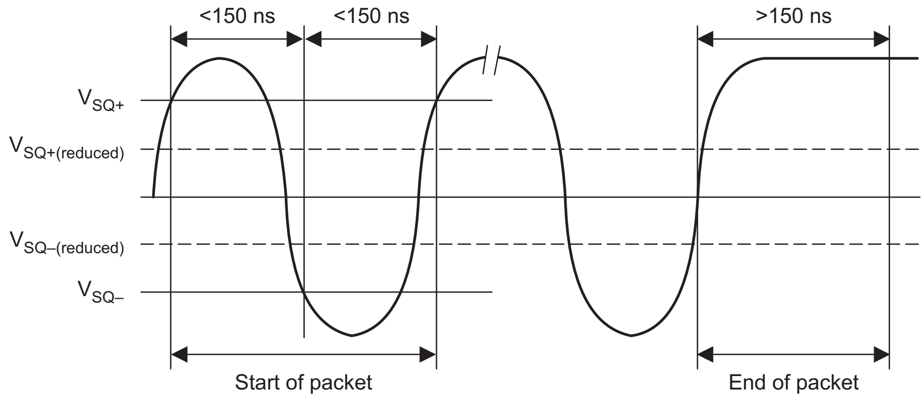


Figure 35. 10BASE-T Twisted Pair Smart Squelch Operation

8.3.3.3 Collision Detection and SQE

When in half duplex, a 10BASE-T collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII. Collisions are also reported when a jabber condition is detected.

The COL signal remains set for the duration of the collision. If the PHY is receiving when a collision is detected it is reported immediately (through the COL pin).

When heartbeat is enabled, approximately 1 µs after the transmission of each packet, a signal quality error (SQE) signal of approximately 10-bit times is generated to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

The SQE test is inhibited when the PHY is set in full duplex mode. SQE can also be inhibited by setting the HEARTBEAT_DIS bit in the 10BTSCR register.

8.3.3.4 Carrier Sense

Carrier sense (CRS) may be asserted due to receive activity once valid data is detected via the squelch function.

For 10 Mb/s half Dduplex operation, CRS is asserted during either packet transmission or reception.

For 10 Mb/s full duplex operation, CRS is asserted only during receive activity.

CRS is deasserted following an end of packet.

8.3.3.5 Normal Link Pulse Detection/Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-T standard. Each link pulse is nominally 100 ns in duration and transmitted every 16 ms in the absence of transmit data.

Link pulses are used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10BASE-T twisted pair transmitter, receiver and collision detection functions.

When the link integrity function is disabled (FORCE_LINK_10 of the 10BTSCR register), a good link is forced and the 10BASE-T transceiver will operate regardless of the presence of link pulses.

8.3.3.6 Jabber Function

The jabber function monitors the DP83848's output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 85 ms.

Once disabled by the Jabber function, the transmitter stays disabled for the entire time that the ENDEC module's internal transmit enable is asserted. This signal has to be deasserted for approximately 500 ms (the “unjab” time) before the Jabber function re-enables the transmit outputs.

The Jabber function is only relevant in 10BASE-T mode.

8.3.3.7 Automatic Link Polarity Detection and Correction

The DP83848's 10BASE-T transceiver module incorporates an automatic link polarity detection circuit. When three consecutive inverted link pulses are received, bad polarity is reported.

A polarity reversal can be caused by a wiring error at either end of the cable, usually at the main distribution frame (MDF) or patch panel in the wiring closet.

The bad polarity condition is latched in the 10BTSCR register. The DP83848's 10BASE-T transceiver module corrects for this error internally and will continue to decode received data correctly. This eliminates the need to correct the wiring error immediately.

8.3.3.8 Transmit and Receive Filtering

External 10BASE-T filters are not required when using the DP83848, as the required signal conditioning is integrated into the device.

Only isolation transformers and impedance matching resistors are required for the 10BASE-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated by at least 30 dB.

8.3.3.9 Transmitter

The encoder begins operation when the transmit enable input (TX_EN) goes high and converts NRZ data to preemphasized Manchester data for the transceiver. For the duration of TX_EN, the serialized transmit data (TXD) is encoded for the transmit-driver pair (PMD Output Pair). TXD must be valid on the rising edge of transmit clock (TX_CLK). Transmission ends when TX_EN deasserts. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

8.3.3.10 Receiver

The decoder detects the end of a frame when no additional mid-bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted. Receive clock stays active for five more bit times after CRS goes low, to guarantee the receive timings of the controller.

8.3.4 Reset Operation

The DP83848 includes an internal power-on reset (POR) function and does not need to be explicitly reset for normal operation after power up. If required during normal operation, the device can be reset by a hardware or software reset.

8.3.4.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to the RESET_N. This will reset the device such that all registers will be reinitialized to default values and the hardware configuration values will be re-latched into the device (similar to the power-up/reset operation).

8.3.4.2 Software Reset

A software reset is accomplished by setting the reset bit (bit 15) of the basic mode control register (BMCR). The period from the point in time when the reset bit is set to the point in time when software reset has concluded is approximately 1 µs.

The software reset will reset the device such that all registers will be reset to default values and the hardware configuration values will be maintained. Software driver code must wait 3 µs following a software reset before allowing further serial MII operations with the DP83848.

8.4 Device Functional Modes

The DP83848 supports several modes of operation using the MII interface pins. The options are defined in the following sections and include:

- MII mode
- RMII mode
- 10 Mb serial network interface (SNI)

The modes of operation can be selected by strap options or register control. For RMII mode, it is required to use the strap option, since it requires a 50 MHz clock instead of the normal 25 MHz.

In each of these modes, the IEEE 802.3 serial management interface is operational for device configuration and status. The serial management interface of the MII allows for the configuration and control of multiple PHY devices, gathering of status, error information, and the determination of the type and capabilities of the attached PHY(s).

8.4.1 MII Interface

The DP83848 incorporates the media independent interface (MII) as specified in Clause 22 of the IEEE 802.3u standard. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems. This section describes the nibble wide MII data interface.

The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC).

8.4.1.1 Nibble-Wide MII Data Interface

Clause 22 of the IEEE 802.3u specification defines the media independent Interface. This interface includes a dedicated receive bus and a dedicated transmit bus. These two data buses, along with various control and status signals, allow for the simultaneous exchange of data between the DP83848 and the upper layer agent (MAC).

The receive interface consists of a nibble wide data bus RXD[3:0], a receive error signal RX_ER, a receive data valid flag RX_DV, and a receive clock RX_CLK for synchronous transfer of the data. The receive clock operates at either 2.5 MHz to support 10 Mb/s operation modes or at 25 MHz to support 100 Mb/s operational modes.

The transmit interface consists of a nibble wide data bus TXD[3:0], a transmit enable control signal TX_EN, and a transmit clock TX_CLK which runs at either 2.5 MHz or 25 MHz.

Additionally, the MII includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in half duplex mode. The COL signal asserts as an indication of a collision which can occur during half duplex operation when both a transmit and receive operation occur simultaneously.

8.4.1.2 Collision Detect

For half duplex, a 10BASE-T or 100BASE-TX collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII.

If the DP83848 is transmitting in 10 Mb/s mode when a collision is detected, the collision is not reported until seven bits have been received while in the collision state. This prevents a collision being reported incorrectly due to noise on the network. The COL signal remains set for the duration of the collision.

If a collision occurs during a receive operation, it is immediately reported by the COL signal.

When heartbeat is enabled (only applicable to 10 Mb/s operation), approximately 1μs after the transmission of each packet, a signal quality error (SQE) signal of approximately 10 bit times is generated (internally) to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII.

8.4.1.3 Carrier Sense

Carrier sense (CRS) is asserted due to receive activity, once valid data is detected via the squelch function during 10 Mb/s operation. During 100 Mb/s operation CRS is asserted when a valid link (SD) and two non-contiguous zeros are detected on the line.

For 10 or 100 Mb/s half duplex operation, CRS is asserted during either packet transmission or reception.

Device Functional Modes (continued)

For 10 or 100 Mb/s full duplex operation, CRS is asserted only due to receive activity.

CRS is deasserted following an end of packet.

8.4.2 Reduced MII Interface

The DP83848 incorporates the reduced media independent interface (RMII) as specified in the RMII specification (rev1.2) from the RMII Consortium. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s systems using a reduced number of pins. In this mode, data is transferred 2-bits at a time using the 50 MHz RMII_REF clock for both transmit and receive. The following pins are used in RMII mode:

- TX_EN
- TXD[1:0]
- RX_ER (optional for Mac)
- CRS_DV
- RXD[1:0]
- X1 (RMII Reference clock is 50 MHz)

In addition, the RMII mode supplies an RX_DV signal which allows for a simpler method of recovering receive data without having to separate RX_DV from the CRS_DV indication. This is especially useful for systems which do not require CRS, such as systems that only support fullduplex operation. This signal is also useful for diagnostic testing where it may be desirable to loop Receive RMII data directly to the transmitter.

Since the reference clock operates at 10 times the data rate for 10 Mb/s operation, transmit data is sampled every 10 clocks. Likewise, receive data will be generated every 10th clock so that an attached device can sample the data every 10 clocks.

RMII mode requires a 50 MHz oscillator be connected to the device X1 pin. A 50 MHz crystal is not supported.

To tolerate potential frequency differences between the 50 MHz reference clock and the recovered receive clock, the receive RMII function includes a programmable elasticity buffer. The elasticity buffer is programmable to minimize propagation delay based on expected packet size and clock accuracy. This allows for supporting a range of packet sizes including jumbo frames.

The elasticity buffer will force frame check sequence errors for packets which overrun or underrun the FIFO. Underrun and Overrun conditions can be reported in the RMII and bypass register (RBR). The following table indicates how to program the elasticity buffer fifo (in 4-bit increments) based on expected max packet size and clock accuracy. It assumes both clocks (RMII reference clock and far-end transmitter clock) have the same accuracy.

Table 31. Supported Packet Sizes at ±50ppm and ±100ppm for Each Clock

START THRESHOLD RBR[1:0]	LATENCY TOLERANCE	RECOMMENDED PACKET SIZE at ±50 ppm	RECOMMENDED PACKET SIZE at ±100 ppm
1 (4-bits)	2 bits	2400 bytes	1200 bytes
2 (8-bits)	6 bits	7200 bytes	3600 bytes
3 (12-bits)	10 bits	12000 bytes	6000 bytes
0 (16-bits)	14 bits	16800 bytes	8400 bytes

8.4.3 10 Mb Serial Network Interface (SNI)

The DP83848 incorporates a 10 Mb serial network interface (SNI) which allows a simple serial data interface for 10 Mb only devices. This is also referred to as a 7-wire interface. While there is no defined standard for this interface, it is based on early 10 Mb physical layer devices. Data is clocked serially at 10 MHz using separate transmit and receive paths. The following pins are used in SNI mode:

- TX_CLK
- TX_EN
- TXD[0]
- RX_CLK
- RXD[0]

- CRS
- COL

8.4.4 802.3u MII Serial Management Interface

8.4.4.1 Serial Management Register Access

The serial management MII specification defines a set of thirty-two 16-bit status and control registers that are accessible through the management interface pins MDC and MDIO. The DP83848 implements all the required MII registers as well as several optional registers. A description of the serial management access protocol follows.

8.4.4.2 Serial Management Access Protocol

The serial control interface consists of two pins, management data clock (MDC) and management data input/output (MDIO). MDC has a maximum clock rate of 25 MHz and no minimum rate. The MDIO line is bi-directional and may be shared by up to 32 devices. The MDIO frame format is shown below in Table 32.

The MDIO pin requires a pull-up resistor (1.5 kΩ) which, during IDLE and turnaround, will pull MDIO high. In order to initialize the MDIO interface, the station management entity sends a sequence of 32 contiguous logic ones on MDIO to provide the DP83848 with a sequence that can be used to establish synchronization. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles, or by simply allowing the MDIO pull-up resistor to pull the MDIO pin high during which time 32 MDC clock cycles are provided. In addition 32 MDC clock cycles should be used to re-sync the device if an invalid start, opcode, or turnaround bit is detected.

The DP83848 waits until it has received this preamble sequence before responding to any other transaction. Once the DP83848 serial management port has been initialized no further preamble sequencing is required until after a power-on/reset, invalid start, invalid opcode, or invalid turnaround bit has occurred.

The start code is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state.

Turnaround is defined as an idle bit time inserted between the register address field and the data field. To avoid contention during a read transaction, no device shall actively drive the MDIO signal during the first bit of turnaround. The addressed DP83848 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. Figure 36 shows the timing relationship between MDC and the MDIO as driven or received by the station (STA) and the DP83848 (PHY) for a typical register read access.

For write transactions, the station management entity writes data to the addressed DP83848 thus eliminating the requirement for MDIO turnaround. The turnaround time is filled by the management entity by inserting <10>. Figure 37 shows the timing relationship for a typical MII register write access.

Table 32. Typical MDIO Frame Format

MII MANAGEMENT SERIAL PROTOCOL	<idle><start><op code><device addr><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

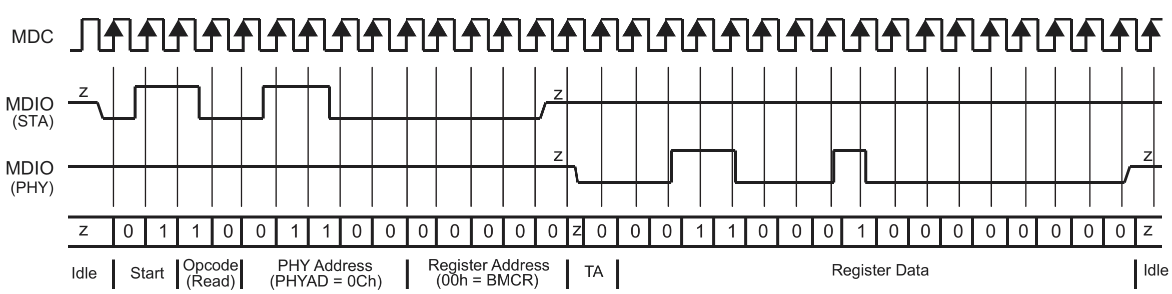


Figure 36. Typical MDC/MDIO Read Operation

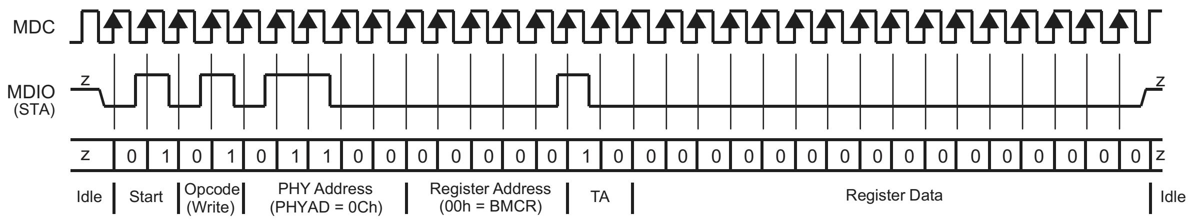


Figure 37. Typical MDC/MDIO Write Operation

8.4.4.3 Serial Management Preamble Suppression

The DP83848 supports a preamble suppression mode as indicated by a one in bit 6 of the basic mode status register (BMSR, address 01h.) If the station management entity (i.e. MAC or other management controller) determines that all PHYs in the system support preamble suppression by returning a one in this bit, then the station management entity need not generate preamble for each management transaction.

The DP83848 requires a single initialization sequence of 32 bits of preamble following hardware/software reset.

This requirement is generally met by the mandatory pull-up resistor on MDIO in conjunction with a continuous MDC, or the management access made to determine whether preamble suppression is supported.

While the DP83848 requires an initial preamble sequence of 32 bits for management initialization, it does not require a full 32-bit sequence between each subsequent transaction. A minimum of one idle bit between management transactions is required as specified in the IEEE 802.3u specification.

8.5 Programming

8.5.1 Auto-Negotiation

The auto-negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast link pulse (FLP) bursts provide the signalling used to communicate auto-negotiation abilities between two devices at each end of a link segment. For further detail regarding auto-negotiation, refer to Clause 28 of the IEEE 802.3u specification. The DP83848 supports four different ethernet protocols (10 Mb/s half duplex, 10 Mb/s full duplex, 100 Mb/s half duplex, and 100 Mb/s full duplex), so the inclusion of auto-negotiation ensures that the highest performance protocol will be selected based on the advertised ability of the link partner. The auto-negotiation function within the DP83848 can be controlled either by internal register access or by the use of the AN_EN, AN1 and AN0 pins.

8.5.1.1 Auto-Negotiation Pin Control

The state of AN_EN, AN0 and AN1 determines whether the DP83848 is forced into a specific mode or auto-negotiation will advertise a specific ability (or set of abilities) as given in Table 33. These pins allow configuration options to be selected without requiring internal register access.

The state of AN_EN, AN0 and AN1, upon power-up/reset, determines the state of bits [8:5] of the ANAR register.

The auto-negotiation function selected at power-up or reset can be changed at any time by writing to the basic mode control register (BMCR) at address 0x00h.

Table 33. Auto-Negotiation Modes

AN_EN	AN1	AN0	Forced Mode
0	0	0	10BASE-T, Half Duplex
0	0	1	10BASE-T, Full Duplex
0	1	0	100BASE-TX, Half Duplex
0	1	1	100BASE-TX, Full Duplex
AN_EN	**AN1**	**AN0**	**Advertised Mode**
1	0	0	10BASE-T, Half or Full Duplex
1	0	1	100BASE-TX, Half or Full Duplex

Programming (continued)

Table 33. Auto-Negotiation Modes (continued)

AN_EN	AN1	AN0	Forced Mode
1	1	0	10BASE-T Half Duplex 100BASE-TX, Half Duplex
1	1	1	10BASE-T, Half/Full Duplex 100BASE-TX, Half/Full Duplex

8.5.1.2 Auto-Negotiation Register Control

When auto-negotiation is enabled, the DP83848 transmits the abilities programmed into the auto-negotiation advertisement register (ANAR) at address 04h via FLP Bursts. Any combination of 10 Mb/s, 100 Mb/s, half duplex, and full duplex modes may be selected.

Auto-negotiation priority resolution:

1. 100BASE-TX full duplex (highest priority)
2. 100BASE-TX half duplex
3. 10BASE-T full duplex
4. 10BASE-T half duplex (lowest priority)

The basic mode control register (BMCR) at address 00h provides control for enabling, disabling, and restarting the auto-negotiation process. When auto-negotiation is disabled, the speed selection bit in the BMCR controls switching between 10 Mb/s or 100 Mb/s operation, and the duplex mode bit controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the auto-negotiation enable bit is set.

The link speed can be examined through the PHY status register (PHYSTS) at address 10h after a Link is achieved.

The BMSR indicates the set of available abilities for technology types, auto-negotiation ability, and extended register capability. These bits are permanently set to indicate the full functionality of the DP83848 (only the 100BASE-T4 bit is not set since the DP83848 does not support that function).

The BMSR also provides status on:

- Whether or not auto-negotiation is complete
- Whether or not the Link Partner is advertising that a remote fault has occurred
- Whether or not valid link has been established
- Support for management frame preamble suppression

The ANAR indicates the auto-negotiation abilities to be advertised by the DP83848. All available abilities are transmitted by default, but any ability can be suppressed by writing to the ANAR. Updating the ANAR to suppress an ability is one way for a management agent to change (restrict) the technology that is used.

The auto-negotiation link partner ability register (ANLPAR) at address 05h is used to receive the base link code word as well as all next page code words during the negotiation. Furthermore, the ANLPAR will be updated to either 0081h or 0021h for parallel detection to either 100 Mb/s or 10 Mb/s respectively.

The auto-negotiation expansion register (ANER) indicates additional auto-negotiation status. The ANER provides status on:

- Whether or not a parallel detect fault has occurred
- Whether or not the link partner supports the next page function
- Whether or not the DP83848 supports the next page function
- Whether or not the current page being exchanged by auto-negotiation has been received
- Whether or not the link partner supports auto negotiation

8.5.1.3 Auto-Negotiation Parallel Detection

The DP83848 supports the parallel detection function as defined in the IEEE 802.3u specification. Parallel detection requires both the 10 Mb/s and 100 Mb/s receivers to monitor the receive signal and report link status to the auto-negotiation function. Auto-negotiation uses this information to configure the correct technology in the event that the link partner does not support auto-negotiation but is transmitting link signals that the 100BASE-TX or 10BASET PMAs recognize as valid link signals.

If the DP83848 completes auto-negotiation as a result of parallel detection, bits 5 and 7 within the ANLPAR register will be set to reflect the mode of operation present in the link partner. Note that bits 4:0 of the ANLPAR will also be set to 00001 based on a successful parallel detection to indicate a valid 802.3 selector field. Software may determine that negotiation completed via parallel detection by reading a zero in the link partner auto-negotiation able bit once the auto-negotiation complete bit is set. If configured for parallel detect mode and any condition other than a single good link occurs then the parallel detect fault bit will be set.

8.5.1.4 Auto-Negotiation Restart

Once auto-negotiation has completed, it may be restarted at any time by setting bit 9 (restart auto-negotiation) of the BMCR to one. If the mode configured by a successful auto-negotiation loses a valid link, then the auto-negotiation process will resume and attempt to determine the configuration for the link. This function ensures that a valid configuration is maintained if the cable becomes disconnected.

A renegotiation request from any entity, such as a management agent, will cause the DP83848 to halt any transmit data and link pulse activity until the break_link_timer expires (~1500 ms). Consequently, the link partner will go into link fail and normal auto-negotiation resumes. The DP83848 will resume auto-negotiation after the break_link_timer has expired by issuing FLP bursts.

8.5.1.5 Enabling Auto-Negotiation via Software

It is important to note that if the DP83848 has been initialized upon power-up as a non-auto-negotiating device (forced technology), and it is then required that auto-negotiation or re-auto-negotiation be initiated via software, bit 12 (auto-negotiation enable) of the BMCR must first be cleared and then set for any auto-negotiation function to take effect.

8.5.1.6 Auto-Negotiation Complete Time

Parallel detection and auto-negotiation take approximately 2 to 3 seconds to complete. In addition, auto-negotiation with next page should take approximately 2 to 3 seconds to complete, depending on the number of next pages sent.

Refer to Clause 28 of the IEEE 802.3u standard for a full description of the individual timers related to auto-negotiation.

8.5.2 Auto-MDIX

When enabled, this function utilizes auto-negotiation to determine the proper configuration for transmission and reception of data and subsequently selects the appropriate MDI pair for MDI/MDIX operation. The function uses a random seed to control switching of the crossover circuitry. This implementation complies with the corresponding IEEE 802.3 auto-negotiation and crossover specifications.

Auto-MDIX is enabled by default and can be configured via strap or via PHYCR (0x19h) register, bits [15:14].

Neither auto-negotiation nor auto-MDIX is required to be enabled in forcing crossover of the MDI pairs. Forced crossover can be achieved through the FORCE_MDIX bit, bit 14 of PHYCR (0x19h) register.

NOTE

Auto-MDIX will not work in a forced mode of operation.

8.5.3 PHY Address

The 5 PHY address inputs pins are shared with the RXD[3:0] pins and COL pin as shown in Table 34.

Table 34. PHY Address Mapping

PIN NUMBER	PHYAD FUNCTION	RXD FUNCTION
42	PHYAD0	COL
43	PHYAD1	RXD_0
44	PHYAD2	RXD_1
45	PHYAD3	RXD_2
46	PHYAD4	RXD_3

The DP83848 can be set to respond to any of 32 possible PHY addresses via strap pins. The information is latched into the PHYCR (address 19h, bits [4:0]) at device power-up and hardware reset. The PHY address pins are shared with the RXD and COL pins. Each DP83848 or port sharing an MDIO bus in a system must have a unique physical address.

The DP83848 supports PHY address strapping values 0 (<00000>) through 31 (<11111>). Strapping PHY address 0 puts the part into isolate mode. It should also be noted that selecting PHY address 0 via an MDIO write to PHYCR will not put the device in isolate mode.

For further detail relating to the latch-in timing requirements of the PHY address pins, as well as the other hardware configuration pins, refer to the Reset summary in *Reset Operation*.

Since the PHYAD[0] pin has weak internal pull-up resistor and PHYAD[4:1] pins have weak internal pull-down resistors, the default setting for the PHY address is 00001 (01h).

Refer to Figure 38 for an example of a PHYAD connection to external components. In this example, the PHYAD strapping results in address 00011 (03h).

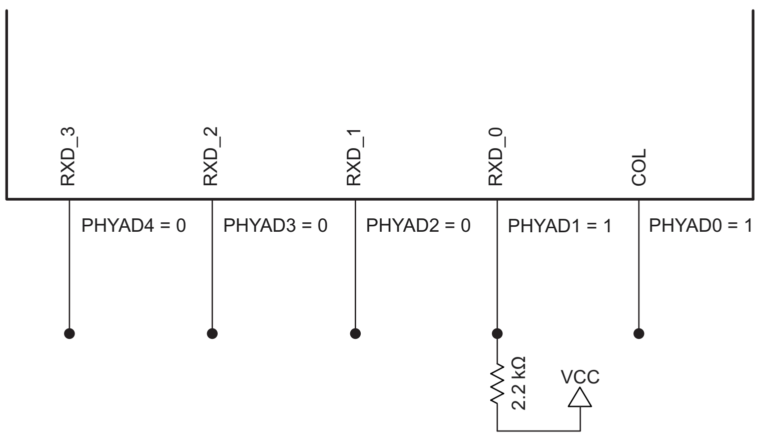


Figure 38. PHYAD Strapping Example

8.5.3.1 MII Isolate Mode

The DP83848 can be put into MII isolate mode by writing to bit 10 of the BMCR register or by strapping in physical address 0. It should be noted that selecting physical address 0 via an MDIO write to PHYCR will not put the device in the MII isolate mode.

When in the MII isolate mode, the DP83848 does not respond to packet data present at TXD[3:0], TX_EN inputs and presents a high impedance on the TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS outputs. When in Isolate mode, the DP83848 will continue to respond to all management transactions.

While in Isolate mode, the PMD output pair will not transmit packet data but will continue to source 100BASE-TX scrambled idles or 10BASE-T normal link pulses.

The DP83848 can auto-negotiate or parallel detect to a specific technology depending on the receive signal at the PMD input pair. A valid link can be established for the receiver even when the DP83848 is in Isolate mode.

8.5.4 LED Interface

The DP83848 supports three configurable light emitting diode (LED) pins. The device supports three LED configurations: Link, Speed, Activity and Collision. Functions are multiplexed among the LEDs. The PHYCR for the LEDs can also be selected through address 19h, bits [6:5].

Table 35. LED Mode Select

MODE	LED_CGF[1] (BIT 6)	LED_CFG[0] (BIT 5) or (PIN 40)	LED_LINK	LED_SPEED	LED_ACT/COL
1	don't care	1	ON for good link OFF for no link	ON in 100 Mb/s OFF in 10 Mb/s	ON for activity OFF for no activity
2	0	0	ON for good Link BLINK for activity	ON in 100 Mb/s OFF in 10 Mb/s	ON for collision OFF for no collision
3	1	0	ON for good link BLINK for activity	ON in 100 Mb/s OFF in 10 Mb/s	ON for full duplex OFF for half duplex

The LED_LINK pin in Mode 1 indicates the link status of the port. In 100BASE-T mode, link is established as a result of input receive amplitude compliant with the TPPMD specifications which will result in internal generation of signal detect. A 10 Mb/s Link is established as a result of the reception of at least seven consecutive normal link pulses or the reception of a valid 10BASE-T packet. This will cause the assertion of LED_LINK. LED_LINK will deassert in accordance with the Link Loss Timer as specified in the IEEE 802.3 specification.

The LED_LINK pin in Mode 1 will be OFF when no LINK is present.

The LED_LINK pin in Mode 2 and Mode 3 will be ON to indicate Link is good and BLINK to indicate activity is present on either transmit or receive activity.

The LED_SPEED pin indicates 10 or 100 Mb/s data rate of the port. The standard CMOS driver goes high when operating in 100 Mb/s operation. The functionality of this LED is independent of mode selected.

The LED_ACT/COL pin in Mode 1 indicates the presence of either transmit or receive activity. The LED will be ON for Activity and OFF for No Activity. In Mode 2, this pin indicates the Collision status of the port. The LED will be ON for Collision and OFF for No Collision.

The LED_ACT/COL pin in Mode 3 indicates the presence of duplex status for 10 Mb/s or 100 Mb/s operation. The LED will be ON for full duplex and OFF for half duplex.

In 10 Mb/s half duplex mode, the collision LED is based on the COL signal.

Since these LED pins are also used as strap options, the polarity of the LED is dependent on whether the pin is pulled up or down.

8.5.4.1 LEDs

Since the auto-negotiation (AN) strap options share the LED output pins, the external components required for strapping and LED usage must be considered in order to avoid contention.

Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding AN input upon power-up/reset. For example, if a given AN input is resistively pulled low then the corresponding output will be configured as an active high driver. Conversely, if a given AN input is resistively pulled high, then the corresponding output will be configured as an active low driver.

Refer to Figure 39 for an example of AN connections to external components. In this example, the AN strapping results in auto-negotiation with 10/100 half or full duplex advertised.

The adaptive nature of the LED outputs helps to simplify potential implementation issues of these dual purpose pins.

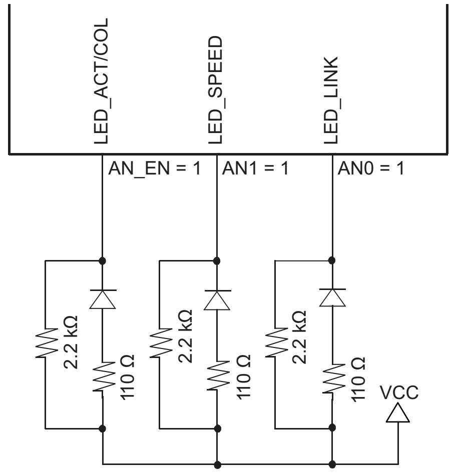


Figure 39. AN Strapping and LED Loading Example

8.5.4.2 LED Direct Control

The DP83848 provides another option to directly control any or all LED outputs through the LED direct control register (LEDCR), address 18h. The register does not provide read access to LEDs.

8.5.5 Half Duplex vs Full Duplex

The DP83848 supports both half and full duplex operation at both 10 Mb/s and 100 Mb/s speeds.

Half duplex relies on the CSMA/CD protocol to handle collisions and network access. In half duplex mode, CRS responds to both transmit and receive activity in order to maintain compliance with the IEEE 802.3 specification.

Since the DP83848 is designed to support simultaneous transmit and receive activity it is capable of supporting fullduplex switched applications with a throughput of up to 200 Mb/s per port when operating in 100BASE-TX mode. Because the CSMA/CD protocol does not apply to fullduplex operation, the DP83848 disables its own internal collision sensing and reporting functions and modifies the behavior of carrier sense (CRS) such that it indicates only receive activity. This allows a full duplex capable MAC to operate properly.

All modes of operation (100BASE-TX and 10BASE-T) can run either half duplex or full duplex. Additionally, other than CRS and collision reporting, all remaining MII signaling remains the same regardless of the selected duplex mode.

It is important to understand that while auto-negotiation with the use of fast link pulse code words can interpret and configure to full duplex operation, parallel detection can not recognize the difference between full and half duplex from a fixed 10 Mb/s or 100 Mb/s link partner over twisted pair. As specified in the 802.3u specification, if a far-end link partner is configured to a forced full duplex 100BASE-TX ability, the parallel detection state machine in the partner would be unable to detect the full duplex capability of the far-end link partner. This link segment would negotiate to a half duplex 100BASE-TX configuration (same scenario for 10 Mb/s).

8.5.6 Internal Loopback

The DP83848 includes a loopback test mode for facilitating system diagnostics. The loopback mode is selected through bit 14 (loopback) of the BMCR. Writing 1 to this bit enables MII transmit data to be routed to the MII receive outputs. Loopback status may be checked in bit 3 of PHYSTS. While in loopback mode the data will not be transmitted onto the media. To ensure that the desired operating mode is maintained, Auto-Negotiation should be disabled before selecting the loopback mode.

8.5.7 BIST

The DP83848 incorporates an internal built-in self test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be utilized to test the integrity of the transmit and receive data paths. BIST testing can be performed with the part in the internal loopback mode or externally looped back using a loopback cable fixture.

The BIST is implemented with independent transmit and receive paths, with the transmit block generating a continuous stream of a pseudo random sequence. The user can select a 9 bit or 15 bit pseudorandom sequence from the PSR_15 bit in the PHYCR. The received data is compared to the generated pseudo-random data by the BIST linear feedback shift register (LFSR) to determine the BIST pass or fail status.

The pass or fail status of the BIST is stored in the BIST status bit in the PHYCR register. The status bit defaults to 0 (BIST fail) and transitions on a successful comparison. If an error (mis-compare) occurs, the status bit is latched and is cleared upon a subsequent write to the Start/Stop bit.

For transmit VOD testing, the packet BIST continuous mode can be used to allow continuous data transmission, setting BIST_CONT_MODE, bit 5, of CDCTRL1 (0x1Bh).

The number of BIST errors can be monitored through the BIST error count in the CDCTRL1 (0x1Bh), bits [15:8].

8.6 Register Maps

8.6.1 Register Block

Table 36. Register Map

OFFSET		ACCESS	TAG	DESCRIPTION
HEX	DECIMAL			
00h	0	RW	BMCR	Basic Mode Control Register
01h	1	RO	BMSR	Basic Mode Status Register
02h	2	RO	PHYIDR1	PHY Identifier Register 1
03h	3	RO	PHYIDR2	PHY Identifier Register 2
04h	4	RW	ANAR	Auto-Negotiation Advertisement Register
05h	5	RW	ANLPAR	Auto-Negotiation Link Partner Ability Register (Base Page)
05h	5	RW	ANLPARNP	Auto-Negotiation Link Partner Ability Register (Next Page)
06h	6	RW	ANER	Auto-Negotiation Expansion Register
07h	7	RW	ANNPTR	Auto-Negotiation Next Page TX
08h-Fh	15-Aug	RW	RESERVED	RESERVED
EXTENDED REGISTERS				
10h	16	RO	PHYSTS	PHY Status Register
11h	17	RW	MICR	MII Interrupt Control Register
12h	18	RO	MISR	MII Interrupt Status Register
13h	19	RW	RESERVED	RESERVED
14h	20	RO	FCSCR	False Carrier Sense Counter Register
15h	21	RO	RECR	Receive Error Counter Register
16h	22	RW	PCSR	PCS Sub-Layer Configuration and Status Register
17h	23	RW	RBR	RMII and Bypass Register
18h	24	RW	LEDCR	LED Direct Control Register
19h	25	RW	PHYCR	PHY Control Register
1Ah	26	RW	10BTSCR	10Base-T Status/Control Register
1Bh	27	RW	CDCTRL1	CD Test Control Register and BIST Extensions Register
1Ch	28	RW	RESERVED	RESERVED
1Dh	29	RW	EDCR	Energy Detect Control Register
1Eh-1Fh	30-31	RW	RESERVED	RESERVED

Table 37. Register Table

REGISTER NAME	ADDRESS	TAG	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT0
Basic Mode Control Register	00h	BMCR	Reset	Loop- back	Speed Selection	Auto- Neg Enable	Power Down	Isolate	Restart Auto- Neg	Duplex Mode	Collision Test	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served
Basic Mode Status Register	01h	BMSR	100Base - T4	100Base - TX FDX	100Base - TX HDX	10Base- T FDX	10Base- T HDX	Re- served	Re- served	Re- served	Re- served	MF Pre- amble Sup- press	Auto- Neg Com- plete	Remote Fault	Auto- Neg Ability	Link Status	Jabber Detect	Extend- ed Capa- bility
PHY Identifier Register 1	02h	PHYIDR 1	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB
PHY Identifier Register 2	03h	PHYIDR 2	OUI LSB	OUI LSB	OUI LSB	OUI LSB	OUI LSB	OUI LSB	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	MDL_ REV	MDL_ REV	MDL_ REV	MDL_ REV
Auto-Negotiation Advertise-ment Register	04h	ANAR	Next Page Ind	Re- served	Remote Fault	Re- served	ASM_ DIR	PAUSE	T4	TX_FD	TX	10_FD	10	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection
Auto-Negotiation Link Partner Ability Register (Base Page)	05h	ANLPAR	Next Page Ind	ACK	Remote Fault	Re- served	ASM_ DIR	PAUSE	T4	TX_FD	TX	10_FD	10	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection
Auto-Negotiation Link Partner Ability Register Next Page	05h	AN-LPARNP	Next Page Ind	ACK	Mes- sage Page	ACK2	Toggle	Code	Code	Code	Code	Code	Code	Code	Code	Code	Code	Code
Auto-Negotiation Expansion Register	06h	ANER	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	PDF	LP_NP_ ABLE	NP_ ABLE	PAGE_ RX	LP_AN_ ABLE
Auto-Negotiation Next Page TX Register	07h	ANNPTR	Next Page Ind	Re- served	Message Page	ACK2	TOG_TX	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE
Reserved	08-0fh	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served	Re- served

Table 37. Register Table (continued)

REGISTER NAME	ADDRESS	TAG	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT0
EXTENDED REGISTERS																		
PHY Status Register	10h	PHYSTS	Reserved	MDI-X mode	Rx Err Latch	Polarity Status	False Carrier Sense	Signal Detect	Descram Lock	Page Receive	MII Interrupt	Remote Fault	Jabber Detect	Auto- Neg Complete	Loopback Status	Duplex Status	Speed Status	Link Status
MII Interrupt Control Register	11h	MICR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TINT	INTEN	INT_OE
MII Interrupt Status and Misc. Control Register	12h	MISR	Reserved	ED_INT	LINK_ INT	SPD_ INT	DUP_ INT	ANC_ INT	FHF_ INT	RHF_ INT	Reserved	UNMSK_ ED	UNMSK_ LINK	UNMSK_ JAB	UNMSK_ RF	UNMSK_ ANC	UNMSK_ FHF	UNMSK_ RHF
Reserved	13h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
False Carrier Sense Counter Register	14h	FCSCR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT	FCSCNT
Receive Error Counter Register	15h	RECR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT
PCS Sub-Layer Configura-tion and Status Register	16h	PCSR	Reserved	Reserved	Reserved	BYP_4B 5B	Reserved	TQ_EN	SD_FOR CE_PMA	SD_ OPTION	DESC_ TIME	Reserved	FORCE_ 100_OK	Reserved	Reserved	NRZI_ BYPASS	SCRAM_ BYPASS	DE SCRAM_ BYPASS
RMII and Bypass Register	17h	RBR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RMII_ MODE	RMII_ REV1_0	RX_OVF _STS	RX_UNF _STS	RX_RD_ PTR[1]	RX_RD_ PTR[0]
LED Direct Control Register	18h	LEDCR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DRV_SP DLED	DRV_LN KLED	DRV_AC TLED	SPDLED	LNKLED	ACTLED
PHY Control Register	19h	PHYCR	MDIX_EN	FORCE_ MDIX	PAUSE_ RX	PAUSE_ TX	BIST_fe	PSR_15	BIST_ STATUS	BIST_ START	BP_ STRETCH	LED_ CNFG[1]	LED_ CNFG[0]	PHY ADDR	PHY ADDR	PHY ADDR	PHY ADDR	PHY ADDR
10Base-T Status/ Control Register	1Ah	10BT_S ERIAL	10BT_S ERIAL	REJECT 100 BASE T	ERROR RANGE	ERROR RANGE	SQUELCH	SQUELCH	SQUELCH	LOOPBA CK_10_ DIS	LP_DIS	FORC_ LINK_10	Reserved	POLARITY	Reserved	Reserved	HEART_ DIS	JABBER _DIS
CD Test Control and BIST Extensions Register	1Bh	CDCTRL 1	BIST_ ERROR _COUNT	BIST_ ERROR _COUNT	BIST_ ERROR _COUNT	BIST_ ERROR _COUNT	BIST_ ERROR _COUNT	BIST_ ERROR _COUNT	BIST_ ERROR _COUNT	BIST_ ERROR _COUNT	Reserved	Reserved	BIST_ CONT_ MODE	CDPattE N_10	Reserved	10Meg_ Patt_ Gap	CDPatt-Sel	CDPatt-Sel
Reserved	1Ch	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Energy Detect Control Register	1Dh	EDCR	ED_EN	ED_ AUTO_ UP	ED_ AUTO_ DOWN	ED_ MAN	ED_ BURST_ DIS	ED_ PWR_ STATE	ED_ERR _MET	ED_ DATA_ MET	ED_ERR _COUNT	ED_ERR _COUNT	ED_ERR _COUNT	ED_ERR _COUNT	ED_ DATA_ COUNT	ED_ DATA_ COUNT	ED_ DATA_ COUNT	ED_ DATA_ COUNT
Reserved	1Eh-1Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

8.6.2 Register Definition

In the register definitions under the 'Default' heading, the following definitions hold true:

- RW = Read Write access
- SC = Register sets on event occurrence and Self-Clears when event ends
- RW/SC = Read Write access/Self Clearing bit
- RO = Read Only access
- COR = Clear on Read
- RO/COR = Read Only, Clear on Read
- RO/P = Read Only, Permanently set to a default value
- LL = Latched Low and held until read, based upon the occurrence of the corresponding event
- LH = Latched High and held until read, based upon the occurrence of the corresponding event

8.6.2.1 Basic Mode Control Register (BMCR)

Table 38. Basic Mode Control Register (BMCR), Address 0x00

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	Reset	0, RW/SC	Reset: 1 = Initiate software Reset/Reset in Process 0 = Normal operation This bit, which is self-clearing, returns a value of one until the reset process is complete. The configuration is re-strapped.
14	Loopback	0, RW	Loopback: 1 = Loopback enabled 0 = Normal operation The loopback function enables MII transmit data to be routed to the MII receive data path. Setting this bit may cause the descrambler to lose synchronization and produce a 500 µs "dead time" before any valid data will appear at the MII receive outputs.
13	Speed Selection	Strap, RW	Speed Select: When auto-negotiation is disabled writing to this bit allows the port speed to be selected. 1 = 100 Mb/s 0 = 10 Mb/s
12	Auto-Negotiation Enable	Strap, RW	Auto-Negotiation Enable: Strap controls initial value at reset 1 = Auto-Negotiation Enabled - bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled - bits 8 and 13 determine the port speed and duplex mode.
11	Power Down	0, RW	Power Down: 1 = Power down 0 = Normal opeation. Setting this bit powers down the PHY. Only the register block is enabled during a power down condition. This bit is OR'd with the input from the PWR_DOWN/INT pin. When the active low PWR_DOWN/INT pin is asserted, this bit will be set.
10	Isolate	0, RW	Isolate: 1 = Isolates the Port from the MII with the exception of the serial man-agement. 0 = Normal operation

Table 38. Basic Mode Control Register (BMCR), Address 0x00 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
9	Restart Auto- Negotiation	0, RW/SC	Restart Auto-Negotiation: 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation pro- cess. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal operation
8	Duplex Mode	Strap, RW	Duplex Mode: When auto-negotiation is disabled writing to this bit allows the port Duplex capability to be selected. 1 = Full Duplex operation 0 = Half Duplex operatio.
7	Collision Test	0, RW	Collision Test: 1 = Collision test enabled 0 = Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TX_EN.
6:00	RESERVED	0, RO	RESERVED: Write ignored, read as 0

8.6.2.2 Basic Mode Status Register (BMSR)

Table 39. Basic Mode Status Register (BMSR), Address 0x01

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100BASE-T4	0, RO/P	100BASE-T4 Capable: 0 = Device not able to perform 100BASE-T4 mode
14	100BASE-T Full Duplex	1, RO/P	100BASE-TX Full Duplex Capable: 1 = Device able to perform 100BASE-TX in full duplex mode
13	100BASE-T Half Duplex	1, RO/P	100BASE-TX Half Duplex Capable: 1 = Device able to perform 100BASE-TX in half duplex mode
12	10BASE-T Full Duplex	1, RO/P	10BASE-T Full Duplex Capable: 1 = Device able to perform 10BASE-T in full duplex mode
11	10BASE-T Half Duplex	1, RO/P	10BASE-T Half Duplex Capable: 1 = Device able to perform 10BASE-T in half duplex mode
10:07	RESERVED	0, RO	RESERVED: Write as 0, read as 0
6	MF Preamble Suppression	1, RO/P	Preamble suppression Capable: 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. 0 = Normal management operation
5	Auto-Negotiation Com- plete	0, RO	Auto-Negotiation Complete: 1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Remote Fault	0, RO/LH	Remote Fault: 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected
3	Auto-Negotiation Ability	1, RO/P	Auto Negotiation Ability: 1 = Device is able to perform Auto-Negotiation 0 = Device is not able to perform Auto-Negotiation

Table 39. Basic Mode Status Register (BMSR), Address 0x01 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
2	Link Status	0, RO/LL	Link Status: 1 = Valid link established (for either 10 or 100 Mb/s operation) 0 = Link not established The criteria for link validity is implementation specific. The occurrence of a link failure condition will causes the Link Status bit to clear. Once cleared, this bit may only be set by establishing a good link condition and a read via the management interface.
1	Jabber Detect	0, RO/LH	Jabber Detect: This bit only has meaning in 10 Mb/s mode 1 = Jabber condition detected 0 = No Jabber This bit is implemented with a latching function, such that the occurrence of a jabber condition causes it to set until it is cleared by a read to this register by the management interface or by a reset.
0	Extended Capability	1, RO/P	Extended Capability: 1 = Extended register capabilities 0 = Basic register set capabilities only

8.6.2.3 PHY Identifier Register 1 (PHYIDR1)

The PHY Identifier Registers 1 and 2 together form a unique identifier for the DP83848. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. National's IEEE assigned OUI is 080017h.

Table 40. PHY Identifier Register 1 (PHYIDR1), Address 0x02

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	OUI_MSB	<0010 0000 0000 0000>, RO/P	OUI Most Significant Bits: Bits 3 to 18 of the OUI (080017h) are stored in bits 15 to 0 of this register. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

8.6.2.4 PHY Identifier Register 2 (PHYIDR2)

Table 41. PHY Identifier Register 2 (PHYIDR2), Address 0x03

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	OUI_LSB	<0101 11>, RO/P	OUI Least Significant Bits: Bits 19 to 24 of the OUI (080017h) are mapped from bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	<00 1001 >, RO/P	Vendor Model Number: The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	<0000>, RO/P	Model Revision Number: Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

8.6.2.5 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-Negotiation.

Table 42. Negotiation Advertisement Register (ANAR), Address 0x04

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	Next Page Indication: 0 = Next Page Transfer not desired 1 = Next Page Transfer desired
14	RESERVED	0, RO/P	RESERVED by IEEE: Writes ignored, Read as 0
13	RF	0, RW	Remote Fault: 1 = Advertises that this device has detected a Remote Fault 0 = No Remote Fault detected
12	RESERVED	0, RW	RESERVED for Future IEEE use: Write as 0, Read as 0
11	ASM_DIR	0, RW	Asymmetric PAUSE Support for Full Duplex Links: The ASM_DIR bit indicates that asymmetric PAUSE is supported. Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12]. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0 = No MAC based full duplex flow control
10	PAUSE	0, RW	PAUSE Support for Full Duplex Links: The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12]. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0= No MAC based full duplex flow control
9	T4	0, RO/P	100BASE-T4 Support: 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 not supported
8	TX_FD	Strap, RW	100BASE-TX Full Duplex Support: 1 = 100BASE-TX Full Duplex is supported by the local device 0 = 100BASE-TX Full Duplex not supported
7	TX	Strap, RW	100BASE-TX Support: 1 = 100BASE-TX is supported by the local device 0 = 100BASE-TX not supported
6	10_FD	Strap, RW	10BASE-T Full Duplex Support: 1 = 10BASE-T Full Duplex is supported by the local device 0 = 10BASE-T Full Duplex not supported
5	10	Strap, RW	10BASE-T Support: 1 = 10BASE-T is supported by the local device 0 = 10BASE-T not supported
4:0	Selector	<00001>, RW	Protocol Selection Bits: These bits contain the binary encoded protocol selector supported by this port. <00001> indicates that this device supports IEEE 802.3u.

8.6.2.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page)

This register contains the advertised abilities of the link partner as received during auto-negotiation. The content changes after the successful auto-negotiation if next-pages are supported.

Table 43. Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page), Address 0x05

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	Next Page Indication: 0 = Link Partner does not desire Next Page Transfer 1 = Link Partner desires Next Page Transfer
14	ACK	0, RO	Acknowledge: 1 = Link Partner acknowledges reception of the ability data word 0 = Not acknowledged The Auto-Negotiation state machine will automatically control the this bit based on the incoming FLP bursts.
13	RF	0, RO	Remote Fault: 1 = Remote Fault indicated by Link Partner 0 = No Remote Fault indicated by Link Partner
12	RESERVED	0, RO	RESERVED for Future IEEE use: Write as 0, read as 0
11	ASM_DIR	0, RO	ASYMMETRIC PAUSE: 1 = Asymmetric pause is supported by the Link Partner 0 = Asymmetric pause is not supported by the Link Partner
10	PAUSE	0, RO	PAUSE: 1 = Pause function is supported by the Link Partner 0 = Pause function is not supported by the Link Partner
9	T4	0, RO	100BASE-T4 Support: 1 = 100BASE-T4 is supported by the Link Partner 0 = 100BASE-T4 not supported by the Link Partner
8	TX_FD	0, RO	100BASE-TX Full Duplex Support: 1 = 100BASE-TX Full Duplex is supported by the Link Partner 0 = 100BASE-TX Full Duplex not supported by the Link Partner
7	TX	0, RO	100BASE-TX Support: 1 = 100BASE-TX is supported by the Link Partner 0 = 100BASE-TX not supported by the Link Partner
6	10_FD	0, RO	10BASE-T Full Duplex Support: 1 = 10BASE-T Full Duplex is supported by the Link Partner 0 = 10BASE-T Full Duplex not supported by the Link Partner
5	10	0, RO	10BASE-T Support: 1 = 10BASE-T is supported by the Link Partner 0 = 10BASE-T not supported by the Link Partner
4:0	Selector	<0 0000>, RO	Protocol Selection Bits: Link Partner’s binary encoded protocol selector

8.6.2.7 Auto-Negotiation Link Partner Ability Register (ANLPAR) (Next Page)

Table 44. Auto-Negotiation Link Partner Ability Register (ANLPAR) (Next Page), Address 0x05

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	Next Page Indication: 1 = Link Partner desires Next Page Transfer 0 = Link Partner does not desire Next Page Transfer

Table 44. Auto-Negotiation Link Partner Ability Register (ANLPAR) (Next Page), Address 0x05 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
14	ACK	0, RO	Acknowledge: 1 = Link Partner acknowledges reception of the ability data word 0 = Not acknowledged The Auto-Negotiation state machine will automatically control the this bit based on the incoming FLP bursts. Software should not attempt to write to this bit.
13	MP	0, RO	Message Page: 1 = Message Page 0 = Unformatted Page
12	ACK2	0, RO	Acknowledge 2: 1 = Link Partner does have the ability to comply to next page message 0 = Link Partner does not have the ability to comply to next page message
11	Toggle	0, RO	Toggle: 1 = Previous value of the transmitted Link Code word equalled 0 0 = Previous value of the transmitted Link Code word equalled 1
10:0	CODE	<000 0000 0000>, RO	Code: This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a “Message Page,” as defined in annex 28C of Clause 28. Otherwise, the code shall be interpreted as an “Unformatted Page,” and the interpretation is application specific.

8.6.2.8 Auto-Negotiate Expansion Register (ANER)

This register contains additional local device and link partner status information.

Table 45. Auto-Negotiate Expansion Register (ANER), Address 0x06

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:5	RESERVED	0, RO	RESERVED: Writes ignored, Read as 0
4	PDF	0, RO	Parallel Detection Fault: 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected
3	LP_NP_ABLE	0, RO	Link Partner Next Page Able: 1 = Link Partner does support Next Page 0 = Link Partner does not support Next Page
2	NP_ABLE	1, RO/P	Next Page Able: 1 = Indicates local device is able to send additional “Next Pages”
1	PAGE_RX	0, RO/COR	Link Code Word Page Received: 1 = Link Code Word has been received, cleared on a read 0 = Link Code Word has not been received
0	LP_AN_ABLE	0, RO	Link Partner Auto-Negotiation Able: 1 = indicates that the Link Partner supports Auto-Negotiation 0 = indicates that the Link Partner does not support Auto-Negotiation

8.6.2.9 Auto-Negotiation Next Page Transmit Register (ANNPTR)

This register contains the next page information sent by this device to its link partner during auto-negotiation.

Table 46. Auto-Negotiation Next Page Transmit Register (ANNPTR), Address 0x07

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	Next Page Indication: 0 = No other Next Page Transfer desired 1 = Another Next Page desired
14	RESERVED	0, RO	RESERVED: Writes ignored, read as 0
13	MP	1, RW	Message Page: 1 = Message Page 0 = Unformatted Page
12	ACK2	0, RW	Acknowledge2: 1 = Will comply with message 0 = Cannot comply with message Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	TOG_TX	0, RO	Toggle: 1 = Value of toggle bit in previously transmitted Link Code Word was 0 0 = Value of toggle bit in previously transmitted Link Code Word was 1 Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	<000 0000 0001>, RW	This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page", as defined in annex 28C of IEEE 802.3u. Otherwise, the code shall be interpreted as an "Unformatted Page", and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

8.6.3 Extended Registers

8.6.3.1 PHY Status Register (PHYSTS)

This register provides a single location within the register set for quick access to commonly accessed information.

Table 47. PHY Status Register (PHYSTS), Address 0x10

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED: Write ignored, read as 0
14	MDI-X Mode	0, RO	MDI-X mode as reported by the Auto-Negotiation logic: This bit will be affected by the settings of the MDIX_EN and FORCE_MDIX bits in the PHYCR register. When MDIX is enabled, but not forced, this bit will update dynamically as the Auto-MDIX algorithm swaps between MDI and MDI-X configurations. 1 = MDI pairs swapped (Receive on TPTD pair, Transmit on TPRD pair) 0 = MDI pairs normal (Receive on TRD pair, Transmit on TPTD pair)

Table 47. PHY Status Register (PHYSTS), Address 0x10 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
13	Receive Error Latch	0, RO/LH	Receive Error Latch: This bit will be cleared upon a read of the RECR register. 1 = Receive error event has occurred since last read of RXERCNT (address 0x15, Page 0) 0 = No receive error event has occurred
12	Polarity Status	0, RO	Polarity Status: This bit is a duplication of bit 4 in the 10BTSCR register. This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register. 1 = Inverted Polarity detected 0 = Correct Polarity detected
11	False Carrier Sense Latch	0, RO/LH	False Carrier Sense Latch: This bit will be cleared upon a read of the FCSR register. 1 = False Carrier event has occurred since last read of FCSCR (address 0x14) 0 = No False Carrier event has occurred
10	Signal Detect	0, RO/LL	100Base-TX unconditional Signal Detect from PMD
9	Descrambler Lock	0, RO/LL	100Base-TX Descrambler Lock from PMD
8	Page Received	0, RO	Link Code Word Page Received: This is a duplicate of the Page Received bit in the ANER register, but this bit will not be cleared upon a read of the PHYSTS register. 1 = A new Link Code Word Page has been received. Cleared on read of the ANER (address 0x06, bit 1) 0 = Link Code Word Page has not been received
7	MII Interrupt	0, RO	MII Interrupt Pending: 1 = Indicates that an internal interrupt is pending. Interrupt source can be determined by reading the MISR Register (0x12h). Reading the MISR will clear the Interrupt. 0= No interrupt pending
6	Remote Fault	0, RO	Remote Fault: 1 = Remote Fault condition detected (cleared on read of BMSR (address 01h) register or by reset). Fault criteria: notification from Link Partner of Remote Fault via Auto-Negotiation. 0 = No remote fault condition detected
5	Jabber Detect	0, RO	Jabber Detect: This bit only has meaning in 10 Mb/s mode This bit is a duplicate of the Jabber Detect bit in the BMSR register, except that it is not cleared upon a read of the PHYSTS register. 1 = Jabber condition detected 0 = No Jabber
4	Auto-Neg Complete	0, RO	Auto-Negotiation Complete: 1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete
3	Loopback Status	0, RO	Loopback: 1 = Loopback enabled 0 = Normal operation

Table 47. PHY Status Register (PHYSTS), Address 0x10 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
2	Duplex Status	0, RO	Duplex: This bit indicates duplex status and is determined from Auto-Negotiation or Forced Modes. 1 = Full duplex mode 0 = Half duplex mode Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.
1	Speed Status	0, RO	Speed10: This bit indicates the status of the speed and is determined from Auto-Negotiation or Forced Modes. 1 = 10 Mb/s mode 0 = 100 Mb/s mode Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.
0	Link Status	0, RO	Link Status: This bit is a duplicate of the Link Status bit in the BMSR register, except that it will not be cleared upon a read of the PHYSTS register. 1 = Valid link established (for either 10 or 100 Mb/s operation) 0 = Link not established

8.6.3.2 MII Interrupt Control Register (MICR)

This register implements the MII interrupt PHY specific control register. Sources for interrupt generation include: energy detect state change, link state change, speed status change, duplex status change, auto-negotiation complete or any of the counters becoming half-full. The individual interrupt events must be enabled by setting bits in the MII interrupt status and event control register (MISR).

Table 48. MII Interrupt Control Register (MICR), Address 0x11

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:3	RESERVED	0, RO	Reserved: Write ignored, Read as 0
2	TINT	0, RW	Test Interrupt: Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set. 1 = Generate an interrupt 0 = Do not generate interrupt
1	INTEN	0, RW	Interrupt Enable: Enable interrupt dependent on the event enables in the MISR register. 1 = Enable event based interrupts 0 = Disable event based interrupts
0	INT_OE	0, RW	Interrupt Output Enable: Enable interrupt events to signal via the PWR_DOWN/INT pin by configuring the PWR_DOWN/INT pin as an output. 1 = PWR_DOWN/INT is an Interrupt Output 0 = PWR_DOWN/INT is a Power Down Input

8.6.3.3 MII Interrupt Status and Miscellaneous Control Register (MISR)

This register contains event status and enables for the interrupt function. If an event has occurred since the last read of this register, the corresponding status bit will be set. If the corresponding enable bit in the register is set, an interrupt will be generated if the event occurs. The MICR register controls must also be set to allow interrupts. The status indications in this register will be set even if the interrupt is not enabled.

Table 49. MII Interrupt Status and Miscellaneous Control Register (MISR), Address 0x12

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	RESERVED: Writes ignored, Read as 0
14	ED_INT	0, RO/COR	Energy Detect interrupt: 1 = Energy detect interrupt is pending and is cleared by the current read 0 = No energy detect interrupt pending
13	LINK_INT	0, RO/COR	Change of Link Status interrupt: 1 = Change of link status interrupt is pending and is cleared by the current read 0 = No change of link status interrupt pending
12	SPD_INT	0, RO/COR	Change of speed status interrupt: 1 = Speed status change interrupt is pending and is cleared by the current read 0 = No speed status change interrupt pending
11	DUP_INT	0, RO/COR	Change of duplex status interrupt: 1 = Duplex status change interrupt is pending and is cleared by the current read 0 = No duplex status change interrupt pending
10	ANC_INT	0, RO/COR	Auto-Negotiation Complete interrupt: 1 = Auto-negotiation complete interrupt is pending and is cleared by the current read 0 = No Auto-negotiation complete interrupt pending
9	FHF_INT	0, RO/COR	False Carrier Counter half-full interrupt: 1 = False carrier counter half-full interrupt is pending and is cleared by the current read 0 = No false carrier counter half-full interrupt pending
8	RHF_INT	0, RO/COR	Receive Error Counter half-full interrupt: 1 = Receive error counter half-full interrupt is pending and is cleared by the current read 0 = No receive error carrier counter half-full interrupt pending
7	RESERVED	0, RO	RESERVED: Writes ignored, Read as 0
6	ED_INT_EN	0, RW	Enable Interrupt on energy detect event
5	LINK_INT_EN	0, RW	Enable Interrupt on change of link status
4	SPD_INT_EN	0, RW	Enable Interrupt on change of speed status
3	DUP_INT_EN	0, RW	Enable Interrupt on change of duplex status
2	ANC_INT_EN	0, RW	Enable Interrupt on Auto-negotiation complete event
1	FHF_INT_EN	0, RW	Enable Interrupt on False Carrier Counter Register half-full event
0	RHF_INT_EN	0, RW	Enable Interrupt on Receive Error Counter Register half-full event

8.6.3.4 False Carrier Sense Counter Register (FCSCR)

This counter provides information required to implement the “False Carriers” attribute within the MAU managed object class of Clause 30 of the IEEE 802.3u specification.

Table 50. False Carrier Sense Counter Register (FCSCR), Address 0x14

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	RESERVED: Writes ignored, Read as 0
7:0	FCSCNT[7:0]	0, RO/COR	False Carrier Event Counter: This 8-bit counter increments on every false carrier event. This counter sticks when it reaches its max count (FFh).

8.6.3.5 Receiver Error Counter Register (RECR)

This counter provides information required to implement the “Symbol Error During Carrier” attribute within the PHY managed object class of Clause 30 of the IEEE 802.3u specification.

Table 51. Receiver Error Counter Register (RECR), Address 0x15

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	RESERVED: Writes ignored, Read as 0
7:0	RXERCNT[7:0]	0, RO/COR	RX_ER Counter: When a valid carrier is present and there is at least one occurrence of an invalid data symbol, this 8-bit counter increments for each receive error detected. This event can increment only once per valid carrier event. If a collision is present, the attribute will not increment. The counter sticks when it reaches its max count.

8.6.3.6 100 Mb/s PCS Configuration and Status Register (PCSR)

This register contains event status and enables for the interrupt function. If an event has occurred since the last read of this register, the corresponding status bit will be set. If the corresponding enable bit in the register is set, an interrupt will be generated if the event occurs. The MICR register controls must also be set to allow interrupts. The status indications in this register will be set even if the interrupt is not enabled.

Table 52. 100 Mb/s PCS Configuration and Status Register (PCSR), Address 0x16

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	RESERVED	<00>, RO	RESERVED: Writes ignored, Read as 0
12	RESERVED	0	RESERVED: Must be zero
11	RESERVED	0	RESERVED: Must be zero
10	TQ_EN	0, RW	100Mbs True Quiet Mode Enable: 1 = Transmit True Quiet Mode 0 = Normal Transmit Mode
9	SD FORCE PMA	0, RW	Signal Detect Force PMA: 1 = Forces Signal Detection in PMA 0 = Normal SD operation
8	SD_OPTION	1, RW	Signal Detect Option: 1 = Enhanced signal detect algorithm 0 = Reduced signal detect algorithm
7	DESC_TIME	0, RW	Descrambler Timeout: Increase the descrambler timeout. When set this should allow the device to receive larger packets (>9k bytes) without loss of synchronization. 1 = 2 ms 0 = 722 µs (per ANSI X3.263: 1995 (TP-PMD) 7.2.3.3e)
6	RESERVED	0	RESERVED: Must be zero
5	FORCE_100_OK	0, RW	Force 100Mb/s Good Link: 1 = Forces 100Mb/s Good Link 0 = Normal 100Mb/s operation
4	RESERVED	0	RESERVED: Must be zero
3	RESERVED	0	RESERVED: Must be zero
2	NRZI_BYPASS	0, RW	NRZI Bypass Enable: 1 = NRZI Bypass Enabled 0 = NRZI Bypass Disabled
1	RESERVED	0	RESERVED: Must be zero
0	RESERVED	0	RESERVED: Must be zero

8.6.3.7 RMII and Bypass Register (RBR)

This register configures the RMII Mode of operation. When RMII mode is disabled, the RMII functionality is bypassed.

Table 53. RMII and Bypass Register (RBR), Addresses 0x17

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:6	RESERVED	0, RO	Reserved: Writes ignored, Read as 0
5	RMII_MODE	Strap, RW	Reduced MII Mode: 0 = Standard MII Mode 1 = Reduced MII Mode
4	RMII_REV1_0	0, RW	Reduce MII Revision 1.0: 0 = (RMII revision 1.2) CRS_DV will toggle at the end of a packet to indicate deassertion of CRS. 1 = (RMII revision 1.0) CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet.
3	RX_OVF_STS	0, RO	RX FIFO Over Flow Status: 0 = Normal 1 = Overflow detected
2	RX_UNF_STS	0, RO	RX FIFO Under Flow Status: 0 = Normal 1 = Underflow detected
1:0	ELAST_BUF[1:0]	01, RW	Receive Elasticity Buffer: This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at ±50ppm accuracy for both RMII and Receive clocks. For greater frequency tolerance the packet lengths may be scaled (i.e. for ±100ppm, the packet lengths need to be divided by 2). 00 = 14 bit tolerance (up to 16800 byte packets) 01 = 2 bit tolerance (up to 2400 byte packets) 10 = 6 bit tolerance (up to 7200 byte packets) 11 = 10 bit tolerance (up to 12000 byte packets)

8.6.3.8 LED Direct Control Register (LEDCR)

This register provides the ability to directly control any or all LED outputs. It does not provide read access to LEDs.

Table 54. LED Direct Control Register (LEDCR), Address 0x18

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:6	RESERVED	0, RO	Reserved: Writes ignored, Read as 0
5	DRV_SPDLED	0, RW	1 = Drive value of SPDLED bit onto LED_SPD output 0 = Normal operation
4	DRV_LNKLED	0, RW	1 = Drive value of LNKLED bit onto LED_LNK output 0 = Normal operation
3	DRV_ACTLED	0, RW	1 = Drive value of ACTLED bit onto LED_ACT/COL output 0 = Normal operation
2	SPDLED	0, RW	Value to force on LED_SPD output
1	LNKLED	0, RW	Value to force on LED_LNK output
0	ACTLED	0, RW	Value to force on LED_ACT/COL output

8.6.3.9 PHY Control Register (PHYCR)

Table 55. PHY Control Register (PHYCR), Address 0x19

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	MDIX_EN	Strap, RW	Auto-MDIX Enable: 1 = Enable Auto-neg Auto-MDIX capability 0 = Disable Auto-neg Auto-MDIX capability The Auto-MDIX algorithm requires that the Auto-Negotiation Enable bit in the BMCR register to be set. If Auto-Negotiation is not enabled, Auto-MDIX should be disabled as well.
14	FORCE_MDIX	0, RW	Force MDIX: 1 = Force MDI pairs to cross (Receive on TPTD pair, Transmit on TPRD pair) 0 = Normal operation
13	PAUSE_RX	0, RO	Pause Receive Negotiated: Indicates that pause receive should be enabled in the MAC. Based on ANAR[11:10] and ANLPAR[11:10] settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, “Pause Resolution”, only if the Auto-Negotiated Highest Common Denominator is a full duplex technology.
12	PAUSE_TX	0, RO	Pause Transmit Negotiated: Indicates that pause transmit should be enabled in the MAC. Based on ANAR[11:10] and ANLPAR[11:10] settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, “Pause Resolution”, only if the Auto-Negotiated Highest Common Denominator is a full duplex technology.
11	BIST_FE	0, RW/SC	BIST Force Error: 1 = Force BIST Error 0 = Normal operation This bit forces a single error, and is self clearing
10	PSR_15	0, RW	BIST Sequence select: 1 = PSR15 selected 0 = PSR9 selected
9	BIST_STATUS	0, LL/RO	BIST Test Status: 1 = BIST pass 0 = BIST fail. Latched, cleared when BIST is stopped For a count number of BIST errors, see the BIST Error Count in the CDCTRL1 register.
8	BIST_START	0, RW	BIST Start: 1 = BIST start 0 = BIST stop
7	BP_STRETCH	0, RW	Bypass LED Stretching: This will bypass the LED stretching and the LEDs will reflect the internal value. 1 = Bypass LED stretching 0 = Normal operation
6 5	LED_CNFG[1] LED_CNFG[0]	0, RW Strap, RW	LEDs Configuration: LED_CNFG [1] | LED_ CNFG[0] | Mode Description Don’t care | 1 | Mode 1 0 | 0 | Mode 2 1 | 0 | Mode 3 In Mode 1, LEDs are configured as follows:

Table 55. PHY Control Register (PHYCR), Address 0x19 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
			LED_LINK = ON for Good Link, OFF for No Link LED_SPEED = ON in 100 Mb/s, OFF in 10 Mb/s LED_ACT/COL = ON for Activity, OFF for No Activity In Mode 2, LEDs are configured as follows: LED_LINK = ON for good Link, BLINK for Activity LED_SPEED = ON in 100 Mb/s, OFF in 10 Mb/s LED_ACT/COL = ON for Collision, OFF for No Collision Full Duplex, OFF for Half Duplex In Mode 3, LEDs are configured as follows: LED_LINK = ON for Good Link, BLINK for Activity LED_SPEED = ON in 100 Mb/s, OFF in 10 Mb/s LED_ACT/COL = ON for Full Duplex, OFF for Half Duplex
4:0	PHYADDR[4:0]	Strap, RW	PHY Address: PHY address for port

8.6.3.10 10Base-T Status/Control Register (10BTSCR)

Table 56. 10Base-T Status/Control Register (10BTSCR), Address 0x1A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	10BT_SERIAL	Strap, RW	10Base-T Serial Mode (SNI): 1 = Enables 10Base-T Serial Mode 0 = Normal Operation Places 10 Mb/s transmit and receive functions in Serial Network Interface (SNI) Mode of operation. Has no effect on 100 Mb/s operation.
14:12	RESERVED	0, RW	RESERVED: Must be zero
11:9	SQUELCH	100, RW	Squelch Configuration: Used to set the Squelch ‘ON’ threshold for the receiver Default Squelch ON is 330mV peak
8	LOOPBACK_10_D IS	0, RW	In half-duplex mode, default 10BASE-T operation loops Transmit data to the Receive data in addition to transmitting the data on the physical medium. This is for consistency with earlier 10BASE2 and 10BASE5 implementations which used a shared medium. Setting this bit disables the loopback function. This bit does not affect loopback due to setting BMCR[14].
7	LP_DIS	0, RW	Normal Link Pulse Disable: 1 = Transmission of NLPs is disabled 0 = Transmission of NLPs is enabled
6	FORCE_LINK_10	0, RW	Force 10Mb Good Link: 1 = Forced Good 10Mb Link 0 = Normal Link Status
5	RESERVED	0, RW	RESERVED: Must be zero
4	POLARITY	RO/LH	10Mb Polarity Status: This bit is a duplication of bit 12 in the PHYSTS register. Both bits will be cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register. 1 = Inverted Polarity detected 0 = Correct Polarity detected
3	RESERVED	0, RW	RESERVED: Must be zero
2	RESERVED	1, RW	RESERVED: Must be zero

Table 56. 10Base-T Status/Control Register (10BTSCR), Address 0x1A (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
1	HEARTBEAT_DIS	0, RW	Heartbeat Disable: This bit only has influence in half-duplex 10Mb mode. 1 = Heartbeat function disabled 0 = Heartbeat function enabled When the device is operating at 100Mb or configured for full duplex operation, this bit will be ignored - the heartbeat function is disabled.
0	JABBER_DIS	0, RW	Jabber Disable: Applicable only in 10BASE-T. 1 = Jabber function disabled 0 = Jabber function enabled

8.6.3.11 CD Test and BIST Extensions Register (CDCTRL1)

Table 57. CD Test and BIST Extensions Register (CDCTRL1), Address 0x1B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	BIST_ERROR_CO UNT	0, RO	BIST ERROR Counter: Counts number of errored data nibbles during Packet BIST. This value will reset when Packet BIST is restarted. The counter sticks when it reaches its max count.
7:6	RESERVED	0, RW	RESERVED: Must be zero
5	BIST_CONT_MOD E	0, RW	Packet BIST Continuous Mode: Allows continuous pseudo random data transmission without any break in transmission. This can be used for transmit VOD testing. This is used in conjunction with the BIST controls in the PHYCR Register (0x19h). For 10Mb operation, jabber function must be disabled, bit 0 of the 10BTSCR (0x1Ah), JABBER_DIS = 1.
4	CDPATTEN_10	0, RW	CD Pattern Enable for 10Mb: 1 = Enabled 0 = Disabled
3	RESERVED	0, RW	RESERVED: Must be zero
2	10MEG_PATT_GA P	0, RW	Defines gap between data or NLP test sequences: 1 = 15 μs 0 = 10 μs
1:0	CDPATTSEL[1:0]	00, RW	CD Pattern Select[1:0]: If CDPATTEN_10 = 1: 00 = Data, EOP0 sequence 01 = Data, EOP1 sequence 10 = NLPs 11 = Constant Manchester 1s (10MHz sine wave) for harmonic distortion testing

8.6.3.12 Energy Detect Control (EDCR)

Table 58. Energy Detect Control (EDCR), Address 0x1D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	ED_EN	0, RW	Energy Detect Enable: Allow Energy Detect Mode. When Energy Detect is enabled and Auto-Negotiation is disabled via the BMCR register, Auto-MDIX should be disabled via the PHYCR register.

Table 58. Energy Detect Control (EDCR), Address 0x1D (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
14	ED_AUTO_UP	1, RW	Energy Detect Automatic Power Up: Automatically begin power up sequence when Energy Detect Data Threshold value (EDCR[3:0]) is reached. Alternatively, device could be powered up manually using the ED_MAN bit (ECDR[12]).
13	ED_AUTO_DOWN	1, RW	Energy Detect Automatic Power Down: Automatically begin power down sequence when no energy is detected. Alternatively, device could be powered down using the ED_MAN bit (EDCR[12]).
12	ED_MAN	0, RW/SC	Energy Detect Manual Power Up/Down: Begin power up/down sequence when this bit is asserted. When set, the Energy Detect algorithm will initiate a change of Energy Detect state regardless of threshold (error or data) and timer values. In managed applications, this bit can be set after clearing the Energy Detect interrupt to control the timing of changing the power state.
11	ED_BURST_DIS	0, RW	Energy Detect Bust Disable: Disable bursting of energy detect data pulses. By default, Energy Detect (ED) transmits a burst of 4 ED data pulses each time the CD is powered up. When bursting is disabled, only a single ED data pulse will be send each time the CD is powered up.
10	ED_PWR_STATE	0, RO	Energy Detect Power State: Indicates current Energy Detect Power state. When set, Energy Detect is in the powered up state. When cleared, Energy Detect is in the powered down state. This bit is invalid when Energy Detect is not enabled.
9	ED_ERR_MET	0, RO/COR	Energy Detect Error Threshold Met: No action is automatically taken upon receipt of error events. This bit is informational only and would be cleared on a read.
8	ED_DATA_MET	0, RO/COR	Energy Detect Data Threshold Met: The number of data events that occurred met or surpassed the Energy Detect Data Threshold. This bit is cleared on a read.
7:4	ED_ERR_COUNT	0001, RW	Energy Detect Error Threshold: Threshold to determine the number of energy detect error events that should cause the device to take action. Intended to allow averaging of noise that may be on the line. Counter will reset after approximately 2 seconds without any energy detect data events.
3:0	ED_DATA_COUNT	0001, RW	Energy Detect Data Threshold: Threshold to determine the number of energy detect events that should cause the device to take actions. Intended to allow averaging of noise that may be on the line. Counter will reset after approximately 2 seconds without any energy detect data events.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DP83848 is a robust, full featured, low power, 10/100 Physical Layer devices. The DP83848 features integrated sublayers to support both 10BASE-T and 100BASE-TX Ethernet protocols, which ensure compatibility and interoperability with all other standards based Ethernet products in these applications:

- High-end peripheral devices
- Industrial controls
- Factor automation
- General embedded applications

9.2 Typical Application

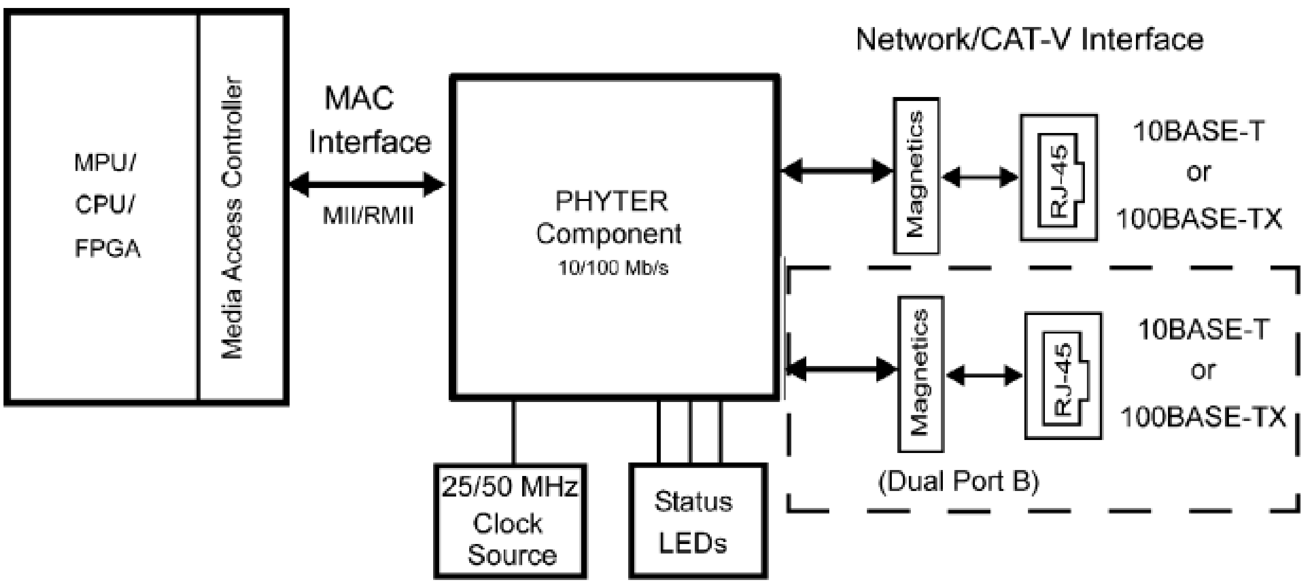


Figure 40. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Clock Requirements

DP83848 supports either an external CMOS-level oscillator source or a crystal resonator device. The X1 pin is the clock input, requiring either 25 or 50 MHz depending on the MII mode used. In MII mode (or RMII master mode in some products) either a 25-MHz crystal or 25-MHz oscillator may be used. For all PHYTER family products, the use of standard RMII mode (not RMII master mode) requires the use of a 50-MHz oscillator.

Table 59. 25-MHz Crystal Oscillator Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Frequency	25/50 MHz
Frequency stability	±50 ppm
Rise/fall time	Max 6 ns
Jitter (short term)	Max 800 ps
Jitter (long term)	Max 800 ps
Load capacitance	Minimum 15 pF
Symmetry	40% to 60%
Logic 0	Max 10% VDD, VDD = 3.3 V
Logic 1	Min. 90% VDD, VDD = 3.3 V

9.2.1.2 Magnetics

The magnetics have a large impact on the PHY performance as well. While several components are listed, others may be compatible following the requirements listed in Table 60. TI recommends that the magnetics include both an isolation transformer and an integrated common mode choke to reduce EMI.

Table 60. Magnetics Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Turn ratio	1:1, ±2%
Insertion loss	–1 dB, 1 to 100 MHz
Return loss	–16 dB, 1 to 30 MHz
	–12 dB, 30 to 60 MHz
	–10 dB, 60 to 80 MHz
Differential to common rejection ration	–30 dB, 1 to 50 MHz
	–20 dB, 50 to 150 MHz
Crosstalk	–35 dB, 30 MHz
	–30 dB, 60 MHz
Isolation	1500 Vrms

9.2.2 Detailed Design Procedure

9.2.2.1 TPI Network Circuit

Figure 41 shows the recommended circuit for a 10/100 Mb/s twisted pair interface. The transmitter and the receiver of each node are DC isolated from the network cable by 1:1 transformers. A typical network configuration provides the services of autonegotiation, Auto-MDIX, 10-Mb/s operation, and 100-Mb/s operation. Autonegotiation is a feature which automatically determines the optimal network operating speed. Auto-MDIX is a feature allowing either straight-through or cross-over cables to be used. Autonegotiation uses link pulses to determine the operating mode. Link pulses appear as differential 2.5-V signals when ideal 50-Ω balanced loading is provided. 100 Mb/s data appears as 1 V, 0 V, and –1-V differential signals, and 10-Mb/s data appears as 2.5-V and –2.5-V differential signals across ideal loading. See Figure 44, Figure 45, and Figure 46.

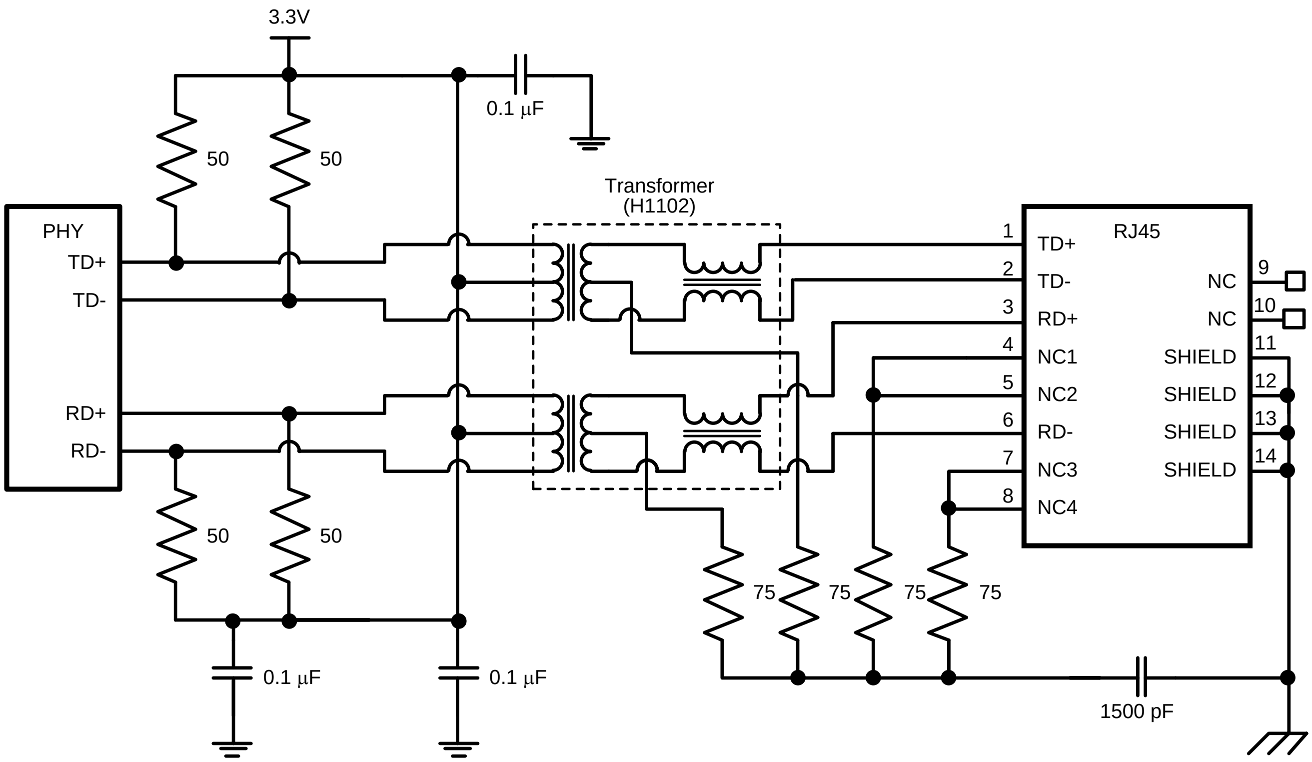


Figure 41. Typical 10/100 Mb/s Twisted Pair Interface

9.2.2.2 Clock In (X1) Requirements

The DP83848 supports an external CMOS level oscillator source or a crystal resonator device.

9.2.2.2.1 Oscillator

If an external clock source is used, X1 should be tied to the clock source and X2 should be left floating.

Specifications for CMOS oscillators: 25 MHz in MII Mode and 50 MHz in RMII Mode are listed in Table 61 and Table 62.

9.2.2.2.2 Crystal

A 25-MHz, parallel, 20-pF load crystal resonator should be used if a crystal source is desired. Figure 42 shows a typical connection for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads.

The oscillator circuit is designed to drive a parallel resonance at cut crystal with a minimum drive level of 100 µW and a maximum of 500 µW. If a crystal is specified for a lower drive level, a current limiting resistor should be placed in series between X2 and the crystal.

As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, CL1 and CL2 should be set at 33 pF, and R1 should be set at 0 Ω.

Specification for 25 MHz crystal are listed in Table 63.

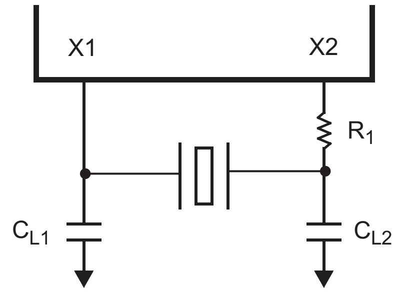


Figure 42. Crystal Oscillator Circuit

Table 61. 25-MHz Oscillator Specification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency tolerance	Operational temperature			±50	ppm
Frequency stability	1 year aging			±50	ppm
Rise/Fall time	20% to 80%			6	ns
Jitter	Short term			800 (1)	ps
Jitter	Long term			800 (1)	ps
Symmetry	Duty cycle	40%		60%	

(1) This limit is provided as a guideline for component selection and to ensure by production testing. Refer to AN-1548, *PHYTER™ 100 Base-TX Reference Clock Jitter Tolerance*, SNLA091 for details on jitter performance.

Table 62. 50 MHz Oscillator Specification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			50		MHz
Frequency tolerance	Operational temperature			±50	ppm
Frequency stability	Operational temperature			±50	ppm
Rise/Fall time	20% - 80%			6	ns
Jitter	Short term			800 (1)	ps
Jitter	Long term			800 (1)	ps
Symmetry	Duty cycle	40%		60%	

(1) This limit is provided as a guideline for component selection and to guaranteed by production testing. Refer to AN-1548, “PHYTER 100 Base-TX Reference Clock Jitter Tolerance,“ for details on jitter performance.

Table 63. 25 MHz Crystal Specification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency tolerance	Operational temperature			±50	ppm
Frequency stability	1 year aging			±50	ppm
Load capacitance		25		40	pF

9.2.2.3 Power Feedback Circuit

To ensure correct operation for the DP83848, parallel caps with values of 10 μF (Tantalum) and 0.1 μF should be placed close to pin 23 (PFBOUT) of the device.

Pin 18 (PFBIN1) and pin 37 (PFBIN2) must be connected to pin 23 (PFBOUT), each pin requires a small capacitor (.1 μF). See Figure 43 for proper connections.

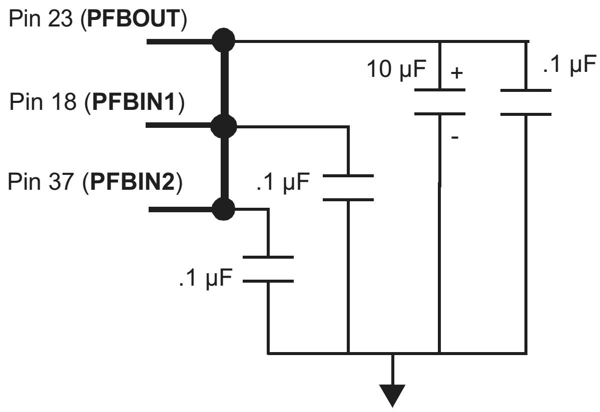


Figure 43. Power Feedback Connection

9.2.2.4 Power Down and Interrupt

The power down and interrupt functions are multiplexed on pin 7 of the device. By default, this pin functions as a power down input and the interrupt function is disabled. Setting bit 0 (INT_OE) of MICR (0x11h) will configure the pin as an active low interrupt output.

9.2.2.4.1 Power-Down Control Mode

The PWR_DOWN/INT pin can be asserted low to put the device in a power down mode. This is equivalent to setting bit 11 (power down) in the basic mode control register, BMCR (0x00h). An external control signal can be used to drive the pin low, overcoming the weak internal pull-up resistor. Alternatively, the device can be configured to initialize into a power down state by use of an external pulldown resistor on the PWR_DOWN/INT pin. Since the device will still respond to management register accesses, setting the INT_OE bit in the MICR register will disable the PWR_DOWN/INT input, allowing the device to exit the power down state.

9.2.2.4.2 Interrupt Mechanisms

The interrupt function is controlled via register access. All interrupt sources are disabled by default. Setting bit 1 (INTEN) of MICR (0x11h) will enable interrupts to be output, dependent on the interrupt mask set in the lower byte of the MISR (0x12h). The PWR_DOWN/INT pin is asynchronously asserted low when an interrupt condition occurs. The source of the interrupt can be determined by reading the upper byte of the MISR. One or more bits in the MISR will be set, denoting all currently pending interrupts. Reading of the MISR clears ALL pending interrupts.

Example: To generate an interrupt on a change of link status or on a change of energy detect power state, the steps would be:

- Write 0003h to MICR to set INTEN and INT_OE
- Write 0060h to MISR to set ED_INT_EN and LINK_INT_EN
- Monitor PWR_DOWN/INT pin

When PWR_DOWN/INT pin asserts low, user would read the MISR register to see if the ED_INT or LINK_INT bits are set, i.e. which source caused the interrupt. After reading the MISR, the interrupt bits should clear and the PWR_DOWN/INT pin will deassert.

9.2.2.5 Energy Detect Mode

When energy detect is enabled and there is no activity on the cable, the DP83848 will remain in a low power mode while monitoring the transmission line. Activity on the line will cause the DP83848 to go through a normal power up sequence. Regardless of cable activity, the DP83848 will occasionally wake up the transmitter to put ED pulses on the line, but will otherwise draw as little power as possible. Energy detect functionality is controlled via register energy detect control (EDCR), address 0x1Dh.

9.2.3 Application Curves

Transformers provide the functions of DC isolation from the cable, and DC biasing at the physical layer device. Isolation is necessary to meet IEEE 802.3 AC and DC isolation specifications for cabled configurations. IEEE 802.3 isolation requirements are described in section 14.3.1.1 of the specification, and include the ability to sustain cable faults to 1500-V 50- or 60-Hz or 2250-Vdc voltage levels for 60 s. PHYTER product transmitters and receivers are DC biased internally, from the transformer centertap, and through 50-Ω load resistors used in typical applications.

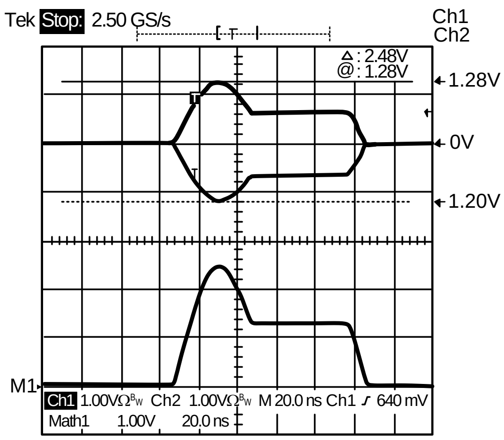


Figure 44. Sample Link Pulse Waveform

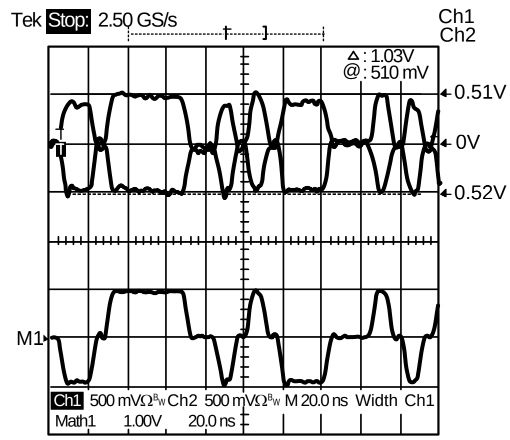


Figure 45. Sample 100-Mb/s Waveform (MLT-3)

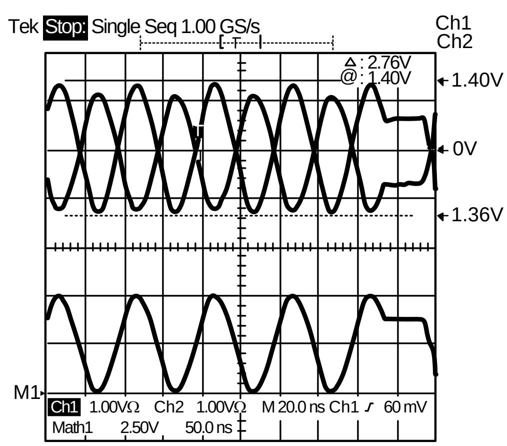


Figure 46. Sample 10-Mb/s Waveform

10 Power Supply Recommendations

The device Vdd supply pins should be bypassed with low impedance 0.1-μF surface mount capacitors. To reduce EMI, the capacitors should be places as close as possible to the component Vdd supply pins, preferably between the supply pins and the vias connecting to the power plane. In some systems it may be desirable to add 0-Ω resistors in series with supply pins, as the resistor pads provide flexibility if adding EMI beads becomes necessary to meet system level certification testing requirements. (See Figure 47.)

TI recommends the PCB have at least one solid ground plane and one solid Vdd plane to provide a low impedance power source to the component. This also provides a low impedance return path for nondifferential digital MII and clock signals. A 10-μF capacitor should also be placed near the PHY component for local bulk bypassing between the Vdd and ground planes.

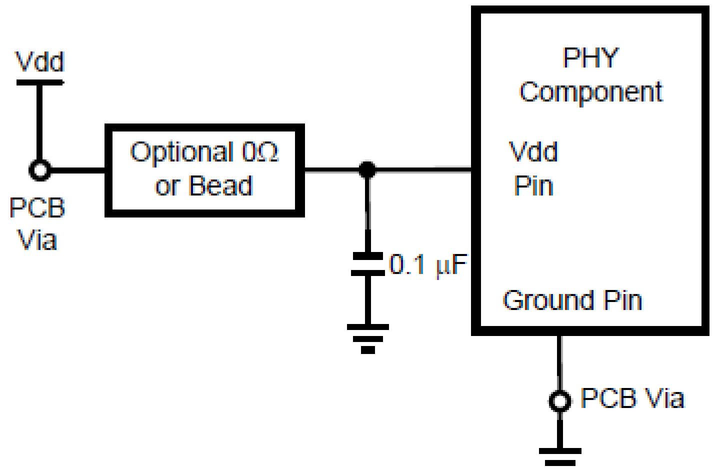


Figure 47. Vdd Bypass Layout

11 Layout

11.1 Layout Guidelines

- Place the 49.9-Ω,1% resistors, and 0.1-μF decoupling capacitor, near the PHYTER TD± and RD± pins and via directly to the Vdd plane.
- Stubs should be avoided on all signal traces, especially the differential signal pairs. See Figure 48.
- Within the pairs (for example, TD+ and TD–) the trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and increased EMI. See Figure 48.
- All high speed data signal should have 50-Ω controlled impedance, or 100-Ω differential controlled impedance for differential signal pairs. Ideally there should be no crossover or via on the signal paths. Vias present impedance discontinuities and should be minimized. Route an entire trace or trace pair on a single layer if possible.

Layout Guidelines (continued)

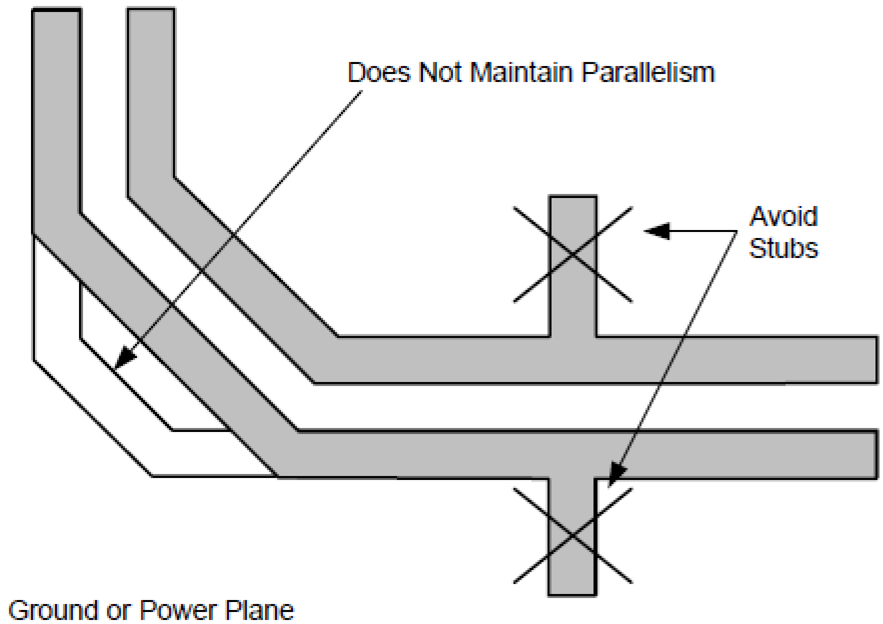


Figure 48. Differential Signal Pail - Stubs

- Signal traces should not be run such that they cross a plane split. See Figure 9-2. A signal crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems.

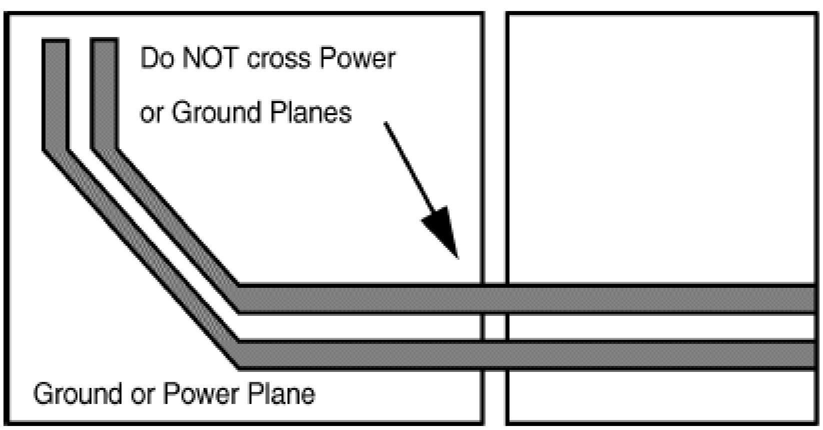


Figure 49. Differential Signal Pair-Plane Crossing

- Medium Dependent Interface (MDI) signal traces should have 50-Ω to ground or 100-Ω differential controlled impedance.
- To reduce digital signal energy, 50-Ω series termination resistors are recommended for all MII output signals (including RXCLK, TXCLK, and RX Data signals.)
- PCB trace lengths should be kept as short as possible. Ideally, keep the traces under 6 inches.
- Trace length matching, to within 2 inches on the MII or RMII bus is also recommended. Significant differences in the trace lengths can cause data timing issues.

Layout Guidelines (continued)

11.1.1 PCB Layer Stacking

To meet signal integrity and performance requirements, at minimum a four layer PCB is recommended for implementing PHYTER components in end user systems. The following layer stack-ups are recommended for four, six, and eight-layer boards, although other options are possible.

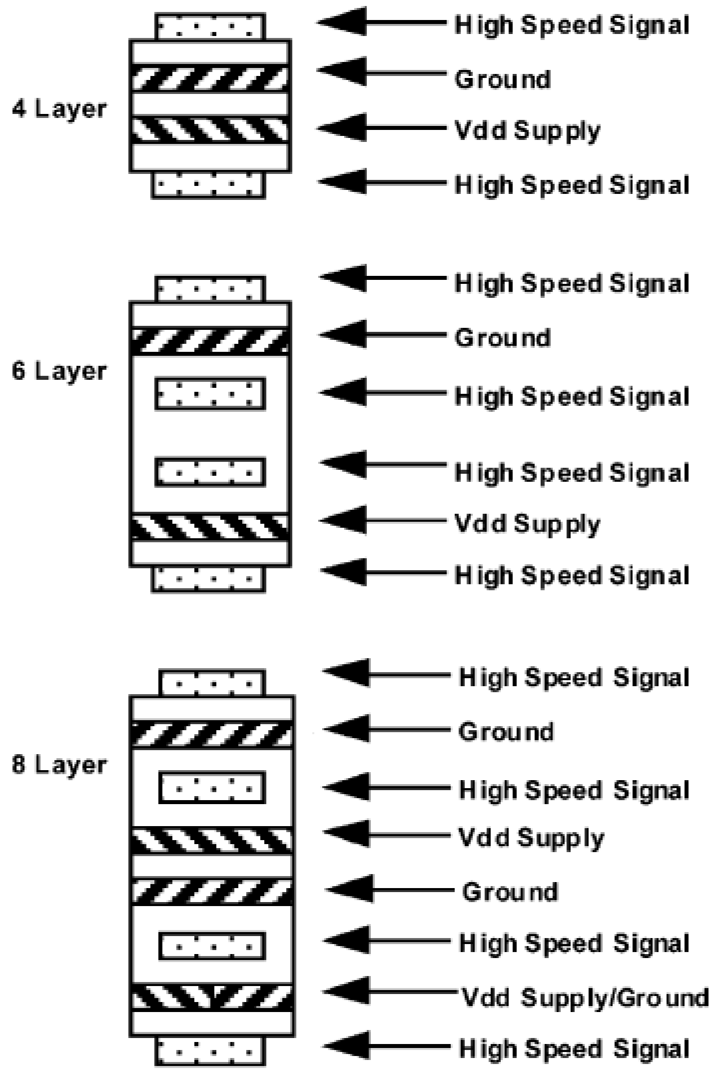


Figure 50. PCB Stripline Layer Stacking

Within a PCB it may be desirable to run traces using different methods, microstrip vs. stripline, depending on the location of the signal on the PCB. For example, it may be desirable to change layer stacking where an isolated chassis ground plane is used. Figure 51 illustrates alternative PCB stacking options.

Layout Guidelines (continued)

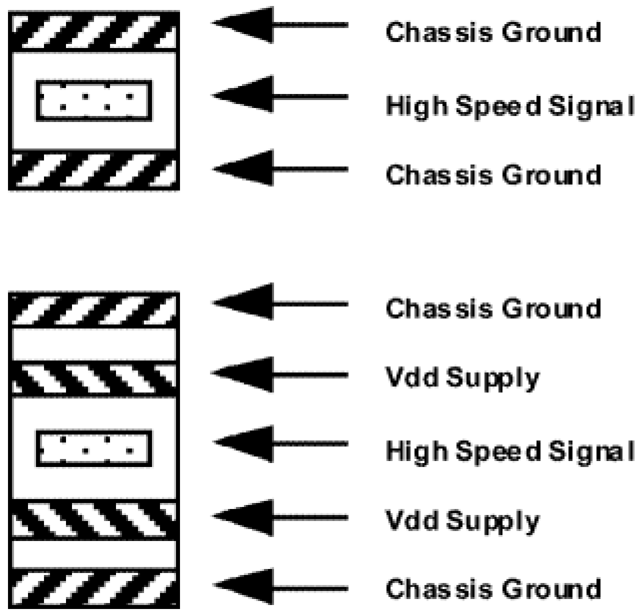


Figure 51. Alternative PCB Stripline Layer Stacking

11.2 Layout Example

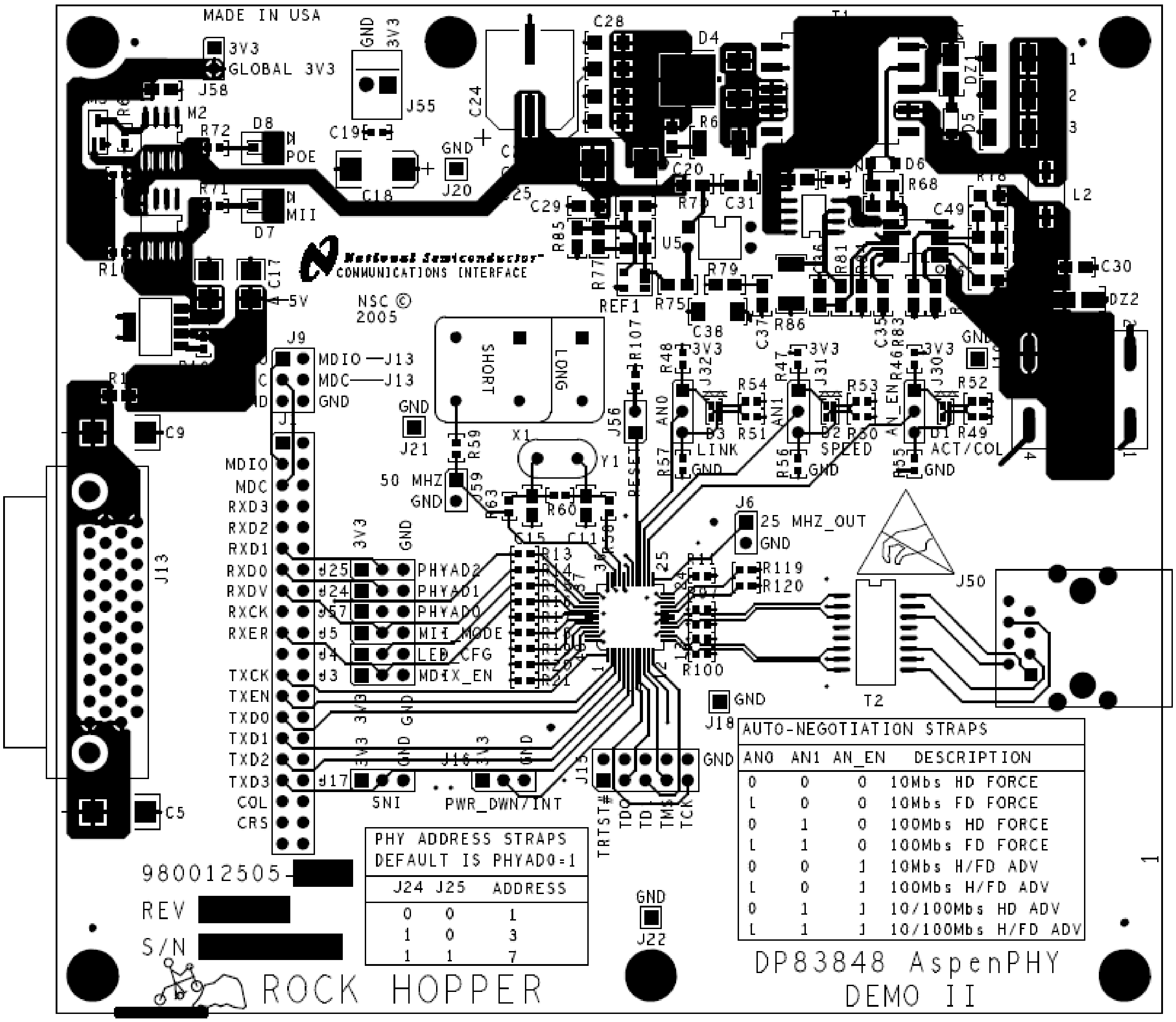
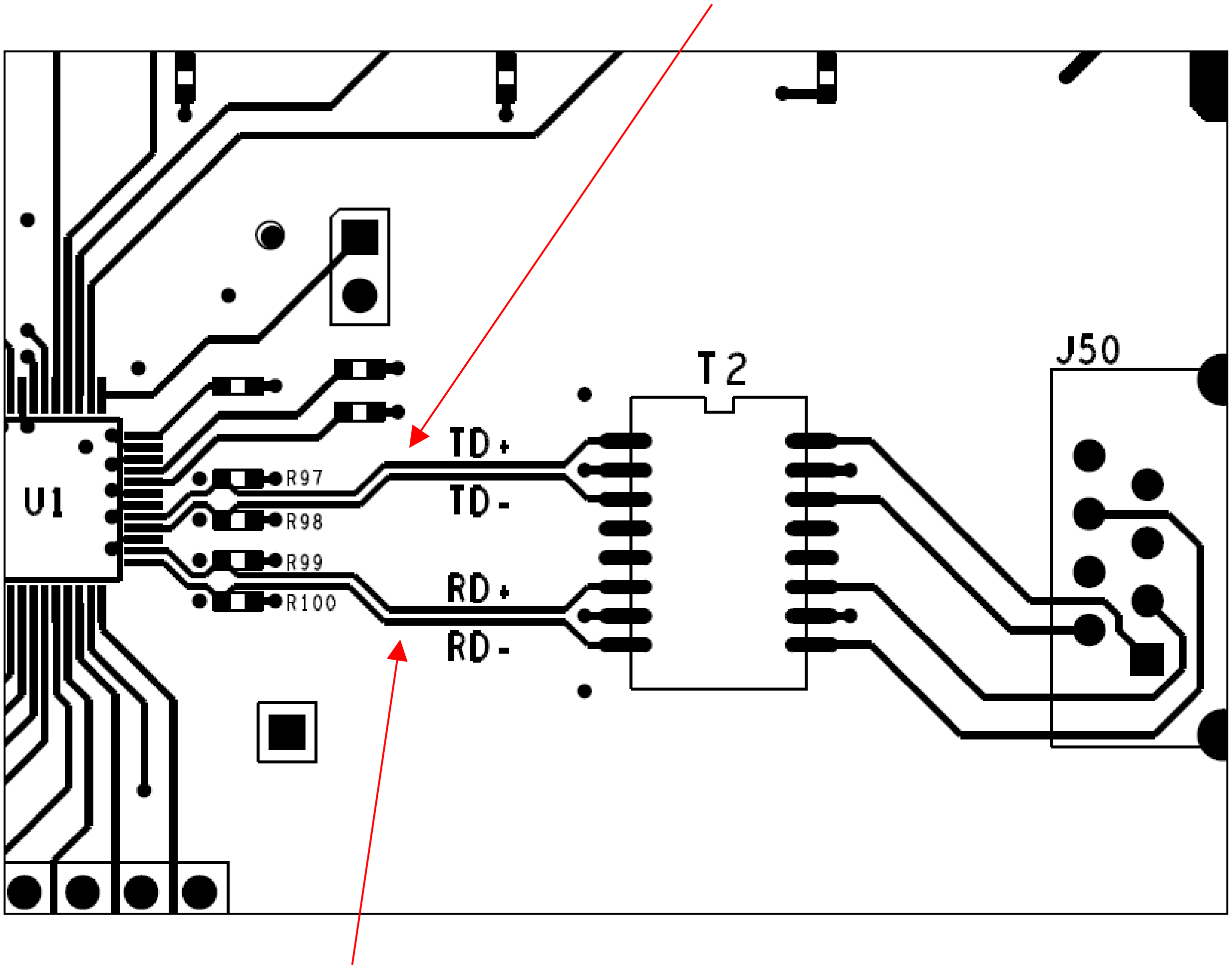


Figure 52. Top Layer

Layout Example (continued)

100 Ω or 50 Ω to ground matched length differential pairs



100 Ω or 50 Ω to ground matched length differential pairs

Figure 53. Differential Pairs

Layout Example (continued)

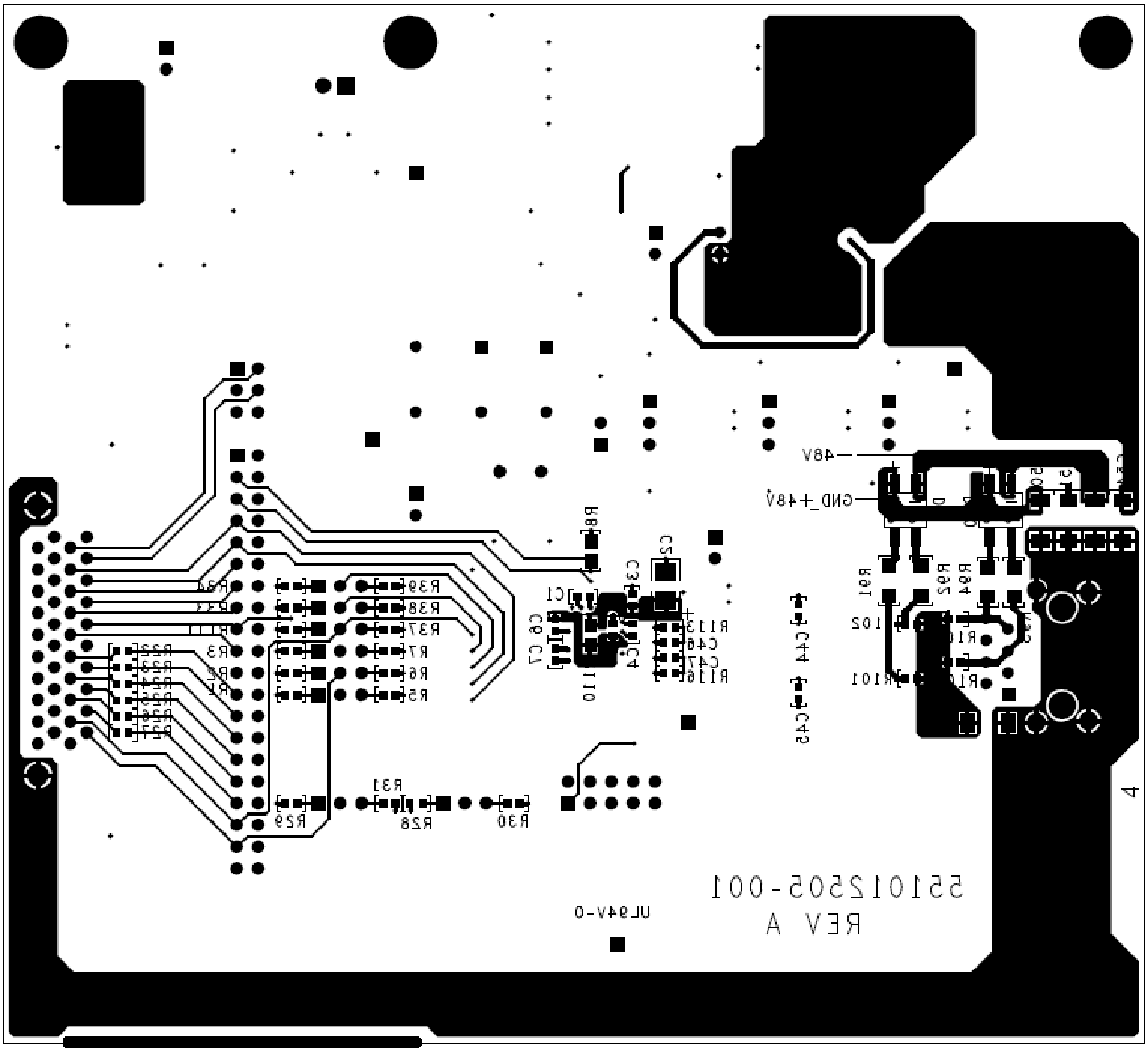


Figure 54. Bottom Layer

11.3 ESD Protection

Typically, ESD precautions are predominantly in effect when handling the devices or board before being installed in a system. In those cases, strict handling procedures need be implemented during the manufacturing process to greatly reduce the occurrences of catastrophic ESD events. After the system is assembled, internal components are less sensitive from ESD events.

See *ESD Ratings* for ESD rating.

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

本文档应结合以下文档一块使用，这样有助于您设计 PHYTER 产品：

- *《DP83848C/I/YB 原理图》*（文献编号：SNLR019）
- *《DP83848C/I/YB 物料清单》*（文献编号：SNLR020）
- *《DP83848C/I/YB 用户指南》*（文献编号：SNLU094）
- *《DP83848C/I/YB 布局》*（文献编号：SNLC032）

12.2 商标

PHYTER is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DP83848SKGD1	Active	Production	XCEPT (KGD) | 0	100 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 150	
DP83848SKGD1.A	Active	Production	XCEPT (KGD) | 0	100 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DP83848-HT :

- Enhanced Product : DP83848-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265