DLPA3005 PMIC 和高电流 LED 驱动器 IC

1 特性

- 高效、高电流 RGB LED 驱动器
- 外部降压 FET 驱动器，驱动电流高达 16A
- 外部 RGB 开关驱动器
- 每通道 10 位可编程电流
- 用于选择色彩时序 RGB LED 的输入
- 可生成 DMD 高电压电源
- 配有两个高效降压转换器，用于生成 DLPC343x 和 DMD 电源
- 配有一个高效 8 位可编程降压转换器，用于风扇驱动器应用或通用电源。当前支持通用 Buck2 (PWR6)。
- 两个 LDO，用于提供辅助电压
- 模拟 MUX，用于测量内部和外部节点，例如热敏电阻和基准电平
- 监测/保护：热关断、热模和欠压锁定 (UVLO)

2 应用

DLP® Pico™ 便携式投影仪

3 说明

DLPA3005 是一款高度集成的电源管理 IC，针对 DLP® Pico™ 投影仪系统进行了优化。DLPA3005 采用集成式高效降压控制器，支持多个 LED 投影仪，每个 LED 的电流可高达 16A，串联 LED 的电流可高达 32A。此外，其顶部配有一个 RGB 开关，支持红色、绿色和蓝色 LED 排序。DLPA3005 包含五个降压转换器，其中两个专用于 DLPC 低压电源。另有一个专用于稳压电源，为 DMD 生成三个时序关键型直流电源：VBIAS、VRST 和 VOFS。

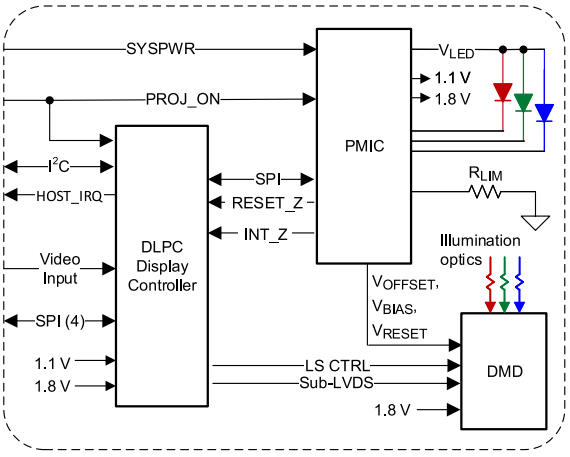
DLPA3005 包含多个辅助块，可灵活使用。因此可以量身定制 Pico 投影仪系统。可以使用一个 8 位可编程降压转换器，例如用于驱动 RGB 投影仪风扇或用于提供辅助电源线。当前支持通用 Buck2 (PWR6)。两个 LDO 可用于提供至多 200mA 的低电流。这两个 LDO 预定义为 2.5V 和 3.3V。

DLPA3005 的所有块均可通过 SPI 寻址。此外，该器件还包含以下特性：生成系统复位，电源排序，用于顺序选择活动 LED 的输入信号，IC 自我保护以及用于将模拟信息传送到外部 ADC 的模拟 MUX。

器件信息

器件型号	封装	封装尺寸（标称值）
DLPA3005(1)	HTQFP (100)	14.00mm × 14.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型简化系统图

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2015) to Revision A (February 2023)	Page
• 删除了特性中不支持的通用降压转换器和电池模式	1
• 更新了对串联 LED 的新支持，删除了不支持的降压转换器，并更新了说明 中的系统方框图	1
• Updated Pin Configuration and Functions	4
• Removed INT_Z from Input Voltage range Table and updated the max value of CH1,2,3_SWITCH, ILLUM_A,B_FB in Recommended Operating Conditions	9
• Updated with new support for series LEDs, removed unsupported General Purpose Buck Converters in Electrical Characteristics	11
• Removed unsupported General Purpose Buck Converters and battery mode in Overview	18
• Updated the System Block Diagram in Functional Block Description	18
• Removed unsupported General Purpose Buck Converters in Supply	19
• Updated register names in Monitoring	21
• Removed battery mode in Auto LED Turn Off Functionality	21
• Updated with new support for series LEDs in RGB Strobe Decoder	26
• Updated Break Before Make (BBM)	27
• Updated register name in Openloop Voltage	27
• Updated register name in Illumination Monitoring	28
• Updated register names in Power Good	28
• Updated register name in DMD Supplies	31
• Removed unsupported General Purpose Buck Converters in DMD/DLPC Buck Converters	32
• Updated register name in DMD Monitoring	34
• Removed unsupported General Purpose Buck Converters 1 and 3 in Buck Converters	35
• Removed unsupported General Purpose Buck Converters in LDO Bucks	35
• Removed unsupported General Purpose Buck Converters 1 and 3 and updated register names in General Purpose Buck Converter	35
• Removed unsupported General Purpose Buck Converters 1 and 3 in Buck Converter Monitoring	36

- Removed unsupported General Purpose Buck Converters 1 and 3 in Power Good 36
- Removed light sensor use-case and updated register names in Measurement System 37
- Removed unsupported General Purpose Buck Converters and battery mode in Interrupt 42
- Updated Register Maps 44
- Updated Application Information for a series LED use case..... 46
- Updated the System Block Diagram in Typical Application 46
- Removed unsupported General Purpose Buck Converters and battery mode in Design Requirements 46
- Updated System Example With DLPA3005 Internal Block Diagram 49
- Removed battery mode in Power Supply Recommendations 50
- Updated the High AC Current Paths in a Buck Converter Diagram and removed battery mode in Layout Guidelines 54
- Removed unsupported General Purpose Buck Convert in SPI Connections 55
- Updated R_{LIM} Routing 55
- Updated LED Connection 55
- Updated Layout Example 57
- Updated Thermal Considerations 57

5 Pin Configuration and Functions

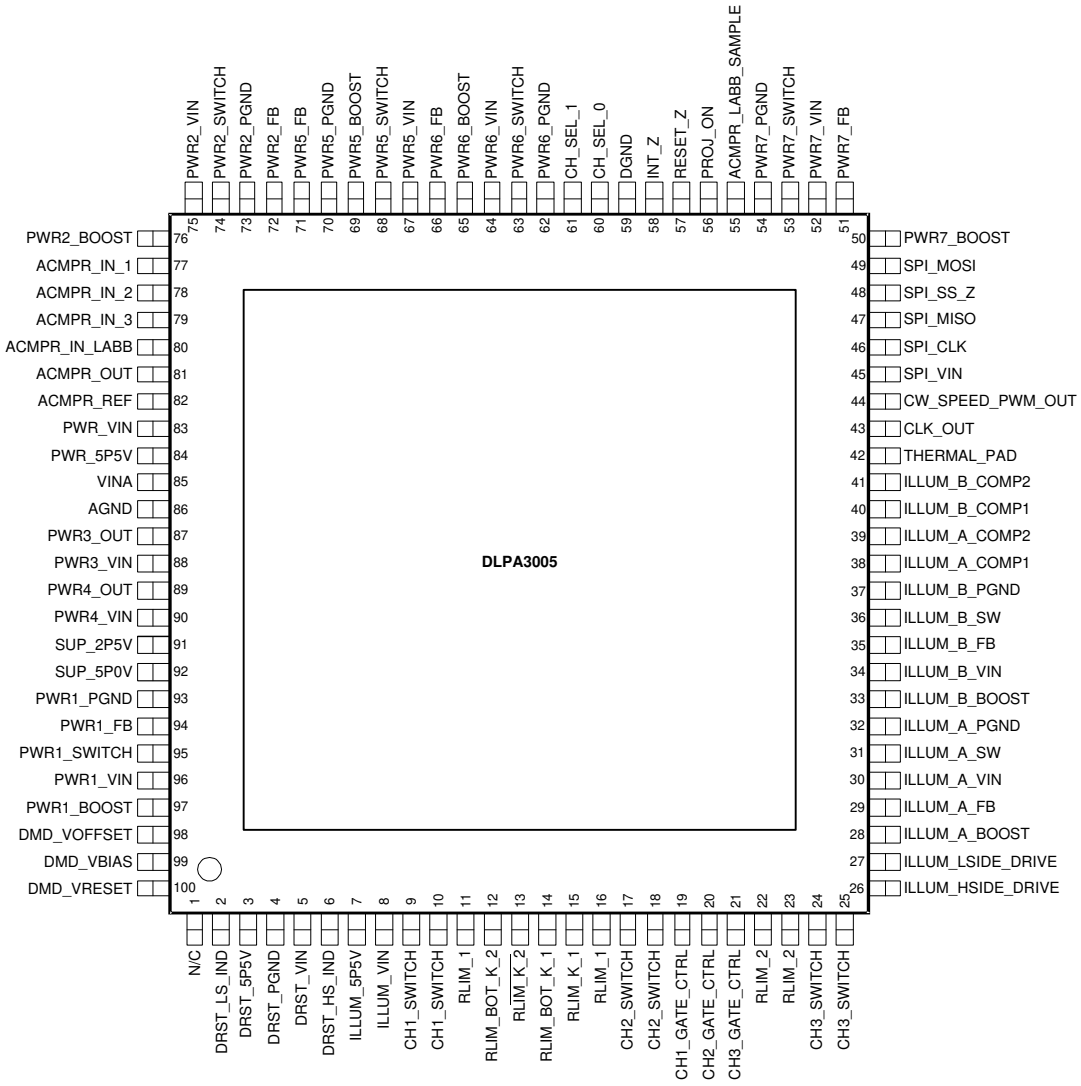


图 5-1. PFD Package 100-Pin HTQFP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
N/C	1	—	No connect
DRST_LS_IND	2	I/O	Connection for the DMD SMPS-inductor (low-side switch)
DRST_5P5V	3	O	Filter pin for LDO DMD. Power supply for internal DMD reset regulator, typical 5.5 V
DRST_PGND	4	GND	Power ground for DMD SMPS. Connect to ground plane.
DRST_VIN	5	POWER	Power supply input for LDO DMD. Connect to system power.
DRST_HS_IND	6	I/O	Connection for the DMD SMPS-inductor (high-side switch)
ILLUM_5P5 V	7	O	Filter pin for LDO ILLUM. Power supply for internal ILLUM block, typical 5.5 V
ILLUM_VIN	8	POWER	Supply input of LDO ILLUM. Connect to system power.
CH1_SWITCH	9	I	Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly.
CH1_SWITCH	10	I	Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly.
RLIM_1	11	O	Connection to LED current sense resistor for CH1 and CH2

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RLIM_BOT_K_2	12	I	Kelvin sense connection to ground side of LED current sense resistor
RLIM_K_2	13	I	Kelvin sense connection to top side of current sense resistor
RLIM_BOT_K_1	14	I	Kelvin sense connection to ground side of LED current sense resistor
RLIM_K_1	15	I	Kelvin sense connection to top side of current sense resistor
RLIM_1	16	O	Connection to LED current sense resistor for CH1 and CH2
CH2_SWITCH	17	I	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
CH2_SWITCH	18	I	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
CH1_GATE_CTRL	19	O	Gate control of CH1 external MOSFET switch for LED cathode
CH2_GATE_CTRL	20	O	Gate control of CH2 external MOSFET switch for LED cathode
CH3_GATE_CTRL	21	O	Gate control of CH3 external MOSFET switch for LED cathode
RLIM_2	22	O	Connection to LED current sense resistor for CH3
RLIM_2	23	O	Connection to LED current sense resistor for CH3
CH3_SWITCH	24	I	Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly.
CH3_SWITCH	25	I	Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly.
ILLUM_HSIDE_DRIVE	26	O	Gate control for external high-side MOSFET for ILLUM Buck converter
ILLUM_LSIDE_DRIVE	27	O	Gate control for external low-side MOSFET for ILLUM Buck converter
ILLUM_A_BOOST	28	I	Supply voltage for high-side N-channel MOSFET gate driver. A 100-nF capacitor (typical) must be connected between this pin and ILLUM_A_SW.
ILLUM_A_FB	29	I	Input to the buck converter loop controlling I_{LED}
ILLUM_A_VIN	30	POWER	Power input to the ILLUM Driver A
ILLUM_A_SW	31	I/O	Switch node connection between high-side NFET and low-side NFET. Serves as common connection for the flying high side FET driver
ILLUM_A_PGND	32	GND	Ground connection to the ILLUM Driver A
ILLUM_B_BOOST	33	I	Supply voltage for high-side N-channel MOSFET gate driver
ILLUM_B_VIN	34	POWER	Power input to the ILLUM driver B
ILLUM_B_FB	35	I	Input to the buck converter loop controlling I_{LED}
ILLUM_B_SW	36	I/O	Switch node connection between high-side NFET and low-side NFET
ILLUM_B_PGND	37	GND	Ground connection to the ILLUM driver B
ILLUM_A_COMP1	38	I/O	Connection node for feedback loop components
ILLUM_A_COMP2	39	I/O	Connection node for feedback loop components
ILLUM_B_COMP1	40	I/O	Connection node for feedback loop components
ILLUM_B_COMP2	41	I/O	Connection node for feedback loop components
THERMAL_PAD	42	GND	Thermal pad. Connect to a clean system ground.
CLK_OUT	43	O	No connect. Reserved for color wheel clock output
CW_SPEED_PWM_OUT	44	O	No connect. Reserved for color wheel PWM output
SPI_VIN	45	I	Supply for SPI interface
SPI_CLK	46	I	SPI clock input
SPI_MISO	47	O	SPI data output
SPI_SS_Z	48	I	SPI chip select (active low)
SPI_MOSI	49	I	SPI data input
PWR7_BOOST	50	I	Reserved for general purpose buck converter. Charge-pump-supply input for the high-side FET gate drive circuit. Connect 100-nF capacitor between PWR7_BOOST and PWR7_SWITCH pins.
PWR7_FB	51	I	Reserved for general purpose buck converter. Converter feedback input. Connect to converter output voltage.
PWR7_VIN	52	POWER	Reserved for general purpose buck converter. Power supply input for converter

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PWR7_SWITCH	53	I/O	Reserved for general purpose buck converter. Switch node connection between high-side NFET and low-side NFET
PWR7_PGND	54	GND	Reserved for general purpose buck converter. Ground pin. Power ground return for switching circuit
ACMPR_LABB_SAMPLE	55	I	Control signal to sample voltage at ACMPR_IN_LABB
PROJ_ON	56	I	Input signal to enable and or disable the IC and DLP projector
RESET_Z	57	O	Reset output to the DLP system (active low). The pin is held low to reset DLP system.
INT_Z	58	O	Interrupt output signal (open drain, active low). Connect to the pullup resistor.
DGND	59	GND	Digital ground. Connect to ground plane.
CH_SEL_0	60	I	Control signal to enable either of CH1,2,3
CH_SEL_1	61	I	Control signal to enable either of CH1,2,3
PWR6_PGND	62	GND	Ground pin. Power ground return for switching circuit
PWR6_SWITCH	63	I/O	Switch node connection between high-side NFET and low-side NFET
PWR6_VIN	64	POWER	Power supply input for converter
PWR6_BOOST	65	I	Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100-nF capacitor between PWR6_BOOST and PWR6_SWITCH pins.
PWR6_FB	66	I	Converter feedback input. Connect to output voltage.
PWR5_VIN	67	POWER	Reserved for general purpose buck converter. Power supply input for converter
PWR5_SWITCH	68	I/O	Reserved for general purpose buck converter. Switch node connection between high-side NFET and low-side NFET
PWR5_BOOST	69	I	Reserved for general purpose buck converter. Charge-pump-supply input for the high-side FET gate drive circuit. Connect the 100-nF capacitor between PWR5_BOOST and PWR5_SWITCH pins.
PWR5_PGND	70	GND	Reserved for general purpose buck converter. Ground pin. Power ground return for switching circuit
PWR5_FB	71	I	Reserved for general purpose buck converter. Converter feedback input. Connect to output voltage.
PWR2_FB	72	I	Converter feedback input. Connect to output voltage.
PWR2_PGND	73	GND	Ground pin. Power ground return for switching circuit
PWR2_SWITCH	74	I/O	Switch node connection between high-side NFET and low-side NFET
PWR2_VIN	75	POWER	Power supply input for converter
PWR2_BOOST	76	I	Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100-nF capacitor between PWR2_BOOST and PWR2_SWITCH pins.
ACMPR_IN_1	77	I	Reserved. Input for analog sensor signal
ACMPR_IN_2	78	I	Input for analog sensor signal
ACMPR_IN_3	79	I	Input for analog sensor signal
ACMPR_IN_LABB	80	I	Input for ambient light sensor, sampled input
ACMPR_OUT	81	O	Analog comparator out
ACMPR_REF	82	I	Reference voltage input for analog comparator
PWR_VIN	83	POWER	Power supply input for LDO_bucks. Connect to system power.
PWR_5P5V	84	O	Filter pin for LDO_BUCKS. Internal analog supply for buck converters, typical 5.5 V
VINA	85	POWER	Input voltage supply pin for reference system
AGND	86	GND	Analog ground pin
PWR3_OUT	87	O	Filter pin for LDO_2 DMD/DLPC/AUX, typical 2.5 V
PWR3_VIN	88	POWER	Power supply input for LDO_2. Connect to system power.
PWR4_OUT	89	O	Filter pin for LDO_1 DMD/DLPC/AUX, typical 3.3 V
PWR4_VIN	90	POWER	Power supply input for LDO_1. Connect to system power.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SUP_2P5V	91	O	Filter pin for LDO_V2V5. Internal supply voltage, typical 2.5 V
SUP_5P0V	92	O	Filter pin for LDO_V5V. Internal supply voltage, typical 5 V
PWR1_PGND	93	GND	Ground pin. Power ground return for switching circuit
PWR1_FB	94	I	Converter feedback input. Connect to output voltage.
PWR1_SWITCH	95	I/O	Switch node connection between high-side NFET and low-side NFET
PWR1_VIN	96	POWER	Power supply input for converter
PWR1_BOOST	97	I	Charge-pump-supply input for the high-side FET gate drive circuit. Connect an100-nF capacitor between PWR1_BOOST and PWR1_SWITCH pins.
DMD_VOFFSET	98	O	VOFS output rail. Connect to ceramic capacitor.
DMD_VBIAS	99	O	VBIAS output rail. Connect to ceramic capacitor.
DMD_VRESET	100	O	VRESET output rail. Connect to ceramic capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	ILLUM_A,B_BOOST	–0.3	28	V
	ILLUM_A,B_BOOST (10 ns transient)	–0.3	30	
	ILLUM_A,B_BOOST vs ILLUM_A,B_SWITCH	–0.3	7	
	ILLUM_LSIDE_DRIVE	–0.3	7	
	ILLUM_HSIDE_DRIVE	–2	28	
	ILLUM_A_BOOST vs ILLUM_HSIDE_DRIVE	–0.3	7	
	ILLUM_A,B_SW	–2	22	
	ILLUM_A,B_SW (10-ns transient)	–3	27	
	PWR_VIN, PWR1,2,3,4,5,6,7_VIN, VINA, ILLUM_VIN, ILLUM_A,B_VIN, DRST_VIN	–0.3	22	
	PWR1,2,5,6,7_BOOST	–0.3	28	
	PWR1,2,5,6,7_BOOST (10 ns transient)	–0.3	30	
	PWR1,2,5,6,7_SWITCH	–2	22	
	PWR1,2,5,6,7_SWITCH (10 ns transient)	–3	27	
	PWR1,2,5,6,7_FB	–0.3	6.5	
	PWR1,2,5,6,7_BOOST vs PWR1,2,5,6,7_SWITCH	–0.3	6.5	
	CH1,2,3_SWITCH, DRST_LS_IND, ILLUM_A,B_FB	–0.3	20	
	ILLUM_A,B_COMP1,2, INT_Z, PROJ_ON	–0.3	7	
	DRST_HS_IND	–18	7	
	ACMPR_IN_1,2,3, ACMPR_REF, ACMPR_IN_LABB, ACMPR_LABB_SAMPLE, ACMPR_OUT	–0.3	3.6	
	SPI_VIN, SPI_CLK, SPI_MOSI, SPI_SS_Z, SPI_MISO, CH_SEL_0,1, RESET_Z	–0.3	3.6	
	RLIM_K_1,2, RLIM_1,2	–0.3	3.6	
	DGND, AGND, DRST_PGND, ILLUM_A,B_PGND, PWR1,2,5,6,7_PGND, RLIM_BOT_K_1,2	–0.3	0.3	
	DRST_5P5V, ILLUM_5P5V, PWR_5P5, PWR3,4_OUT, SUP_5P0V	–0.3	7	
	CH1,2,3_GATE_CTRL	–0.3	7	
	CLK_OUT	–0.3	3.6	
	CW_SPEED_PWM	–0.3	7	
	SUP_2P5V	–0.3	3.6	
	DMD_VOFFSET	–0.3	12	
	DMD_VBIAS	–0.3	20	
	DMD_VRESET	–18	7	
Source current	RESET_Z, ACMPR_OUT		1	mA
	SPI_DOUT		5.5	
Sink current	RESET_Z, ACMPR_OUT		1	mA
	SPI_DOUT, INT_Z		5.5	
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	PWR_VIN, PWR1,2,3,4,5,6,7_VIN, VINA, ILLUM_VIN, ILLUM_A,B_VIN, DRST_VIN	6	20	V
	CH1,2,3_SWITCH, ILLUM_A,B_FB	–0.1	20	
	PROJ_ON	–0.1	6	
	PWR1,2,5,6,7_FB	–0.1	5	
	ACMPR_REF, CH_SEL_0,1, SPI_CLK, SPI_MOSI, SPI_SS_Z	–0.1	3.6	
	RLIM_BOT_K_1,2	–0.1	0.1	
	ACMPR_IN_1,2,3, LABB_IN_LABB	–0.1	1.5	
	SPI_VIN	1.7	3.6	
	RLIM_K_1,2	–0.1	0.25	
	ILLUM_A,B_COMP1,2	–0.1	5.7	
Ambient temperature range		0	70	°C
Operating junction temperature		0	120	°C

6.4 Thermal Information

THERMAL METRIC(1)		DLPA3005 PFD (HTQFP) 100 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	7.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter(4)	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter(5)	3.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, but since the device is intended to be cooled with a heatsink from the top case of the package, the simulation includes a fan and heatsink attached to the DLPA3005. The heatsink is a 22 mm × 22 mm × 12 mm aluminum pin fin heatsink with a 12 × 12 × 3 mm stud. Base thickness is 2 mm and pin diameter is 1.5 mm with an array of 6 × 6 pins. The heatsink is attached to the DLPA3005 with 100 um thick thermal grease with 3 W/m-K thermal conductivity. The fan is 20 × 20 × 8 mm with 1.6 cfm open volume flow rate and 0.22 in. water pressure at stagnation.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in note 2.

(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in note 2.

6.5 Electrical Characteristics

Over operating free-air temperature range. V_{IN} = 12 V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to 节 8.2 (V_{IN} =12 V, I_{OUT} = 16 A, LED, external FETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLIES						
INPUT VOLTAGE						
V_{IN}	Input voltage range	VINA – pin	6[6]	12	20	V
V_{UVLO} [7]	UVLO threshold	VINA falling (through a 5-bit trim function, 0.5-V steps)	3.9	6.22	18.4	V
	Hysteresis	VINA rising		90		mV
$V_{STARTUP}$	Startup voltage	DMD_VBIAS, DMD_VOFFSET, DMD_VRESET loaded with 10 mA	6			V
INPUT CURRENT						
I_{IDLE}	Idle current	IDLE mode, all VIN pins combined		15		μA
I_{STD}	Standby current	STANDBY mode, analog, internal supplies and LDOs enabled, DMD, ILLUMINATION and BUCK CONVERTERS disabled.		3.7		mA
I_{Q_DMD}	Quiescent current (DMD)	Quiescent current DMD block (in addition to I_{STD}), VINA + DRST_VIN		0.49		mA
I_{Q_ILLUM}	Quiescent current (ILLUM)	Quiescent current ILLUM block (in addition to I_{STD}), V_openloop= 3 V (ILLUM_OLV_SEL), VINA + ILLUM_VIN + ILLUM_A_VIN + ILLUM_B_VIN		21		mA
I_{Q_BUCK}	Quiescent current (per BUCK)	Quiescent current per BUCK converter (in addition to I_{STD}), Normal mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN, PWR1,2,5,6,7_VOUT = 1 V		4.3		mA
		Quiescent current per BUCK converter (in addition to I_{STD}), Normal mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN, PWR1,2,5,6,7_VOUT = 5 V		15		
		Quiescent current per BUCK converter (in addition to I_{STD}), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN = 1 V		0.41		
		Quiescent current per BUCK converter (in addition to I_{STD}), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN = 5 V		0.46		
I_{Q_TOTAL}	Quiescent current (Total)	Typical Application: ACTIVE mode, all VIN pins combined, DMD, ILLUMINATION and PWR1,2 enabled, PWR3,4,5,6,7 disabled.		38		mA
INTERNAL SUPPLIES						
V_{SUP_5P0V}	Internal supply, analog			5		V
V_{SUP_2P5V}	Internal supply, logic			2.5		V
DMD—LDO DMD						
V_{DRST_VIN}			6	12	20	V
V_{DRST_5P5V}				5.5		V
PGOOD	Power good DRST_5P5V	Rising		80%		
		Falling		60%		
OVP	Overvoltage protection DRST_5P5V			7.2		V
	Regulator dropout	At 25 mA, VDRST_VIN= 5.5 V		56		mV
	Regulator current limit[2]		300	340	400	mA
DMD—REGULATOR						

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12 V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to 节 8.2 (V_{IN} =12 V, I_{OUT} = 16 A, LED, external FETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	MOSFET ON-resistance	Switch A (from DRST_5P5V to DRST_HS_IND)		920		mΩ
		Switch B (from DRST_LS_IND to DRST_PGND)		450		
V_{FW}	Forward voltage drop	Switch C (from DRST_LS_IND to DRST_VBIAS(1)), VDRST_LS_IND = 2 V, I_F = 100 mA		1.21		V
		Switch D (from DRST_LS_IND to DRST_VOFFSET(1)), VDRST_LS_IND = 2 V, I_F = 100 mA		1.22		
t_{DIS}	Rail Discharge time	C_{OUT} = 1 µF			40	µs
t_{PG}	Power-good timeout	Not tested in production		15		ms
I_{LIMIT}	Switch current limit			610		mA
VOFFSET REGULATOR						
V_{OFFSET}	Output voltage			10		V
	DC output voltage accuracy	I_{OUT} = 10 mA	-0.3		0.3	V
	DC Load regulation	I_{OUT} = 0 mA to 10 mA		– 10		V/A
	DC Line regulation	I_{OUT} = 10 mA, DRST_VIN = 8 V to 20 V		– 5		mV/V
V_{RIPPLE}	Output ripple	I_{OUT} = 10 mA, C_{OUT}= 1 µF		200		mVpp
I_{OUT}	Output current		0.1		10	mA
PGOOD	Power-good threshold (fraction of nominal output voltage)	VOFFSET rising		86%		
		VOFFSET falling		66%		
C	Output capacitor	Recommended value(5) (use same value as output capacitor on VRESET)	1			µF
		$t_{DISCHARGE}$ <40 µs at VIN = 8 V			1	
VBIAS REGULATOR						
V_{BIAS}	Output voltage			18		V
	DC output voltage accuracy	I_{OUT} = 10 mA	– 0.3		0.3	V
	DC Load regulation	I_{OUT} = 0 to 10 mA		– 18		V/A
	DC Line regulation	I_{OUT} = 10 mA, DRST_VIN = 8 V to 20 V		– 3		mV/V
V_{RIPPLE}	Output ripple	I_{OUT} = 10 mA, C_{OUT}= 470 nF		200		mVpp
I_{OUT}	Output current		0.1		10	mA
PGOOD	Power-good threshold (fraction of nominal output voltage)	VBIAS rising		86%		
		VBIAS falling		66%		
C	Output capacitor	Recommended value(5) (use same or smaller value as output capacitors VOFFSET / VRESET)	470			nF
		$t_{DISCHARGE}$ <40 µs at VIN = 8 V			470	
VRESET REGULATOR						
V_{RST}	Output voltage			– 14		V
	DC output voltage accuracy	I_{OUT} = 10 mA	-0.3		0.3	V
	DC Load regulation	I_{OUT} = 0 to 10 mA		– 4		V/A
	DC Line regulation	I_{OUT} = 10 mA, DRST_VIN = 8 to 20 V		– 2		mV/V
V_{RIPPLE}	Output ripple	I_{OUT} = 10 mA, C_{OUT} = 1 µF		120		mVpp
I_{OUT}	Output current		0.1		10	mA

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12 V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to 节 8.2 (V_{IN} =12 V, I_{OUT} = 16 A, LED, external FETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD	Power-good threshold			90%		
C	Output capacitor	Recommended value(5) (use same value as output capacitor on VOFFSET)	1			µF
		$t_{DISCHARGE}$ <40 µs at VIN = 8 V			1	
DMD - BUCK CONVERTERS						
OUTPUT VOLTAGE						
$V_{PWR\_1\_VOUT}$	Output Voltage			1.1		V
$V_{PWR\_2\_VOUT}$	Output Voltage			1.8		V
	DC output voltage accuracy	I_{OUT}= 0 mA	–3%		3%	
MOSFET						
$R_{ON,H}$	High side switch resistance	25°C, $V_{PWR\_1,2\_Boost}$ – $V_{PWR1,2\_SWITCH}$ = 5.5 V		150		mΩ
$R_{ON,L}$	Low side switch resistance(2)	25°C		85		mΩ
LOAD CURRENT						
	Allowed Load Current(3).				3	A
I_{OCL}	Current limit(2)	L_{OUT}= 3.3 µH	3.2	3.6	4.2	A
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 5 V		120		ns
$t_{OFF(MIN)}$	Minimum off time(2)	T_A = 25°C, V_{FB} = 0 V		270		ns
START-UP						
	Soft start		1	2.5	4	ms
PGOOD						
$Ratio_{OV}$	Overvoltage protection			120%		
$Ratio_{PG}$	Relative power good level	Low to high		72%		
ILLUMINATION—LDO ILLUM						
V_{ILLUM_VIN}			6	12	20	V
V_{ILLUM_5P5V}				5.5		V
PGOOD	Power good ILLUM_5P5V	Rising		80%		
		Falling		60%		
OVP	Overvoltage protection ILLUM_5P5V			7.2		V
	Regulator dropout	At 25 mA, V_{ILLUM_VIN} = 5.5 V		53		mV
	Regulator current limit(2)		300	340	400	mA
ILLUMINATION—DRIVER A,B						
V_{ILLUM_A,B_IN}	Input supply voltage range		6	12	20	V
PWM						
f_{SW}	Oscillator frequency	3 V < V_{IN} < 20 V		600		kHz
t_{DEAD}	Output driver dead time	HDRV off to LDRV on, TRDLY = 0		28		ns
		HDRV off to LDRV on, TRDLY = 1		40		
		LDRV off to HDRV on, TRDLY = 0		35		
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	V_{ILLUM_A,B_BOOT} – V_{ILLUM_A,B_SW} = 5 V, I_{HDRV} = –100 mA		4.9		Ω

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12 V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to 节 8.2 (V_{IN} =12 V, I_{OUT} = 16 A, LED, external FETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{HDLO}	High-side driver pull-down resistance	V_{ILLUM_A,B_BOOT} – V_{ILLUM_A,B_SW} = 5 V, I_{HDRV} = 100 mA		3		Ω
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = – 100 mA		3.1		Ω
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		2.4		Ω
t_{HRISE}	High-side driver rise time(2)	C_{LOAD} = 5 nF		23		ns
t_{HFALL}	High-side driver fall time(2)	C_{LOAD} = 5 nF		19		ns
t_{LRISE}	Low-side driver rise time(2)	C_{LOAD} = 5 nF		23		ns
t_{LFALL}	Low-side driver fall time(2)	C_{LOAD} = 5 nF		17		ns
OVERCURRENT PROTECTION						
HSD OC	High-Side Drive Over Current threshold	External switches, V_{DS} threshold(2)		185		mV
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA		0.75		V
PGOOD						
RatioUV	Undervoltage protection			89%		
DRIVERS EXTERNAL RGB STROBE CONTROLLER SWITCHES						
CHx_GATE_CNTR_HIGH	Gate control high level	ILLUM_SW_ILIM_EN[2:0] = 7, register 0x02, I_{SINK}= 400 µA		4.35		V
		ILLUM_SW_ILIM_EN[2:0] = 0, register 0x02, I_{SINK}= 400 µA		5.25		
CHx_GATE_CNTR_LOW	Gate control low level	ILLUM_SW_ILIM_EN[2:0] = 7, register 0x02, I_{SINK}= 400 µA		55		mV
		ILLUM_SW_ILIM_EN[2:0] = 0, register 0x02, I_{SINK}= 400 µA		55		
LED CURRENT CONTROL						
V_{LED_ANODE}	LED Anode voltage(2)	Ratio with respect to V_{ILLUM_A,B_VIN} (Duty cycle limitation).	0.85x			
					15.5	V
I_{LED}	LED currents	V_{ILLUM_A,B_VIN} ⩾ 8 V. See register SWx_IDAC[9:0] for settings.	1		16(9)	A
	DC current offset, CH1,2,3_SWITCH	R_{LIM} = 12.5 mΩ	– 150	0	150	mA
	Transient LED current limit range (programmable)	20% higher than I_{LED}. Min-setting, R_{LIM}= 12.5 mΩ		11%		
		20% higher than I_{LED}. Max-setting, R_{LIM}= 12.5 mΩ. Percentage of max current		133%		
t_{RISE}	Current rise time	I_{LED} from 5% to 95%, I_{LED} = 600 mA, transient current limit disabled(2)			50	µs
BUCK CONVERTERS—LDO_BUCKS						
V_{PWR_VIN}	Input voltage range PWR1,2,5,6,7_VIN		6	12	20	V
V_{PWR_5P5V}	PWR_5P5V			5.5		V
PGOOD	Power good PWR_5P5V	Rising		80%		
		Falling		60%		

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12 V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to 节 8.2 (V_{IN} =12 V, I_{OUT} = 16 A, LED, external FETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVP	Overvoltage Protection PWR_5P5V			7.2		V
	Regulator dropout	At 25 mA, V_{PWR_VIN}= 5.5 V		41		mV
	Regulator current limit(2)		300	340	400	mA
BUCK CONVERTER - GENERAL PURPOSE BUCK CONVERTER (8)						
OUTPUT VOLTAGE						
$V_{PWR\_6\_VOUT}$	Output Voltage (General Purpose Buck2)	8-bit programmable	1		5	V
	DC output voltage accuracy	I_{OUT}= 0 mA	– 3.5%		3.5%	
MOSFET						
$R_{ON,H}$	High side switch resistance	25°C, V_{PWR6_Boost} – V_{PWR6_SWITCH} = 5.5 V		150		mΩ
$R_{ON,L}$	Low side switch resistance(2)	25°C		85		mΩ
LOAD CURRENT						
	Allowed Load Current PWR6(3).			2		A
I_{OCL}	Current limit(2) (3)	L_{OUT}= 3.3 μH	3.2	3.6	4.2	A
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 5 V		120		ns
$t_{OFF(MIN)}$	Minimum off time(2)	T_A = 25°C, V_{FB} = 0 V		270	310	ns
START-UP						
	Soft start		1	2.5	4	ms
PGOOD						
$Ratio_{OV}$	Overvoltage protection			120%		
$Ratio_{PG}$	Relative power good level	Low to high		72%		
AUXILIARY LDOs						
$V_{PWR3,4\_VIN}$	Input voltage range	LDO1 (PWR4), LDO2 (PWR3)	3.3	12	20	V
PGOOD	Power good PWR3,4_VOUT	PWR3,4_VOUT rising		80%		
		PWR3,4_VOUT falling		60%		
OVP	Overvoltage Protection PWR3,4_VOUT			7		V
	DC output voltage accuracy PWR3,4_VOUT	I_{OUT}= 0 mA	– 3%		3%	
	Regulator current limit(2)		300	340	400	mA
t_{ON}	Turn-on time	to 80% of V_{OUT} = PWR3 and PWR4, C= 1 μF		40		μs
LDO2 (PWR3)						
V_{PWR3_VOUT}	Output Voltage PWR3_VOUT			2.5		V
	Load Current capability			200		mA
	DC Load regulation PWR3_VOUT	V_{OUT}= 2.5 V, I_{OUT}= 5 to 200 mA		– 70		mV/A
	DC Line regulation PWR3_VOUT	V_{OUT}= 2.5 V, I_{OUT}= 5 mA, PWR3_VIN = 3.3 to 20 V		30		μV/V
LDO1 (PWR4)						
V_{PWR4_VOUT}	Output Voltage PWR4_VOUT			3.3		V

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12 V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to 节 8.2 (V_{IN} =12 V, I_{OUT} = 16 A, LED, external FETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Load Current capability			200		mA
	DC Load regulation PWR4_VOUT	V_{OUT}= 3.3 V, I_{OUT}= 5 to 200 mA		–70		mV/A
	DC Line regulation PWR4_VOUT	V_{OUT}= 3.3V, I_{OUT}= 5 mA, PWR4_VIN= 4 to 20 V		30		µV/V
	Regulator dropout	At 25 mA, V_{OUT}= 3.3 V, V_{PWR4_VIN}= 3.3 V		48		mV
MEASUREMENT SYSTEM						
LABB						
τ_{RC}	Settling time	To 1% of final value(2)		4.6	6.6	µs
		To 0.1% of final value(2)		7	10	
$V_{ACMPR\_IN\_LABB}$	Input voltage range ACMPR_IN_LABB		0		1.5	V
	Sampling window ACMPR_IN_LABB	Programmable per 7 µs	7		28	µs
DIGITAL CONTROL - LOGIC LEVELS AND TIMING CHARACTERISTICS						
V_{SPI_VIN}	SPI supply voltage range	SPI_VIN	1.7		3.6	V
V_{OL}	Output low-level	RESET_Z, ACMPR_OUT, CLK_OUT. I_O = 0.3 mA sink current	0		0.3	V
		SPI_DOUT. I_O = 5 mA sink current	0		0.3 × V_{SPI_VIN}	
		INT_Z. I_O = 1.5 mA sink current	0		0.3 × V_{SPI_VIN}	
V_{OH}	Output high-level	RESET_Z, ACMPR_OUT, CLK_OUT. I_O = 0.3 mA source current	1.3		2.5	V
		SPI_DOUT. I_O = 5 mA source current	0.7 × V_{SPI_VIN}		V_{SPI_VIN}	
V_{IL}	Input low-level	PROJ_ON, CH_SEL_0, CH_SEL_1	0		0.4	V
		SPI_CSZ, SPI_CLK, SPI_DIN	0		0.3 × V_{SPI_VIN}	
V_{IH}	Input high-level	PROJ_ON, CH_SEL_0, CH_SEL_1	1.2			V
		SPI_CSZ, SPI_CLK, SPI_DIN	0.7 × V_{SPI_VIN}		V_{SPI_VIN}	
I_{BIAS}	Input bias current	V_{IO}= 3.3 V, any digital input pin			0.1	µA
SPI_CLK	SPI clock frequency(4)	Normal SPI mode, DIG_SPI_FAST_SEL = 0, f_{OSC} = 9 MHz	0		36	MHz
		Fast SPI mode, DIG_SPI_FAST_SEL = 1, V_{SPI_VIN}> 2.3 V, f_{OSC} = 9 MHz	20		40	
$t_{DEGLITCH}$	Deglitch time	CH_SEL_0, CH_SEL_1(2)		300		ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Frequency accuracy	T_A= 0 °C to 70°C	–5%		5%	
THERMAL SHUTDOWN						
T_{WARN}	Thermal warning (HOT threshold)			120		°C
	Hysteresis			10		

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12 V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to 节 8.2 (V_{IN} =12 V, I_{OUT} = 16 A, LED, external FETs) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SHTDWN}	Thermal shutdown (TSD threshold)			150		°C
	Hysteresis			15		

(1) Including rectifying diode
(2) Not production tested
(3) Care should be taken not to exceed the max power dissipation. Refer to 节 10.3 .
(4) Maximum depends linearly on oscillator frequency f_{OSC}.
(5) Take care that the capacitor has the specified capacitance at the related voltage, that is, V_{OFFSET}, V_{BIAS} , or V_{RESET} .
(6) VIN must be higher than the UVLO voltage setting, including after accounting for AC noise on VIN, for the DLPA3005 to fully operate. While 6.0 V is the min VIN voltage supported, TI recommends that the UVLO is never set below 6.21 V for fault fast power down. 6.21 V gives margin above 6.0 V to protect against the case where someone suddenly removes VIN’s power supply which causes the VIN voltage to drop rapidly. Failure to keep VIN above 6.0V before the mirrors are parked and VOFS, VRST, and VBIAS supplies are properly shut down can result in permanent damage to the DMD. Since 6.21 V is .21 V above 6.0 V, when UVLO trips there is time for the DLPA3005 and DLPC343x to park the DMD mirrors and do a fast shut down of supplies VOFS, VRST, and VBIAS. For whatever UVLO setting is used, if VIN’s power supply is suddenly removed enough bulk capacitance should be included on VIN inside the projector to keep VIN above 6.0V for at least 100us after UVLO trips.
(7) UVLO should not be used for normal power down operation, it is meant as a protection from power loss.
(8) General purpose buck2 (PWR6) is currently supported.
(9) Supports up to 32 A for series LEDs based on reference hardware design.

6.6 SPI Timing Parameters

SPI_VIN = 3.6 V ± 5%, T_A = 0 to 70°C, C_L = 10 pF (unless otherwise noted).

		MIN	NOM	MAX	UNIT
f_{CLK}	Serial clock frequency	0		40	MHz
t_{CLKL}	Pulse width low, SPI_CLK, 50% level	10			ns
t_{CLKH}	Pulse width high, SPI_CLK, 50% level	10			ns
t_t	Transition time, 20% to 80% level, all signals	0.2		4	ns
t_{CSCR}	SPI_SS_Z falling to SPI_CLK rising, 50% level	8			ns
t_{CFCS}	SPI_CLK falling to SPI_CSZ rising, 50% level			1	ns
t_{CDS}	SPI_MOSI data setup time, 50% level	7			ns
t_{CDH}	SPI_MOSI data hold time, 50% level	6			ns
t_{iS}	SPI_MISO data setup time, 50% level	10			ns
t_{iH}	SPI_MISO data hold time, 50% level	0			ns
t_{CFDO}	SPI_CLK falling to SPI_MISO data valid, 50% level		13		ns
t_{CSZ}	SPI_CSZ rising to SPI_MISO HiZ		6		ns

7 Detailed Description

7.1 Overview

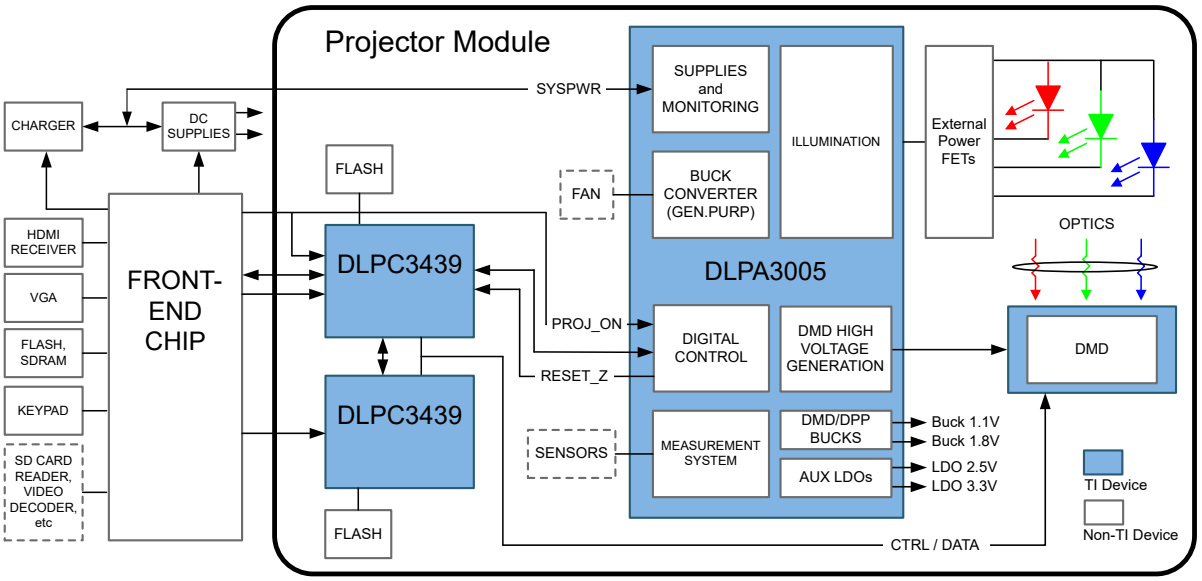
The DLPA3005 is a highly integrated power management IC optimized for DLP Pico Projector systems. It targets accessory applications up to several hundreds of lumen and is designed to support a wide variety of high-current LEDs. 节 7.2 shows a typical DLP Pico Projector implementation using the DLPA3005.

Part of the projector is the projector module, which is an optimized combination of components consisting of, for instance, DLPA3005, LEDs, DMD, DLPC chip, memory, and optional sensors and fan. The front-end chip controls the projector module. More information about the system and projector module configuration can be found in a separate application note.

Within the DLPA3005, several blocks can be distinguished. The blocks are listed below and subsequently discussed in detail:

- Supply and monitoring: Creates internal supply and reference voltages and has functions such as thermal protection
- Illumination: Block to control the light. Contains drivers, strobe decoder for the LEDs and power conversion
- External Power FETs: Capable for 16 A
- DMD: Generates voltages and their specific timing for the DMD. Contains regulators and DMD/DLPC buck converters
- Buck converter: General purpose buck converter
- Auxiliary LDOs: Fixed voltage LDOs for customer usage
- Measurement system: Analog front end to measure internal and external signals
- Digital control: SPI interface, digital control

7.2 Functional Block Description



7.3 Feature Description

7.3.1 Supply and Monitoring

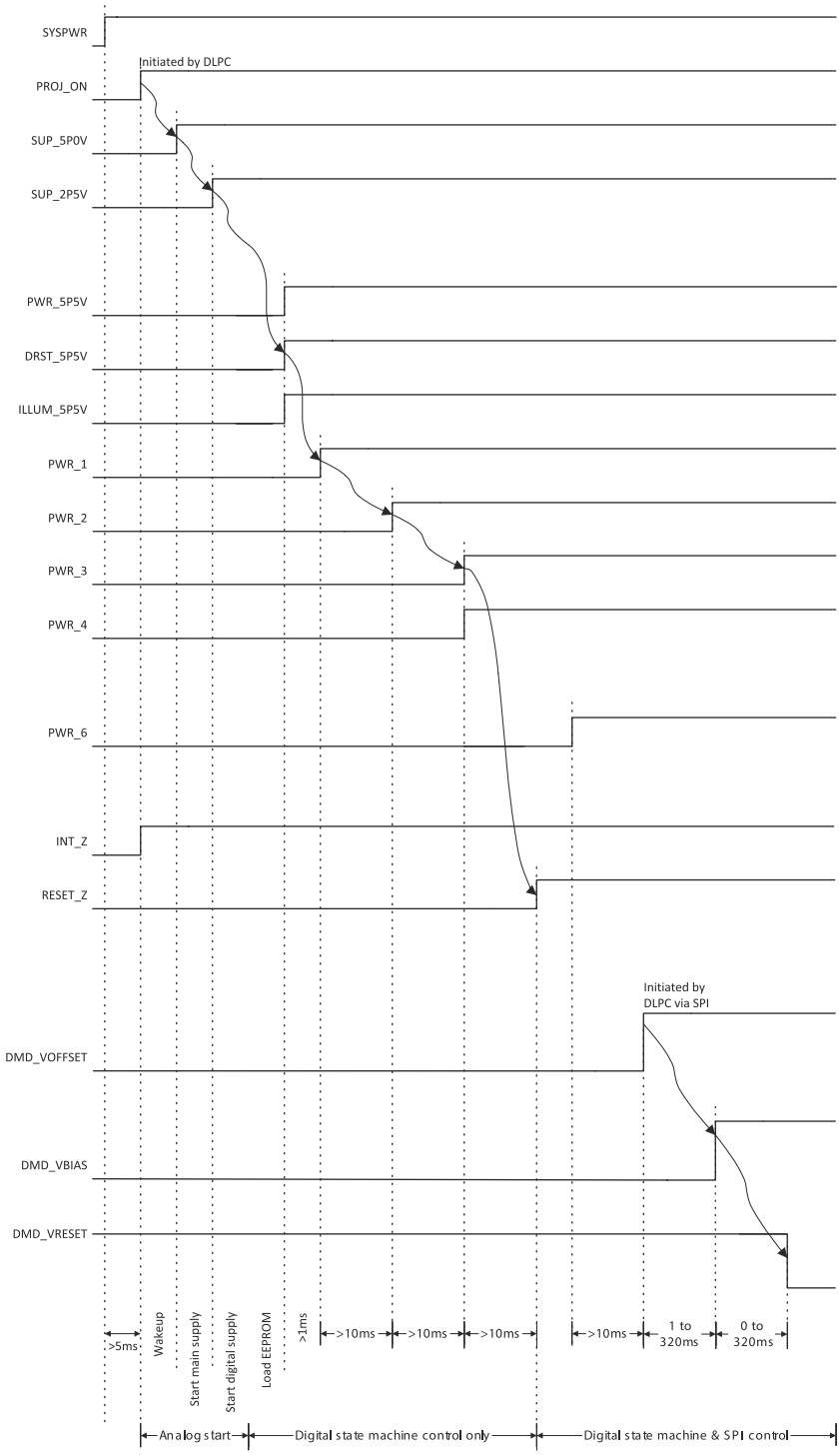
This block takes care of creating several internal supply voltages and monitors correct behavior of the device.

7.3.1.1 Supply

SYSPWR is the main supply of the DLPA3005. It can range from 6 V to 20 V, where the typical is 12 V. At power-up, several (internal) power supplies are started one after the other in order to make the system work correctly (图 7-1). A sequential startup ensures that all the different blocks start in a certain order and prevent excessive startup currents. The main control to start the DLPA3005 is the control pin *PROJ_ON*. Once set high the *basic* analog circuitry is started that is needed to operate the digital and SPI interface. This circuitry is supplied by two LDO regulators that generate 2.5 V (SUP_2P5V) and 5 V (SUP_5P0V). These regulator voltages are for internal use only and should not be loaded by an external application. The output capacitors of those LDOs should be 2.2 µF for the 2.5-V LDO, and 4.7 µF for the 5-V LDO, pin 91 and 92 respectively. Once these are up the digital core is started, and the DLPA3005 Digital State Machine (DSM) takes over.

Subsequently, the 5.5-V LDOs for various blocks are started: PWR_5V5V, DRST_5P5V and ILLUM_5P5V. Next, the buck converters and DMD LDOs are started (PWR_1 to PWR_4). The DLPA3005 is now awake and ready to be controlled by the DLPC (indicated by RESET_Z going high).

The general purpose buck converter (PWR_6) can be started (if used) as well as the regulator that supplies the DMD. The DMD regulator generates the timing critical VOFFSET, VBIAS, and VRESET supplies.



1. Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.
2. SUP_5P0V and SUP_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ_ON is pulled high.

图 7-1. Powerup Timing

7.3.1.2 Monitoring

Several possible faults are monitored by the DLPA3005. If a fault has occurred and what kind of fault it is can be read in Main Status register. Subsequently, an interrupt can be generated if such a fault occurs. The fault conditions for which an interrupt is generated can be configured individually in the Interrupt Mask register.

7.3.1.2.1 Block Faults

Fault conditions for several supplies can be observed such as the low voltage supplies (SUPPLY_FAULT). ILLUM_FAULT monitors correct supply and voltage levels in the illumination block and DMD_FAULT monitors a correct functioning DMD block. The PROJ_ON_INT bit indicates if PROJ_ON was asserted.

7.3.1.2.2 Auto LED Turn Off Functionality

The DLPA3005 can be supplied from an adapter. The DLPA3005 use several warning and detection levels, as indicated in the previous paragraphs, to prevent system damage in case the supply voltage becomes too low or even interrupted.

Interruption of the supply voltage occurs when, for example, the adapter is switched to another mains outlet. A change of supply voltage from, for example, 20 V to 8 V can occur, and thus the OVP level (which is ratio metric, see 节 7.3.2.5.2) could become lower than V_{LED}. An OVP fault will be triggered and the system switches off.

The Auto_LED_Turn_Off functionality can be used to prevent the system from turning off in these circumstances. This function disables the LEDs when the supply voltage drops below LED_AUTO_OFF_LEVEL. When the Auto_LED_Turn_Off functionality is enabled (reg 0x01h), once a supply voltage drop is detected to below LED_AUTO_OFF_LEVEL, the LEDs will be switched off and the system should start sending lower current levels to have a lower V_{LED}. After start using lower currents, the LEDs can be switched on again by disabling AUTO_LED_TURN_OFF function. As a result the system can continue working at the lower supply voltage using a lower intensity. Once the mains adapter is plugged in again, the Auto_LED_Turn_Off functionality can be enabled again. Now the LED currents can be restored to their original levels from before the supply voltage drop.

7.3.1.2.3 Thermal Protection

The chip temperature is monitored constantly to prevent overheating of the device. There are two levels of a fault condition. The first is TS_WARN to warn for overheating. This is an indication that the chip temperature raises to a critical temperature. The next level of warning is TS_SHUT. This occurs at a higher temperature than TS_WARN and shuts down the chip to prevent permanent damage. Both temperature faults have hysteresis on their levels to prevent rapid switching around the temperature threshold.

7.3.2 Illumination

The illumination function includes all blocks needed to generate light for the DLP system. In order to accurately set the current through the LEDs, a control loop is used (图 7-2). The intended LED current is set through IDAC[9:0]. The Illumination driver controls the LED anode voltage V_{LED} and as a result a current will flow through one of the LEDs. The LED current is measured from the voltage across sense resistor R_{LIM}. Based on the difference between the actual and intended current, the loop controls the output of the buck converter (V_{LED}) higher or lower. The LED which conducts the current is controlled by switches P, Q, and R. The *Openloop feedback circuitry* ensures that the control loop can be closed for cases when there is no path through the LED (for instance, when I_{LED}= 0).

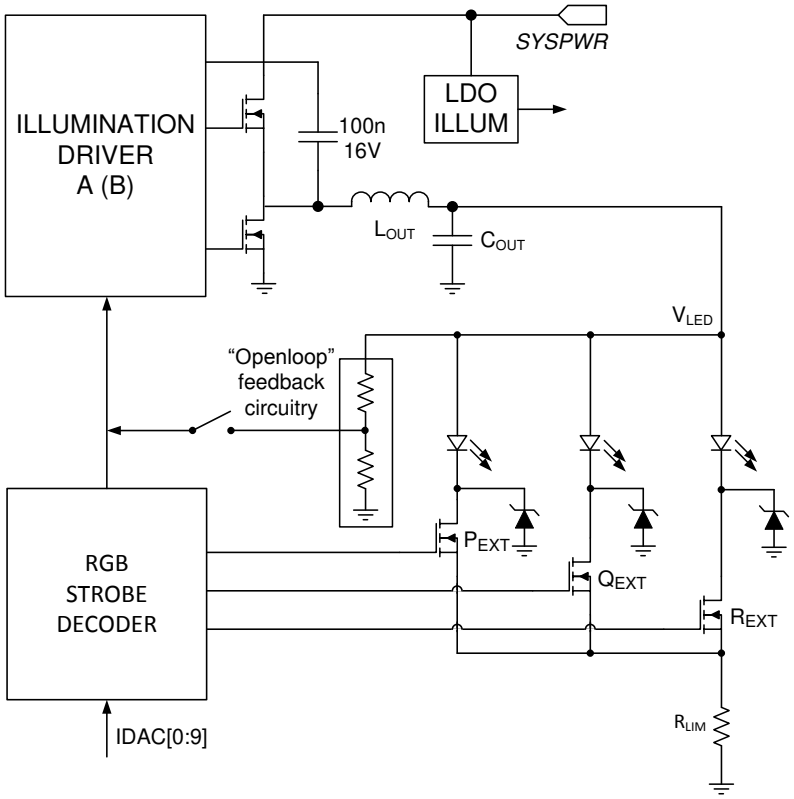


图 7-2. Illumination Control Loop

Within the illumination block, the following blocks can be distinguished:

- Programmable gain block
- LDO ILLUM, analog supply voltage for internal illumination blocks
- Illumination driver A, primary driver for the external FETs
- Illumination driver B, secondary driver – for future purpose. Will not be discussed
- RGB strobe decoder, driver for external switches to control the on-off rhythm of the LEDs and measures the LED current

7.3.2.1 Programmable Gain Block

The current through the LEDs is determined by a digital number stored in the respective SWx_IDAC(x) registers, 0x03h to 0x08h. These registers determine the LED current which is measured through the sense resistor R_{LIM}. The voltage across R_{LIM} is compared with the current setting from the IDAC registers and the loop regulates the current to its set value.

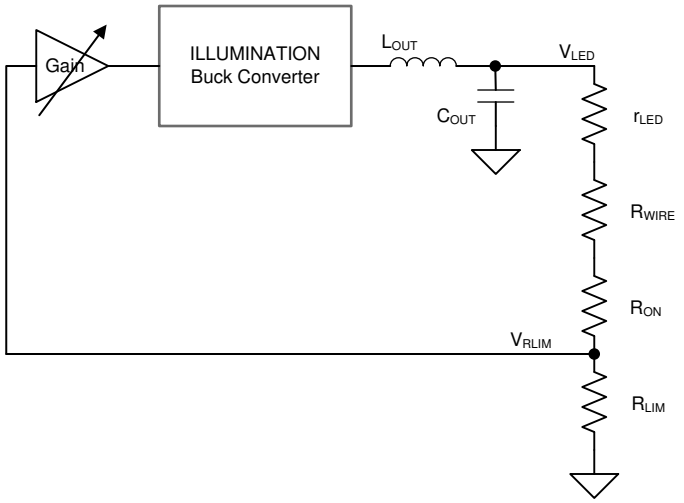


图 7-3. Programmable Gain Block in the Illumination Control Loop

When current is flowing through an LED, a forward voltage is built up over the LED. The LED also represents a (low) differential resistance which is part of the load circuit for V_{LED}. Together with the wire resistance (R_{WIRE}) and the R_{ON} resistance of the FET switch a voltage divider is created with R_{LIM} that is a factor in the loop gain of the ILED control. Under normal conditions, the loop is able to produce a well regulated LED current up to 16 Amps.

Since this voltage divider is part of the control loop, care must be taken while designing the system.

When, for instance, two LEDs in series are connected, or when a relatively high wiring resistance is present in the loop, the loop gain will reduce due to the extra attenuation caused by the increased series resistances of r_{LED} + R_{WIRE} +R_{ON}. As a result, the loop response time lowers. To compensate for this increased attenuation, the loop gain can be increased by selecting a higher gain for the programmable gain block. The gain increase can be set through register ILLUM_BW_BCx.

Under normal circumstances the default gain setting (00h) is sufficient. In case of a series connection of two LEDs setting 01h or 02h might suffice.

As discussed previously, wiring resistance also impacts the control-loop performance. It is advisable to prevent unnecessary large wire length in the loop. Keeping wiring resistance as low as possible is good for efficiency reasons. In case wiring resistance still impacts the response time of the loop, an appropriate setting of the gain block can be selected. The same goes for connector resistance and PCB tracks. Note that every milliohm (mΩ) counts. These precautions help to ensure the proper functioning of the I_{LED} current loop.

7.3.2.2 LDO Illumination

This regulator is dedicated to the illumination block and provides an analog supply of 5.5 V to the internal circuitry. It is recommended to use 1-µF capacitors on both the input and output of the LDO.

7.3.2.3 Illumination Driver A

The illumination driver of the DLPA3005 is a buck controller for driving two external low-ohmic N-channel FETs (图 7-4). The theory of operation of a buck converter is explained in the application note *Understanding Buck Power Stages in Switchmode Power Supplies*. For proper operation, selection of the external components is very important, especially the inductor L_{OUT} and the output capacitor C_{OUT}. For best efficiency and ripple performance, an inductor and capacitor should be chosen with low equivalent series resistance (ESR).

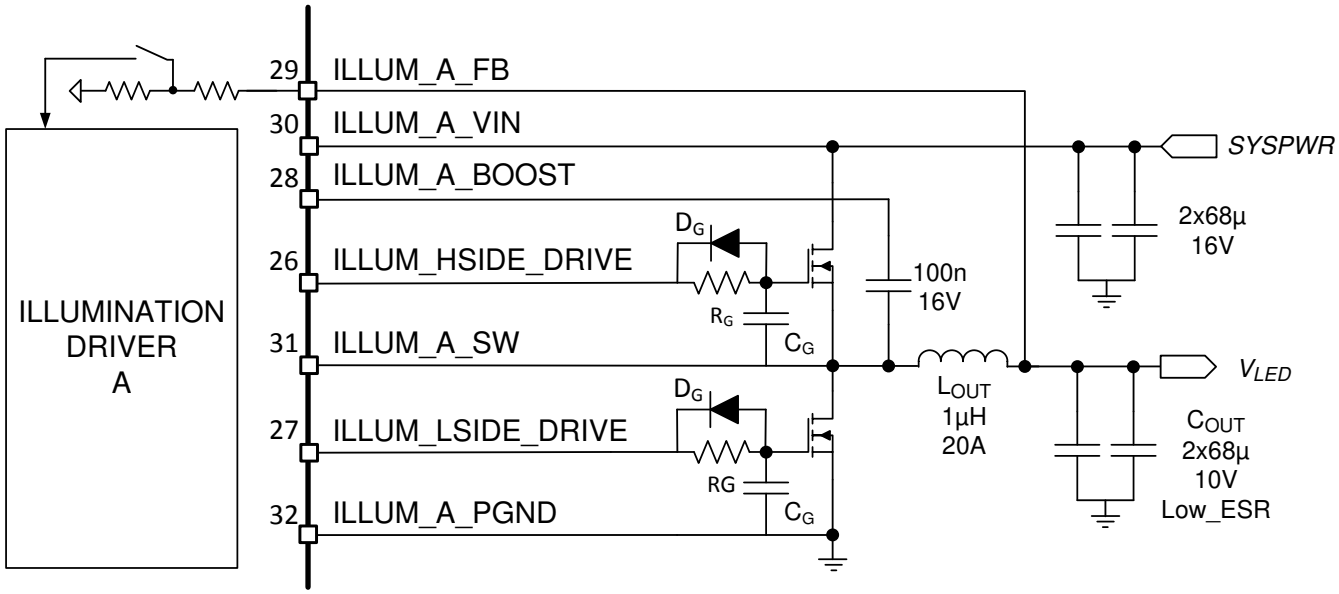


图 7-4. Typical Illumination Driver Configuration

Several factors determine the component selection of the buck converter, such as input voltage (SYSPWR), desired output voltage (V_{LED}) and the allowed output current ripple. Configuration starts with selecting the inductor L_{OUT}.

The value of the inductance of a buck power stage is selected such that the peak-to-peak ripple current flowing in the inductor stays within a certain range. Here, the target is set to have an inductor current ripple, k_{I_RIPPLE}, less than 0.3 (30%). The minimum inductor value can be calculated given the input and output voltage, output current, switching frequency of the buck converter (f_{SWITCH}= 600 kHz), and inductor ripple of 0.3 (30%):

$$L_{OUT} = \frac{\frac{V_{OUT}}{V_{IN}} \cdot (V_{IN} - V_{OUT})}{k_{I\_RIPPLE} \cdot I_{OUT} \cdot f_{SWITCH}} \quad (1)$$

Example: V_{IN}= 12 V, V_{OUT}= 4.3 V, I_{OUT}= 16 A results in an inductor value of L_{OUT}= 1 µH

Once the inductor is selected, the output capacitor C_{OUT} can be determined. The value is calculated using the fact that the frequency compensation of the illumination loop has been designed for an LC-tank resonance frequency of 15 kHz:

$$f_{RES} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}} = 15kHz \quad (2)$$

Example: C_{OUT}= 110 µF given that L_{OUT}= 1 µH. A practical value is 2 × 68 µF. Here, a parallel connection of two capacitors is chosen to lower the ESR even further.

The selected inductor and capacitor determine the output voltage ripple. The resulting output voltage ripple V_{LED_RIPPLE} is a function of the inductor ripple k_{I_RIPPLE}, output current I_{OUT}, switching frequency f_{SWITCH} and the capacitor value C_{OUT}:

$$V_{LED\_RIPPLE} = \frac{k_{I\_RIPPLE} \cdot I_{OUT}}{8 \cdot f_{SWITCH} \cdot C_{OUT}} \quad (3)$$

Example: k_{I_RIPPLE}= 0.3, I_{OUT}= 16 A, f_{SWITCH}= 600 kHz and C_{OUT}= 2 x 68 µF results in an output voltage ripple of V_{LED_RIPPLE}= 7 mVpp

As can be seen, this is a relatively small ripple.

It is strongly advised to keep the capacitance value low. The larger the capacitor value the more energy is stored. In case of a V_{LED} going down stored energy needs to be dissipated. This might result in a large discharge current. For a V_{LED} step down from V_1 to V_2, while the LED current was I_1. The theoretical peak reverse current is:

$$I_{2,MAX} = \sqrt{\frac{C_{OUT}}{L_{OUT}} \times \left(V_1^2 - V_2^2\right) + I_1^2} \quad (4)$$

Depending on the selected external FETs, the following three components might need to be added for each power FET:

- Gate series resistor (R_G)
- Gate series diode (D_G)
- Gate parallel capacitance (C_G)

It is advisable to have placeholders for these components in the board design.

The gate series resistors can be used to slow down the enable transient of the power FET. Since large currents are being switched, a fast transient implies a potential risk on ringing. Slowing down the turn-on transient reduces the edge steepness of the drain current and thus reduces the induced inductive ringing. A resistance of a few Ohm typically is sufficient.

The gate series resistance is also present in the turn-off transient of the power FET. This might have a negative effect on the non-overlap timing. In order to keep the turn-off transient of the power FET fast, a parallel diode with the gate series resistance can be used. The cathode of the diode should be directed to the DLPA3005 device in order have fast gate pull-down.

A third component that might be needed, depending on the specific configuration and FET selection, is an extra gate-source filter capacitance. Specifically, for the higher supply voltages this capacitance is advisable. Due to a large drain voltage swing and the drain-gate capacitance, the gate of a disabled power FET might be pulled high parasitically.

For the low-side FET this can happen at the end of the non-overlap time while the power converter is supplying current. For that case the switch node is low at the end of the non-overlap time. Enabling the high-side FET pulls high the switch node. Due to the large and steep switch node edge, charge is injected through the drain-gate capacitance of the low-side FET into the gate of the low-side FET. As a result the low-side FET can be enabled for a short period of time causing a shoot-through current.

For the high-side FET a dual case exists. If the power converter is discharging VLED, the power converter current is directed inward and thus at the end of the non-overlap time the switch node is high. If at that moment the low-side FET is enabled, via the gate-drain capacitance of the high-side FET charge is being injected into the gate of the high-side FET potentially causing the device to switch on for a short amount of time. That will cause a shoot through current as well.

To reduce the effect of the charge injection through the drain-gate capacitance, an extra gate-source filter capacitance can be used. Assuming a linear voltage division between gate-source capacitance and gate-drain capacitance, for a 20V supply voltage the ratio of gate-source capacitance and gate-drain capacitance should be kept to about 1:10 or larger. It is advised to carefully test the gate-drive signals and the switch node for potential cross conduction.

Sometimes dual FETs are used to spread out power dissipation (heat). To prevent parasitic gate-oscillation a structure, as shown in 图 7-5 is suggested. Each gate is being isolated with R_{ISO} to damp potential oscillations. A resistance of 1 Ohm is typically sufficient.

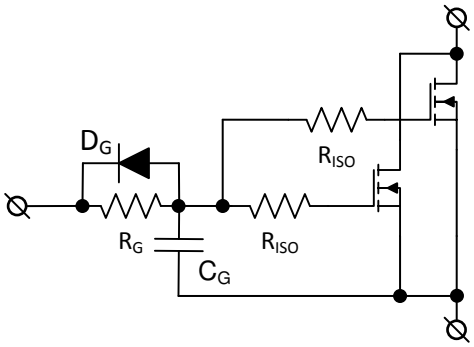


图 7-5. Using R_{ISO} to Prevent Gate Oscillations When Using Power FETs in Parallel

Finally, two other components need to be selected in the buck converter. The value of the input-capacitor (pin ILLUM_A_VIN) should be equal or greater than the selected output capacitance C_{OUT}, in this case ⩾2 × 68 µF. The capacitor between ILLUM_A_SWITCH and ILLUM_A_BOOST is a charge pump capacitor to drive the high side FET. The recommended value is 100 nF.

7.3.2.4 RGB Strobe Decoder

The DLPA3005 contains circuitry to sequentially control the three color-LEDs (red, green, and blue). This circuitry consists of three drivers to control external switches, the actual strobe decoder, and the LED current control (图 7-6). The NMOS switches are connected to the cathode terminals of the external LED package and turn on and off the currents through the LEDs.

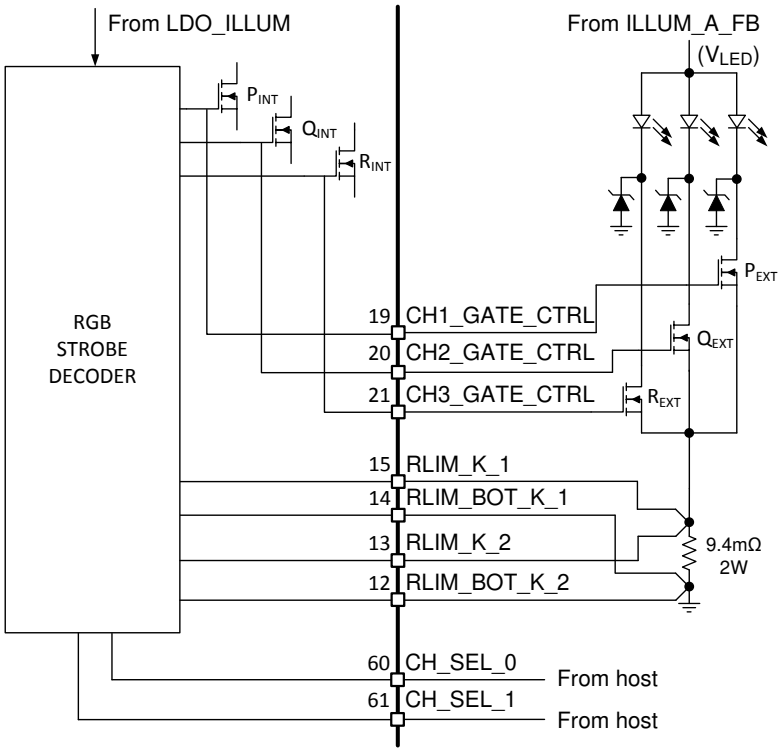


图 7-6. Switch Connection for a Common-Anode LED Assembly

The NMOS FETs P, Q, and R are controlled by the CH_SEL_0 and CH_SEL_1 pins. CH_SEL[1:0] typically receive a rotating code switching from RED to GREEN to BLUE and then back to RED. The relation between CH_SEL[0:1] and which switch is closed is indicated in 表 7-1.

表 7-1. Switch Positions for Common Anode RGB LEDs

PINS CH_SEL[1:0]	SWITCH			IDAC REGISTER
	P	Q	R	
00	Open	Open	Open	N/A
01	Closed	Open	Open	0x03 and 0x04 SW1_IDAC[9:0]
10	Open	Closed	Open	0x05 and 0x06 SW2_IDAC[9:0]
11	Open	Open	Closed	0x07 and 0x08 SW3_IDAC[9:0]

Besides enabling one of the switches, CH_SEL[1:0] also selects a 10-bit current setting for the control IDAC that is used as the set current for the LED. This set current together with the measured current through R_{LIM} is used to control the illumination driver to the appropriate V_{LED}. The current through the 3 LEDs can be set independently by registers SWx_IDAC(x), 0x03 to 0x08 (表 7-1).

Each current level can be set from *off* to 150 mV/R_{LIM} in 1023 steps:

$$\text{Led current(A)} = 0 \text{ for bit value} = 0$$

$$\text{Led current(A)} = \frac{\text{Bit value} + 1}{1024} \cdot \frac{150\text{mV}}{R_{LIM}} \text{ for bit value} = 1 \text{ to } 1023 \quad (5)$$

For single LED, the maximum current for R_{LIM}= 9.4 mΩ is thus 16A.

For two LEDs in series, the maximum current is 32A, thus R_{LIM} (for example, R_{LIM}= 4.7 mΩ to support configuration for 32A) need to change for higher LED current.

For proper operation a minimum LED current of 5% of I_{LED_MAX} is required.

7.3.2.4.1 Break Before Make (BBM)

The switching of the three LED NMOS switches (P, Q, R) is controlled such that a switch is returned to the OPEN position first before the subsequent switch is set to the CLOSED position (BBM), 图 7-7. The dead time between opening and closing switches is controlled through the BBM register. Switches that already are in the CLOSED position and are to remain in the CLOSED state, are not opened during the BBM delay time.

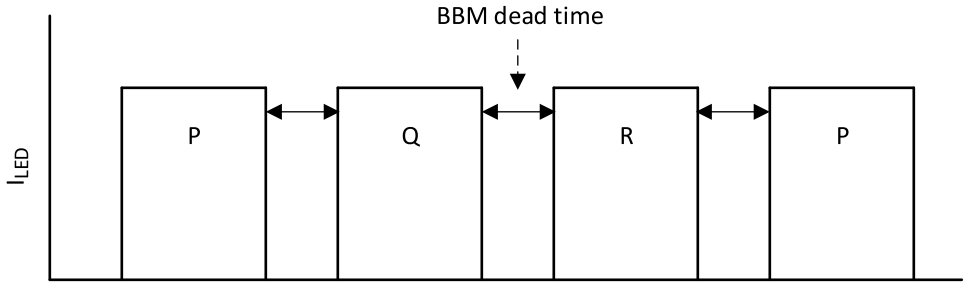


图 7-7. BBM Timing

7.3.2.4.2 Openloop Voltage

Several situations exist in which the control loop for the buck converter through the LED is not present. To prevent the output voltage of the buck converter to "run-away," the loop is closed by means of an internal resistive divider (see 图 7-2—Openloop feedback circuitry). Situations in which the openloop voltage control is active:

- During the BBM period. Transitions from one LED to another implies that during the BBM time all LEDs are off.
- Current setting for all three LEDs is 0.

It is advised to set the openloop voltage to about the lowest LED forward voltage. The openloop voltage can be set between 3 V and 18 V in steps of 1 V through register ILLUM_OLV_SEL.

7.3.2.4.3 Transient Current Limit

Typically, the forward voltages of the GREEN and BLUE diodes are close to each other (about 3 V to 5 V) however the forward voltage of the red diode is significantly lower (2 V to 4 V). This can lead to a current spike in the RED diode when the strobe controller switches from green or blue to red. This happens because V_{LED} is initially at a higher voltage than required to drive the red diode. DLPA3005 provides transient current limiting for each switch to limit the current in the LEDs during the transition. The transient current limit value is controlled through register 0x02 (ILLUM_ILIM). In a typical application it is required only for the RED diode. The value for ILLUM_ILIM should be set at least 20% higher than the DC regulation current. Register 0x02 (ILLUM_SW_ILIM_EN) contains three bits to select which switch employs the transient current limiting feature. The effect of the transient current limit on the LED current is shown in 图 7-8.

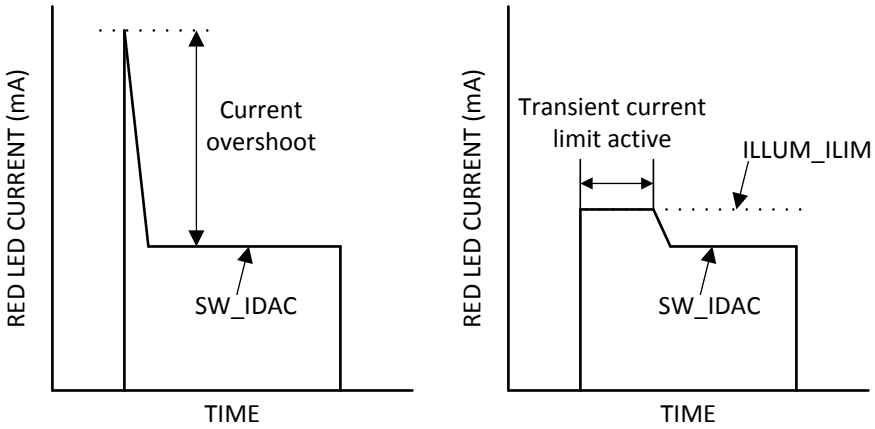


图 7-8. LED Current Without (Left) and With (Right) Transient Current Limit

7.3.2.5 Illumination Monitoring

The illumination block is continuously monitored for system failures to prevent damage to the DLPA3005 and LEDs. Several possible failures are monitored such as a broken control loop and a too high or too low output voltage V_{LED}. The overall illumination fault bit is in Main Status register (ILLUM_FAULT). If any of the below failures occur, the ILLUM_FAULT bit may be set high:

- ILLUM_BC1_PG_FAULT
- ILLUM_BC1_OV_FAULT

Where, PG= Power Good and OV= Over Voltage

7.3.2.5.1 Power Good

Both the Illumination driver and the Illumination LDO have a power good indication. The power good for the driver indicates if the output voltage (V_{LED}) is within a defined window indicating that the LED current has reached the set point. If for some reason the LED current cannot be controlled to the intended value, this fault occurs. Subsequently, bit ILLUM_BC1_PG_FAULT in the Detailed status register1 is set high. The illumination LDO output voltage is also monitored. When the power good of the LDO is asserted it implies that the LDO voltage is below a predefined minimum of 80% (rising) or 60% (falling) edge. The power good indication for the LDO is in the Detailed status register1.

7.3.2.5.2 Ratio Metric Overvoltage Protection

The DLPA3005 illumination driver LED outputs are protected against open circuit use. In case no LED is connected and the DLPA3005 is instructed to set the LED current to a specific level, the LED voltage (ILLUM_A_FB) will quickly rise and potentially rail to VIN. This should be prevented. The OVP protection circuit triggers once V_{LED} crosses a predefined level. As a result, the DLPA3005 is switched off.

The same protection circuit is triggered in case the supply voltage (VINA) will become too low to have the DLPA3005 work properly given the V_{LED} level. This protection circuit is constructed around a comparator that will sense both the LED voltage and the VINA supply voltage. The fraction of the VINA is connected to the minus

input of the comparator while the fraction of the V_{LED} voltage is connected to the plus input. Triggering occurs when the plus input rises above the minus input and an OVP fault is set. The fraction of the VINA must be set between 1 V and 4 V to ensure proper operation of the comparator.

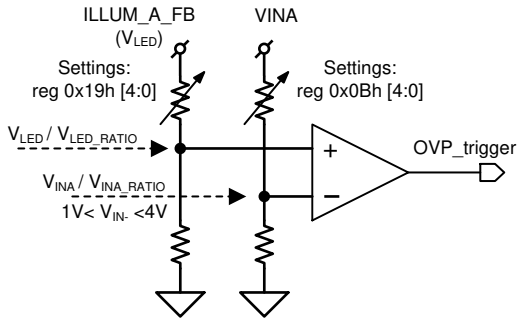


图 7-9. Ratio Metric OVP

The fraction of the ILLUM_A_FB voltage is set by the register VLED_OVP_VLED_RATIO, while the setting of the fraction of the VINA voltage is done by register VLED_OVP_VIN_RATIO. In general, an OVP fault is set when:

$$V_{LED}/V_{LED\_RATIO} \geqslant V_{INA}/V_{INA\_RATIO}$$

thus when:

$$V_{LED} \geqslant V_{INA} * V_{LED\_RATIO}/V_{INA\_RATIO}.$$

Clearly, the OVP level is ratio-metric; that is, can be set to a fixed fraction of V_{INA}.

7.3.2.6 Illumination Driver plus Power FETs Efficiency

Below (图 7-10) an overview is given of the efficiency of the illumination driver plus power FETs for an input voltage of 12 V. Used external components (图 7-4): High-side FET (L) CDS17506Q5A, Low-side FET (M) CDS17501Q5A, L_{OUT} = 2 x 2.2 µH parallel, C_{OUT} = 88 µF. The efficiency is shown for several output voltage levels (V_{LED}) versus output current.

图 7-11 depict the efficiency versus input voltage ($V_{ILLUM\_A\_VIN}$) at various output voltage levels (V_{LED}) for an output current of 16 A.

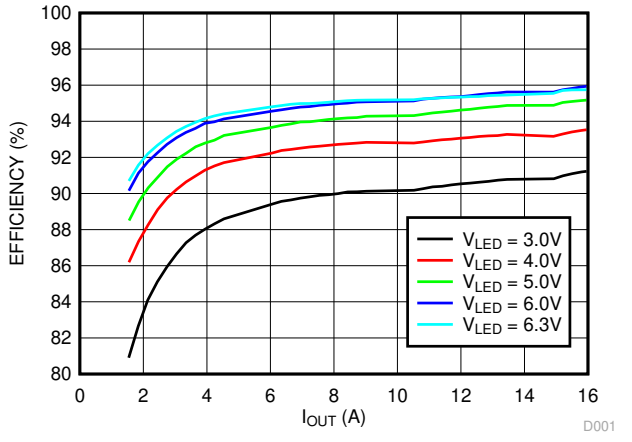


图 7-10. Illumination Driver Plus Power FETs Efficiency ($V_{ILLUM\_A\_IN}$= 12 V)

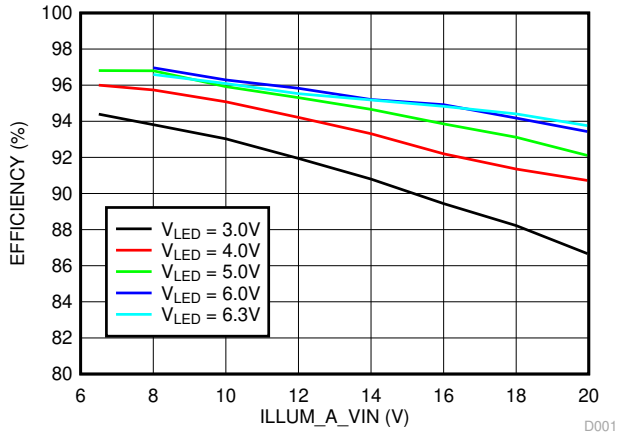


图 7-11. Illumination Driver Plus Power FETs Efficiency vs $V_{ILLUM\_A\_IN}$ (I_{OUT} = 16 A)

7.3.3 External Power FET Selection

The DLPA3005 requires five external N-type Power FETs for proper operation. Two power FETs are required for the illumination buck converter section (FETs L_{EXT} and M_{EXT} in 图 8-3) and three power FETs are required for the LED selection switches (FETs P_{EXT}, Q_{EXT} , and R_{EXT} in 图 8-3). This section discusses the selection criteria for these FETs:

- Threshold voltage
- Gate charge and gate timing
- $R_{DS(ON)}$

7.3.3.1 Threshold Voltage

The DLPA3005 has five drive outputs for the respective five power FETs. The signal swing at these outputs is about 5 V. Thus, FETs should be selected that are turned on adequately with a gate-source voltage of 5 V. For the three LED selection outputs (CHx_GATE_CTRL) and the low-side drive (ILLUM_LSIDE_DRIVE), the drive signal is ground referred. For the ILLUM_HSIDE_DRIVE output the signal swing is referred to the switch node of the converter, ILLUM_A_SW. All five power FETs should be N-type.

7.3.3.2 Gate Charge and Gate Timing

For power FETs a typically specified parameter is the total gate charge required to turn-on or turn-off the FET. The selection of the illumination buck-converter FETs with respect to their total gate charge is mainly relative to gate-source rise and fall times. For proper operation it is advised to have the gate-source rise and fall times maximum on the order of 20 ns – 30 ns. Given the typical high-side driver pullup resistance of about 5 Ohm, an equivalent maximum gate capacitance of 4-6nF is appropriate. Since the gate-source swing is about 5 V, a total turn-on/off gate charge of maximum 20 nC – 30 nC is therefore advised.

The DPLA3005 has built-in non-overlap timing to prevent that both the high-side and low-side FET of the illumination buck converter are turned-on simultaneously. The typical non-overlap timing is about 35 ns. In most applications this should give sufficient margins. On top of this non-overlap timing the DLPA3005 measures the gate-source voltage of the external FETs to determine whether a FET is actually on or off. This measurement is done at the pins of the DLPA3005. For the low-side FET this measurement is done between ILLUM_LSIDE_DRIVE and ILLUM_A_GND. Similarly, for the high-side FET the gate-source voltage is measured between ILLUM_HSIDE_DRIVE and ILLUM_A_SW. The location of these measurement nodes imply that at all times no additional drivers or circuitry should be inserted between the DLPA3005 and the external power FETs of the buck converter. Inserting circuitry (delays) could potentially lead to incorrect on-off detection of the FETs and cause shoot-through currents. These shoot-through currents are negatively affecting the efficiency, but more seriously can potentially damage the power FETs.

For the LED selection switches no specific selection criteria are present on gate charge / timing. This is because the timing of the LED selection signals is in the microsecond range rather than nanosecond range.

7.3.3.3 $R_{DS(ON)}$

The selection of the FET relative to its drain-source on-resistance, $R_{DS(ON)}$, has two aspects. First, for the high-side FET of the illumination buck-converter, the $R_{DS(ON)}$ is a factor in the overcurrent detection. Second, for the other four FETs, the power dissipation drives the choice of the FETs $R_{DS(ON)}$.

To detect an overcurrent situation, the DLPA3005 measures the drain-source voltage drop of the high-side FET when turned on. The overcurrent detection circuit triggers, and switches off the high-side FET, when the threshold $V_{DC\text{-}Th}$ = 185 mV (typical) is reached. Therefore, the actual current, I_{OC}, at which this overcurrent detection triggers, is given by:

$$I_{OC} = \frac{V_{DC-Th}}{R_{DS(ON)}} = \frac{185\ mV}{R_{DS(ON)}} \quad (6)$$

Note that the $R_{DS(ON)}$ should be taken from the FET data sheet at high-temperature , that is, at overcurrent the FETs will likely by hot.

For example, the CSD17510Q5A NexFET has an $R_{DS(ON)}$ of 7 mΩ at 125°C. Using this FET will result in an overcurrent level of 26 A. This FET would be a good choice for a 16 A application.

For the low-side FET and the three LED selection FETs the $R_{DS(ON)}$ selection is mainly governed by the power dissipation due to conduction losses. The power dissipated in these FETs is given by:

$$P_{DISS} = \int_{t} I_{DS}^{2}(t) R_{DS(ON)} \quad (7)$$

In which I_{DS} is the current running through the respective FET. The lower the $R_{DS(ON)}$, the lower is the dissipation.

For example, the CSD17501Q5A has $R_{DS(ON)}$= 3 mΩ. For a drain-source current of 16 A with a duty cycle of 25% (assuming the FET is used as LED selection switch), the dissipation is about 0.2 W in this FET.

7.3.4 DMD Supplies

This block contains all the supplies needed for the DMD and DLPC (图 7-12). The block comprises:

- LDO_DMD: for internal supply
- DMD_HV: regulator generates high voltage supplies
- Two buck converters: for DLPC/DMD voltages

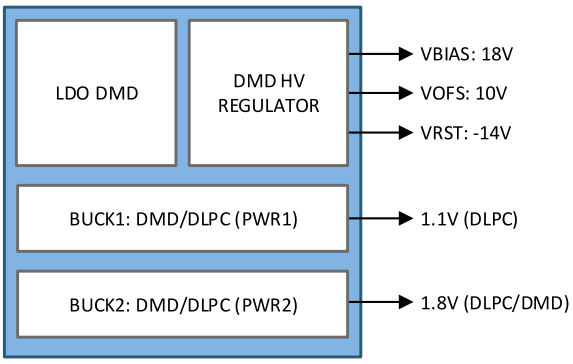


图 7-12. DMD Supplies Blocks

The DMD supplies block is designed to work with the DMD and the related DLPC. The DMD has its own set of supply voltage requirements. Besides the three high voltages, two supplies are needed for the DMD and the related DLPC (DLPC343x-family for instance). These supplies are made by two buck converters.

The EEPROM of the DLPA3005 is factory programmed for a certain configuration, such as which buck converters are used. Which configuration is programmed in EEPROM can be read in the capability register. It concerns the following bits:

- DMD_BUCK1_USE
- DMD_BUCK2_USE

7.3.4.1 LDO DMD

This regulator is dedicated to the DMD supplies block and provides an analog supply voltage of 5.5 V to the internal circuitry.

7.3.4.2 DMD HV Regulator

The DMD HV regulator generates three high voltage supplies: DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET (图 7-13). The DMD HV regulator uses a switching regulator (switch A-D), where the inductor is time shared between all three supplies. The inductor is charged up to a certain current value (current limit) and then discharged into one of the three supplies. If not all supplies need charging the time available will be equally shared between those that do need charging.

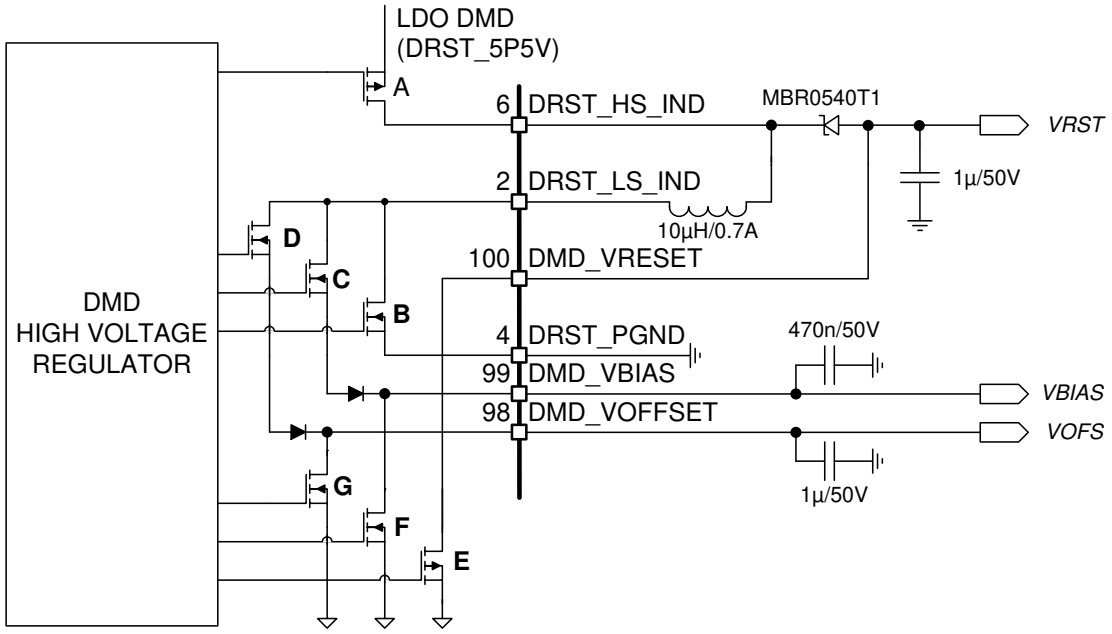


图 7-13. DMD High Voltage Regulator

7.3.4.3 DMD/DLPC Buck Converters

Each of the two DMD buck converters creates a supply voltage for the DMD and/or DLPC. The values of the voltages for the DMD and DLPC used, for instance:

- DMD+DLPC3439: 1.1 V (DLPC) and 1.8 V (DLPC/DMD)

The topology of the buck converters is the same as the general purpose buck converter discussed later in this document. How to configure the inductor and capacitor will be discussed in 节 7.3.5 .

A typical configuration is 3.3 µH for the inductor and 2 × 22 µF for the output capacitor.

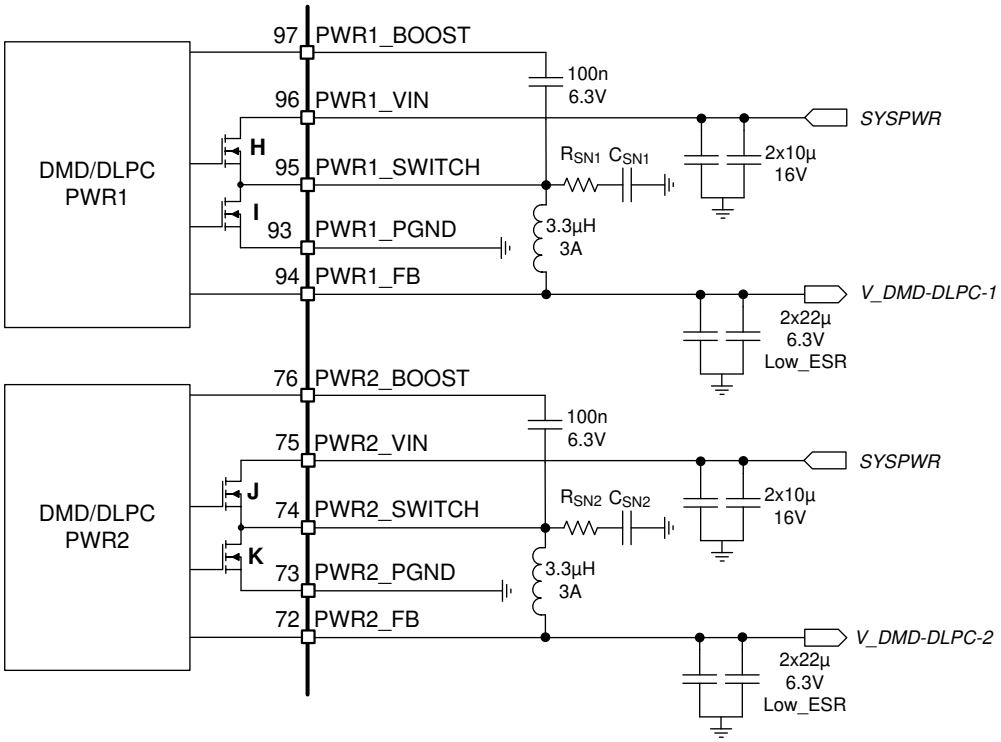


图 7-14. DMD/DLPC Buck Converters

7.3.4.4 DMD Monitoring

The DMD block is continuously monitored for failures to prevent damage to the DLPA3005 and/ or the DMD. Several possible failures are monitored such that the DMD voltages can be ensured. Failures could be for instance a broken control loop or a too high or too low converter output voltage. The overall DMD fault bit is in Main Status register, DMD_FAULT. If any of the failures in 表 7-2 occur, the DMD_FAULT bit will be set high.

表 7-2. DMD FAULT Indication

POWER GOOD		
BLOCK	**REGISTER BIT**	**THRESHOLD**
HV Regulator	DMD_PG_FAULT	DMD_VRESET: 90%, DMD_VOFFSET and DMD_VBIAS: 86% rising, 66% falling
PWR1	BUCK_DMD1_PG_FAULT	Ratio: 72%
PWR2	BUCK_DMD2_PG_FAULT	Ratio: 72%
PWR3 (LDO_2)	LDO_GP2_PG_FAULT / LDO_DMD1_PG_ FAULT	80% rising, 60% falling
PWR4 (LDO_1)	LDO_GP1_PG_FAULT / LDO_DMD1_PG_ FAULT	80% rising, 60% falling
OVER-VOLTAGE		
BLOCK	**REGISTER BIT**	**THRESHOLD** (V)
PWR1	BUCK_DMD1_OV_FAULT	Ratio: 120%
PWR2	BUCK_DMD2_OV_FAULT	Ratio: 120%
PWR3 (LDO_2)	LDO_GP2_OV_FAULT / LDO_DMD1_OV_FAULT	7
PWR4 (LDO_1)	LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT	7

7.3.4.4.1 Power Good

The DMD HV regulator, DMD buck converters, DMD LDOs, and the LDO_DMD that supports the HV regulator have a power good indication.

The DMD HV regulator is continuously monitored to check if the output rails DMD_VRESET, DMD_VOFFSET, and DMD_VBIAS are in regulation. If either one of the output rails drops out of regulation (for example, due to a shorted output or overloading), the DMD_ PG_FAULT bit in Detailed Status Register3 is set. Threshold for DMD_VRESET is 90% and the thresholds for DMD_VOFFSET/ DMD_VBIAS are 86% (rising edge) and 66% (falling edge).

The power good signal for the two DMD buck converters indicate if their output voltage (PWR1_FB and PWR2_FB) are within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set output voltage the power good bit is asserted. The power good bits are in register BUCK_DMD1_PG_FAULT and BUCK_DMD2_PG_FAULT.

DMD_LDO1 and DMD_LDO2 output voltages are also monitored. When the power good fault of the LDO is asserted it implies that the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for the LDOs is in register LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT and LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT.

The LDO_DMD used for the DMD HV regulator has its own power good signaling. The power good fault of the LDO_DMD is asserted if the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for this LDO is in register V5V5_LDO_DMD_PG_FAULT.

7.3.4.4.2 Overvoltage Fault

An overvoltage fault occurs when an output voltage rises above a pre-defined threshold. Overvoltage faults are indicated for the DMD buck converters, DMD LDOs and the LDO_DMD supporting the DMD HV regulator. The overvoltage fault of LDO1 and LDO2 are not incorporated in the overall DMD_FAULT when the LDOs are used

as general purpose LDOs. 表 7-2 provides an overview of the possible DMD overvoltage faults and their threshold levels.

7.3.5 Buck Converters

The DLPA3005 contains one general purpose buck converter and a supporting LDO (LDO_BUCKS). The programmable 8-bit buck converter can generate a voltage between 1 V and 5 V and have an output current limit of 3 A. General purpose buck2 (PWR6) is currently supported. One buck converter and the LDO_BUCKS is depicted in 图 7-15.

The two DMD/DLPC buck converters discussed earlier in 节 7.3.4 have the same architecture as these three buck converters and can be configured in the same way.

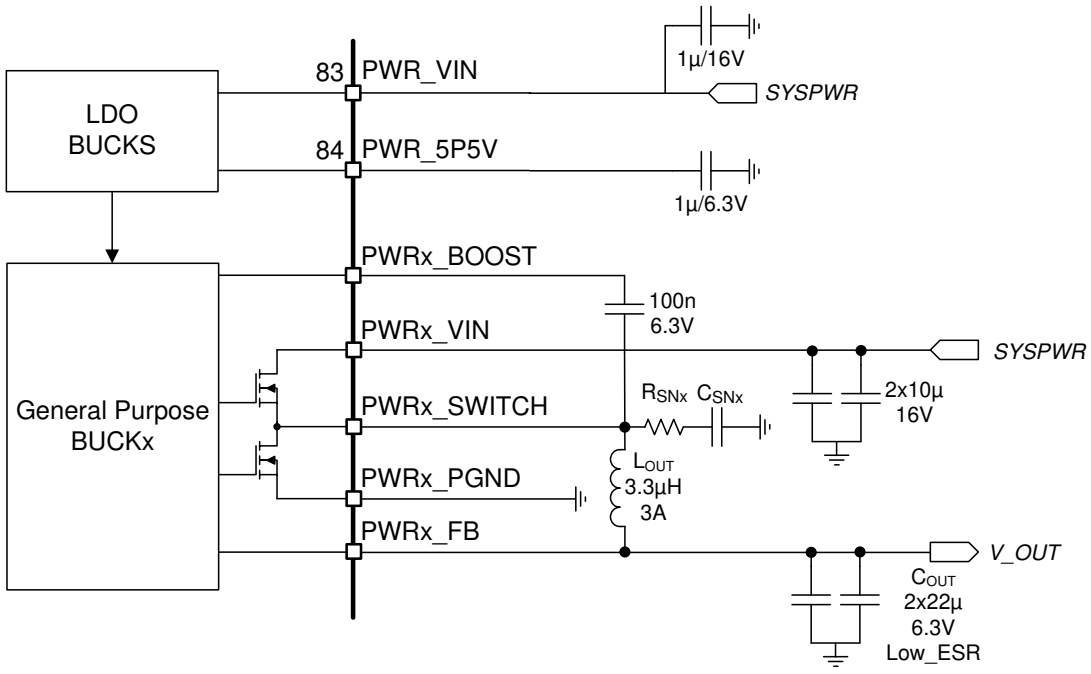


图 7-15. Buck Converter

7.3.5.1 LDO Bucks

This regulator supports the general purpose buck converter and the two DMD/DLPC buck converters, and provides an analog voltage of 5.5 V to the internal circuitry.

7.3.5.2 General Purpose Buck Converter

The Buck converter is for general purpose usage (图 7-15). The converter can be enabled or disabled through the Enable Register, 0x01 bit:

- BUCK_GP2_EN

The output voltage of the converter is configurable between 1 V and 5 V with an 8-bit resolution. This can be done through the register BUCK_GP2_TRIM.

General purpose buck2 (PWR6) has a current capability of 2 A.

The buck converter can operate in two switching modes: Normal, 600-kHz switching frequency mode and the skip mode. The skip mode is designed to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller

load current to the level of the reference voltage. The skip mode can be enabled/disabled the buck converter in register BUCK_SKIP_ON.

7.3.5.3 Buck Converter Monitoring

The buck converter block is continuously monitored for system failures to prevent damage to the DLPA3005 and peripherals. Several possible failures are monitored such as a too high or too low output voltage. The possible faults are summarized in 表 7-3.

表 7-3. Buck Converter Fault Indication

POWER GOOD		
BLOCK	**REGISTER BIT**	**THRESHOLD (RISING EDGE)**
Gen.Buck2	BUCK_GP2_PG_FAULT	Ratio 72%
OVERVOLTAGE		
Gen.Buck2	BUCK_GP2_OV_FAULT	Ratio 120%

7.3.5.3.1 Power Good

The buck converter as well as the supporting LDO_BUCK have a power good indication. The buck converter has a separate indication.

The power good for the buck converter indicate if their output voltage (PWR6_FB) is within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set voltage the PG_fault bit is set high. The power good bit of the buck converter is in the Detailed status register1 bit:

- BUCK_GP2_PG_FAULT for BUCK2 (PWR6)

The LDO_BUCKS that supports the buck converters has its own power good indication. The power good of the LDO_BUCKS is asserted if the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for the LDO_BUCKS is in Detailed status register3, V5V5_LDO_BUCK_PG_FAULT.

7.3.5.3.2 Overvoltage Fault

An overvoltage fault occurs when an output voltage rises above a predefined threshold. Overvoltage faults are indicated for the buck converter and LDO_BUCKS. The overvoltage fault of the LDO_BUCKS is asserted if the LDO voltage is above 7.2 V and can be found in register V5V5_LDO_BUCK_OV_FAULT. The overvoltage of the general purpose buck converter is 120% of the set value and can be read through the register BUCK_GP1,2,3_OV_FAULT.

7.3.5.4 Buck Converter Efficiency

图 7-16 shows an overview of the efficiency of the buck converter for an input voltage of 12 V. The efficiency is shown for several output voltage levels where the load current is swept.

图 7-17 depicts the buck converter efficiency versus input voltage (V_{IN}) for a load current (I_{OUT}) of 1 A for various output voltage levels (V_{OUT}).

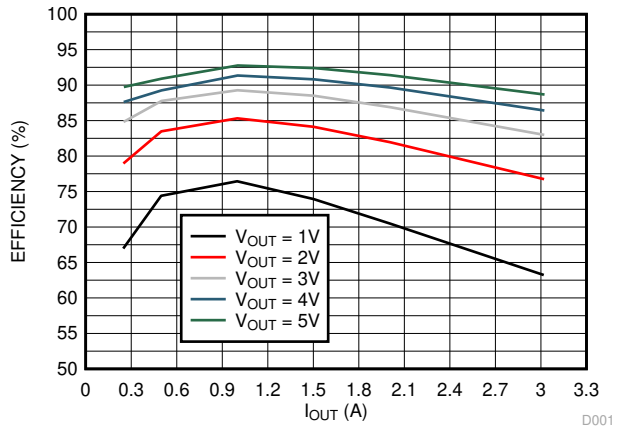


图 7-16. Buck Converter Efficiency vs I_{OUT} (V_{IN} = 12 V)

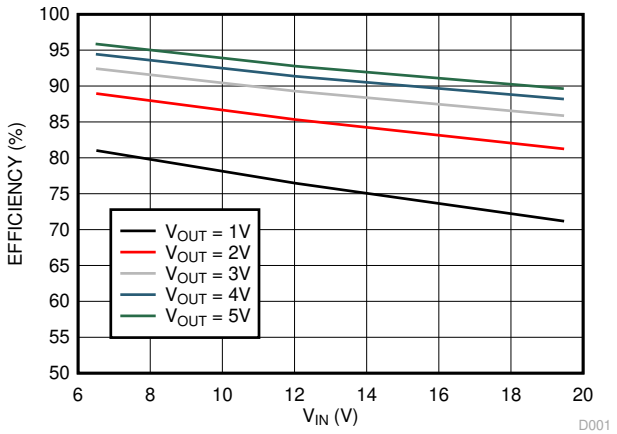


图 7-17. Buck Converter Efficiency vs V_{IN} (I_{OUT} = 1 A) Schematic

7.3.6 Auxiliary LDOs

LDO_1 and LDO_2 are the two auxiliary LDOs that can freely be used by an additional external application. All other LDOs are for internal usage only and should not be loaded. LDO1 (PWR4) is a fixed voltage of 3.3 V, while LDO2 (PWR3) is a fixed voltage of 2.5 V. Both LDOs are capable to deliver 200 mA.

7.3.7 Measurement System

The measurement system (图 7-18) is designed to sense internal and external nodes and convert them to digital by the implemented AFE comparator. The AFE can be enabled through register AFE_EN. The reference signal for this comparator, ACMPR_REF, is a low pass filtered PWM signal coming from the DLPC. To be able to cover a wide range of input signals a variable gain amplifier (VGA) is added with three gain settings (1x, 9.5x, and 18x). The gain of the VGA can be set through register AFE_GAIN. The maximum input voltage of the VGA is 1.5 V. Some of the internal voltage are too large though to be handled by the VGA and are divided down first.

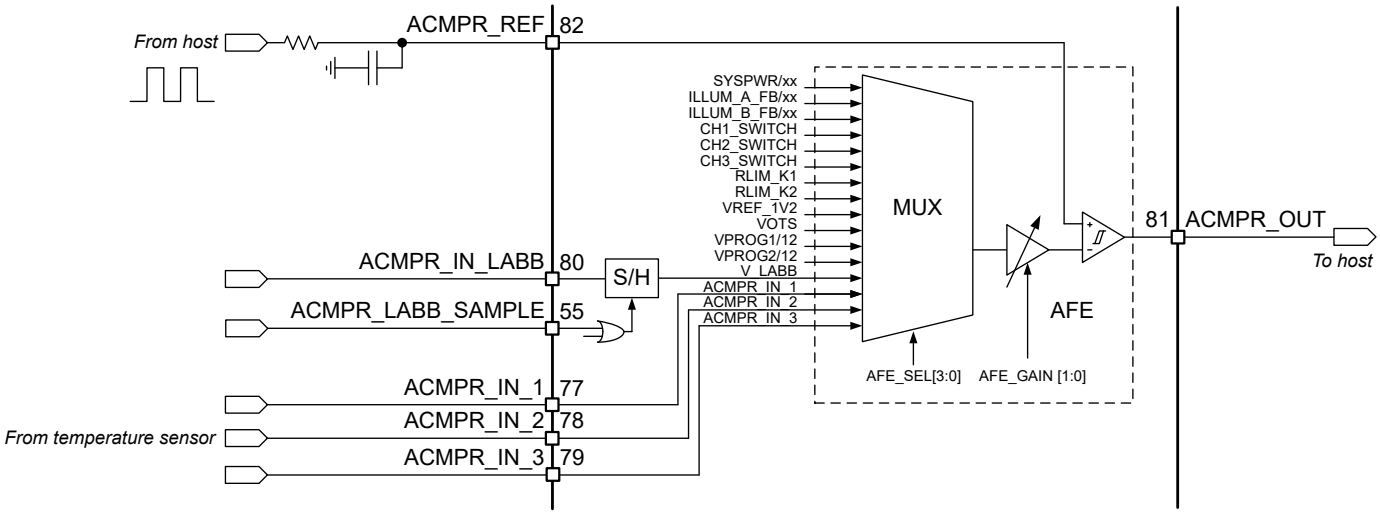


图 7-18. Measurement System Schematic

The multiplexer (MUX) connects to a wide range of nodes. Selection of the MUX input can be done through register AFE_SEL. Signals that can be selected:

- System input voltage, SYSPWR
- LED anode cathode voltage, ILLUM_A_FB
- LED cathode voltage, CHx_SWITCH

- V_R_{LIM} to measure LED current
- Internal reference, VREF_1V2
- Die Temperature represented by voltage VOTS
- EEPROM programming voltage, VPROG1,2/12
- LABB sensor, V_LABB
- External sense pins, ACMPR_IN_1,2,3

The system input voltage SYSPWR can be measured by selecting the SYSPWR/xx input of the MUX. Before the system input voltage is supplied to the MUX the voltage needs to be divided. This is because the variable gain amplifier (VGA) can handle voltages up-to 1.5 V whereas the system voltage can be as high as 20 V. The division is done internally in the DLPA3005. The division factor selection (VIN division factor) is combined with the auto LED turn off functionality of the illumination driver and can be set through register ILLUM_LED_AUTO_OFF_SEL.

The LED voltages can be monitored by measuring both the common anode of the LEDs as well as the cathode of each LED individually. The LED anode voltage (V_{LED}) is measured by sensing the feedback pin of the illumination driver (ILLUM_A_FB). Likewise the SYSPWR, the LED anode voltage needs to be divided before feeding it to the MUX. The division factor is combined with the overvoltage fault level of the illumination driver and can be set through register VLED_OVP_VLED_RATIO. The cathode voltages CH1,2,3_SWITCH are fed directly to the MUX without division factor.

The LED current can be determined knowing the value of sense resistor R_{LIM} and the voltage across the resistor. The voltage at the top-side of the sense resistor can be measured by selecting MUX-input RLIM_K1. The bottom side of the resistor is connected to GND.

VOTS is connected to an on-chip temperature sensor. The voltage is a measure for the chip’s junction temperature: Temperature (°C) = 300 × VOTS (V) – 270

For storage of trim bits, but also for the USER EEPROM bytes, the DLPA3005 has two EEPROM blocks. The programming voltage of EEPROM block 1 and 2 can be measured through MUX input VPROG1/12 and VPROGR2/12, respectively. The EEPROM programming voltage is divided by 12 before it is supplied to the MUX to prevent a too large voltage on the MUX input. The EEPROM programming voltage is about 12 V.

LABB is a feature that is Local Area Brightness Boost. LABB increases the brightness locally while maintaining good contrast and saturation. The sensor needed for this feature should be connected to pin ACMPR_IN_LABB. The light sensor signal is sampled and held such that it can be read independently of the sensor timing. To use this feature it should be ensured that:

- The AFE block is enabled (AFE_EN = 1).
- The LABB input is selected (AFE_SEL<3:0>=3h).
- The AFE gain is set appropriately to have AFE_Gain × VLABB < 1.5 V (AFE_GAIN<1:0>).

Sampling of the signal can be done through one of the following methods:

1. Writing to register TSAMPLE_SEL by specifying the sample time window and set bit SAMPLE_LABB=1 to start sampling. The SAMPLE_LABB bit is automatically reset to 0 at the end of the sample period to be ready for a next sample request.
2. Use the input ACMPR_LABB_SAMPLE-pin as a sample signal. As long as this signal is high the signal on ACMPR_IN_LABB is tracked. Once the ACMP_LABB_SAMPLE is set low again the value at that moment will be held.

ACMPR_IN_1,2,3 can measure external signals from for instance a temperature sensor. It should be ensured that the voltage on the input does not exceed 1.5 V.

7.4 Device Functional Modes

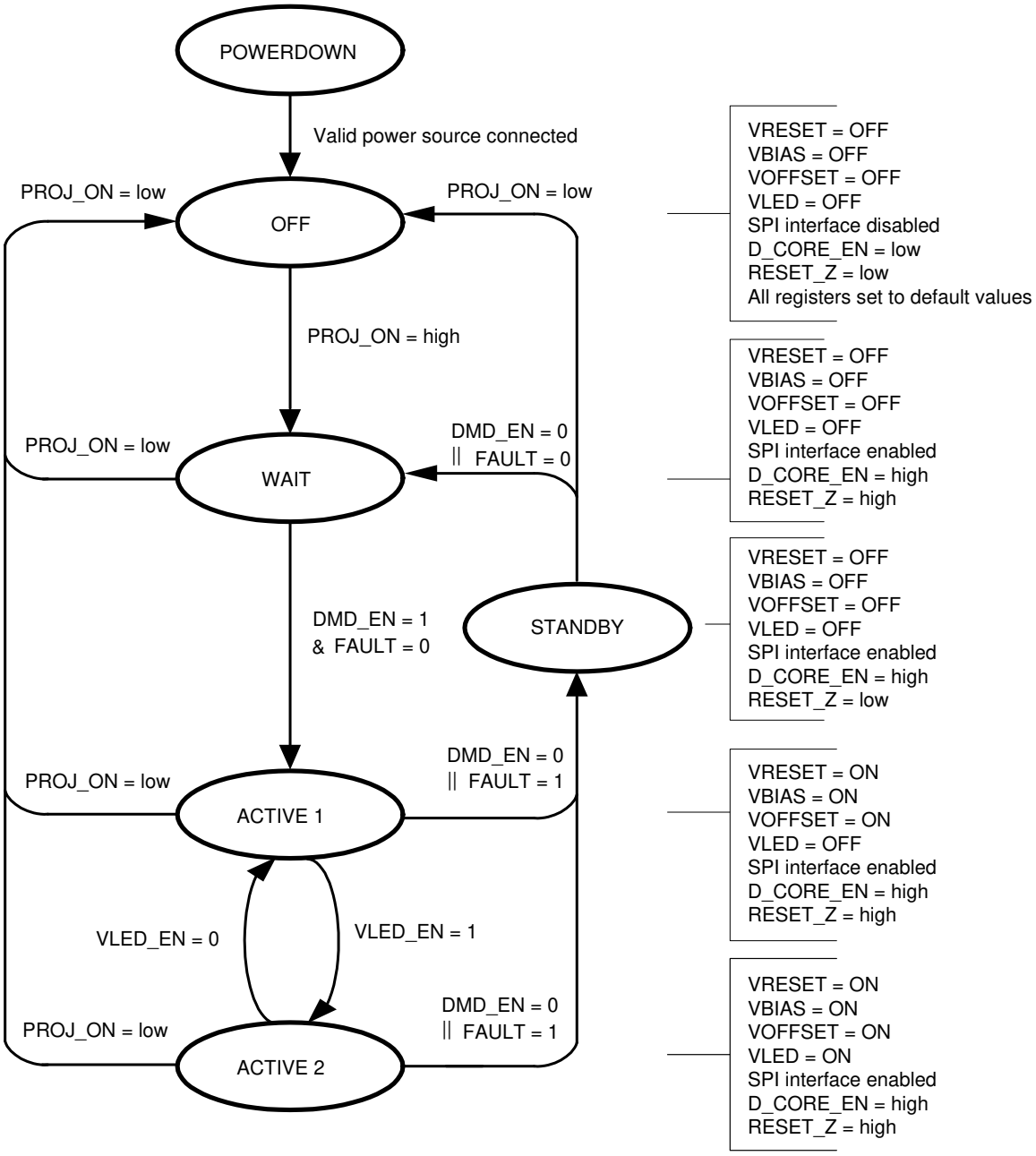
表 7-4. Modes of Operation

MODE	DESCRIPTION
OFF	This is the lowest-power mode of operation. All power functions are turned off, registers are reset to their default values, and the IC does not respond to SPI commands. RESET_Z pin is pulled low. The IC will enter OFF mode whenever the PROJ_ON pin is low.
WAIT	The DMD regulators and LED power (V_{LED}) are turned off, but the IC does respond to the SPI. The device enters WAIT mode whenever PROJ_ON is set high, DMD_EN(1) bit is set to 0 or a FAULT is resolved.
STANDBY	The device also enters STANDBY mode when a fault condition is detected(2). (See also 节 7.5.2). Once the fault condition is resolved, WAIT mode is entered.
ACTIVE1	The DMD supplies are enabled but LED power (V_{LED}) is disabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1, and ILLUM_EN(3) bit is set to 0.
ACTIVE2	DMD supplies and LED power are enabled. PROJ_ON pin must be high and DMD_EN and ILLUM_EN bits must both be set to 1.

(1) Settings can be done through register 0x01.
(2) Power-good faults, overvoltage, overtemperature shutdown, and undervoltage lockout
(3) Settings can be done through register 0x01; the bit is named ILLUM_EN.

表 7-5. Device State as a Function of Control-Pin Status

PROJ_ON Pin	STATE
LOW	OFF
HIGH	WAIT STANDBY ACTIVE1 ACTIVE2 (The device state depends on DMD_EN and ILLUM_EN bits and whether there are any fault conditions.)



A. || = OR, & = AND
B. FAULT = Undervoltage on any supply, thermal shutdown, or UVLO detection
C. UVLO detection, per the diagram, causes the DLPA3005 to go into the standby state. This is not the lowest power state. If lower power is desired, PROJ_ON should be set low.
D. DMD_EN register bit can be reset or set by SPI writes. DMD_EN defaults to 0 when PROJ_ON goes from low to high and then the DLPC ASIC software automatically sets it to 1. Also, FAULT = 1 causes the DMD_EN register bit to be reset.
E. D_CORE_EN is a signal internal to the DLPA3005. This signal turns on the VCORE regulator.

图 7-19. State Diagram

7.5 Programming

This section discusses the serial protocol interface (SPI) of the DLPA3005 as well as the interrupt handling, device shutdown and register protection.

7.5.1 SPI

The DLPA3005 provides a 4-wire SPI port that supports two SPI clock frequency modes: 0 MHz to 36 MHz and 20 MHz to 40 MHz. The clock frequency mode can be set in register DIG_SPI_FAST_SEL. The interface supports both read and write operations. The SPI_SS_Z input serves as the active low chip select for the SPI port. The SPI_SS_Z input must be forced low for writing to or reading from registers. When SPI_SS_Z is forced high, the data at the SPI_MOSI input is ignored, and the SPI_MISO output is forced to a high-impedance state. The SPI_MOSI input serves as the serial data input for the port; the SPI_MISO output serves as the serial data output. The SPI_CLK input serves as the serial data clock for both the input and output data. Data at the SPI_MOSI input is latched on the rising edge of SPI_CLK, while data is clocked out of the SPI_MISO output on the falling edge of SPI_CLK. 图 7-20 illustrates the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit is the write/not-read bit. For the W/nR bit, a 1 indicates a write operation, while a 0 indicates a read operation. The remaining seven bits of the command byte are the register address targeted by the write or read operation. The SPI port supports write and read operations for multiple sequential register addresses through the implementation of an auto-increment mode. As shown in 图 7-20, the auto-increment mode is invoked by simply holding the SPI_SS_Z input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte. After reaching address 0x7Fh the address pointer jumps back to 0x00h.

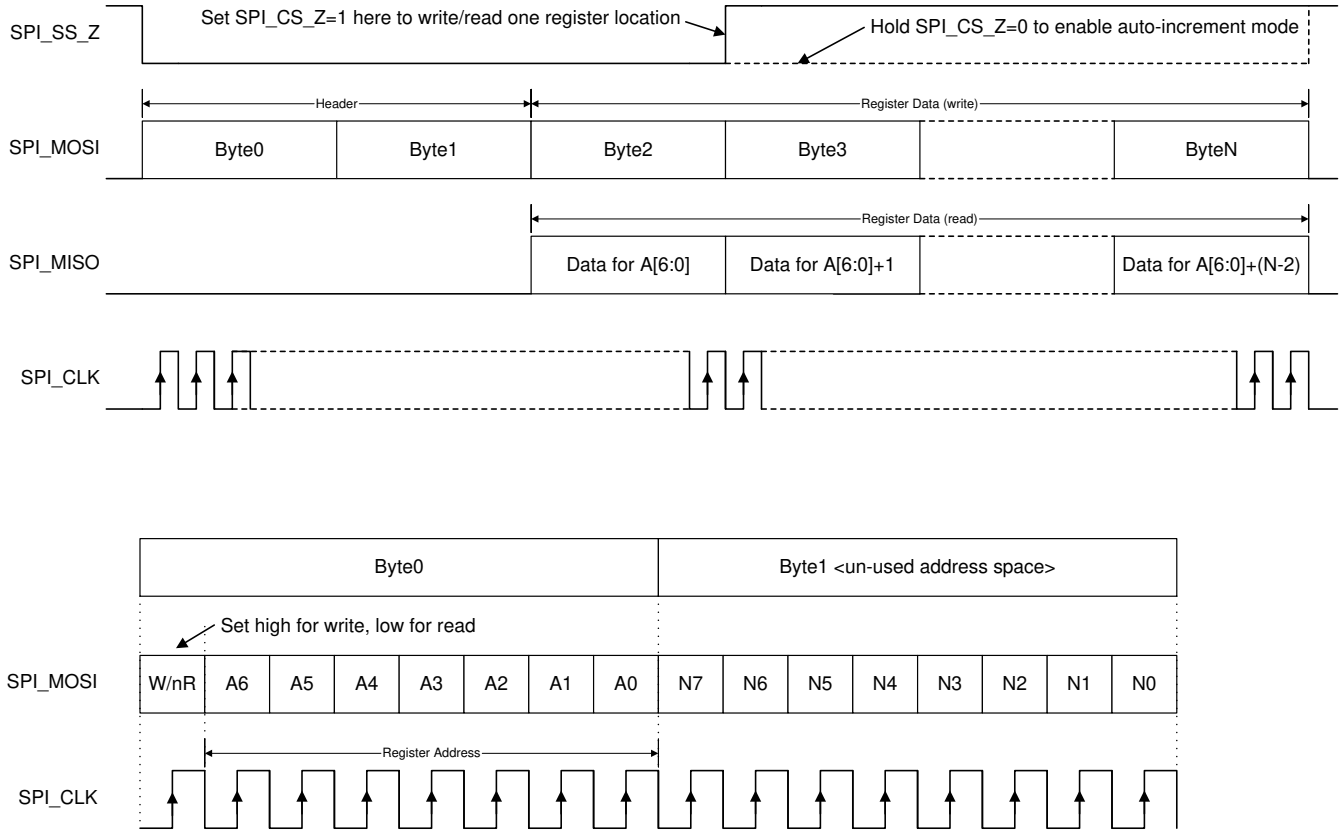


图 7-20. SPI Protocol

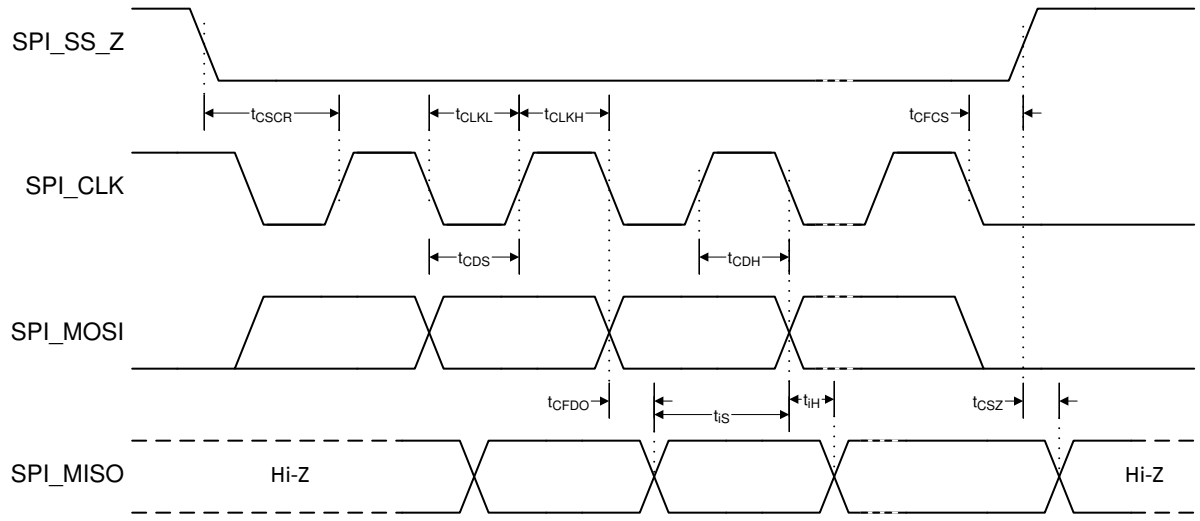


图 7-21. SPI Timing Diagram

7.5.2 Interrupt

The DLPA3005 has the capability to flag for several faults in the system, such as overheating, power good and over voltage faults. If a certain fault condition occurs one or more bits in the interrupt register will be set. The setting of a bit in the Main Status register triggers an interrupt event, which pulls down the INT_Z pin. Interrupts can be masked by setting the respective MASK bits in the Interrupt Mask register. Setting a MASK bit prevents the INT_Z from being pulled low for the particular fault condition. Some high-level faults comprise multiple low-level faults. The high-level faults can be read in Main Status register, while the lower-level faults can be read in Detailed status register1 through Detailed status register 4. 表 7-6 provides an overview of the faults and how they are related.

表 7-6. Interrupt Registers

HIGH-LEVEL	MID-LEVEL	LOW-LEVEL
SUPPLY_FAULT	DMD_FAULT	DMD_PG_FAULT
		BUCK_DMD1_PG_FAULT
		BUCK_DMD1_OV_FAULT
		BUCK_DMD2_PG_FAULT
		BUCK_DMD2_OV_FAULT
		LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT
		LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT
		LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT
		LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT
	BUCK_GP2_PG_FAULT	
	BUCK_GP2_OV_FAULT	
ILLUM_FAULT	ILLUM_BC1_PG_FAULT	
	ILLUM_BC1_OV_FAULT	
	ILLUM_BC2_PG_FAULT	
	ILLUM_BC2_OV_FAULT	
PROJ_ON_INT		
TS_SHUT		
TS_WARN		

7.5.3 Fast-Shutdown in Case of Fault

The DLPA3005 has two shutdown modes: a normal shutdown initiated after pulling PROJ_ON level low and a fast power-down mode. The fast power down feature can be enabled/disabled through register 0x01, FAST_SHUTDOWN_EN. By default, the mode is enabled.

When the fast power-down feature is enabled, a fast shutdown is initiated for specific faults. This shutdown happens autonomously from the DLPC. The DLPA3005 enters the fast-shutdown mode only for specific faults; thus, not for all the faults flagged by the DLPA3005. The faults for which the DLPA3005 goes into fast-shutdown are listed in 表 7-7.

表 7-7. Faults that Trigger a Fast-Shutdown

HIGH-LEVEL	LOW-LEVEL
BAT_LOW_SHUT	
TS_SHUT	
DMD_FAULT	DMD_PG_FAULT
	BUCK_DMD1_PG_FAULT
	BUCK_DMD1_OV_FAULT
	BUCK_DMD2_PG_FAULT
	BUCK_DMD2_OV_FAULT
	LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT
	LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT
	LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT
	LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT
ILLUM_FAULT	ILLUM_BC1_OV_FAULT
	ILLUM_BC2_OV_FAULT

7.5.4 Protected Registers

By default all regular USER registers are writable, except for the READ ONLY registers. Registers can be protected though to prevent accidental write operations. By enabling the protecting, only USER registers are writable. Protection can be enabled/ disabled through register PROTECT_USER_REG.

7.6 Register Maps

Register Address, Default, R/W, Register name. **Boldface** settings are the hardwired defaults.

表 7-8. Register Map

NAME	BITS	DESCRIPTION
0x00, E3, R/W, Chip Identification		
CHIPID	[7:4]	Chip identification number: E (hex)
REVID	[3:0]	Revision number, 3 (hex)
0x01, 82, R/W, Enable Register		
FAST_SHUTDOWN_EN	[7]	0: Fast shutdown disabled **1: Fast shutdown enabled**
CW_EN	[6]	Reserved
BUCK_GP2_EN	[4]	**0: General purpose buck2 disabled** 1: General purpose buck2 enabled
ILLUM_LED_AUTO_OFF_EN	[2]	**0: Illum_led_auto_off_en disabled** 1: Illum_led_auto_off_en enabled
ILLUM_EN	[1]	0: Illum regulators disabled **1: Illum regulators enabled**
DMD_EN	[0]	**0: DMD regulators disabled** 1: DMD regulators enabled
0x02, 70, R/W, IREG Switch Control		
	[7]	Reserved, values don't care
ILLUM_ILIM	[6:3]	Rlim voltage top-side (mV). Illum current limit = Rlim voltage / Rlim 0000: 17 / 1000: 73 0001: 20 / 1001: 88 0010: 23 / 1010: 102 0011: 25 / 1011: 117 0100: 29 / 1100: 133 0101: 37 / 1101: 154 0110: 44 / **1110: 176** 0111: 59 / 1111: 197
ILLUM_SW_ILIM_EN	[2:0]	Bit2: CH3, MOSFET R transient current limit (**0:disabled**, 1:enabled) Bit1: CH2, MOSFET Q transient current limit (**0:disabled**, 1:enabled) Bit0: CH1, MOSFET P transient current limit (**0:disabled**, 1:enabled)
0x03, 00, R/W, SW1_IDAC(1)		
	[7:2]	Reserved, values don't care
SW1_IDAC<9:8>	[1:0]	Led current of CH1(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x03 and 0x04). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]

表 7-8. Register Map (continued)

NAME	BITS	DESCRIPTION
0x04, 00, R/W, SW1_IDAC(2)		
SW1_IDAC<7:0>	[7:0]	Led current of CH1(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x03 and 0x04). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x05, 00, R/W, SW2_IDAC(1)		
	[7:2]	Reserved, value don’t care.
SW2_IDAC<9:8>	[1:0]	Led current of CH2(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x05 and 0x06). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x06, 00, R/W, SW2_IDAC(2)		
SW2_IDAC<7:0>	[7:0]	Led current of CH2(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x05 and 0x06). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x07, 00, R/W, SW3_IDAC(1)		
	[7:2]	Reserved, value don’t care.
SW3_IDAC<9:8>	[1:0]	Led current of CH3(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x07 and 0x08). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]
0x08, 00, R/W, SW3_IDAC(2)		
SW3_IDAC<7:0>	[7:0]	Led current of CH3(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x07 and 0x08). **00 0000 0000 [OFF]** 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. …. 11 1111 1111 [150mV/Rlim]

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

In display applications, using the DLPA3005 provides all needed analog functions including all analog power supplies and the RGB LED driver (up to 16 A per LED and up to 32 A for series LEDs) to provide a robust and efficient display solution. Each DLP application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC3439 DLP controller chips.

8.2 Typical Application

A common application when using DLPA3005 is to use it with a 0.47 1080 DMD (DLP4710) and two DLPC3439 controllers for creating a small, ultra-portable projector. The DLPC3439s in the projector typically receive images from a PC or video player using HDMI or VGA analog as shown in 图 8-1. Card readers and Wi-Fi can also be used to receive images if the appropriate peripheral chips are added. The DLPA3005 provides power supply sequencing and control of the RGB LED currents as required by the application.

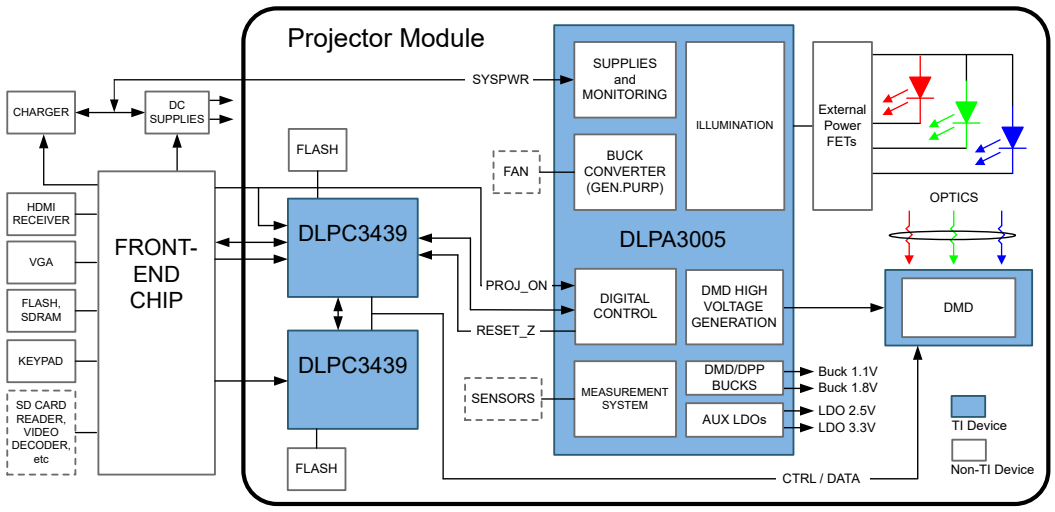


图 8-1. Typical Setup Using DLPA3005

8.2.1 Design Requirements

An ultra-portable projector can be created by using a DLP chip set comprised of a 0.47 1080 DMD (DLP4710), two DLPC3439s controllers, and the DLPA3005 PMIC/LED Driver. The two DLPC3439s do the digital image processing, the DLPA3005 provides the needed analog functions for the projector, and DMD is the display device for producing the projected image. In addition to the three DLP chips in the chip set, other chips may be needed. At a minimum a Flash part is needed to store the software and firmware to control the two DLPC3439s. The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the projector. Power FETs are needed external to the DLPA3005 so that high LED currents can be supported. For connecting the two DLPC3439s to the front end chip for receiving images the parallel interface is typically used. While using the parallel interface, I^2C should be connected to the front end chip for inputting commands to the two DLPC3439s.

The DLPA3005 has three built-in buck switching regulators to serve as projector system power supplies. Two of the regulators are fixed to 1.1 V and 1.8 V for powering the DLP chip set. The remaining one buck regulator is available for general purpose use and its voltage is programmable. The regulator can be used to drive variable-

speed fan or to power other projector chips such as the front-end chip. The only power supply needed at the DLPA3005 input is SYSPWR from an external DC power supply. The entire projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR.

8.2.2 Detailed Design Procedure

To connect the 0.47 1080 DMD (DLP4710), two DLPC3439s, and DLPA3005, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve reliable projector operation. The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

The component selection of the buck converter is mainly determined by the output voltage. 表 8-1 shows the recommended value for inductor L_{OUT} and capacitor C_{OUT} for a given output voltage.

表 8-1. Recommended Buck Converter L_{OUT} and C_{OUT}

V_{OUT} (V)	L_{OUT} (µH)			C_{OUT} (µF)	
	MIN	TYP	MAX	MIN	MAX
1 – 1.5	1.5	2.2	4.7	22	68
1.5 – 3.3	2.2	3.3	4.7	22	68
3.3 – 5	3.3		4.7	22	68

The inductor peak-to-peak ripple current, peak current and RMS current can be calculated using 方程式 8, 方程式 9 and 方程式 10 respectively. The inductor saturation current rating must be greater than the calculated peak current. Likewise, the RMS or heating current rating of the inductor must be greater than the calculated RMS current. The switching frequency of the buck converter is approximately 600 kHz (f_{SWITCH}).

$$I_{L\_OUT\_RIPPLE\_P-P} = \frac{\frac{V_{OUT}}{V_{IN\_MAX}} \cdot (V_{IN\_MAX} - V_{OUT})}{L_{OUT} \cdot f_{SWITCH}} \tag{8}$$

$$I_{L\_OUT\_PEAK} = I_{L\_OUT} + \frac{I_{L\_OUT\_RIPPLE\_P-P}}{2} \tag{9}$$

$$I_{L\_OUT(RMS)} = \sqrt{I_{L\_OUT}^{2} + \frac{1}{12} \cdot I_{L\_OUT\_RIPPLE\_P-P}^{2}} \tag{10}$$

The capacitor value and ESR determines the level of output voltage ripple. The buck converter is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22 to 68 µF. 方程式 11 can be used to determine the required RMS current rating for the output capacitor.

$$I_{C\_OUT(RMS)} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_{OUT} \cdot f_{SWITCH}} \tag{11}$$

Two other components need to be selected in the buck converter configuration. The value of the input-capacitor (pin PWRx_VIN) should be equal or greater than halve the selected output capacitance C_{OUT}. In this case C_{IN} 2 × 10 µF is sufficient. The capacitor between PWRx_SWITCH and PWRx_BOOST is a charge pump capacitor to drive the high side FET. The recommended value is 100 nF.

Since the switching edges of the buck converter are relatively fast, voltage overshoot and ringing can become a problem. To overcome this problem a snubber network is used. The snubber circuit consists of a resistor and capacitor that are connected in series from the switch node to ground. The snubber circuit is used to damp the parasitic inductances and capacitances during the switching transitions. This circuit reduces the ringing voltage

and also reduces the number of ringing cycles. The snubber network is formed by RSNx and CSNx. More information on controlling switch-node ringing in synchronous buck converters and configuring the snubber can be found in *Analog Applications Journal*.

8.2.2.1 Component Selection for General-Purpose Buck Converters

The theory of operation of a buck converter is explained in *Understanding Buck Power Stages in Switchmode Power Supplies Application Note*. This section is limited to the component selection. For proper operation, selection of the external components is very important, especially the inductor L_{OUT} and the output capacitor C_{OUT}. For best efficiency and ripple performance, an inductor and capacitor should be chosen with low equivalent series resistance (ESR).

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents as shown in 图 8-2. For the LED currents shown, it’s assumed that the same current amplitude is applied to the red, green, and blue LEDs. The thermal solution used to heatsink the red, green, and blue LEDs can significantly alter the curve shape shown.

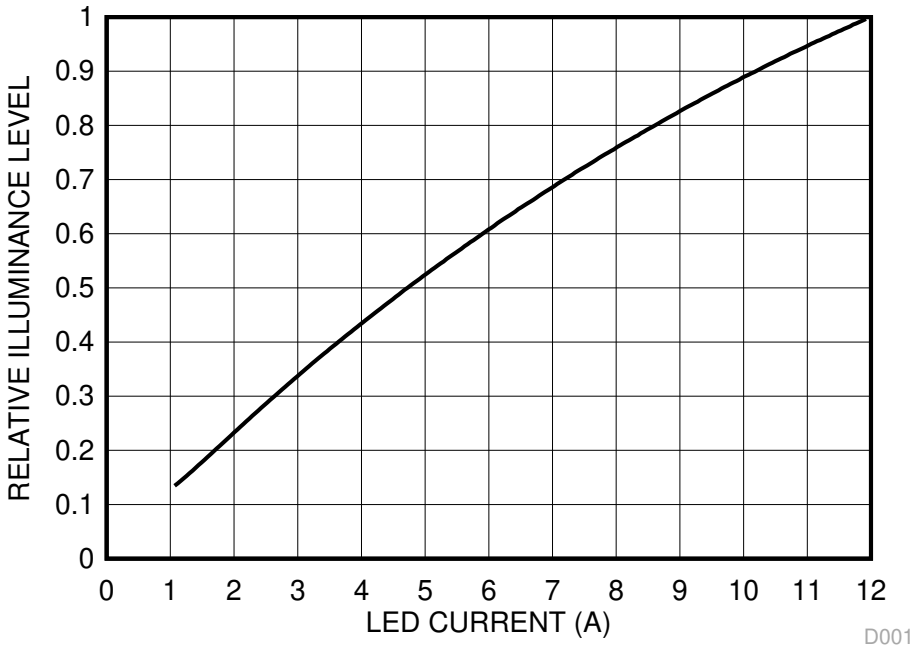


图 8-2. Luminance vs LED Current

8.3 System Example With DLPA3005 Internal Block Diagram

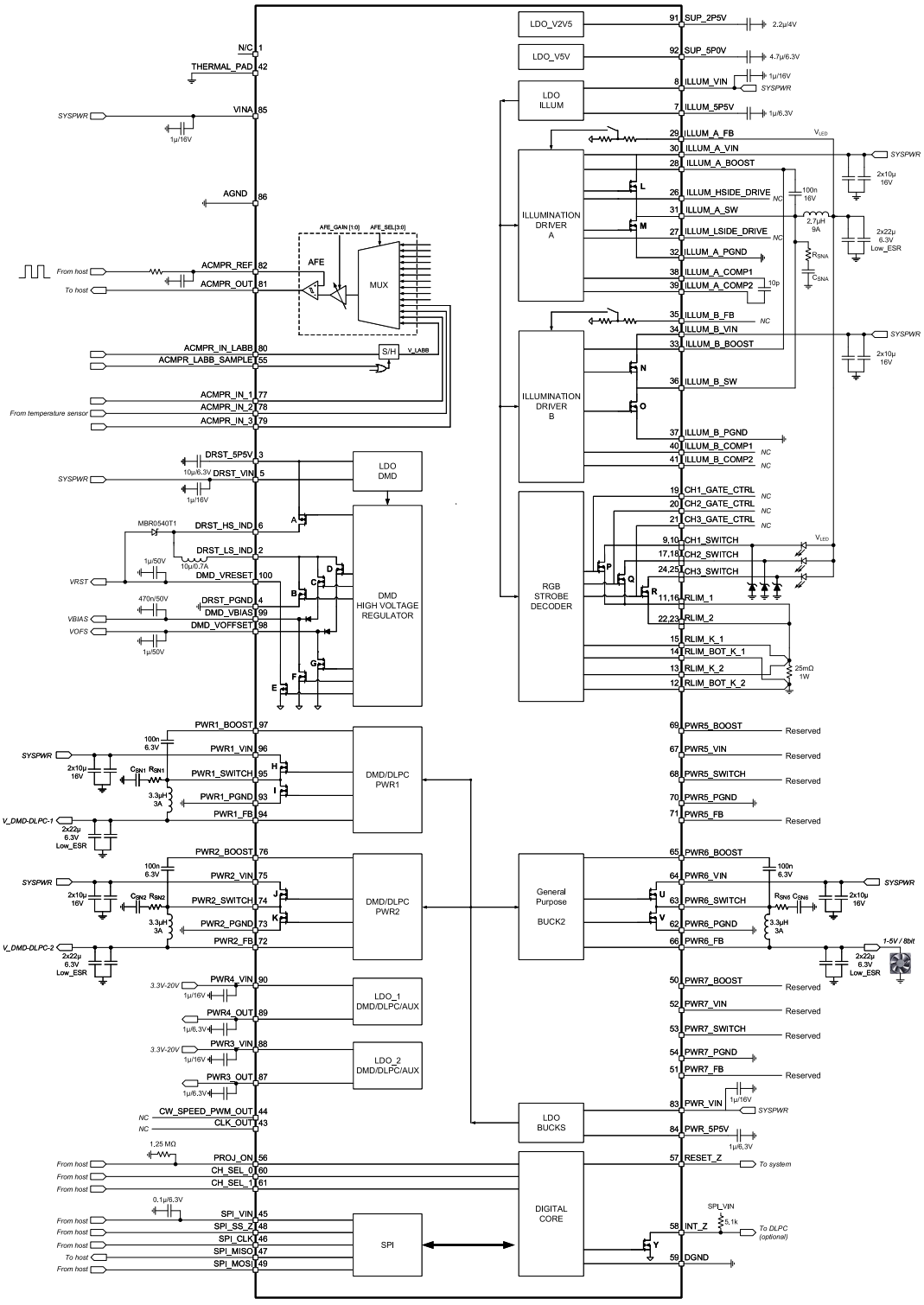


图 8-3. Typical Application: V_{IN} = 12 V, I_{OUT} = 16 A, LED

9 Power Supply Recommendations

The DLPA3005 is designed to operate from a 6 V to 20 V input voltage supply. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminals, or supply peak current limitations, additional bulk capacitance may be required. In the case ringing that is caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum type capacitor may be needed for damping.

The amount of bulk capacitance required should be evaluated such that the input voltage can remain in spec long enough for a proper fast shutdown to occur for the VOFFSET, VRESET, and VBIAS supplies. The shutdown begins when the input voltage drops below the programmable UVLO threshold such as when the external power supply is suddenly removed from the system.

9.1 Power-Up and Power-Down Timing

The power-up and power-down sequence is important to ensure a correct operation of the DLPA3005 and to prevent damage to the DMD. The DLPA3005 controls the correct sequencing of the DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET to ensure a reliable operation of the DMD.

The general startup sequence of the supplies is described earlier in 节 7.3.1 . The power-up sequence of the high voltage DMD lines is especially important in order not to damage the DMD. A too large delta voltage between DMD_VBIAS and DMD_VOFFSET could cause the damage and should therefore be prevented.

After PROJ_ON is pulled high, the DMD buck converters and LDOs are powered (PWR1-4) the DMD high voltage lines (HV) are sequentially enabled. First, DMD_VOFFSET is enabled. After a delay VOFS_STATE_DURATION, DMD_VBIAS is enabled. Finally, again after a delay VBIAS_STATE_DURATION, DMD_VRESET is enabled. Now the DLPA3005 is fully powered and ready for starting projection.

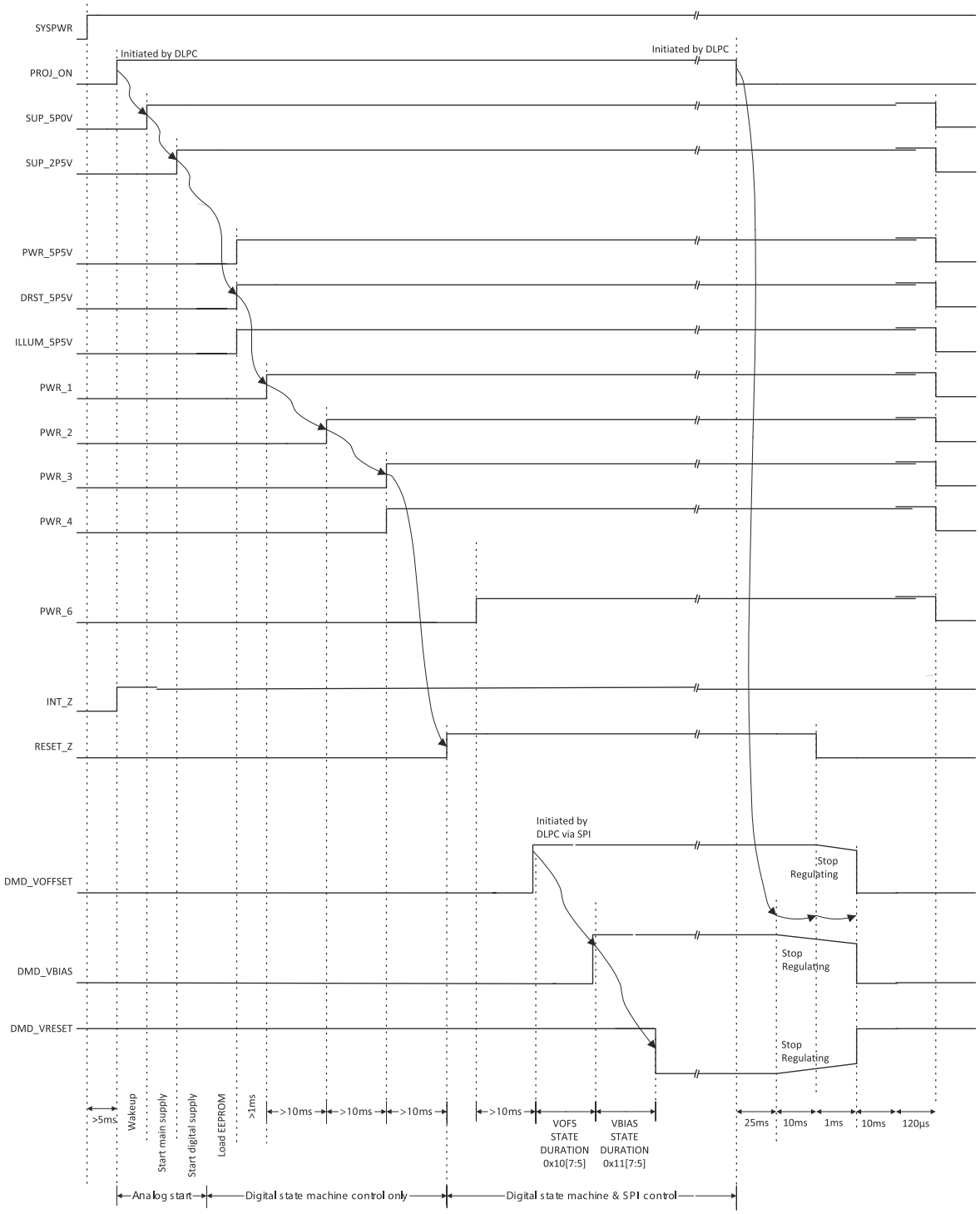
For power down there are two sequences, normal power down (图 9-1) and a fault fast power down used in case a fault occurs (图 9-2).

In normal power down mode, the power down is initiated after pulling PROJ_ON pin low. 25 ms after PROJ_ON is pulled low, first DMD_VBIAS and DMD_VRESET stop regulating, 10 ms later followed by DMD_VOFFSET. When DMD_VOFFSET stopped regulating, RESET_Z is pulled low. 1 ms after the DMD_VOFFSET stopped regulating, all three voltages are discharged. Finally, all other supplies are turned off. INT_Z remains high during the power down sequence since no fault occurred. During power down it is ensured that the HV levels do not violate the DMD specifications on these three lines. For this it is important to select the capacitors such that $C_{VOFFSET}$ is equal to C_{VRESET} and C_{VBIAS} is $\leqslant C_{VOFFSET}$, C_{VRESET}.

The fast power down mode (图 9-2) is started in case a fault occurs (INT_Z will be pulled low), for instance due to overheating. The fast power down mode can be enabled / disabled through register 0x01, FAST_SHUTDOWN_EN. By default the mode is enabled. After the fault occurs, regulation of DMD_VBIAS and DMD_VRESET is stopped. The time (delay) between fault and stop of regulation can be controlled through register VBIAS/VRST_DELAY. The delay can be selected between 4 µs and ≅1.1 ms, where the default is ≅540 µs. A defined delay-time after the regulation stopped, all three high voltages lines are discharged and RESET_Z is pulled low. The delay can be controlled through register VOFS/VRESETZ_DELAY. Delay can be selected between 4 µs and ≅1.1ms. The default is ≅4 µs. Finally the internal DMD_EN signal is pulled low.

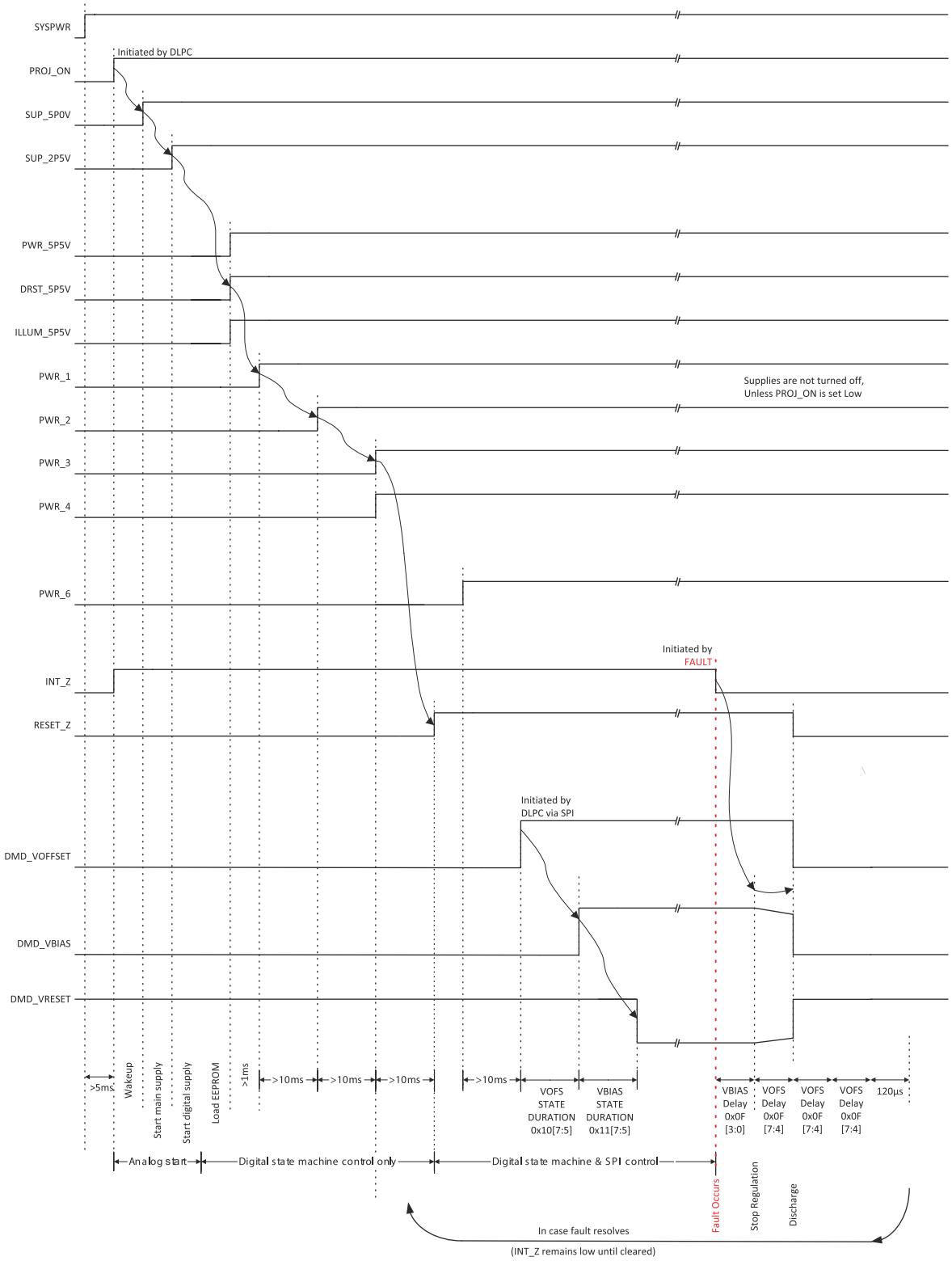
The DLPA3005 is now in a standby state. It remains in standby state until the fault resolves. In case the fault resolves, a restart is initiated. It starts then by powering-up PWR_3 and follows the regular power up, as

depicted in 图 9-2. For proper discharge timing and levels, select the capacitors such that $C_{VOFFSET}$ is equal to C_{VRESET} and C_{VBIAS} is ⩽ $C_{VOFFSET}$, C_{VBIAS}.



1. Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.
2. SUP_5P0V and SUP_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ_ON is pulled high.

图 9-1. Power Sequence Normal Shutdown Mode



1. Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.
2. SUP_5P0V and SUP_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ_ON is pulled high.

图 9-2. Power Sequence Fault Fast Shutdown Mode

10 Layout

10.1 Layout Guidelines

For switching power supplies, the layout is an important step in the design, especially when it concerns high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability issues and/or EMI problems. Therefore, it is recommended to use wide and short traces for high current paths and for their return power ground paths. For the DMD HV regulator, the input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. In order to minimize ground noise coupling between different buck converters it is advised to separate their grounds and connect them together at a central point under the part. For the DMD HV regulator, the recommended value for the capacitors is 1 µF for VRST and VOFS, 470 nF for VBIAS. The inductor value is 10 µH.

The high currents of the buck converter concentrate around pins VIN, SWITCH and PGND (图 10-1). The voltage at the pins VIN, PGND and FB are DC voltages while the pin SWITCH has a switching voltage between VIN and PGND. In case the FET between pins 63 – 64 is closed the red line indicates the current flow while the blue line indicates the current flow when the FET between pins 62 – 63 is closed.

These paths carry the highest currents and must be kept as short as possible.

For the LDO DMD, it is recommended to use a 1 µF/16 V capacitor on the input and a 10 µF/6.3 V capacitor on the output of the LDO.

For LDO bucks, it is recommended to use a 1 µF/16 V capacitor on the input and a 1 µF/6.3 V capacitor on the output of the LDO.

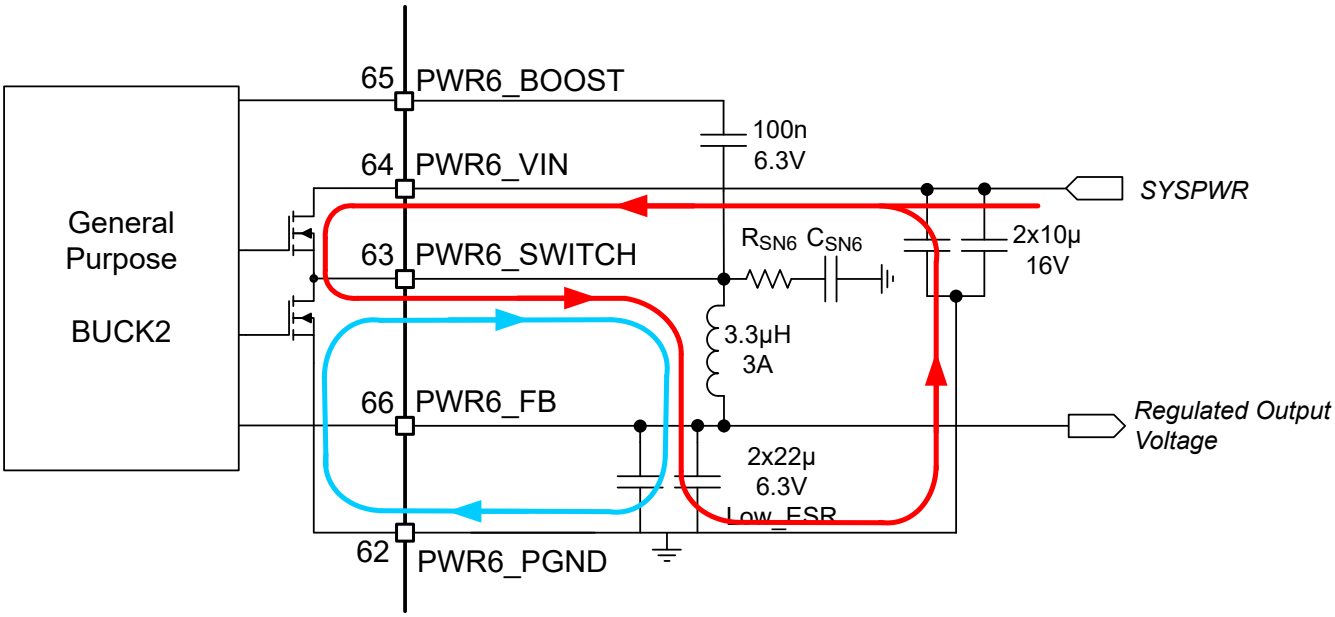


图 10-1. High AC Current Paths in a Buck Converter

The trace to the VIN pin carries high AC currents. Therefore, the trace should be low resistive to prevent voltage drop across the trace. Additionally, the decoupling capacitors should be placed as close to the VIN pin as possible.

The SWITCH pin is connected alternately to the VIN or GND. This means a square wave voltage is present on the SWITCH pin with an amplitude of VIN, and containing high frequencies. This can lead to EMI problems if not properly handled. To reduce EMI problems, a snubber network (RSN6 and CSN6) is placed at the SWITCH pin to prevent and/or suppress unwanted high frequency ringing at the moment of switching.

The PGND pin sinks high current and should be connected to a star ground point such that it does not interfere with other ground connections.

The FB pin is the sense connection for the regulated output voltage which is a DC voltage; no current is flowing through this pin. The voltage on the FB pin is compared with the internal reference voltage in order to control the loop. The FB connection should be made at the load such that I•R drop is not affecting the sensed voltage.

10.1.1 SPI Connections

The SPI interface consists of several digital lines and the SPI supply. If routing of the interface lines is not done properly, communication errors can occur. It should be prevented that SPI lines can pickup noise and possible interfering sources should be kept away from the interface.

Pickup of noise can be prevented by ensuring that the SPI ground line is routed together with the digital lines as much as possible to the respective pins. The SPI interface should be connected by a separate own ground connection to the DGND of the DLPA3005 (图 10-2). This prevents ground noise between SPI ground references of DLPA3005 and DLPC due to the high current in the system.

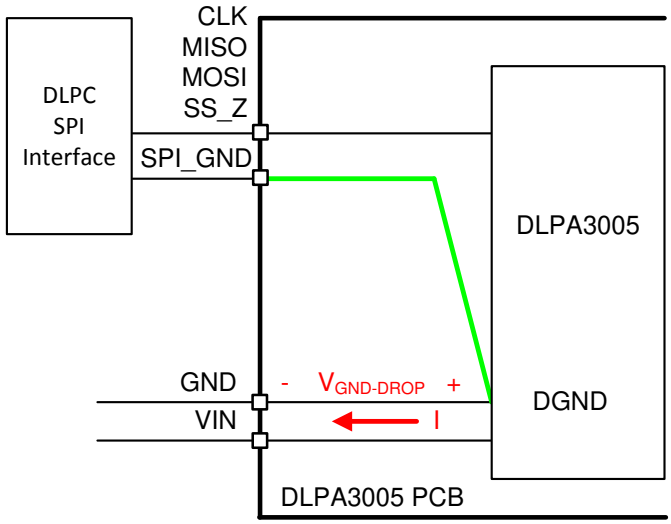


图 10-2. SPI Connections

Interfering sources should be kept away from the interface lines as much as possible. If any power lines are routed too close to the SPI_CLK it could lead to false clock pulses and, thus, communication errors.

10.1.2 R_{LIM} Routing

RLIM is used to sense the LED current. To accurately measure the LED current, the RLIM _K_1,2 lines should be connected close to the top-side of measurement resistor RLIM, while RLIM_BOT_K_1,2 should be connected close to the bottom-side of RLIM. RLIM _K_1,2 and RLIM_BOT_K_1,2 should all have separate traces from their IC pins to their RLIM connection point.

The switched LED current is running through RLIM. Therefore, low-ohmic power and ground connections for RLIM are strongly advised.

10.1.3 LED Connection

High switching currents run through the wiring connecting the external RGB switches and the LEDs. Therefore special attention needs to be paid here. Two perspectives apply to the LED-to-RGB switches wiring:

1. The resistance of the wiring, R_{series}
2. The inductance of the wiring, L_{series}

The location of the parasitic series impedances is depicted in 图 10-3.

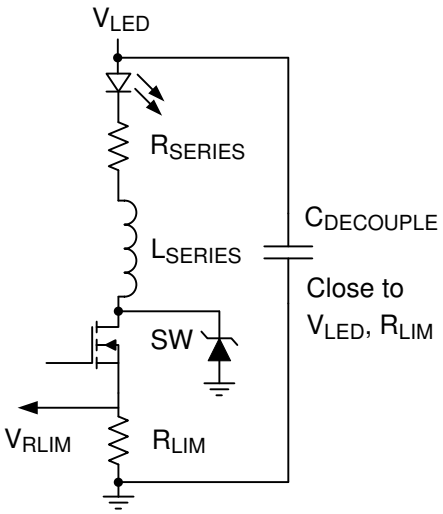


图 10-3. Parasitic Inductance (L_{Series}) and Resistance (R_{series}) in Series with LED

Currents up to 16 A can run through the wires connecting the LEDs to the RGB switches. Some noticeable dissipation can be caused. Every 10 mΩ of series resistances implies for 16 A average LED current a parasitic power dissipation of 2.5 W. This might cause PCB heating, but more important overall system efficiency is deteriorated.

Additionally the resistance of the wiring might impact the control dynamics of the LED current. It should be noted that the routing resistance is part of the LED current control loop. The LED current is controlled by V_{LED}. For a small change in V_{LED} (ΔV_{LED}) the resulting LED current variation (ΔI_{LED}) is given by the total differential resistance in that path, as:

(12)

$$\Delta I_{LED} = \frac{\Delta V_{LED}}{r_{LED} + R_{series} + R_{on\_SW\_Q3,Q4,Q5} + R_{LIM}}$$

where

- r_{LED} is the differential resistance of the LED.
- $R_{on\_SW\_P,Q,R}$ the on resistance of the strobe decoder switch.

In this expression L_{series} is ignored since realistic values are usually sufficiently low to cause any noticeable impact on the dynamics.

All the comprising differential resistances are in the range of 12.5 mΩ to several 100's mΩ. Without paying special attention a series resistance of 100 mΩ can easily be obtained. It is advised to keep this series resistance sufficiently low, that is, <10 mΩ.

The series inductance plays an important role when considering the switched nature of the LED current. While cycling through R,G and B LEDs, the current through these branches is turned-on and turned-off in short time duration. Specifically turning off is fast. A current of 16 A goes to 0 A in a matter of 50 ns. This implies a voltage spike of about 1 V for every 5 nH of parasitic inductance. It is recommended to minimize the series inductance of the LED wiring by:

- Short wires
- Thick wires / Multiple parallel wires
- Small enclosed area of the forward and return current path

If the inductance cannot be made sufficiently low, a Zener diode needs to be used to clamp the drain voltage of the RGB switch such it does not surpass the absolute maximum rating. The clamping voltage need to be chosen

between the maximum expected V_{LED} and the absolute maximum rating. Take care of sufficient margin of the clamping voltage relative to the mentioned minimum and maximum voltage.

10.2 Layout Example

A layout example of a buck converter is shown in 图 10-4, illustrating the optimal routing and placement of components around the DLPA3005. This can be used as a reference for a general purpose buck2 (PWR6). The layout example illustrates the inductor and its accompanying capacitors as close as possible to their corresponding pins using the thickest possible traces. The capacitors use multiple vias to the ground layer to ensure a low resistance path and minimizes the distance between the ground connections of the output capacitors and the ground connections of the buck converter.

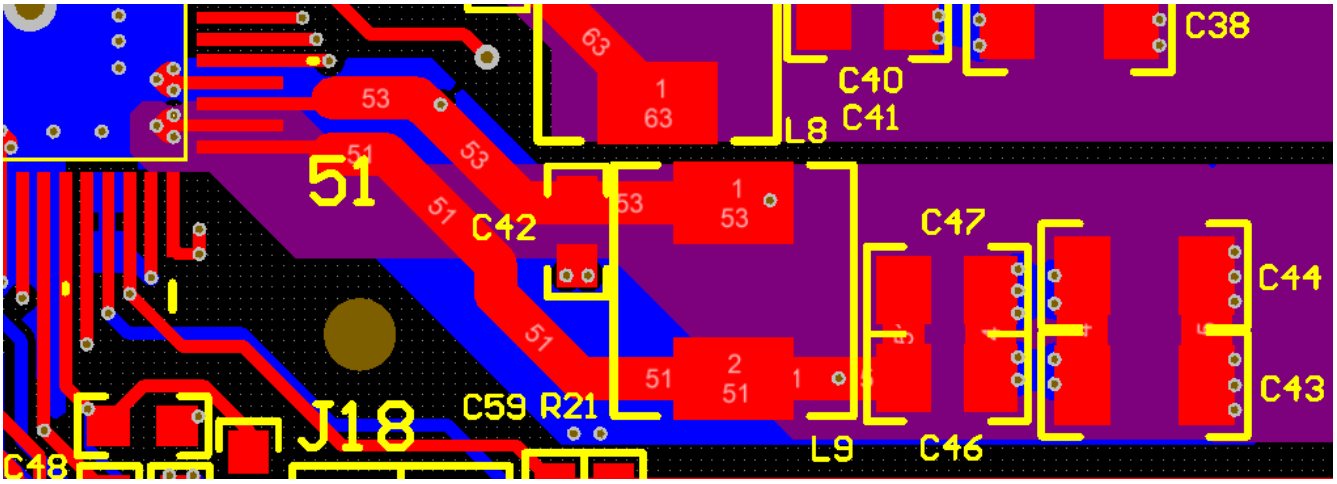


图 10-4. Practical Layout

A proper layout requires short traces and separate power grounds to avoid losses from trace resistance and to avoid ground shifting. Use high quality capacitors with low ESR to keep capacitor losses minimal and to maintain an acceptable voltage ripple at the output.

Use a RC snubber network to avoid EMI that can occur when switching high currents at high frequencies. The EMI may have a higher amplitude and frequency than the switching voltage.

10.3 Thermal Considerations

Power dissipation must be considered when implementing integrated circuits in low-profile and fine-pitch surface-mount packages. Many system related issues may affect power dissipation: thermal coupling, airflow, adding heat sinks and convection surfaces, and the presence of other heat-generating components. In general, there are three basic methods that can be used to improve thermal performance:

- Improve the heat sinking capability of the PCB.
- Reduce thermal resistance to the environment of the chip by adding or increasing heat sink capability on top of the package.
- Add or increase airflow in the system.

Power delivered to the LEDs can be greater than 50 W and the power dissipated by the DLPA3005 can be considerable. For proper DLPA3005 operation, the details below outline thermal considerations for a DLPA3005 application.

The recommended junction temperature for the DLPA3005 is below 120°C during operation. The equation that relates junction temperature, $T_{junction}$, is given by:

$$T_{junction} = T_{ambient} + P_{diss} \times R_{\theta JA} \quad (13)$$

where $T_{ambient}$ is the ambient temperature, P_{diss} is the total power dissipation, and $R_{\theta JA}$ is the thermal resistance from junction to ambient.

The total power dissipation may vary depending on the application of the DLPA3005. The main contributors in the DLPA3005 are typically:

- Buck converters
- LDOs

For the buck converter, the power dissipation is given by:

$$P_{diss\_buck} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta_{buck}} - 1\right) \quad (14)$$

where η_{buck} is the efficiency of the buck converter, P_{in} is the power delivered to the input of the buck converter, and P_{out} is the power delivered to the load of the buck converter. For the buck converter PWR1,2,6, the efficiency can be determined using the curves in 图 7-16.

For the LDO, the power dissipation is given by:

$$P_{diss\_LDO} = (V_{in} - V_{out}) \times I_{load} \quad (15)$$

where V_{in} is the input supply voltage, V_{out} is the output voltage of the LDO, and I_{load} is the load current of the LDO. The voltage drops over the LDO (V_{in}-V_{out}) can be relatively large; a small load current can result in significant power dissipation. For this situation, a general purpose buck converter can be a more efficient solution.

The LDO DMD provides power to the boost converter, and the boost converter provides high voltages for the DMD; that is, V_{BIAS}, V_{OFS}, V_{RST}. The current load on these lines can increase up to $I_{load,max}$=10 mA. Assuming the efficiency of the boost converter, η_{boost}, is 80%, the maximum boost converter power dissipation, $P_{diss\_DMD\_boost,max}$, can be calculated as:

$$P_{diss\_DMD\_boost,max} = I_{load,max}\left(V_{BIAS} + V_{OFS} + |V_{RST}|\right) \times \left(\frac{1}{\eta_{boost}} - 1\right) \approx 0.1W \quad (16)$$

Compared to the power dissipation of the illumination buck converter, the power dissipation of the boost converter is negligible. However, the power dissipation of the LDO DMD, $P_{diss\_LDO\_DMD}$ should be given consideration in the case of a high supply voltage. The worst-case load current for the LDO is given by:

$$I_{load\_LDO,max} = \frac{1}{\eta_{boost}} \frac{\left(V_{BIAS} + V_{OFS} + |V_{RST}|\right)}{V_{DRST\_5P5V}} I_{load,max} \approx 100mA \quad (17)$$

where the output voltage of the LDO is V_{DRST_5P5V}= 5.5 V.

The worst-case power dissipation of the LDO DMD is approximately 1.5 W when the input supply voltage is 19.5 V. For your specific application, it is recommended to check the LDO current level. Therefore, the total power dissipation of the DLPA3005 can be described as:

$$P_{diss\_DLPA3005} = \sum P_{buck\_converter} + \sum P_{LDOs} \quad (18)$$

The following examples calculate of the maximum ambient temperature and the junction temperature based on known information.

If it is assumed that the total dissipation $P_{diss\_DLPA3005}$= 2.5 W, $T_{junction,max}$= 120°C, and $R_{\theta JA}$= 7°C/W (refer to 节 6.4), then the maximum ambient temperature can be calculated using 方程式 13:

$$T_{ambient,max} = T_{junction,max} - P_{diss} \times R_{\theta JA} = 120°C - 2.5W \times 7°C/W = 102.5°C \quad (19)$$

If the total power dissipation and the ambient temperature are known as:

$$T_{ambient}$= 50 °C, $R_{\theta JA}$= 7 °C/W, $P_{diss\_DLPA3005}$= 4 W. \quad (20)$$

the junction temperature can be calculated:

$$T_{junction} = T_{ambient} + P_{diss} \times R_{\theta JA} = 50°C + 4W \times 7°C/W = 78°C \quad (21)$$

If the combination of ambient temperature and the total power dissipation of the DLPA3005 does not produce an acceptable junction temperature, that is, <120°C, there are two approaches:

1. Use larger heat sink or more airflow to reduced $R_{\theta JA}$.
2. Reduce power dissipation in DLPA3005:
   - Use an external buck converter instead of an internal general purpose buck converter.
   - Reduce load current for the buck converter.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

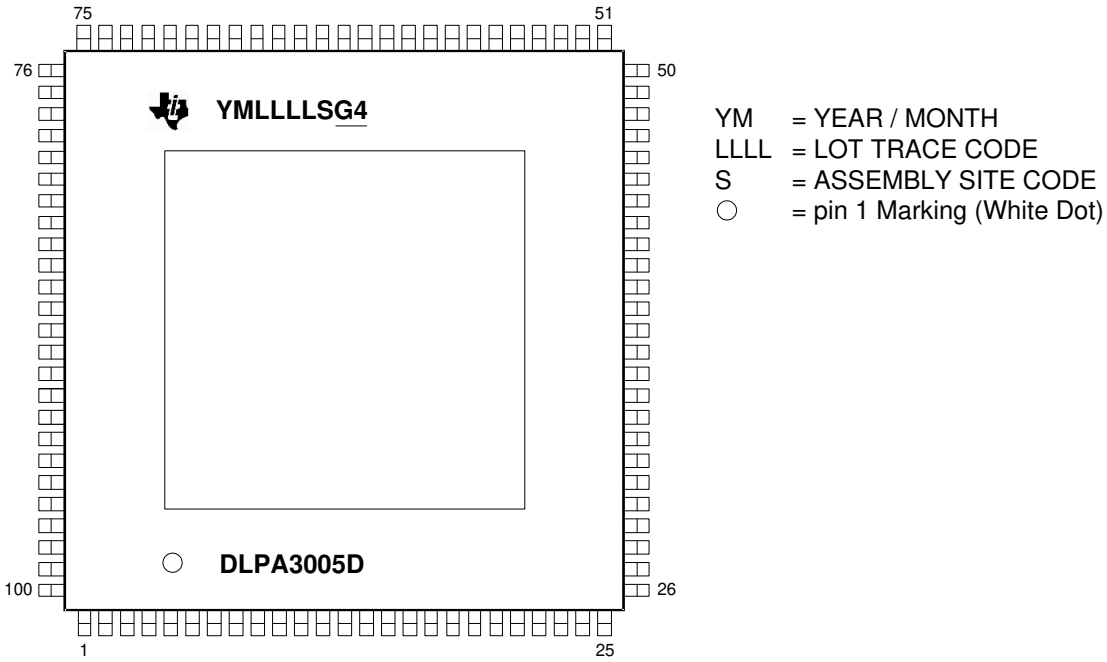


图 11-1. Package Marking DLPA3005 (Top View)

11.2 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLPA3005	Click here	Click here	Click here	Click here	Click here
DLPC3439	Click here	Click here	Click here	Click here	Click here

11.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.6 Trademarks

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DLP® is a registered trademark of Texas Instruments.
is a registered trademark of Texas Instruments.
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11.7 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4) (5)
DLPA3005CPFD	LIFEBUY	HTQFP	PFD	100		TBD	Call TI	Level-2-260C-1 YEAR	0 to 70	DLPA3005C
DLPA3005CPFDR	LIFEBUY	HTQFP	PFD	100		TBD	Call TI	Level-2-260C-1 YEAR	0 to 70	DLPA3005C
DLPA3005DPFD	ACTIVE	HTQFP	PFD	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3005D
DLPA3005DPFDR	ACTIVE	HTQFP	PFD	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3005D

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLPA3005DPFD	Active	Production	HTQFP (PFD) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3005D
DLPA3005DPFD.B	Active	Production	HTQFP (PFD) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3005D
DLPA3005DPFDR	Active	Production	HTQFP (PFD) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3005D
DLPA3005DPFDR.B	Active	Production	HTQFP (PFD) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3005D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

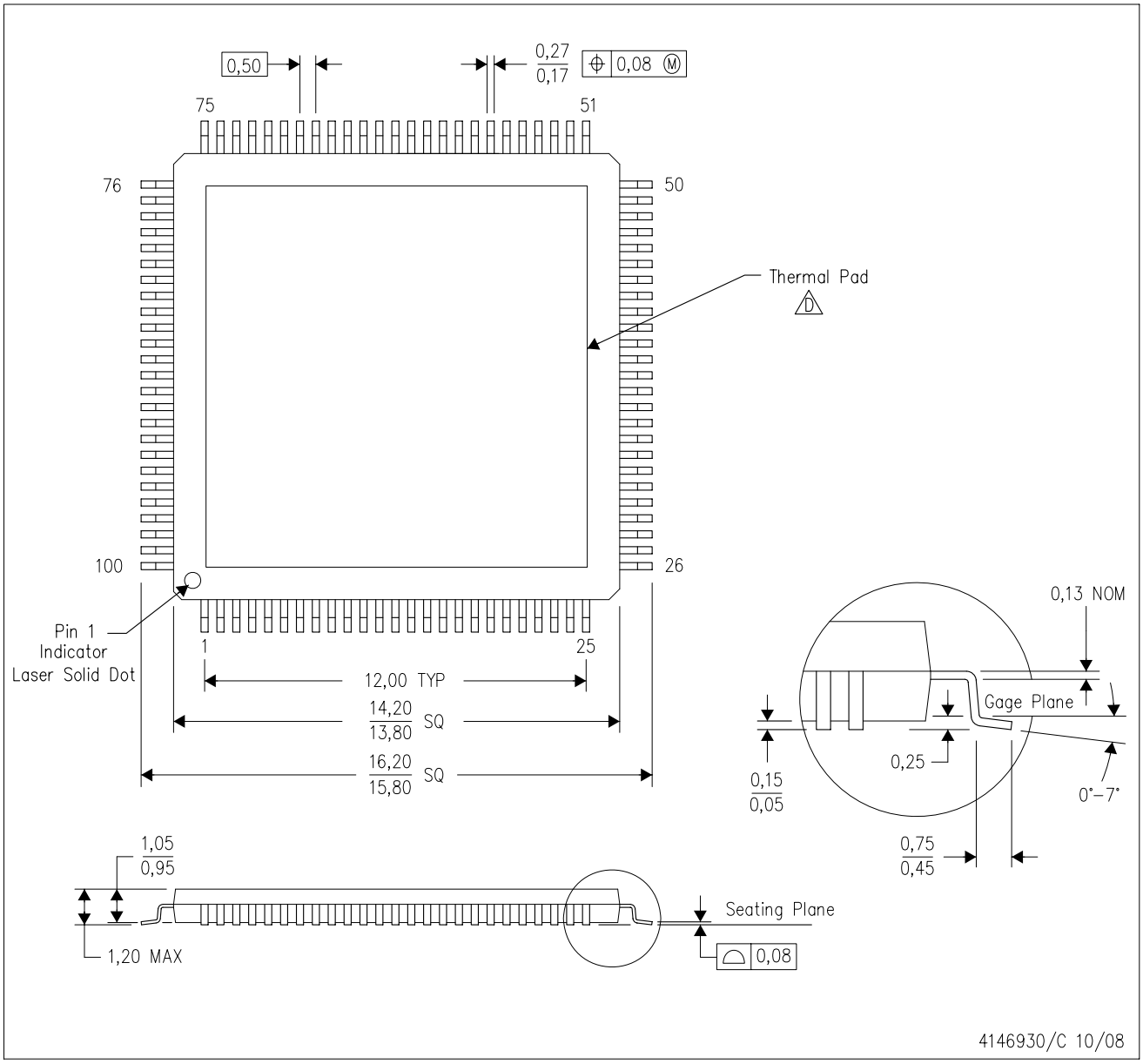
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PFD (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

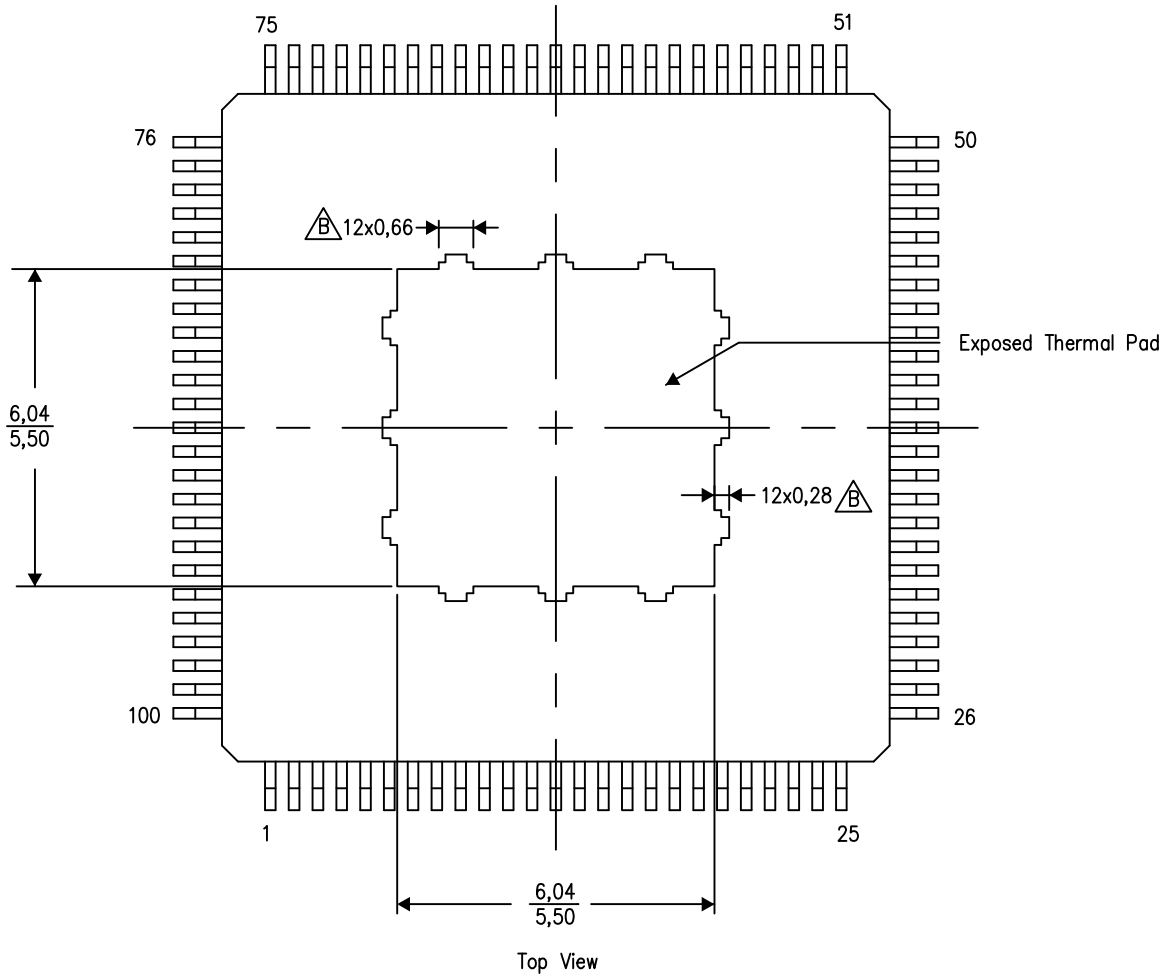
PFD (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

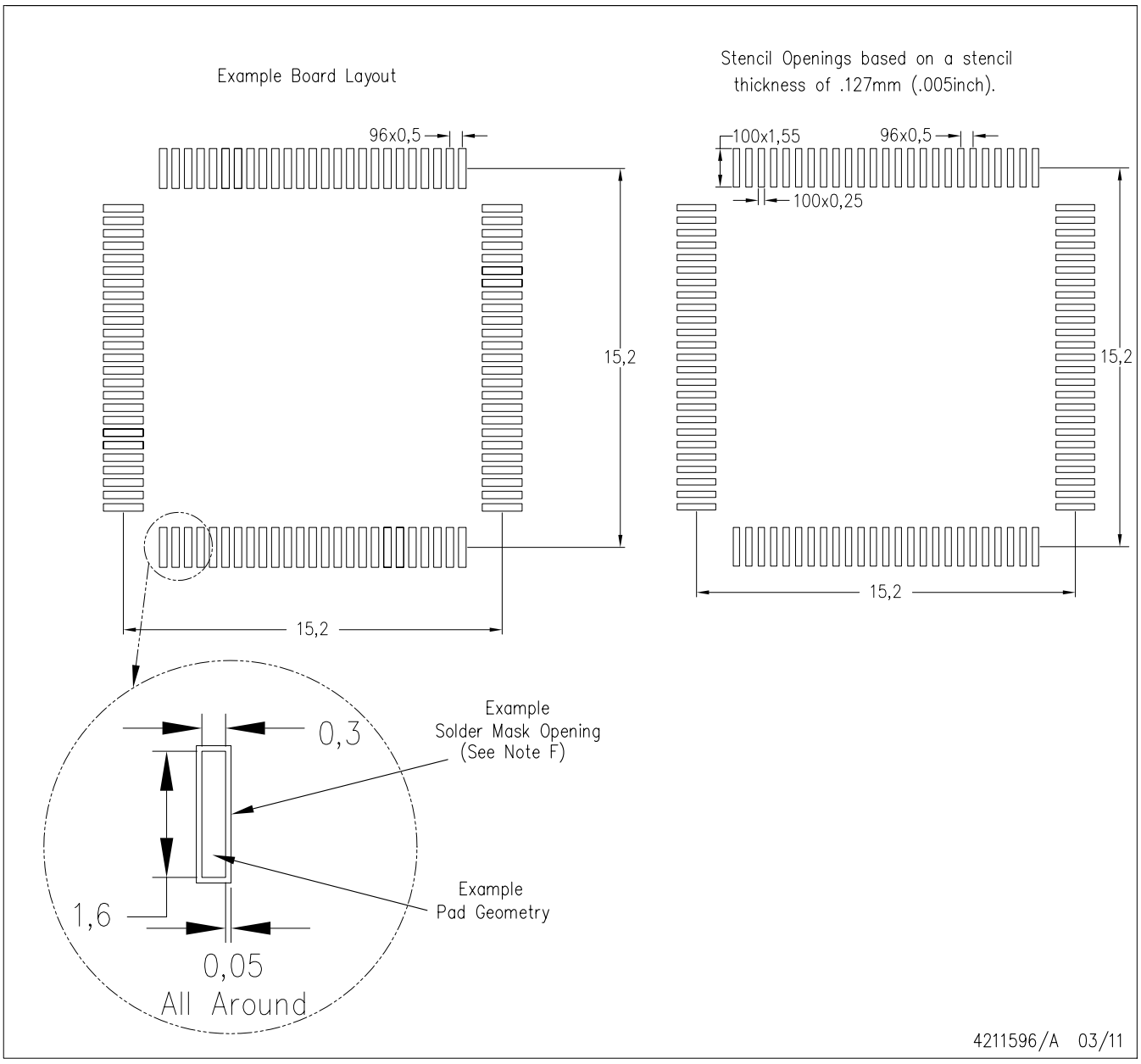
4211595–3/B 06/14

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PFD (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要通知和免责声明

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