DLP650LE 0.65 英寸 WXGA 数字微镜器件

1 特性

- 0.65 英寸对角线微镜阵列
  - 具有超过 100 万个微镜的 WXGA (1280 × 800) 阵列
  - 10.8µm 微镜间距
  - ±12° 微镜倾斜角（相对于平面）
  - 设计用于角落照明
- 2×LVDS 输入数据总线
- DLP650LE 芯片组包括:
  - DLP650LE DMD
  - DLPC4420 控制器
  - DLPA100 控制器电源管理和电机驱动器 IC
  - DLPA200 DMD 电源管理 IC

2 应用

- 智能照明
- 企业投影仪
- 教育投影仪

3 说明

TI DLP® DLP650LE 数字微镜器件 (DMD) 是一款数控微机电系统 (MEMS) 空间照明调制器 (SLM)，可用于实现明亮、经济实惠的 WXGA 显示解决方案。DLP650LE DMD 通过与 DLPC4420 显示控制器、DLPA100 电源和电机驱动器以及 DLPA200 DMD 微镜驱动器配合使用，可提供实现高性能系统的能力，是需要 16:10 纵横比、高亮度和系统简单性的显示应用的理想之选。DLP650LE DMD 还可以使用 DLPC4430 作为显示控制器。

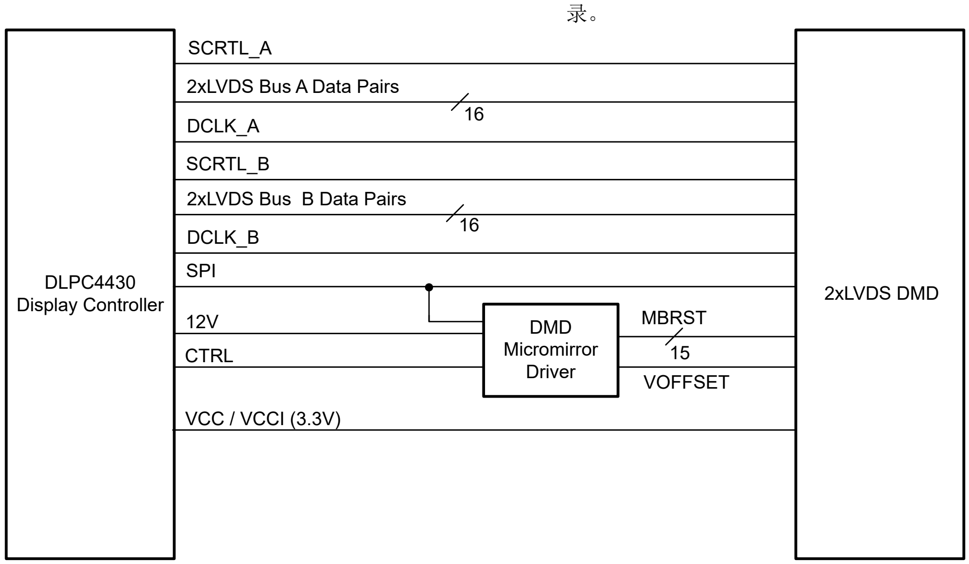
DMD 生态系统提供现成的资源以帮助用户缩短设计周期，请访问 DLP® 产品第三方搜索工具，查找获得批准的光学模块制造商和第三方提供商。

访问 TI DLP 显示技术入门，了解有关使用 DMD 开始设计的更多信息。

器件信息

器件型号	封装(1)	封装尺寸
DLP650LE	FYL (149)	32.20mm × 22.30mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



DLP650LE 简化版应用

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4 Pin Configuration and Functions

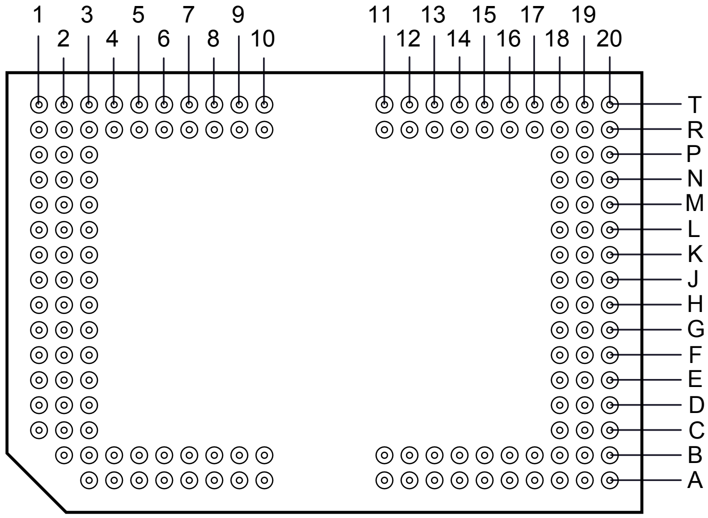


图 4-1. FYL Package 149-Pin CLGA Bottom View

表 4-1. Pin Functions

PIN		NET LENGTH (mils)	SIGNAL	TYPE(1)	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(1)	G20	711.64	LVDS	I	LVDS pair for Data Bus A
D_AN(3)	H19	711.60			
D_AN(5)	F18	711.60			
D_AN(7)	E18	711.60			
D_AN(9)	C20	711.60			
D_AN(11)	B18	711.60			
D_AN(13)	A20	711.60			
D_AN(15)	B19	711.58			
D_AP(1)	H20	711.66			
D_AP(3)	G19	711.61			
D_AP(5)	G18	711.59			
D_AP(7)	D18	711.60			
D_AP(9)	D20	711.59			
D_AP(11)	A18	711.58			
D_AP(13)	B20	711.59			
D_AP(15)	A19	711.59			

表 4-1. Pin Functions （续）

PIN NAME	PIN NO.	NET LENGTH (mils)	SIGNAL	TYPE[(1)]	DESCRIPTION
D_BN(1)	K20	711.61	LVDS	I	LVDS pair for Data Bus B
D_BN(3)	J19	711.59			
D_BN(5)	L18	711.59			
D_BN(7)	M18	711.6			
D_BN(9)	P20	711.6			
D_BN(11)	R18	711.59			
D_BN(13)	T20	711.59			
D_BN(15)	R19	711.59			
D_BP(1)	J20	711.61			
D_BP(3)	K19	711.6			
D_BP(5)	K18	711.58			
D_BP(7)	N18	711.58			
D_BP(9)	N20	711.6			
D_BP(11)	T18	711.61			
D_BP(13)	R20	711.59			
D_BP(15)	T19	711.6			
DCLK_AN	D19	711.59		I	LVDS pair for Data Clock A
DCLK_AP	E19	711.59			
DCLK_BN	N19	711.6		I	LVDS pair for Data Clock B
DCLK_BP	M19	711.61			
DATA CONTROL INPUTS					
SCTRL_AN	F20	711.62		I	LVDS pair for Serial Control (Sync) A
SCTRL_AP	E20	711.6			
SCTRL_BN	L20	711.59		I	LVDS pair for Serial Control (Sync) B
SCTRL_BP	M20	711.59			

表 4-1. Pin Functions （续）

PIN		NET LENGTH (mils)	SIGNAL	TYPE[(1)]	DESCRIPTION
NAME	NO.				
MICROMIRROR BIAS RESET INPUTS					
MBRST(0)	C3	507.20		I	Nonlogic compatible Micromirror Bias Reset signals. Connected directly to the array of pixel micromirrors. Used to hold or release the micromirrors. Bond Pads connect to an internal pulldown resistor.
MBRST(1)	D2	576.83			
MBRST(2)	D3	545.78			
MBRST(3)	E2	636.33			
MBRST(4)	G3	618.42			
MBRST(5)	E1	738.25			
MBRST(6)	G2	718.82			
MBRST(7)	G1	777.04			
MBRST(8)	N3	543.29			
MBRST(9)	M2	612.93			
MBRST(10)	M3	580.97			
MBRST(11)	L2	672.43			
MBRST(12)	J3	653.61			
MBRST(13)	L1	764.00			
MBRST(14)	J2	764.37			
MBRST(15)	J1	813.14			
SCP CONTROL					
SCPCLK	A8			I	Serial Communications Port Clock. Bond Pad connects to an internal pulldown circuit.
SCPDI	A5			I	Serial Communications Port Data. Bond Pad connects to an internal pulldown circuit.
SCPENZ	B7			I	Active low serial communications port enable. Bond pad connects to an internal pulldown circuit.
SCPDO	A9			O	Serial communications port output
OTHER SIGNALS					
EVCC	A3			P	Do not connect on the DLP system board.
MODE_A	A4	415.1		I	Data Bandwidth Mode Select. Bond Pad connects to an internal pulldown circuit. Refer to Table 4 for DLP system board connection information.
PWRDNZ	B9	110.38		I	Active Low Device Reset. Bond Pad connects to an internal pulldown circuit.
POWER					
V_{CC} [(2)]	B11, B12, B13, B16, R12, R13, R16, R17			P	Power supply for low voltage CMOS logic. Power supply for normal high voltage at micromirror address electrodes
V_{CCI} [(2)]	A12, A14, A16, T12, T14, T16			P	Power supply for low voltage CMOS LVDS interface
V_{OFFSET} [(2)]	C1, D1, M1, N1			P	Power supply for high voltage CMOS logic. Power supply for stepped high voltage at micromirror address electrodes

表 4-1. Pin Functions （续）

PIN		NET LENGTH (mils)	SIGNAL	TYPE[(1)]	DESCRIPTION
NAME	NO.				
V_{SS} (Ground)[(3)]	A6, A11, A13, A15, A17, B4, B5, B8, B14, B15, B17, C2, C18, C19, F1, F2, F19, H1, H2, H3, H18, J18, K1, K2, L19, N2, P18, P19, R4, R9, R14, R15, T7, T13, T15, T17			P	Common return for all power
RESERVED SIGNALS					
RESERVED_FC	R7	40.64		I	Connect to GND on the DLP system board. Bond Pad connects to an internal pulldown circuit.
RESERVED_FD	R8	94.37		I	Connect to GND on the DLP system board. Bond Pad connects to an internal pulldown circuit.
RESERVED_PFE	T8	50.74		I	Connect to ground on the DLP system board. Bond Pad connects to an internal pulldown circuit.
RESERVED_STM	B6			I	Connect to GND on the DLP system board. Bond Pad connects to an internal pulldown circuit.
RESERVED_TP0	R10	93.3		I	Do not connect on the DLP system board.
RESERVED_TP1	T11	263.74		I	Do not connect on the DLP system board.
RESERVED_TP2	R11	281.47		I	Do not connect on the DLP system board.
RESERVED_BA	T10	148.85		O	Do not connect on the DLP system board.
RESERVED_BB	A10	105.28		O	Do not connect on the DLP system board.
RESERVED_RA1	T9			O	Do not connect on the DLP system board.
RESERVED_RB1	A7			O	Do not connect on the DLP system board.
RESERVED_TS	B10	145.42		O	Do not connect on the DLP system board.
RESERVED_A(0)	T2			NC	Do not connect on the DLP system board.
RESERVED_A(1)	T3				
RESERVED_A(2)	R3				
RESERVED_A(3)	T4				
RESERVED_M(0)	R2			NC	Do not connect on the DLP system board.
RESERVED_M(1)	P1			NC	Do not connect on the DLP system board.
RESERVED_S(0)	T1			NC	Do not connect on the DLP system board.
RESERVED_S(1)	R1			NC	Do not connect on the DLP system board.
RESERVED_IRQZ	T6			NC	Do not connect on the DLP system board.
RESERVED_OEZ	R5			NC	Do not connect on the DLP system board.
RESERVED_RSTZ	R6			NC	Do not connect on the DLP system board.
RESERVED_STR	T5			NC	Do not connect on the DLP system board.

表 **4-1. Pin Functions（续）**

PIN		NET LENGTH (mils)	SIGNAL	TYPE[(1)]	DESCRIPTION
NAME	NO.				
RESERVED_STR	T5			NC	Do not connect on the DLP system board.
RESERVED_VB	E3, F3, K3, L3			NC	Do not connect on the DLP system board.
RESERVED_VR	B2, B3, P2, P3			NC	Do not connect on the DLP system board.

(1) I = Input, O = Output, G = Ground, A = Analog, P = Power, NC = No Connect.
(2) Power supply pins required for all DMD operating modes are V_{SS}, V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET}.
(3) V_{SS} must be connected for proper DMD operation.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic(2)	–0.5	4	V
V_{CCI}	Supply voltage for LVDS Interface(2)	–0.5	4	V
V_{OFFSET}	Micromirror Electrode and HVCMOS voltage(2) (3)	–0.5	9	V
V_{MBRST}	Input voltage for MBRST(15:0)(2)	–28	28	V
$\|V_{CCI} - V_{CC}\|$	Supply voltage delta (absolute value)(4)		0.3	V
INPUT VOLTAGES				
	Input voltage for all other input pins(2)	–0.5	V_{CC} + 0.3	V
$\|V_{ID}\|$	Input differential voltage (absolute value)(5)		700	mV
CLOCKS				
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_A		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_B		400	MHz
ENVIRONMENTAL				
T_{ARRAY} and T_{WINDOW}	Temperature, operating(6)	0	90	°C
	Temperature, non–operating(6)	–40	90	°C
$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(7)		30	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are referenced to common ground V_{SS}. V_{CC}, V_{CCI}, V_{OFFSET}, and V_{SS} (GND) power supplies are all required for all DMD operating modes.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable voltage difference between V_{CC} and V_{CCI} may result in excessive current draw.
(5) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS differential inputs must not exceed $|V_{ID}|$ = 700mV or damage may result to the internal termination resistors.
(6) The highest temperature of the active array (as calculated using 节 6.6) or of any point along the window edge as defined in 图 6-1. The locations of thermal test points TP2, TP3, TP4, and TP5 in 图 6-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, then that point needs to be used.
(7) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 图 6-1. The window test points TP2, TP3, TP4, and TP5 shown in 图 6-1 are intended to result in the worst-case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, then that point needs to be used.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	°C
$T_{DP\text{-}AVG}$	Average dew point temperature (non-condensing)[1]		28	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing)[2]	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins except MBRST(15:0)	±2000	V
			Pins MBRST(15:0)	< 250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	Supply voltage for LVCMOS core logic[1]	3.0	3.3	3.6	V
V_{CCI}	Supply voltage for LVDS interface[1]	3.0	3.3	3.6	V
V_{OFFSET}	Micromirror electrode and HVCMOS voltage[1] [2]	8.25	8.5	8.75	V
V_{MBRST}	Micromirror bias / reset voltage[1]	–27		26.5	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value)[3]		0	0.3	V
LVCMOS INTERFACE					
V_{IH}	Input high voltage	1.7	2.5	V_{CC} + 0.3	V
V_{IL}	Input low voltage	–0.3		0.7	V
I_{OH}	High level output current			–20	mA
I_{OL}	Low level output current			15	mA
t_{PWRDNZ}	PWRDNZ pulse width[4]	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency[5]	50		500	kHz
t_{SCP_PD}	Propagation delay, clock to Q, from rising-edge of SCPCLK to valid SCPDO[6]	0		900	ns
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling-edge)[6]	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling-edge)[6]	900			ns
$t_{SCP\_NEG\_ENZ}$	Time between falling-edge of SCPENZ and the rising-edge of SCPCLK.[5]	1			us
SCP_POS_ENZ	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			us
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tristate)			$192/f_{DCLK}$	s
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	1			$1/f_{scpclk}$
t_{r_SCP}	Rise time for SCP signals			200	ns

5.4 Recommended Operating Conditions （续）

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
t_{f_SCP}	Fall time for SCP signals			200	ns
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK[7]		320	330	MHz
$\lvert V_{ID}\rvert$	Input differential voltage (absolute value)[8]	100	400	600	mV
V_{CM}	Common mode voltage[8]		1200		mV
V_{LVDS}	LVDS voltage[8]	0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	85	90	95	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operational[9] [10] [11]	10		40 to 70[12]	°C
	Array temperature, short-term operational, 500 hr max[10] [13]	0		10	°C
T_{WINDOW}	Window temperature (all part numbers except *1280-6434B)[14]	10		90	°C
	Window temperature (part number 1280-6434B)[14]	10		85	
$T_{\lvert DELTA\rvert}$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1[15]			26	°C
$T_{DP\text{-}AVG}$	Average dew point average temperature (non-condensing)[16]			28	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing)[17]	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
SOLID STATE ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 410nm[9] [19]			10	mW/cm2
ILL_{VIS}	Illumination power at wavelengths ⩾ 410nm and ⩽ 800nm[18] [19]			23.7	W/cm2
ILL_{IR}	Illumination power at wavelengths > 800nm[19]			10	mW/cm2
ILL_{BLU}	Illumination power at wavelengths ⩾ 410nm and ⩽ 475nm[18] [19]			7.5	W/cm2
ILL_{BLU1}	Illumination power at wavelengths ⩾ 410nm and ⩽ 440nm[18] [19]			1.3	W/cm2
LAMP ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 395nm[9] [19]			2.0	mW/cm2
ILL_{VIS}	Illumination power at wavelengths ⩾ 395nm and ⩽ 800nm[18] [19]			23.7	W/cm2
ILL_{IR}	Illumination power at wavelengths > 800nm[19]			10	mW/cm2

(1) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(2) V_{OFFSET} supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta $\lvert V_{CCI} - V_{CC}\rvert$ must be less than specified limit. See 节 8.
(4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(5) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(6) See 图 5-2.
(7) See LVDS Timing Requirements in 节 5.8 and 图 5-6.
(8) Refer to 图 5-5.
(9) Simultaneous exposure of the DMD to the maximum 节 5.4 for temperature and UV illumination reduces device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 图 6-1 and the package 节 5.5 using the calculation in 节 6.6.
(11) Long-term is defined as the usable life of the device.
(12) Per 图 5-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See 节 6.8 for a definition of micromirror landed duty cycle.
(13) Short-term is defined as cumulative time over the usable life of the device.

(14) The locations of thermal test points TP2, TP3, TP4, and TP5 in 图 6-1 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
(15) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 图 6-1. The window test points TP2, TP3, TP4, and TP5 shown in 图 6-1 are intended to result in the worst-case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.
(16) The average over time (including storage and operating) that the device is not in the "elevated dew point temperature range."
(17) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(18) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
(19) To calculate see 节 6.7.

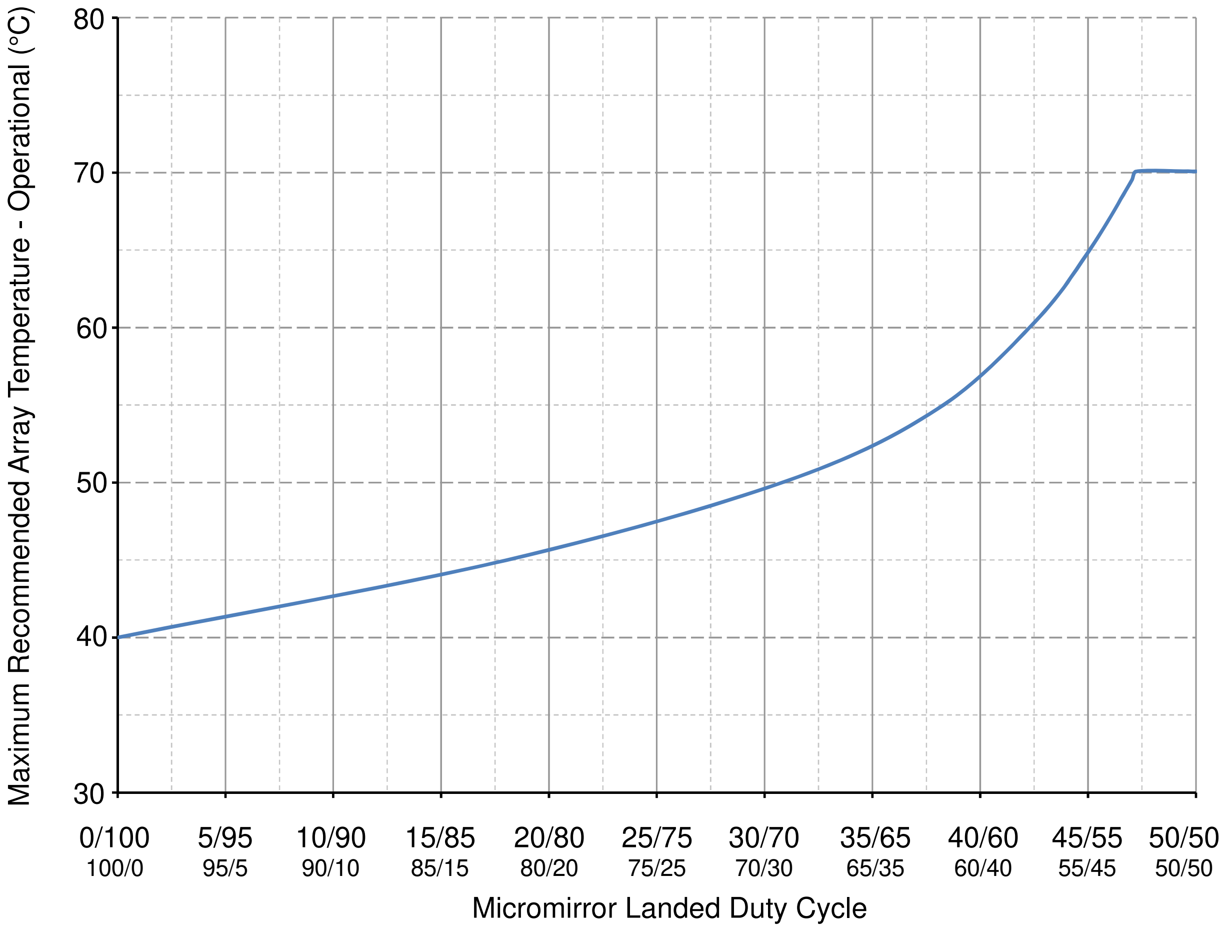


图 5-1. Maximum Recommended Array Temperature—Derating Curve

5.5 Thermal Information

THERMAL METRIC	DLP650LE FYL Package 149 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)(1)	0.50	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the 节 5.4.
The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.
Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 3V, I_{OH} = –20mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 3.6V, I_{OL} = 15mA			0.4	V
I_{OZ}	High-impedance output current	V_{CC} = 3.6V			10	µA
I_{IL}	Low-level input current	V_{CC} = 3.6V, VI = 0			–60	µA
I_{IH}	High-level input current (1)	V_{CC} = 3.6V, VI = V_{CC}			200	µA
I_{CC}	Supply current VCC (2)	V_{CC} = 3.6V			479	mA
I_{CCI}	Supply current VCCI (2)	V_{CCI} = 3.6V			309	mA
I_{OFFSET}	Supply current VOFFSET (3)	V_{OFFSET} = 8.75V			25	mA
	Supply input power total	f = 1MHz			3060	mW

(1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins.
(2) To prevent excess current, the supply voltage delta $|V_{CCI} - V_{CC}|$ must be less than the specified limit in 节 5.4.
(3) To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{OFFSET}|$ must be less than the specified limit in 节 5.4.

5.7 Capacitance at Recommended Operating Conditions

over operating free-air temperature range, f = 1MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_I	Input capacitance			10	pF
C_O	Output capacitance			10	pF
C_{IM}	MBRST(15:0) input capacitance	1280 × 800 array all inputs interconnected	230	290	pF

5.8 Timing Requirements

Over 节 5.4 (unless otherwise noted).

PARAMETER DESCRIPTION		SIGNAL	MIN	TYP	MAX	UNIT
LVDS (1)						
t_C	Clock cycle duration for DCLK_A	LVDS	3.03			ns
t_C	Clock cycle duration for DCLK_B	LVDS	3.03			ns
t_W	Pulse duration for DCLK_A	LVDS	1.36	1.52		ns
t_W	Pulse duration for DCLK_B	LVDS	1.36	1.52		ns
t_{SU}	Setup time for D_A(15:0) before DCLK_A	LVDS	0.35			ns
t_{SU}	Setup time for D_A(15:0) before DCLK_B	LVDS	0.35			ns
t_{SU}	Setup time for SCTRL_A before DCLK_A	LVDS	0.35			ns
t_{SU}	Setup time for SCTRL_B before DCLK_B	LVDS	0.35			ns
t_H	Hold time for D_A(15:0) after DCLK_A	LVDS	0.35			ns
t_H	Hold time for D_B(15:0) after DCLK_B	LVDS	0.35			ns
t_H	Setup time for SCTRL_A after DCLK_A	LVDS	0.35			ns
t_H	Setup time for SCTRL_B after DCLK_B	LVDS	0.35			ns
t_{SKEW}	Channel B relative to Channel A (2) (3)	LVDS	–1.51		1.51	ns

(1) See 图 5-6 for timing requirements for LVDS.
(2) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0).
(3) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0).

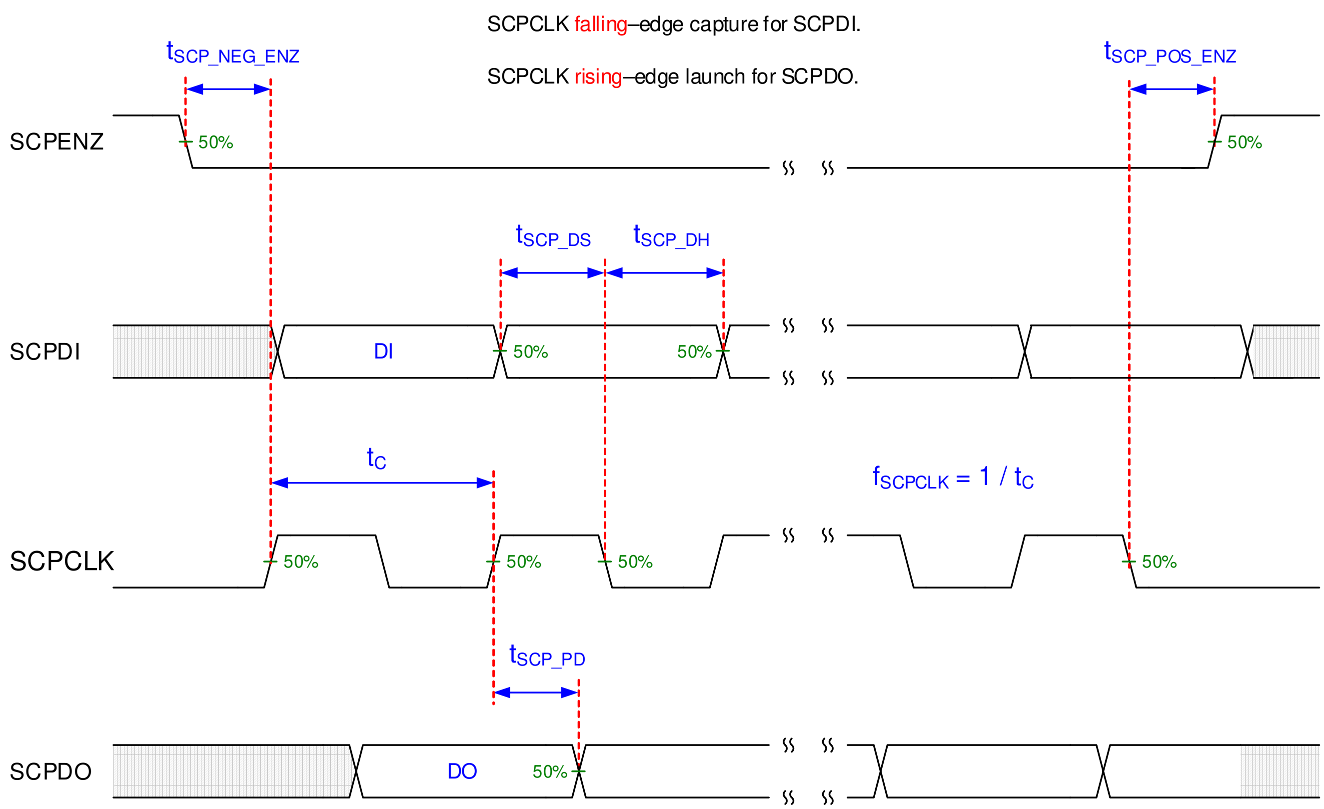
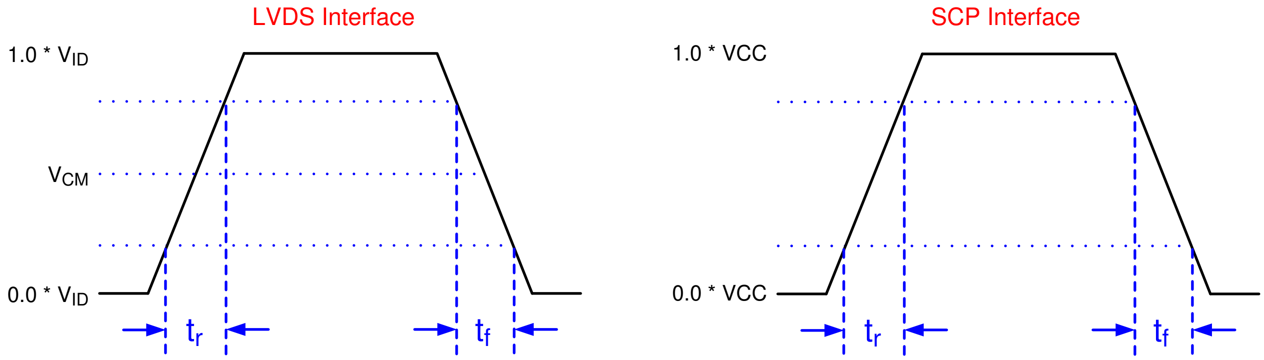


图 5-2. SCP Timing Requirements

See 节 5.4 for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH}, and t_{SCP_PD} specifications.

See 节 5.4 for t_r and t_f specifications and conditions.



Not to scale.

Refer to the 节 5.8.

Refer to 节 4 for list of LVDS pins and SCP pins.

图 5-3. Rise Time and Fall Time

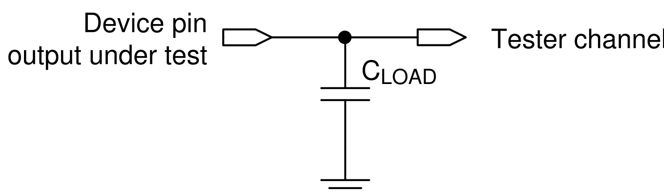


图 5-4. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. See 图 5-4.

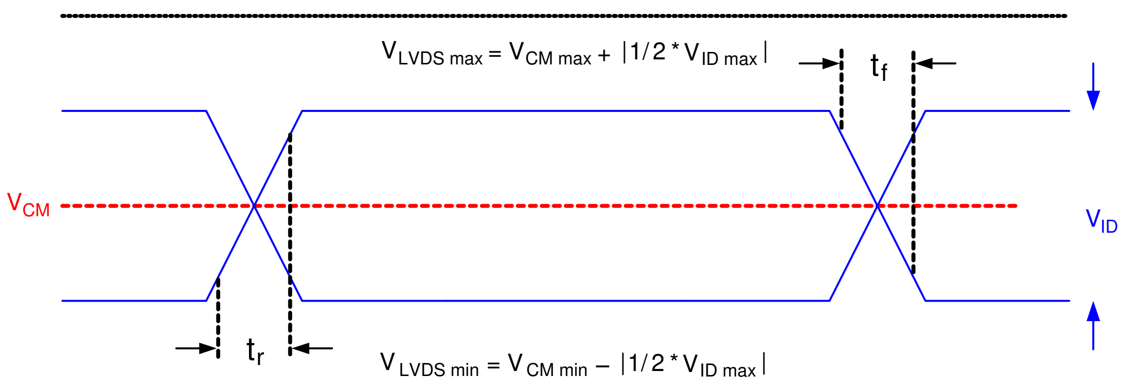


图 5-5. LVDS Waveform Requirements

See 节 5.4 for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

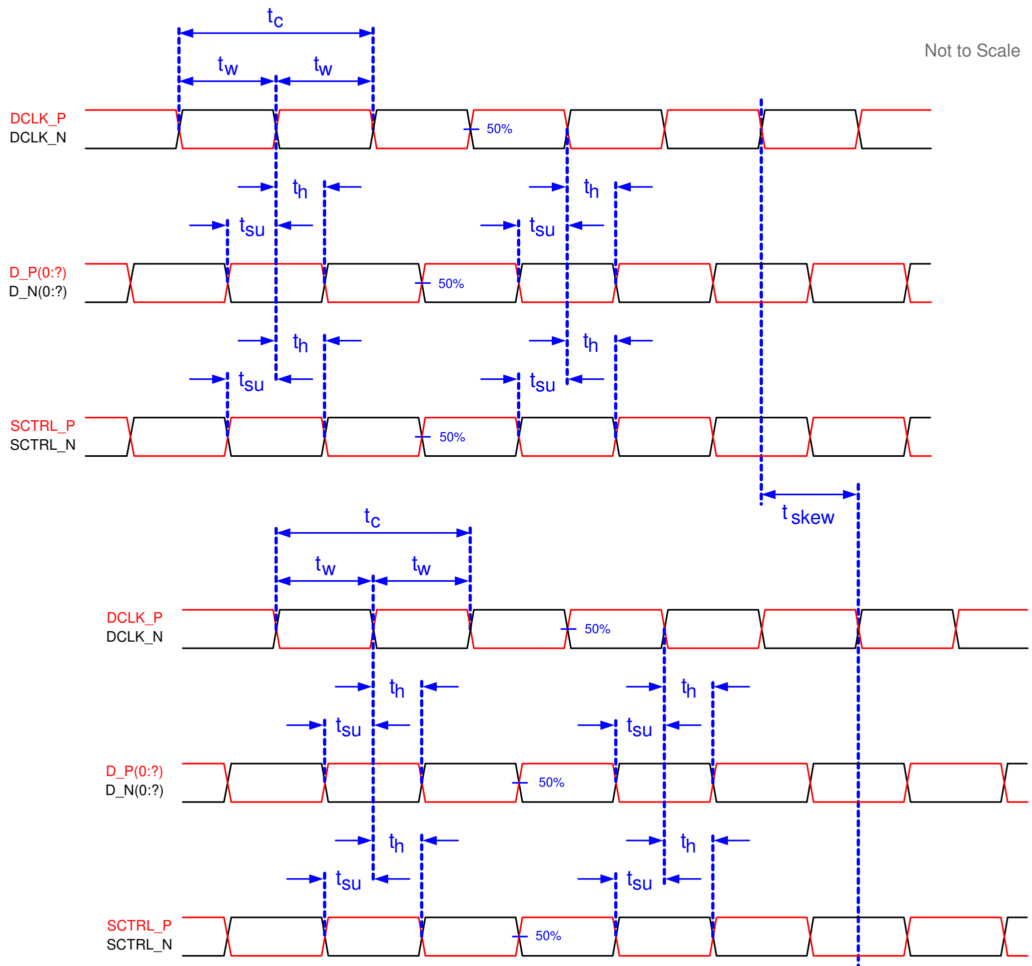


图 5-6. Timing Requirements

See 节 5.8 for timing requirements and LVDS pairs per channel (bus) defining D_P(0:x) and D_N(0:x).

5.9 Window Characteristics

表 5-1. DMD Window Characteristics

PARAMETER	MIN	NOM
Window material		Corning Eagle XG
Window Refractive Index at 546.1 nm		1.5119
Window Transmittance, minimum within the wavelength range 420 – 680 nm. Applies to all angles 0° – 30° AOI. (1) (2)	97%	
Window Transmittance, average over the wavelength range 420 – 680 nm. Applies to all angles 30° – 45° AOI. (1) (2)	97%	

(1) Single-pass through both surfaces and glass
(2) AOI—Angle of incidence is the angle between an incident ray and the normal to a reflecting or refracting surface.

5.10 System Mounting Interface Loads

表 5-2. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Condition 1:				
Thermal Interface area(1)			11.3	kg
Electrical Interface area(1)			11.3	kg
Condition 2:				
Thermal Interface area(1)			0	kg
Electrical Interface area(1)			22.6	kg

(1) Uniformly distributed within area shown in 图 5-7

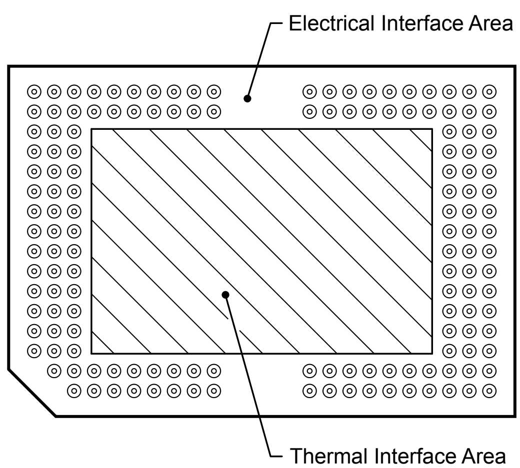


图 5-7. System Mounting Interface Loads

5.11 Micromirror Array Physical Characteristics

表 5-3. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns[(1)]	M	1280	micromirrors
Number of active rows[(1)]	N	800	
Micromirror (pixel) pitch [(1)]	P	10.8	µm
Micromirror active array width[(1)]	Micromirror pitch × number of active columns	13.824	mm
Micromirror active array height[(1)]	Micromirror pitch × number of active rows	8.640	mm
Micromirror active border size[(2)]	Pond of Micromirror (POM)	10	micromirrors / side

(1) See 图 5-8.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the *Pond Of Mirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”

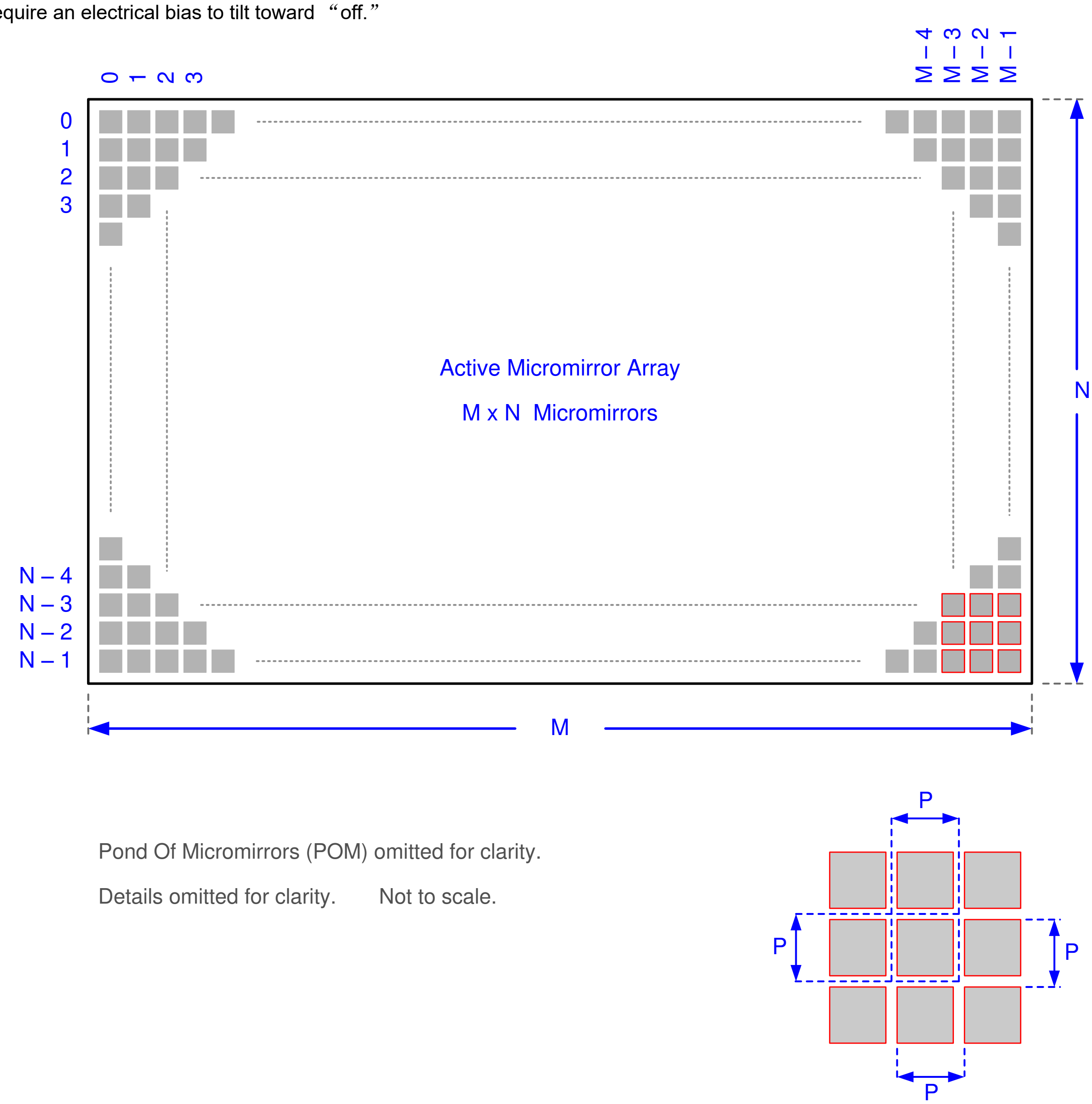


图 5-8. Micromirror Array Physical Characteristics

Refer to 节 5.11 table for M, N, and P specifications.

5.12 Micromirror Array Optical Characteristics

<table>
<tr><th colspan="2">PARAMETER</th><th>TEST CONDITION</th><th>MIN</th><th>NOM</th><th>MAX</th><th>UNIT</th></tr>
<tr><td colspan="2">Micromirror tilt angle, variation device to device [2] [3] [4] [5]</td><td>Landed State[1]</td><td>11</td><td>12</td><td>13</td><td>degrees</td></tr>
<tr><td rowspan="5">Image performance[6]</td><td>Bright pixel(s) in active area[7]</td><td>Gray 10 screen[10]</td><td></td><td></td><td>0</td><td rowspan="5">micromirrors</td></tr>
<tr><td>Bright pixel(s) in the POM[7] [9]</td><td>Gray 10 screen[10]</td><td></td><td></td><td>1</td></tr>
<tr><td>Dark pixel(s) in the active area[8]</td><td>White screen[11]</td><td></td><td></td><td>6</td></tr>
<tr><td>Adjacent pixel(s)[12]</td><td>Any screen</td><td></td><td></td><td>0</td></tr>
<tr><td>Unstable pixel(s) in active area[13]</td><td>Any screen</td><td></td><td></td><td>0</td></tr>
</table>

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) This represents the variation that can occur between any two individual micromirrors, locaed on the same device or located on different devices.
(4) For some applications it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs the micromirror tilt angle variations within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(5) See figure 图 5-9.
(6) Conditions of acceptance. All DMD image performance returns are evaluated using the following projected image test conditions:
- Test set degamma shall be linear.
- Test set brightness and contrast shall be set to nominal.
- The diagonal size of the projected image shall be a minimum of 60 inches.
- The projections screen shall be a 1× gain.
- The projected image shall be inspected from an 8 foot minimum viewing distance.
- The image shall be in focus during all image performance tests.

(7) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
(8) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
(9) POM definition: The rectangular border of off-state mirrors surrounding the active area.
(10) Gray 10 screen definition: A full screen with RGB values set to R=10/255, G=10/255, B=10/255.
(11) White screen definition: A full screen with RGB values set to R=255/255, G=255/255, B=255/255.
(12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point. Also referred to as a cluster.
(13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

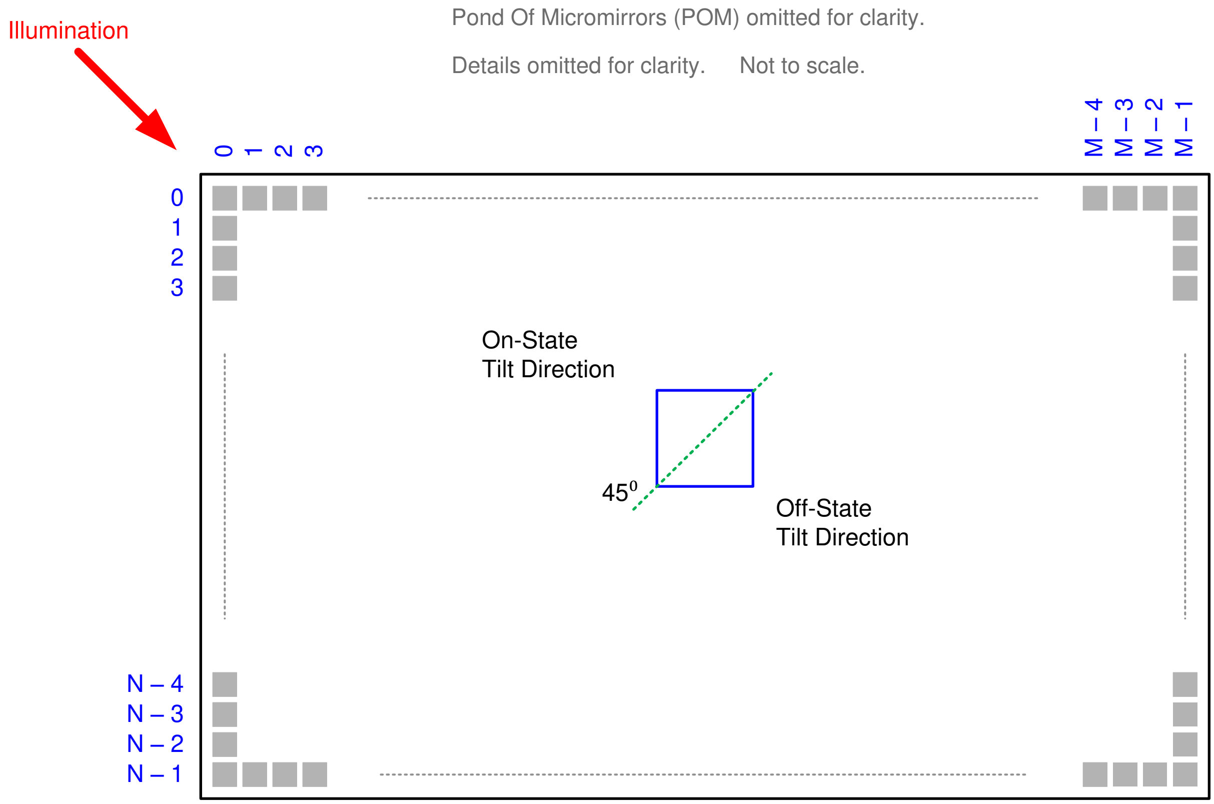


图 5-9. Micromirror Landed Orientation and Tilt

Refer to 节 5.11 table for M, N, and P specifications.

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP650LE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

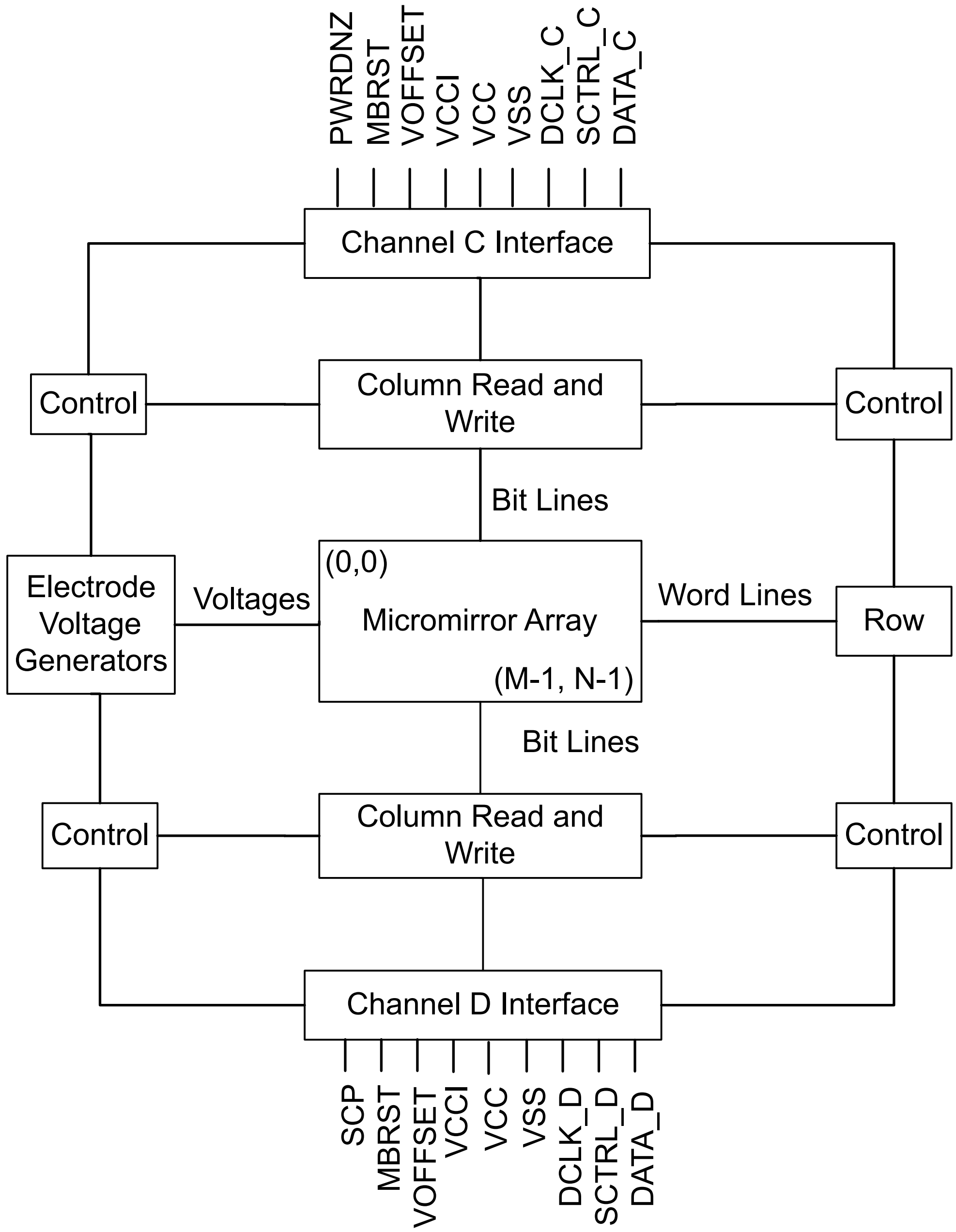
6 Detailed Description

6.1 Overview

The DMD is a 0.65 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to 节 6.2. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP650LE DMD is part of the chipset comprising of the DLP650LE DMD, the DLPC4420 display controller, the DLPA100 power and motor driver and the DLPA200 micromirror driver. To ensure reliable operation, the DLP650LE DMD must always be used with the DLPC4420 display controller, the DLPA100 power and motor driver and the DLPA200 micromirror driver.

6.2 Functional Block Diagram



For pin details on Channels A, B refer to 节 4 and LVDS Interface section of 节 5.8.

6.3 Feature Description

6.3.1 Power Interface

The DMD requires three DC voltages: DMD_P3P3V, V_{OFFSET}, and MBRST. DMD_P3P3V is created by the DLPA100 power and motor driver and the DLPA200 DMD micromirror driver. Both the DLPA100 and DLPA200 create the main DMD voltages, as well as powering various peripherals (TMP411, I^2C, and TI level translators). DMD_P3P3V provides the VCC voltage required by the DMD. V_{OFFSET} (8.5V) and MBRST are made by the DLPA200 and are supplied to the DMD to control the micromirrors.

6.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 图 5-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4420 display controller. See the DLPC4420 Display Controller Data Sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. System optical performance and image quality strongly relate to optical system design parameter trade-offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance with the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation, and objectionable artifacts in the display’s border and/or active area could occur.

6.5.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display’s border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately

10% of the average flux level in the active area. Depending on the particular system’s optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

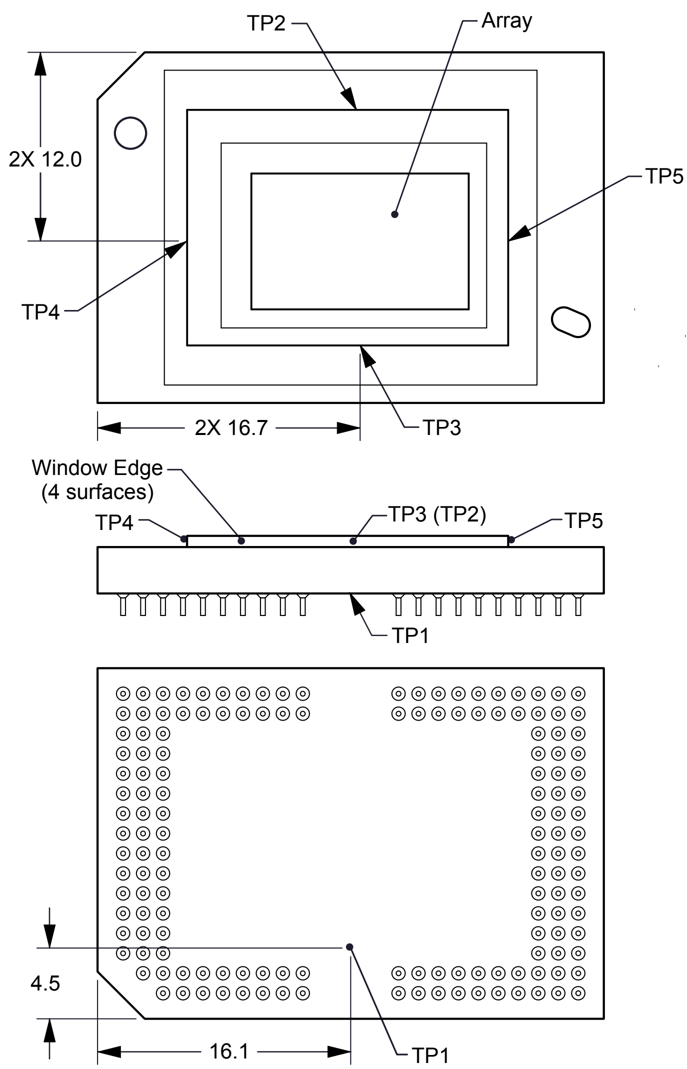


图 6-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array tempreature and the reference ceramic temperature, thermal test TP1 图 6-1 shown above:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 图 6-1

- $R_{ARRAY-TO-CERAMIC}$ = Thermal resistance of package specified in 节 5.5 from array to ceramic TP1 图 6-1 (°C/W).
- Q_{ARRAY} = Total DMD Power (electrical + absorbed) on the array (W)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$ (W)
- DMD average thermal absorptivity = 0.45

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.5W. The absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$Q_{INCIDENT}$ = 33W (measured)

$T_{CERAMIC}$= 55° (measured)

$Q_{ELECTRICAL}$ = 1.5W

Q_{ARRAY} = 1.5W + (0.45 × 33W) = 16.35W

T_{ARRAY} = 55°C + (16.35W × 0.50°C/W) = 63.2°C

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000mW/W \div A_{ILL}$ (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000mW/W \div A_{ILL}$ (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)

- A_{ARRAY} = area of the array (cm ^{2}) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS\text{-}RATIO}$ = ratio of the optical power for wavelengths ⩾410 and ⩽800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR\text{-}RATIO}$ = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU\text{-}RATIO}$ = ratio of the optical power for wavelengths ⩾410 and ⩽475nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1\text{-}RATIO}$ = ratio of the optical power for wavelengths ⩾410 and ⩽440nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 33W (measured)

A_{ARRAY} = (13.8240mm × 8.6400mm) ÷ 100mm^2/cm^2 = 1.1944cm^2 (data sheet)

OV_{ILL} = 16.3% (optical model)

$OP_{UV\text{-}RATIO}$ = 0.00017 (spectral measurement)

$OP_{VIS\text{-}RATIO}$ = 0.99977 (spectral measurement)

$OP_{IR\text{-}RATIO}$ = 0.00006 (spectral measurement)

$OP_{BLU\text{-}RATIO}$ = 0.28100 (spectral measurement)

$OP_{BLU1\text{-}RATIO}$ = 0.03200 (spectral measurement)

A_{ILL} = 1.1944cm^2 ÷ (1 - 0.163) = 1.4270cm^2

ILL_{UV} = [0.00017 × 33W] × 1000mW/W ÷ 1.4270cm^2 = 3.931mW/cm^2

ILL_{VIS} = [0.99977 × 33W] ÷ 1.4270cm^2 = 23.12W/cm^2

ILL_{IR} = [0.00006 × 33W] × 1000mW/W ÷ 1.4270cm^2 = 1.388mW/cm^2

ILL_{BLU} = [0.28100 × 33W] ÷ 1.4270cm^2 = 6.50W/cm^2

ILL_{BLU1} = [0.03200 × 33W] ÷ 1.4270cm^2 = 0.74W/cm^2

6.8 Micromirror Landed-On/Landed-Off Duty Cycle

6.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

6.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD’s micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD’s usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD’s usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD’s usable life. This is quantified in the de-rating curve shown in 图 5-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature at a given long-term average Landed Duty Cycle.

6.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 6-1.

表 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

- Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

Where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (1)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, and blue color intensities would be as shown in 表 6-2 and 表 6-3.

表 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

RED CYCLE	GREEN CYCLE	BLUE CYCLE
50%	20%	30%

表 6-3. Example Landed Duty Cycle for Full-Color

RED SCALE	GREEN SCALE	BLUE SCALE	LANDED DUTY CYCLE
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

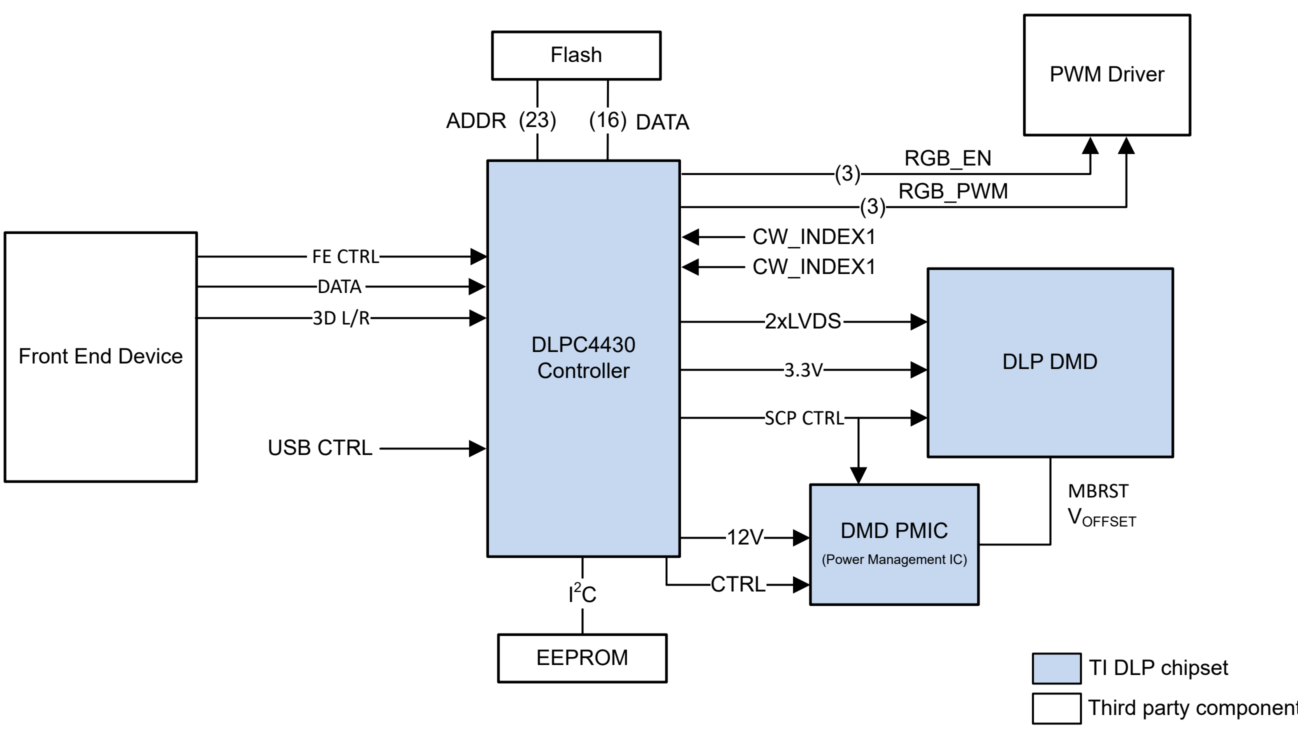
Texas Instruments DLP® technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, either towards the projection optics, or the collection optics. The large micromirror array size and ceramic package provides great thermal performance for bright display applications. Typical applications using the DLP650LE include smart lighting, education projectors, and business projectors. The following orderables have been replaced by the DLP650LE:

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)	MECHANICAL ICD
DLP650LET	FYL (149)	32.20mm × 22.30mm	2512372
1280-6434B	FYL (149)	32.20mm × 22.30mm	2512372
1280-6438B	FYL (149)	32.20mm × 22.30mm	2512372
1280-6439B	FYL (149)	32.20mm × 22.30mm	2512372
1280-643AB	FYL (149)	32.20mm × 22.30mm	2512372

7.2 Typical Application

The DLP650LE DMD combined with a DLPC4420 (or DLPC4430) digital controller, DLPA100 power management device, and DLPA200 micromirror driver provides WXGA resolution for bright, colorful display applications. 图 7-1 shows a typical display system using the DLP650LE and additional system components.



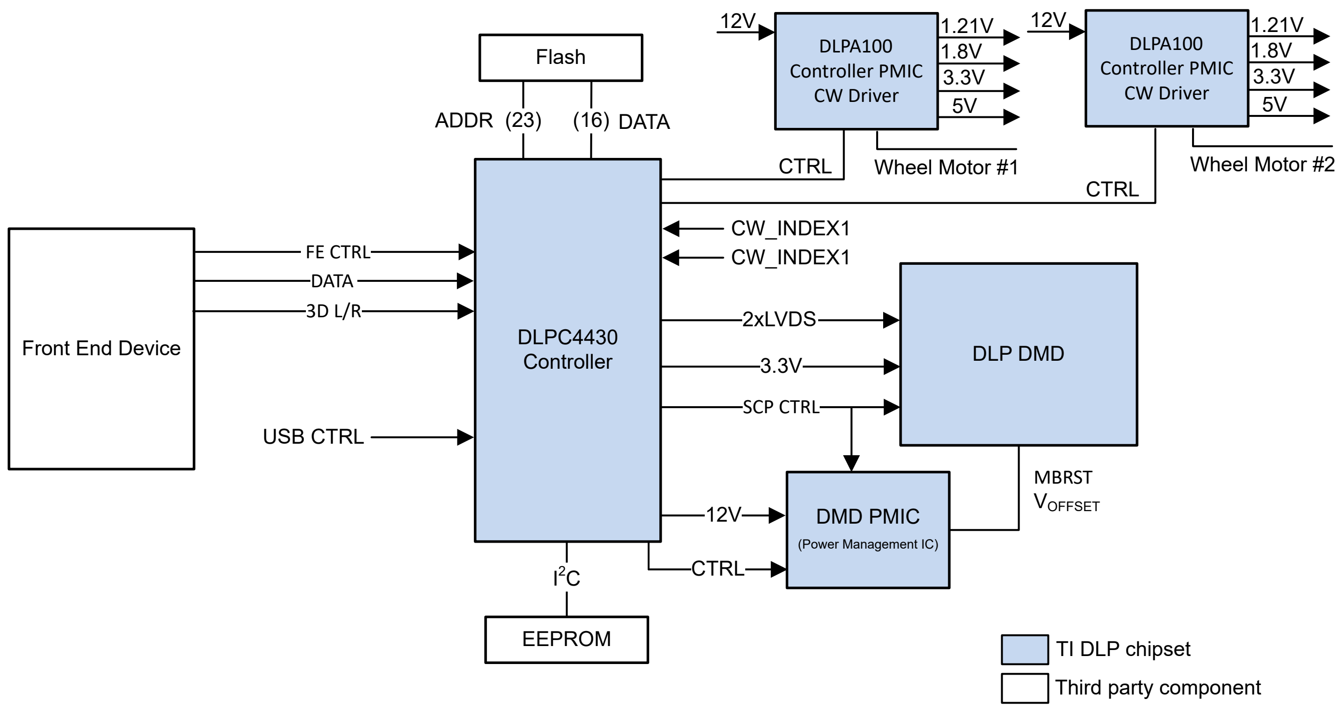


图 7-1. Typical DLPC4430 Application (LED—Top; LPCW—Bottom)

7.2.1 Design Requirements

The DLP 0.65 WXGA chipset can be used to create a powerful projection system. This chipset includes the DLP650LE, DLPC4420, DLPA100, and the DLPA200. The DLP650LE is used as the core imaging device in the display system and contains a 0.65-inch array of micromirrors. The DLPC4420 controller is the digital interface between the DMD and the rest of the system. The controller drives the DMD by taking the converted source data from the front-end receiver and transmitting it to the DMD over a high-speed interface. The DLPA100 power management device provides voltage regulators for the controller and colorwheel motor control. The DLPA200 provides the power and sequencing to drive the DLP650LE. To ensure reliable operation, the DLP650LE DMD must always be used with the DLPC4420 display controller, a DLPA100 PMIC driver, and a DLPA200 DMD micromirror driver.

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser, or laser phosphor. The type of illumination used and desired brightness will have a major effect on the overall system design and size.

7.2.2 Detailed Design Procedure

For help connecting the DLPC4420 display controller and the DLP650LE DMD, see the reference design schematic. For a complete DLP system, an optical module or light engine is required that contains the DLP650LE DMD, associated illumination sources, optical elements, and necessary mechanical components. The optical module is typically supplied by an optical OMM (optical module manufacturer) who specializes in designing optics for DLP projectors.

7.2.3 Application Curve

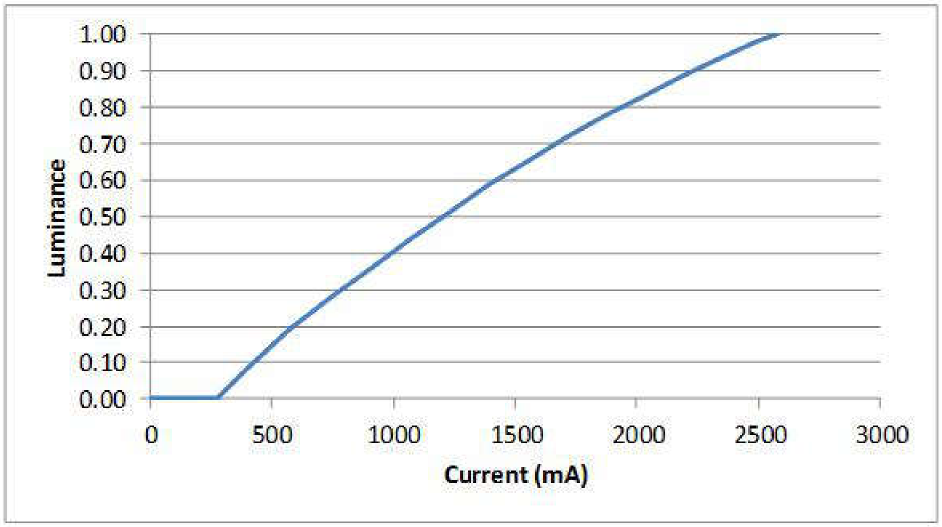


图 7-2. Luminance vs Current

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD: V_{SS}, V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET}. DMD power-up and power-down sequencing are strictly controlled by the DLP display controller.

备注

CAUTION: For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See 图 8-1—DMD Power Supply Sequencing Requirements.

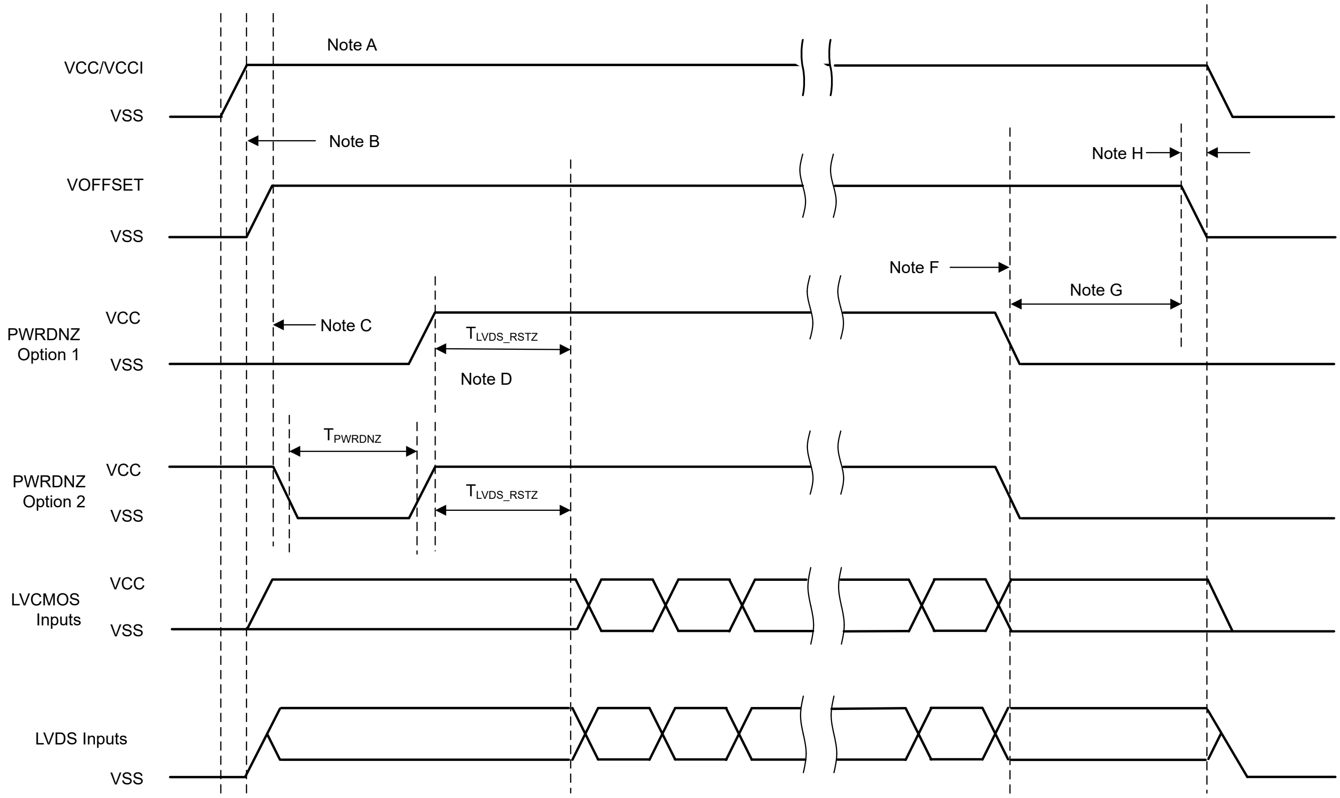
V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD’s reliability and lifetime. Common ground V_{SS} must also be connected.

8.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{CC} and V_{CCI} must always start and settle before V_{OFFSET} is applied to the DMD.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in 节 5.1 and in 节 5.4.
- During power-up, LVCMOS input pins must not be driven high until after V_{CC} and V_{CCI} have settled at the operating voltages listed in 节 5.4 table.

8.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{CC} and V_{CCI} must be supplied until after V_{OFFSET} are discharged to within the specified limit of ground. Refer to 节 5.4.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in 节 5.1 and 节 5.4.
- During power-down, LVCMOS input pins must be less than specified in 节 5.4.



A. See *Pin Configuration and Functions* for pin functions.
B. V_{CC} must be up and stable prior to V_{OFFSET} powering up.
C. PWRDNZ has two turn on options. Option 1: PWRDNZ does not go high until V_{CC} and V_{OFFSET} are up and stable, or Option 2: PWRDNZ must be pulsed low for a minimum of T_{PWRDNZ}, or 10ns after V_{CC} and V_{OFFSET} are up and stable.
D. There is a minimum of T_{LVDS_ARSTZ}, or 2 μs, wait time from PWRDNZ going high for the LVDS receiver to recover.
E. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates the PWRDNZ and disables V_{OFFSET}.
F. Under power-loss conditions, where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, PWRDNZ goes low.
G. V_{CC} must remain high until after V_{OFFSET} goes low.
H. To prevent excess current, the supply voltage delta $|V_{CCI} - V_{CC}|$ must be less than specified limit in the recommended operating conditions.

图 8-1. Power Supply Timing(1)

9 Device and Documentation Support

9.1 第三方产品免责声明

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9.2 Device Support

9.2.1 Device Nomenclature

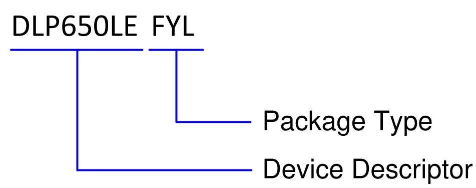


图 9-1. Part Number Description

9.2.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 图 9-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Example: *1280-643AB GHXXXXX LLLLLLM

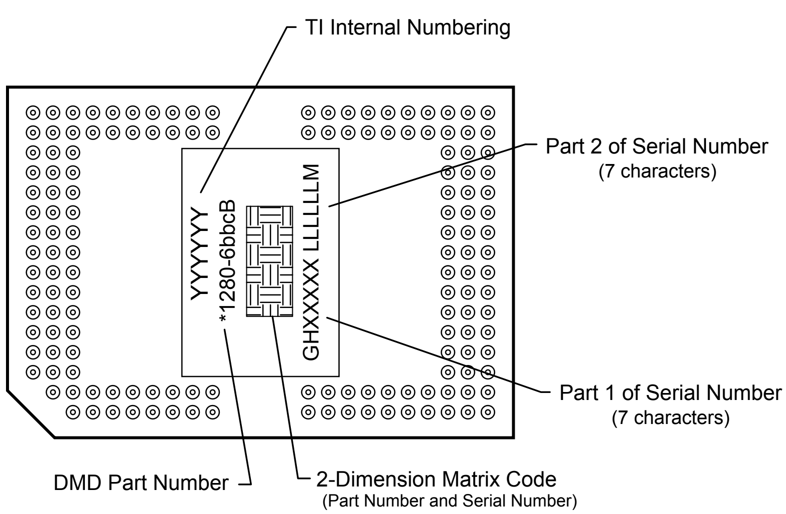


图 9-2. DMD Marking Locations

9.3 Documentation Support

9.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP650LE:

- *DLPC4430 Display Controller Data Sheet*
- *DLPC4420 Display Controller Data Sheet*
- *DLPA100 Power and Motor Driver Data Sheet*

- *DLPA200 Micromirror Driver Data Sheet*

9.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.5 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.7 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.8 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

Changes from Revision A (February 2023) to Revision B (November 2024) **Page**

- 更新了 DLP650LE 的链接......1
- 通篇将主控制器更新为 DLPC4420......1
- 更新了简化版应用图来表示非融合器件......1
- 添加了 DLPC4420 作为支持的显示控制器......1
- 添加了 DLP 产品第三方搜索工具链接，以及 TI DLP 显示技术入门链接......1
- Updated notes to reflect non-fusion device......8
- Expanded and updated table Micromirror Array Optical Characteristics......19
- Updated Function Block Diagram......22
- Updated controller to DLPC4420......23
- Changed Micromirror Array Temperature Calculation......24
- Added section Micromirror Power Density Calculation......25
- Updated Figure to reflect non-fusion device......30
- Updated controller to DLPC4420......31
- Updated section to reflect non-fusion device......33
- Updated Figure and corrected comments from non-fusion related to fusion related. Also removed Transition Points and Delay Timing Requirements tables......33
- Added link to DLPC4420 data sheet......35

Changes from Revision * (November 2017) to Revision A (February 2023)	**Page**
• 将文档状态从“预告信息”更改为“量产数据”	1
• 更新了整个文档中的表格、图和交叉参考的编号格式将控制器更新为 DLPC4430。更新了芯片组元件的链接	1
• 将控制器更新为 DLPC4430	1
• Updated controller to DLPC4430	21
• Updated controller to DLPC4430	23
• Added a table for legacy part numbers and listed the mechanical ICD	30
• Updated controller to DLPC4430	30
• Updated controller to DLPC4430	31
• Updated controller to DLPC4430	31
• Updated controller to DLPC4430, updated the links	35

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP650LEFYL	Active	Production	CLGA (FYL) | 149	33 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	
DLP650LEFYL.B	Active	Production	CLGA (FYL) | 149	33 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

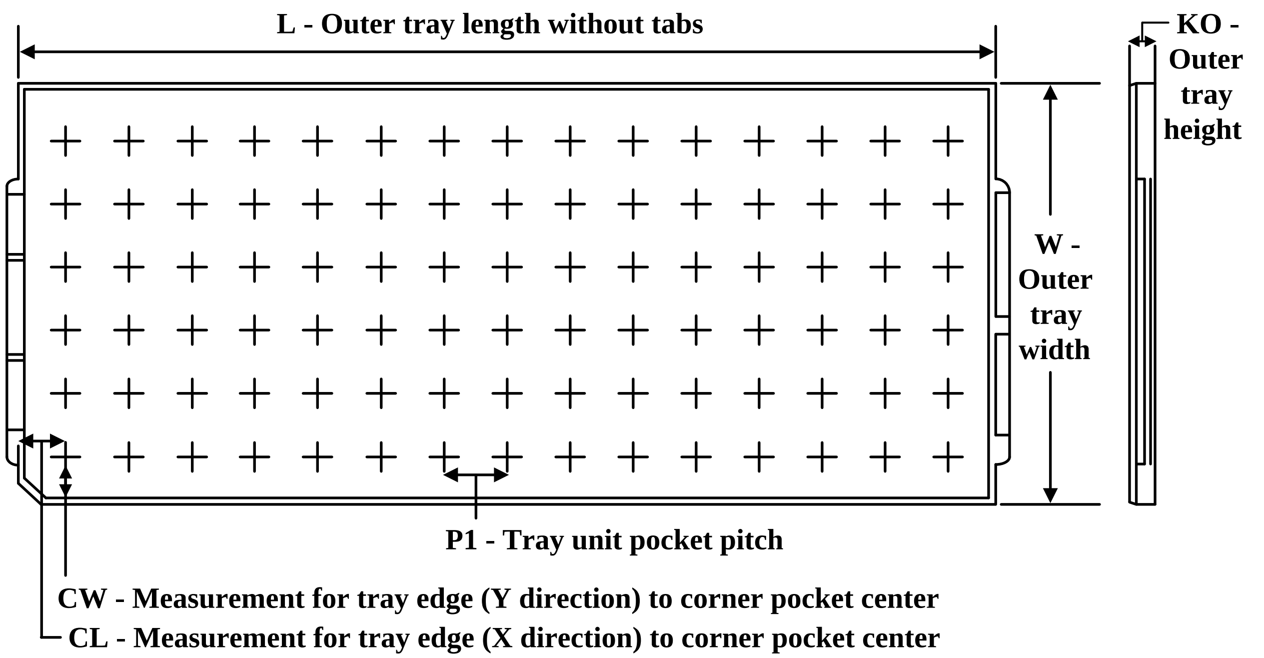
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP650LEFYL	FYL	CLGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45
DLP650LEFYL.B	FYL	CLGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45

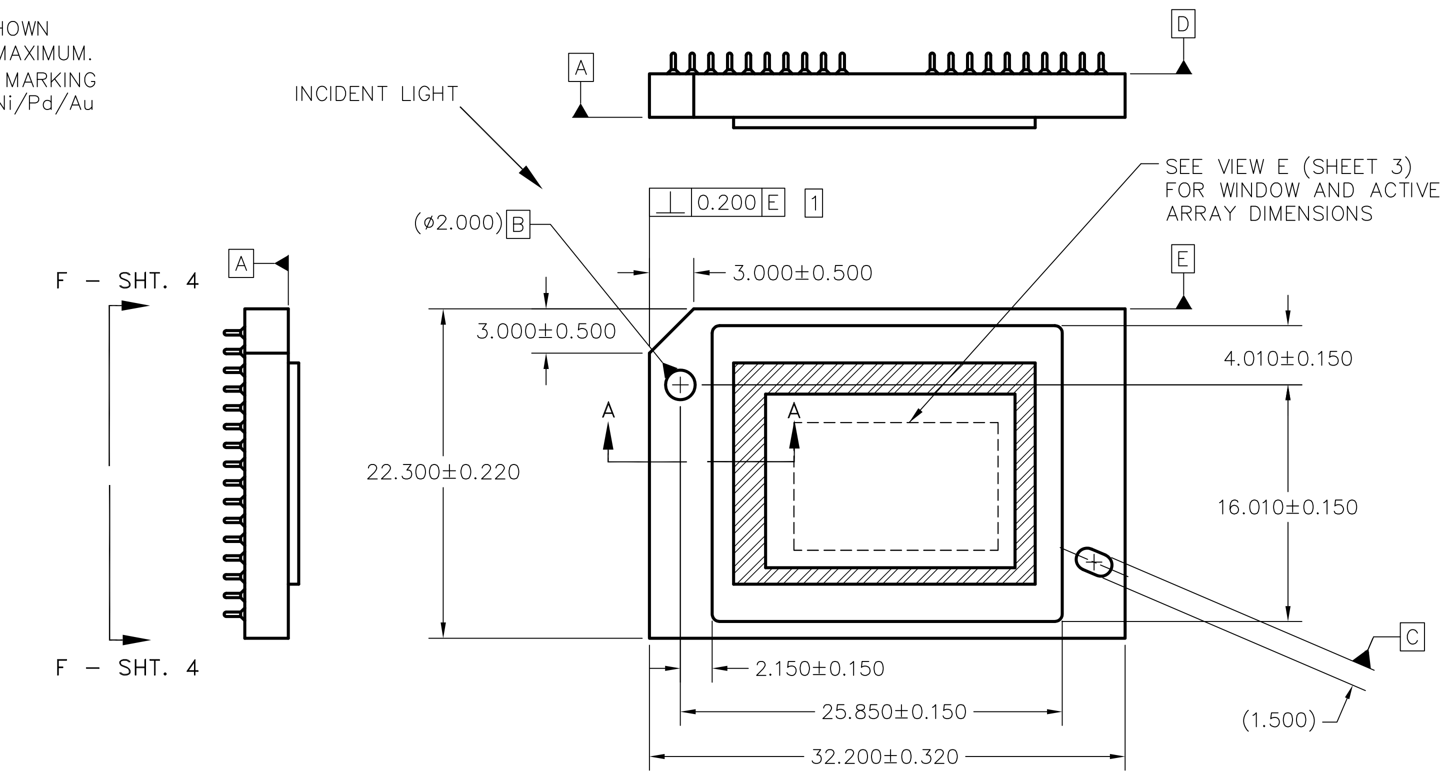
DWG NO 2512372 SH 1

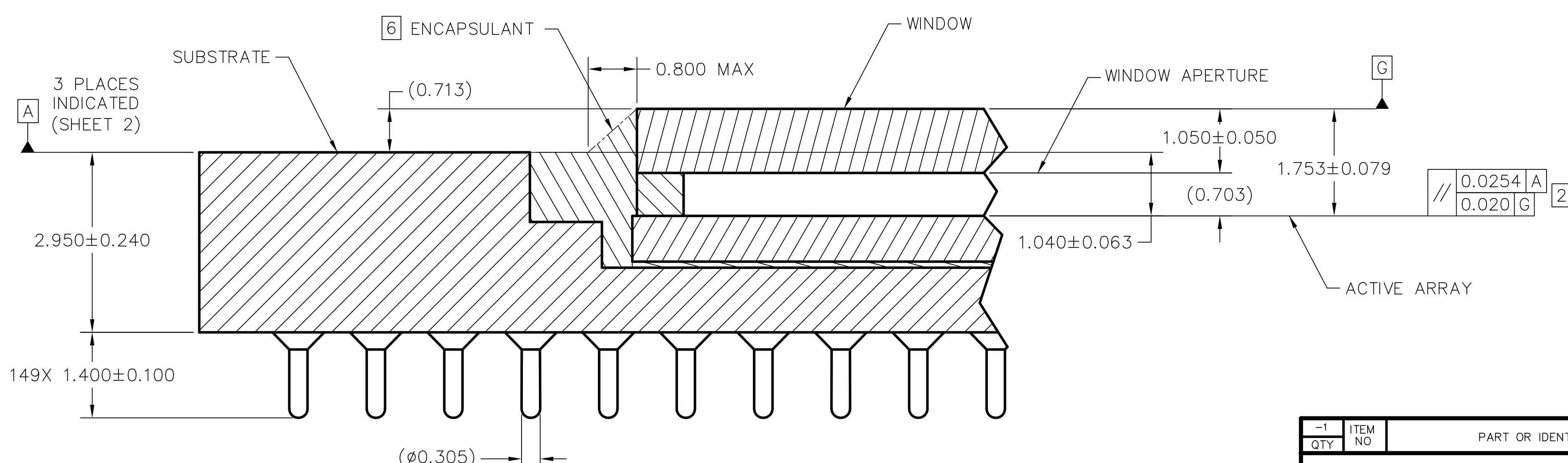
NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2022283, INITIAL RELEASE	02/07/12	F. ARMSTRONG
B	ECO 2123271, CHG TO LARGE SYMBOLIZATION PAD	03/16/12	F. ARMSTRONG
C	ECO 2135104, ADD NOTE 8 TO SHEETS 1 & 4	08/02/13	F. ARMSTRONG
D	ECO 2168423, ADD FYL PACKAGE TO TITLE	08/17/17	M. AVERY





SECTION A–A
SCALE 20/1

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

DWN	F. ARMSTRONG DATE 02/07/12
ENGR	F. ARMSTRONG 02/07/12
QA	P. KONRAD
CE	M. DORAK

THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

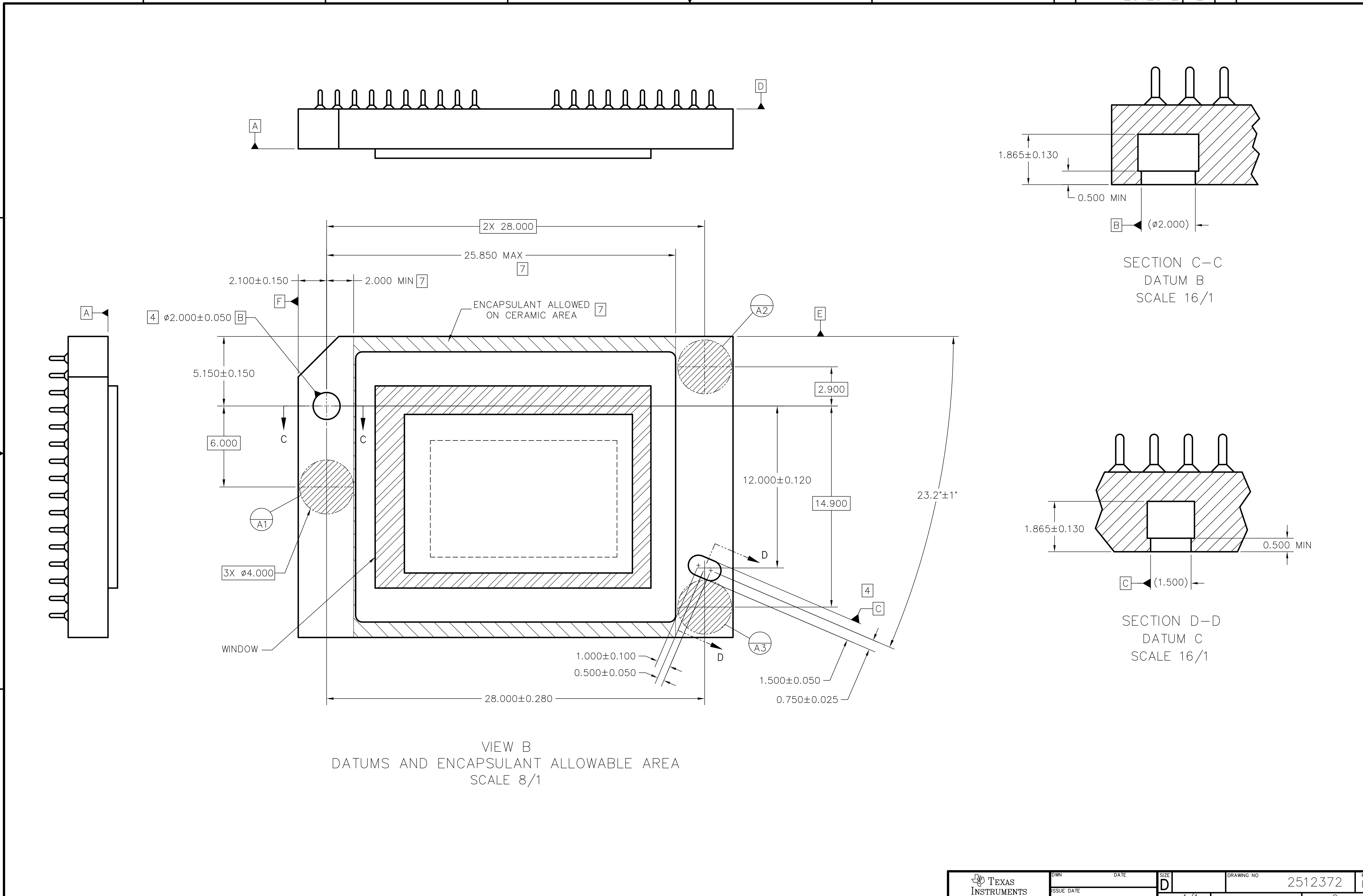
TEXAS INSTRUMENTS
Dallas, Texas

ICD, MECHANICAL, DMD
.65 WXGA-800 2xLVDS V2
SERIES 450 (FYL PACKAGE)

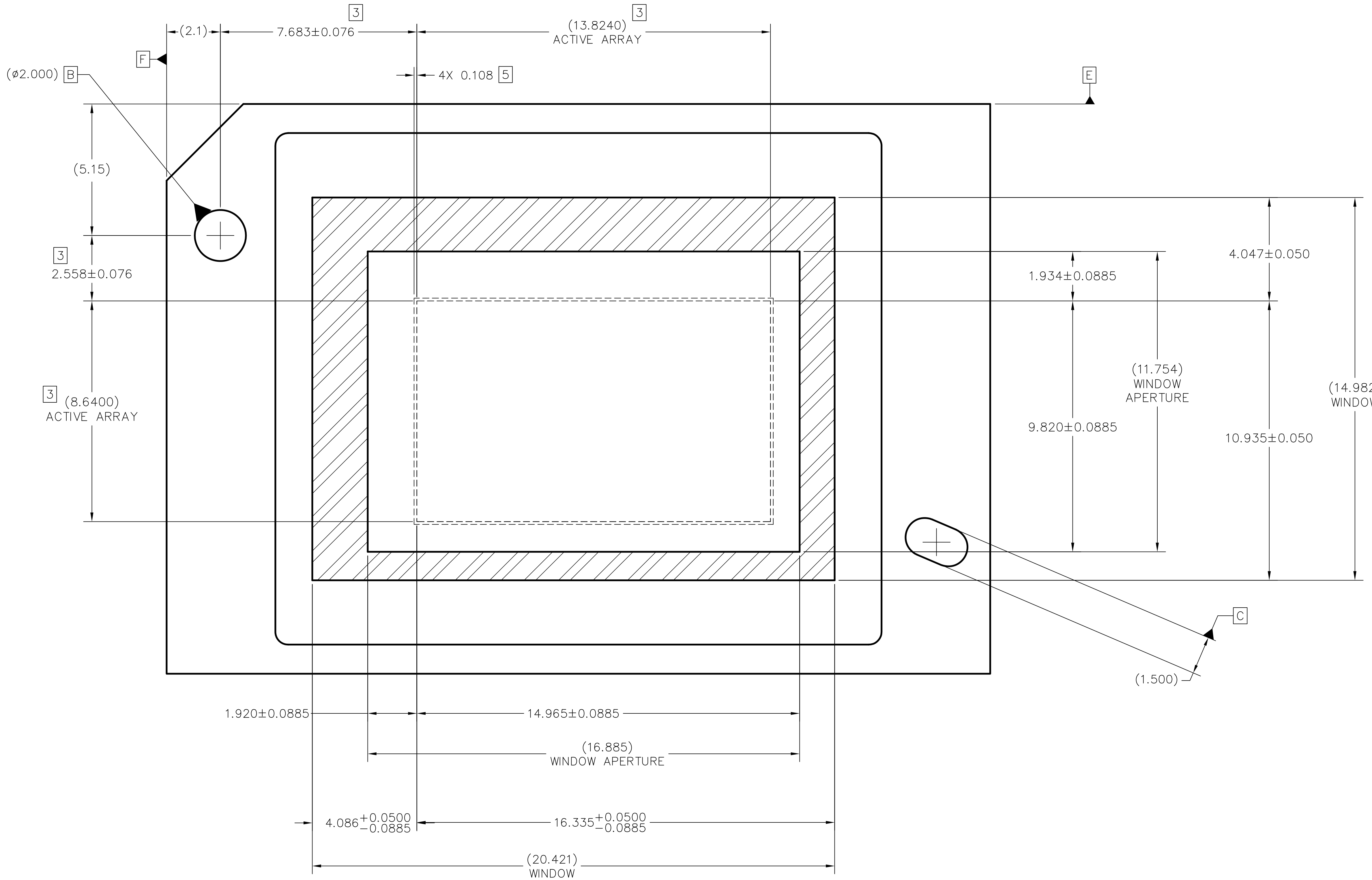
SIZE D | DRAWING NO 2512372 | REV D

SCALE 4/1 | SHEET 1 OF 4

ACED1g

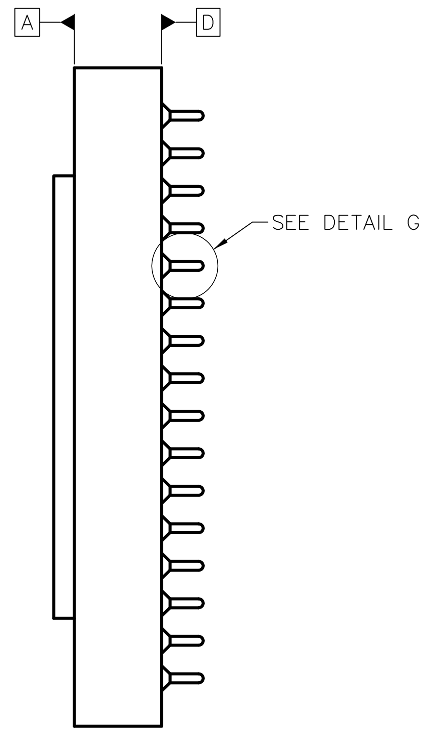


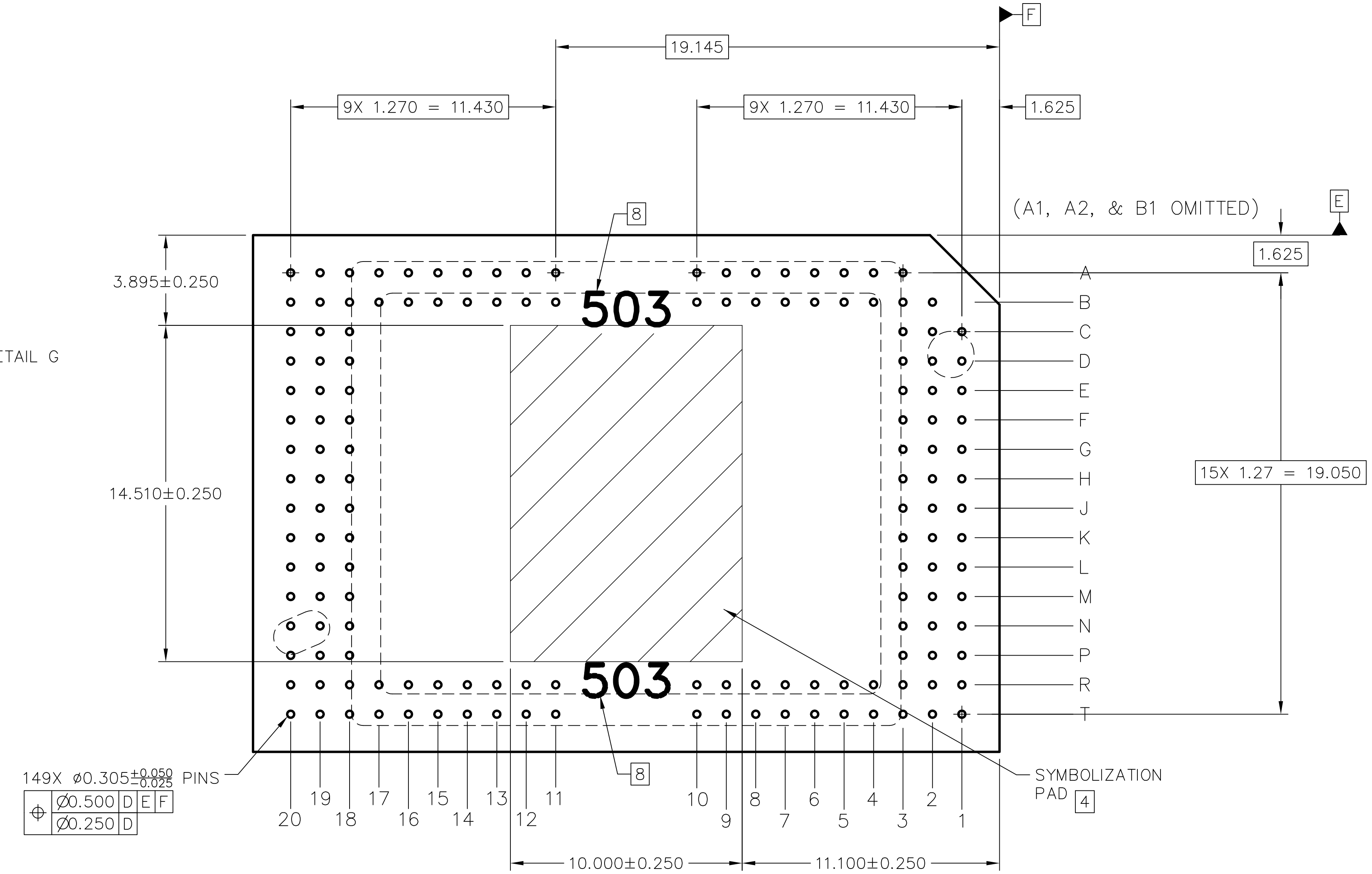
DWG NO 2512372 SH 2
D
A
2.100±0.150
2.000 MIN 7
25.850 MAX 7
2X 28.000
F
A
4 ø2.000±0.050 B
ENCAPSULANT ALLOWED ON CERAMIC AREA 7
A2
E
5.150±0.150
2.900
6.000
C
C
12.000±0.120
14.900
23.2°±1°
A1
3X ø4.000
D
4
C
WINDOW
A3
D
1.000±0.100
0.500±0.050
1.500±0.050
0.750±0.025
28.000±0.280
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1
1.865±0.130
0.500 MIN
B (ø2.000)
SECTION C–C
DATUM B
SCALE 16/1
1.865±0.130
0.500 MIN
C (1.500)
SECTION D–D
DATUM C
SCALE 16/1
TEXAS INSTRUMENTS
Dallas, Texas
DWN
DATE
ISSUE DATE
SIZE D
SCALE 4/1
DRAWING NO 2512372
REV D
SHEET 2
ACED2c



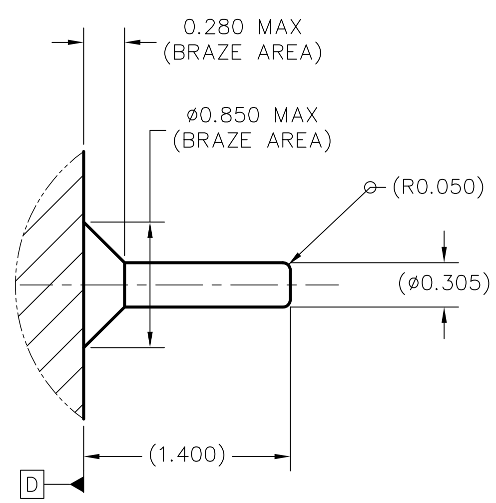
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE	SIZE D	DRAWING NO 2512372	REV D
	ISSUE DATE	SCALE 4/1	SHEET 3	





VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1



DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE	SIZE D	DRAWING NO 2512372	REV D
	ISSUE DATE	SCALE 4/1	SHEET 4	

ACED2c