14-Bit, Serial Input Multiplying Digital-to-Analog Converter

FEATURES

- **14-Bit Monotonic**
- **±1 LSB INL**
- **±0.5 LSB DNL**
- **Low Noise: 12 nV/√Hz**
- **Low Power: I_{DD} = 2 μA**
- **+2.7 V to +5.5 V Analog Power Supply**
- **2 mA Full-Scale Current ±20% with V_{REF} = 10 V**
- **0.5 μs Settling Time**
- **4-Quadrant Multiplying Reference-Input**
- **Reference Bandwidth: 10 MHz**
- **±10 V Reference Input**
- **Reference Dynamics: -105 THD**
- **3-Wire 50-MHz Serial Interface**
- **Tiny 8-Lead 3 x 3 mm SON and 3 x 5 mm MSOP Packages**
- **Industry-Standard Pin Configuration**

APPLICATIONS

- **Automatic Test Equipment**
- **Instrumentation**
- **Digitally Controlled Calibration**
- **Industrial Control PLCs**

DESCRIPTION

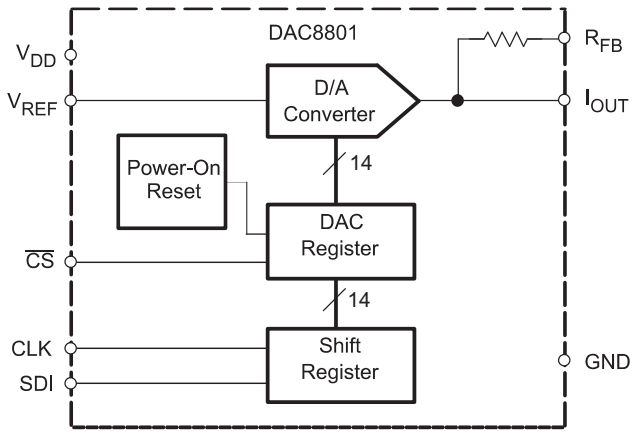
The DAC8801 multiplying digital-to-analog converter is designed to operate from a single 2.7-V to 5.5-V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

A serial-data interface offers high-speed, three-wire microcontroller compatible inputs using data-in (SDI), clock (CLK), and chip select ($\overline{CS}$).

On power-up, the DAC register is filled with zeroes, and the DAC output is at zero scale.

The DAC8801 is packaged in space-saving 8-lead SON and MSOP packages.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION (1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8801	±1	±0.5	MSOP-8	DGK	-40°C to 85°C	F01	DAC8801IDGKT	Tape and Reel, 250
DAC8801	±1	±0.5	MSOP-8	DGK	-40°C to 85°C	F01	DAC8801IDGKR	Tape and Reel, 2500
DAC8801	±1	±0.5	SON-8	DRB	-40°C to 85°C	E01	DAC8801IDRBT	Tape and Reel, 250
DAC8801	±1	±0.5	SON-8	DRB	-40°C to 85°C	E01	DAC8801IDRBR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		DAC8801	UNITS
V_{DD} to GND		–0.3 to 7	V
Digital Input voltage to GND		–0.3 to +V_{DD} + 0.3	V
V_{OUT} to GND		–0.3 to +V_{DD} + 0.3	V
Operating temperature range		–40 to 105	°C
V_{REF}, R_{FB} to GND		–25 to 25	V
Storage temperature range		–65 to 150	°C
Junction temperature range (T_J max)		125	°C
Power dissipation		(T_J max – T_A) / $R_{\Theta JA}$	W
Thermal impedance, $R_{\Theta JA}$		55	°C/W
Lead temperature, soldering	Vapor phase (60s)	215	°C
Lead temperature, soldering	Infrared (15s)	220	°C
ESD rating, HBM		4000	V
ESD rating, CDM		1000	V

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; I_{OUT} = Virtual GND, GND = 0 V; V_{REF} = 10 V; T_A = Full Operating Temperature; all specifications -40°C to 85°C unless otherwise noted.

PARAMETER		CONDITIONS	DAC8801			UNITS
			MIN	TYP	MAX	
STATIC PERFORMANCE						
	Resolution		14			Bits
	Relative accuracy				±1	LSB
	Differential nonlinearity				±0.5	LSB
	Output leakage current	Data = 0000h, T_A = 25°C			10	nA
	Output leakage current	Data = 0000h, $T_A = T_{MAX}$			10	nA
	Full-scale gain error	All ones loaded to DAC register		±1	±4	mV
	Full-scale tempco			±3		ppm of FSR/°C
OUTPUT CHARACTERISTICS(1)						
	Output current			2		mA
	Output capacitance	Code dependent		50		pF
REFERENCE INPUT(1)						
	V_{REF} Range		–15		15	V
	Input resistance			5		kΩ
	Input capacitance			5		pF
LOGIC INPUTS AND OUTPUT(1)						
V_{IL}	Input low voltage	V_{DD} = 2.7V			0.6	V
		V_{DD} = 5V			0.8	V
V_{IH}	Input high voltage	V_{DD} = 2.7V	2.1			V
		V_{DD} = 5V	2.4			V
I_{IL}	Input leakage current				10	µA
C_{IL}	Input capacitance				10	pF
INTERFACE TIMING						
f_{CLK}	Clock input frequency				50	MHz
$t_{(CH)}$	Clock pulse width high		10			ns
$t_{(CL)}$	Clock pulse width low		10			ns
$t_{(CSS)}$	$\overline{CS}$ to Clock setup time		0			ns
$t_{(CSH)}$	Clock to $\overline{CS}$ hold time		10			ns
$t_{(DS)}$	Data setup time		5			ns
$t_{(DH)}$	Data hold time		10			ns
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
	I_{DD} (normal operation)	Logic inputs = 0 V			5	µA
	V_{DD} = 4.5 V to 5.5 V	$V_{IH} = V_{DD}$ and V_{IL} = GND		3	5	µA
	V_{DD} = 2.7 V to 3.6 V	$V_{IH} = V_{DD}$ and V_{IL} = GND		1	2.5	µA
AC CHARACTERISTICS(1)(2)						
t_s	Output voltage settling time	To ±0.1% of full-scale, Data = 0000h to 3FFFh to 0000h		0.3		µs
		To ±0.006% of full-scale, Data = 0000h to 3FFFh to 0000h		0.5		
	Reference multiplying BW	V_{REF} = 5 V_{PP}, Data = 3FFFh		10		MHz
	DAC glitch impulse	V_{REF} = 0 V, Data = 3FFFh to 2000h		2		nV/s
	Feedthrough error	V_{REF} = 100 mV_{RMS}, 100kHz, Data = 0000h		–70		dB
	Digital feedthrough	$\overline{CS}$ = 1 and f_{CLK} = 1MHz		2		nV/s

(1) Specified by design and characterization, not production tested.
(2) All ac characteristic tests are performed in a closed-loop system using the THS4011 I-to-V converter amplifier.

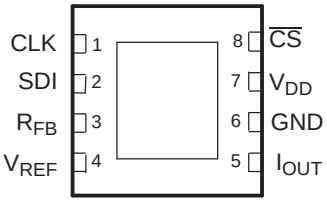
ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 2.7 V to 5.5 V; I_{OUT} = Virtual GND, GND = 0 V; V_{REF} = 10 V; T_A = Full Operating Temperature; all specifications -40°C to 85°C unless otherwise noted.

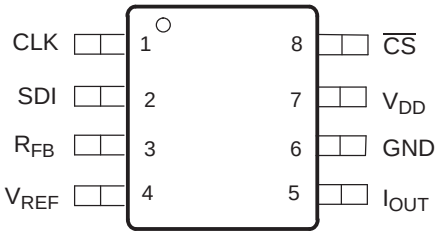
PARAMETER	CONDITIONS	DAC8801			UNITS
		MIN	TYP	MAX	
Total harmonic distortion	V_{REF} = 5 V_{PP}, Data = 3FFFh, f = 1 kHz		–105		dB
Output spot noise voltage	f = 1 kHz, BW = 1 Hz		12		nV/√Hz

PIN ASSIGNMENTS

DRB PACKAGE
(TOP VIEW)



DGK PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

PIN	NAME	DESCRIPTION
1	CLK	Clock input, positive edge triggered clocks data into shift register
2	SDI	Serial register input, data loads directly into the shift register MSB first. Extra leading bits are ignored.
3	R_{FB}	Internal matching feedback resistor. Connect to external op amp output.
4	V_{REF}	DAC reference input pin. Establishes DAC full-scale voltage. Constant input resistance versus code.
5	I_{OUT}	DAC current output. Connects to inverting terminal of external precision I to V op amp.
6	GND	Analog and digital ground
7	V_{DD}	Posiitve power supply input. Specified range of operation 2.7 V to 5.5 V.
8	$\overline{CS}$	Chip select, active low digital input. Transfers shift register data to DAC register on rising edge. See Table 1 for operation.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V

At T_A = 25°C, $+V_{DD}$ = 5 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

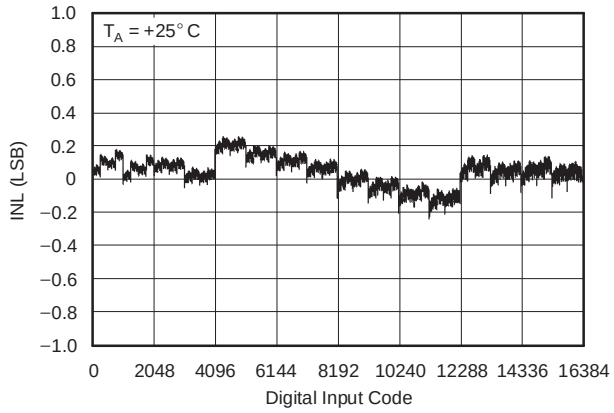


Figure 1.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

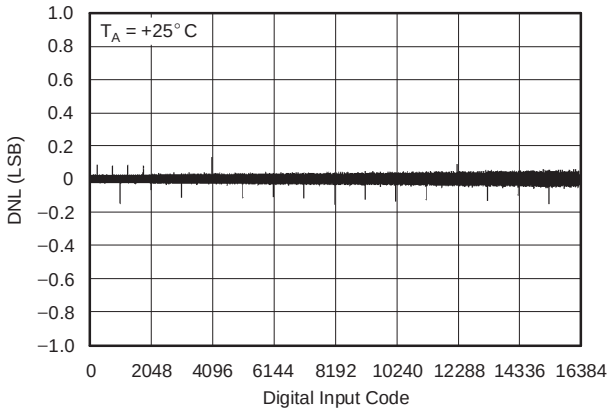


Figure 2.

LINEARITY ERROR vs DIGITAL INPUT CODE

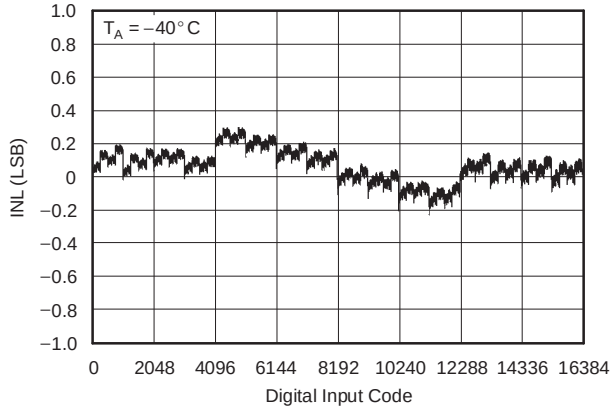


Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

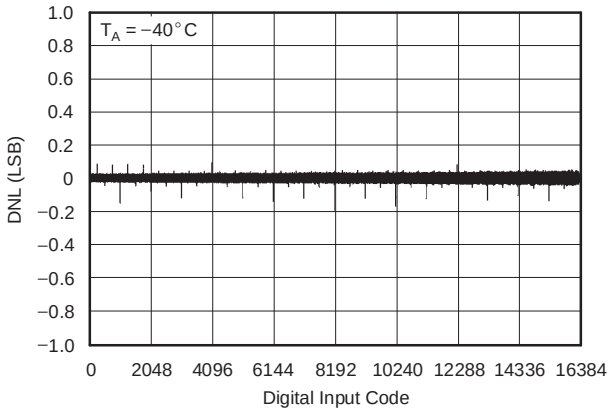


Figure 4.

LINEARITY ERROR vs DIGITAL INPUT CODE

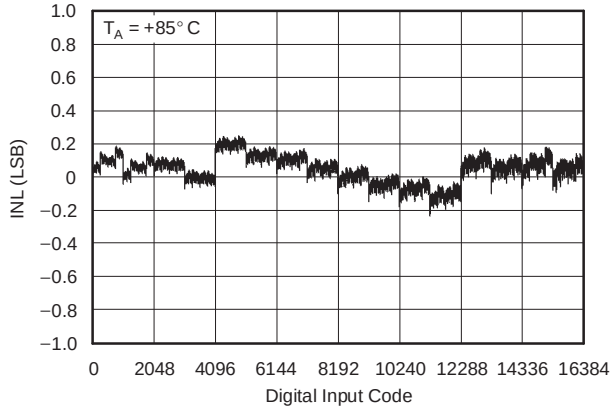


Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

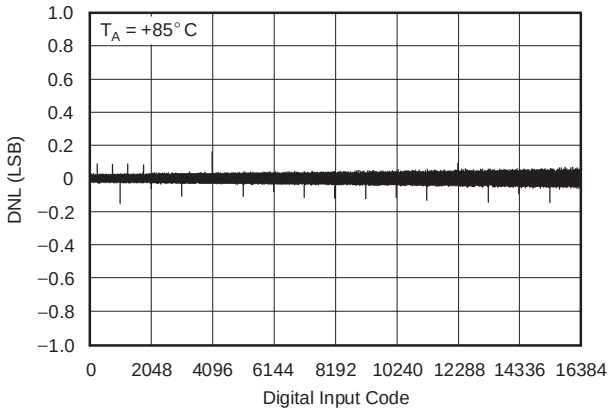


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, +V_{DD} = 5 V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

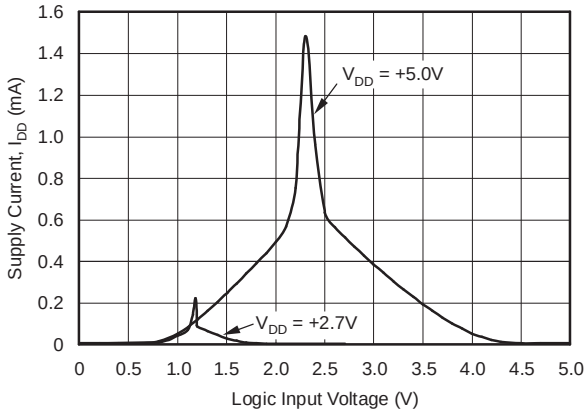


Figure 7.

REFERENCE BANDWIDTH

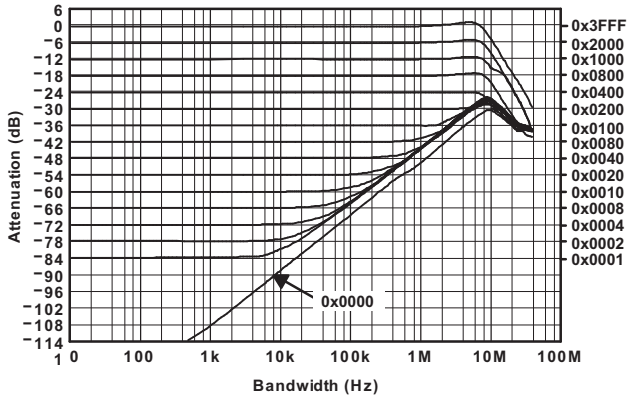


Figure 8.

DAC SETTLING TIME

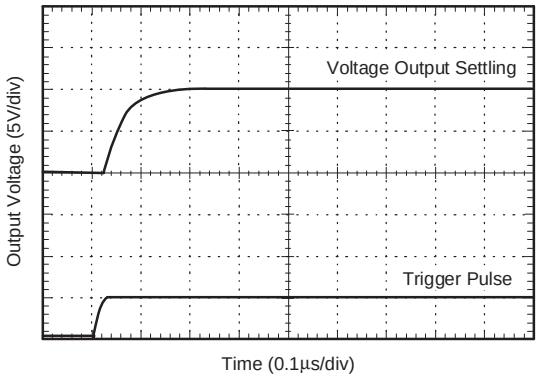


Figure 9.

DAC GLITCH

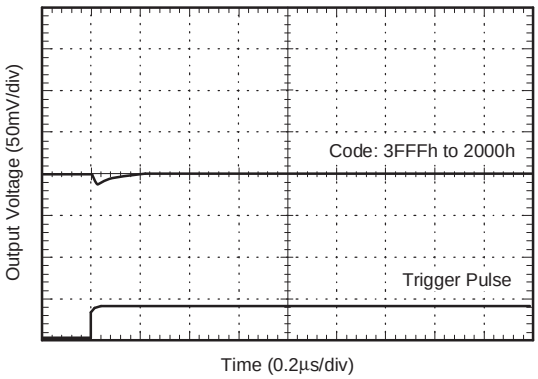


Figure 10.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V

At T_A = 25°C, $+V_{DD}$ = 2.7 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

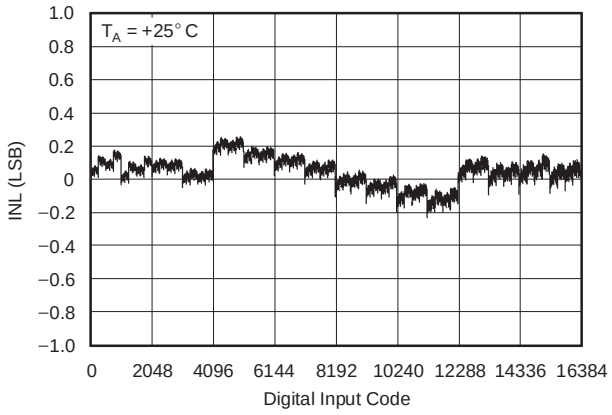


Figure 11.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

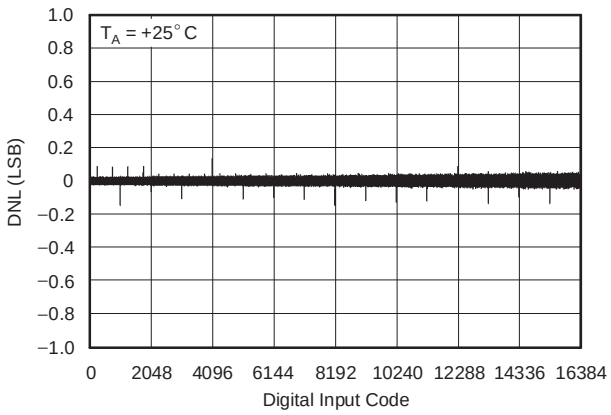


Figure 12.

LINEARITY ERROR vs DIGITAL INPUT CODE

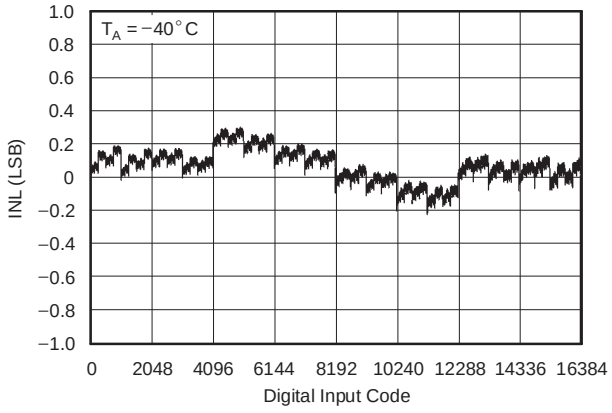


Figure 13.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

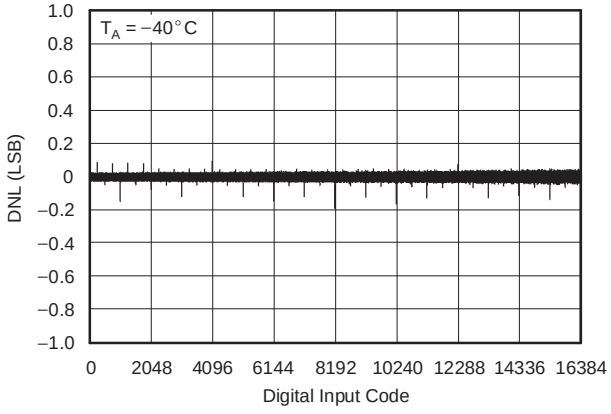


Figure 14.

LINEARITY ERROR vs DIGITAL INPUT CODE

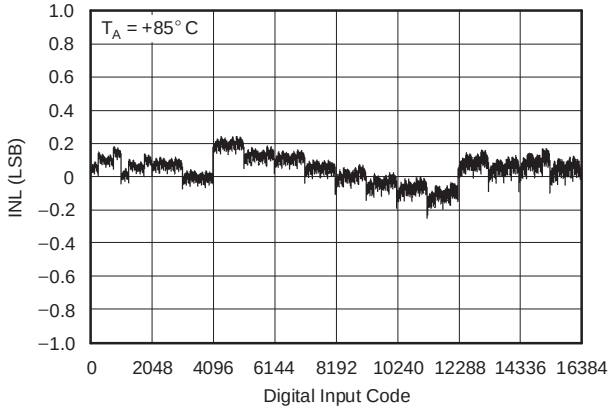


Figure 15.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

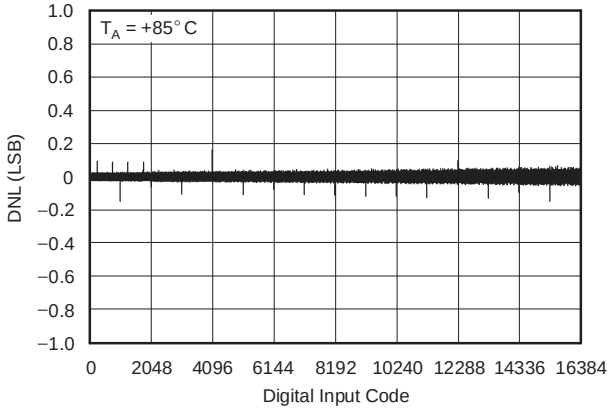


Figure 16.

THEORY OF OPERATION

The DAC8801 is a single channel current output, 16-bit digital-to-analog converter (DAC). The architecture, illustrated in Figure 17, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or the I_{OUT} terminal. The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V_{REF} that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 5 kΩ± 25%. The external reference voltage can vary in a range of -10 V to 10 V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter and the DAC8801 R_{FB} resistor, output voltage ranges of $-V_{REF}$ to V_{REF} can be generated.

When using an external I/V converter and the DAC8801 R_{FB} resistor, the DAC output voltage is given by Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{CODE}{16384} \quad (1)$$

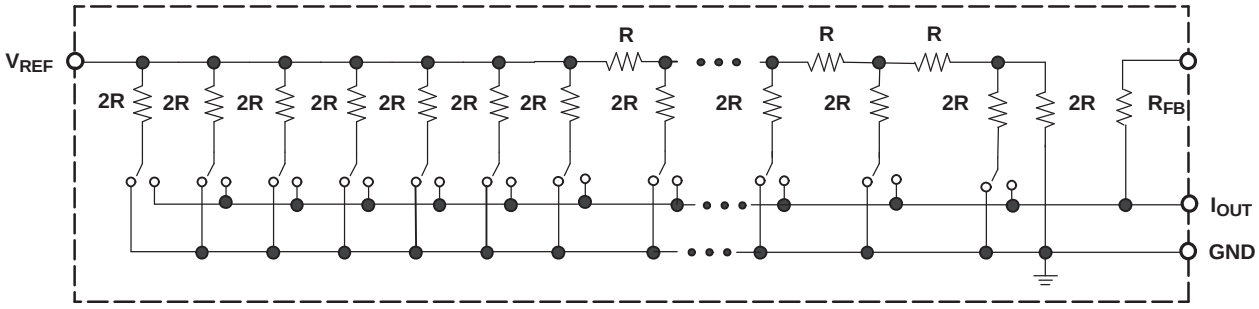


Figure 17. Equivalent R-2R DAC Circuit

Each DAC code determines the 2R leg switch position to either GND or I_{OUT}. Because the DAC output impedance as seen looking into the I_{OUT} terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8801 due to offset modulation versus DAC code. For best linearity performance of the DAC8801, an op amp (OPA277) as shown in Figure 18 is recommended. This circuit allows V_{REF} to swing from -10V to +10V.

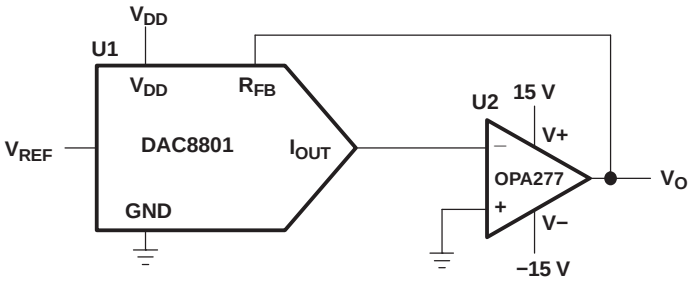


Figure 18. Voltage Output Configuration

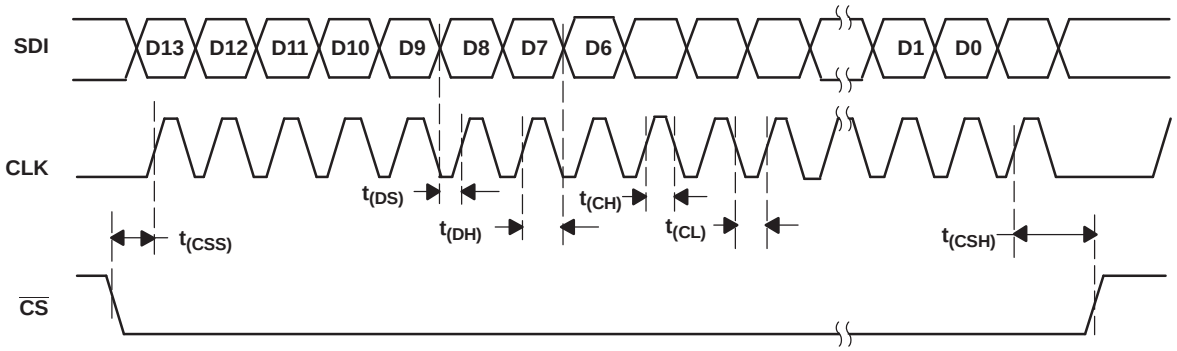


Figure 19. DAC8801 Timing Diagram

Table 1. Control Logic Truth Table(1)

CLK	$\overline{CS}$	Serial Shift Register	DAC Register
X	H	No effect	Latched
↑+	L	Shift register data advanced one bit	Latched
X	H	No effect	Latched
X	↑+	Shift register data transferred to DAC register	New data loaded from serial register

(1) ↑+ Positive logic transition; X = Don't care

Table 1. Serial Input Register Data Format, Data Loaded MSB First

Bit	B13 (MSB)	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data(1)	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) A full 16-bit data word can be loaded into the serial register, but only the last 14 bits are transferred to the DAC register when $\overline{CS}$ goes high.

APPLICATION INFORMATION

Stability Circuit

For a current-to-voltage design as shown in Figure 20, the DAC8801 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct PCB layout design. For each code change there is a step function. If the GBP of the op amp is limited and parasitic capacitance is excessive at the inverting node then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C1 (4 pF to 20 pF typ) can be added to the design as shown in Figure 20.

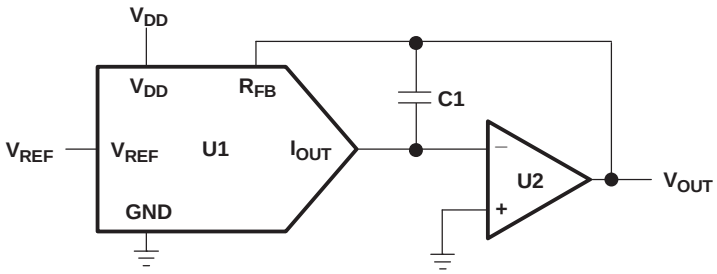


Figure 20. Gain Peaking Prevention Circuit With Compensation Capacitor

Positive Voltage Output Circuit

As shown in Figure 21, in order to generate a positive voltage output, a negative reference is input to the DAC8801. This design is suggested instead of using an inverting amp to invert the output due to tolerance errors of the resistor. For a negative reference, V_{OUT} and GND of the reference are level-shifted to a virtual ground and a -2.5 V input to the DAC8801 with an op amp.

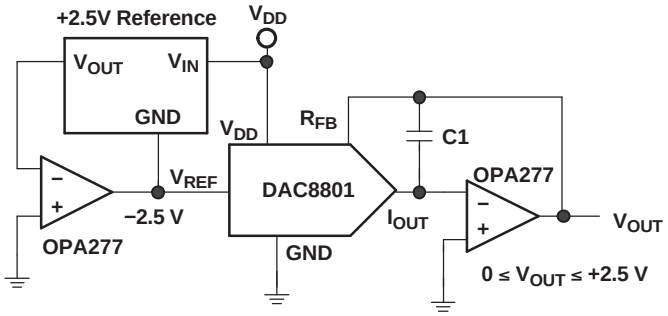


Figure 21. Positive Voltage Output Circuit

APPLICATION INFORMATION (continued)

Bipolar Output Circuit

The DAC8801, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 22, external op amp U4 is added as a summing amp and has a gain of 2X that widens the output span to 5 V. A 4-quadrant multiplying circuit is implemented by using a 2.5-V offset of the reference voltage to bias U4. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full scale produces output voltages of V_{OUT} = -2.5 V to V_{OUT} = 2.5 V.

$$V_{OUT} = \left(\frac{D}{16,384} - 1\right) \times V_{REF} \quad (2)$$

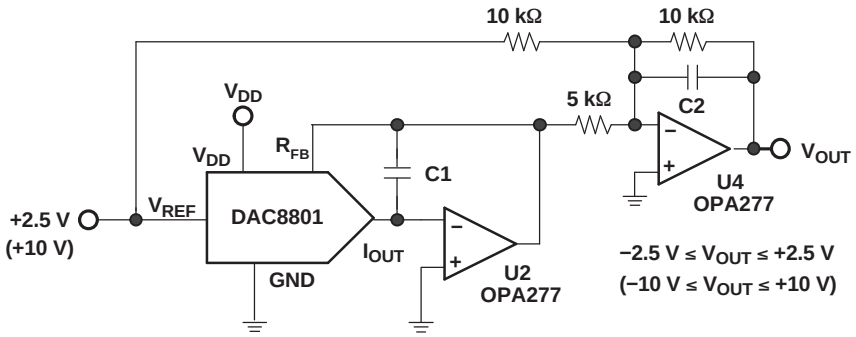


Figure 22. Bipolar Output Circuit

Programmable Current Source Circuit

A DAC8801 can be integrated into the circuit in Figure 23 to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. A application of this circuit includes a 4-mA to 20-mA current transmitter with up to a 500-Ω load. With a matched resistor network, the load current of the circuit is shown in Equation 3:

$$I_L = \frac{(R2 + R3) / R1}{R3} \times V_{REF} \times D \quad (3)$$

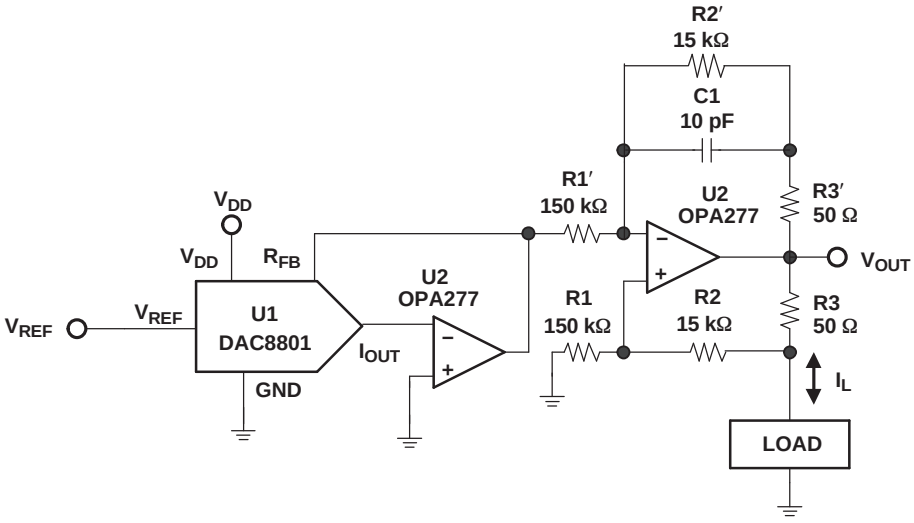


Figure 23. Programmable Bidirectional Current Source Circuit

APPLICATION INFORMATION (continued)

The value of R3 in the previous equation can be reduced to increase the output current drive of U3. U3 can drive ±20 mA in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor C1 in the circuit is not suggested because of the change in the output impedance Z_O, according to Equation 4:

$$Z_O = \frac{R1'R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (4)$$

As shown in Equation 4, with matched resistors, Z_O is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; however, for most applications a value of several pF is suggested.

Cross-Reference

The DAC8801 has an industry-standard pinout. Table 2 provides the cross-reference information.

Table 2. Cross Reference

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCIPTION	PACKAGE OPTION	CROSS REFERENCE
DAC8801IDGK	±1	±1	-40°C to +85°C	8-Lead MicroSOIC	MSOP-8	ADS5553CRM
DAC8801IDRB	±1	±1	-40°C to +85°C	8-Lead Small Outline	SON-8	N/A

Table 3. DAC8801 Revision History

Revision	Date	Description
A	12/04	Removed the "Product Preview" label.
		Added information to the Features.
		Added Output leakage current Data = 0000h, $T_A = T_{MAX}$ in the Electrical Characteristics table.
		Added Input high voltage for 2.7 V and 5 V in the Electrical Characteristics table.
		Changed the values of the *Power Requirements* and the *AC characteristics* in the Electrical Characteristics table.
B	10/06	Changed the ESD rating, HBM from 1500 to 4000 in the Absolute Maximum Ratings.
		Revised Figure 8.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8801IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	F01
DAC8801IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F01
DAC8801IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	F01
DAC8801IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F01
DAC8801IDGKTG4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F01
DAC8801IDRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	E01
DAC8801IDRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	E01
DAC8801IDRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	E01
DAC8801IDRBTG4.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	E01

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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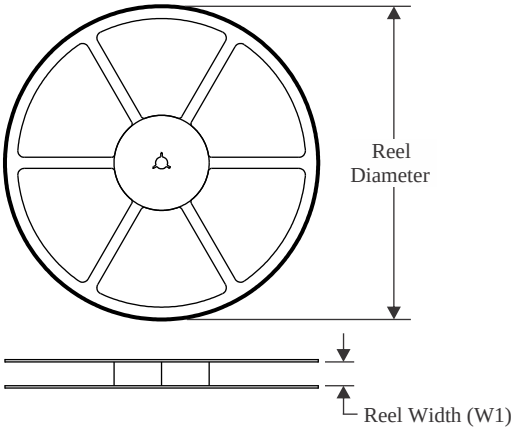
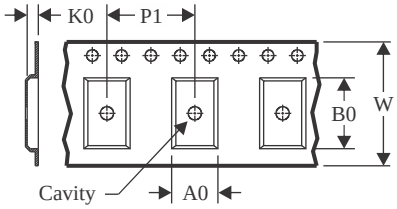
TAPE AND REEL INFORMATION

REEL DIMENSIONS

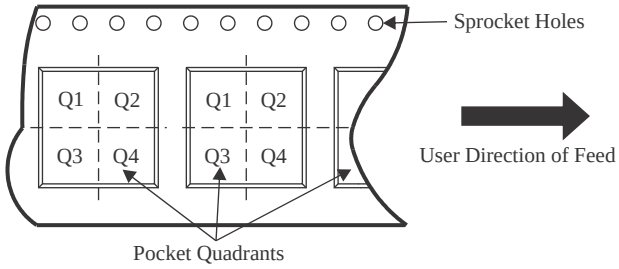


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

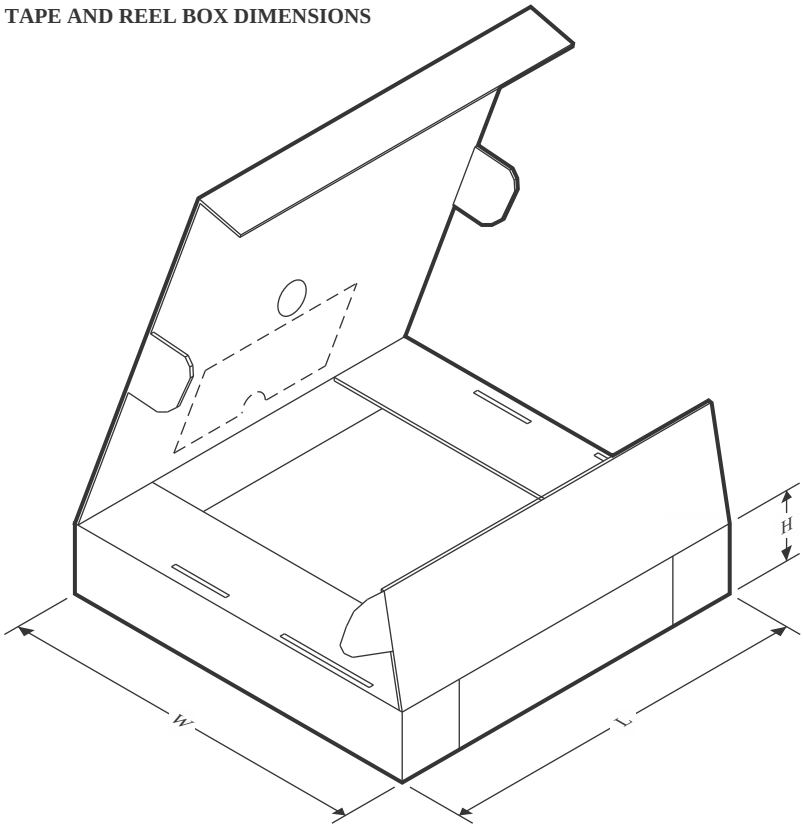
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8801IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8801IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8801IDRBTG4	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8801IDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
DAC8801IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
DAC8801IDRBTG4	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

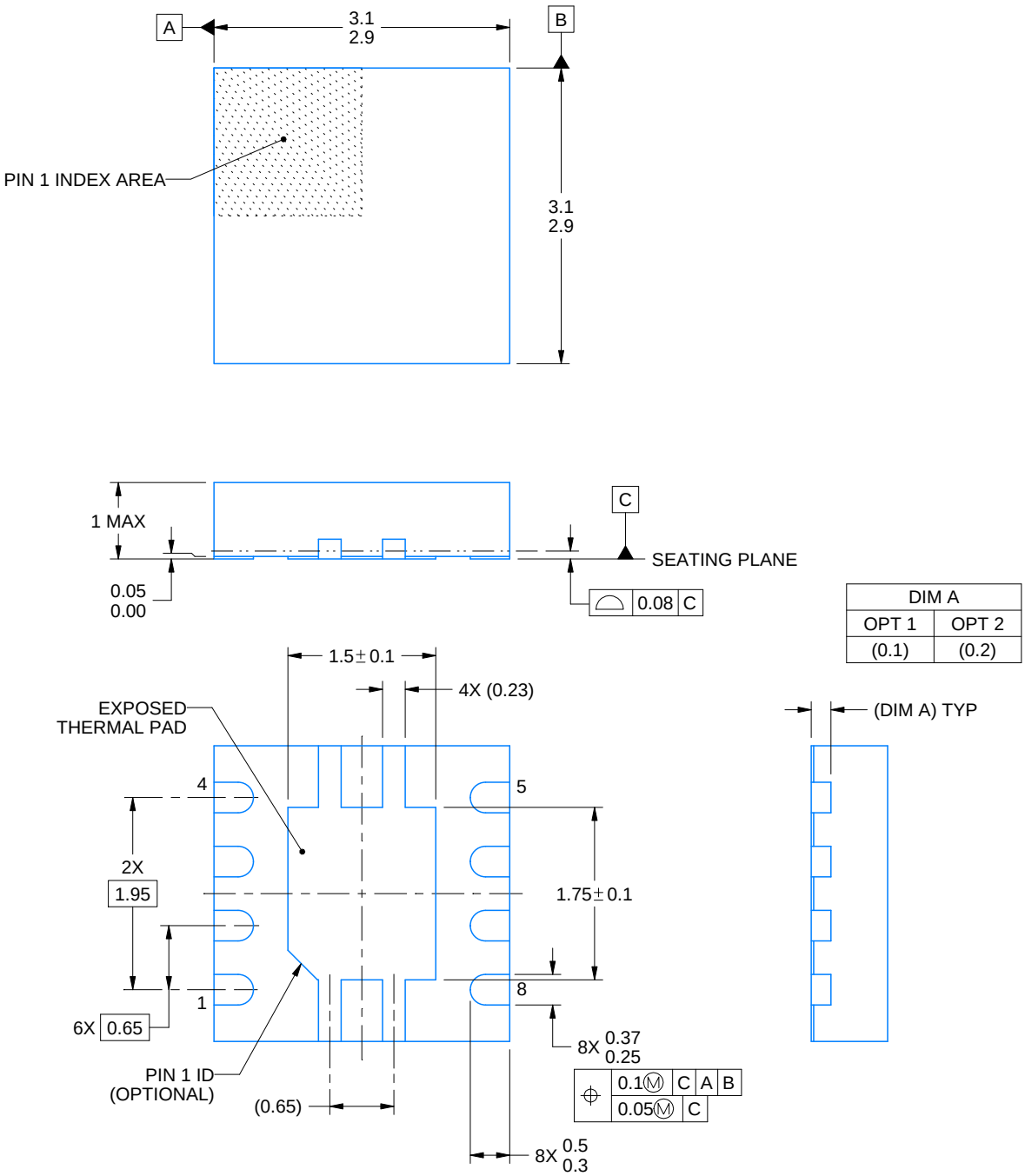
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

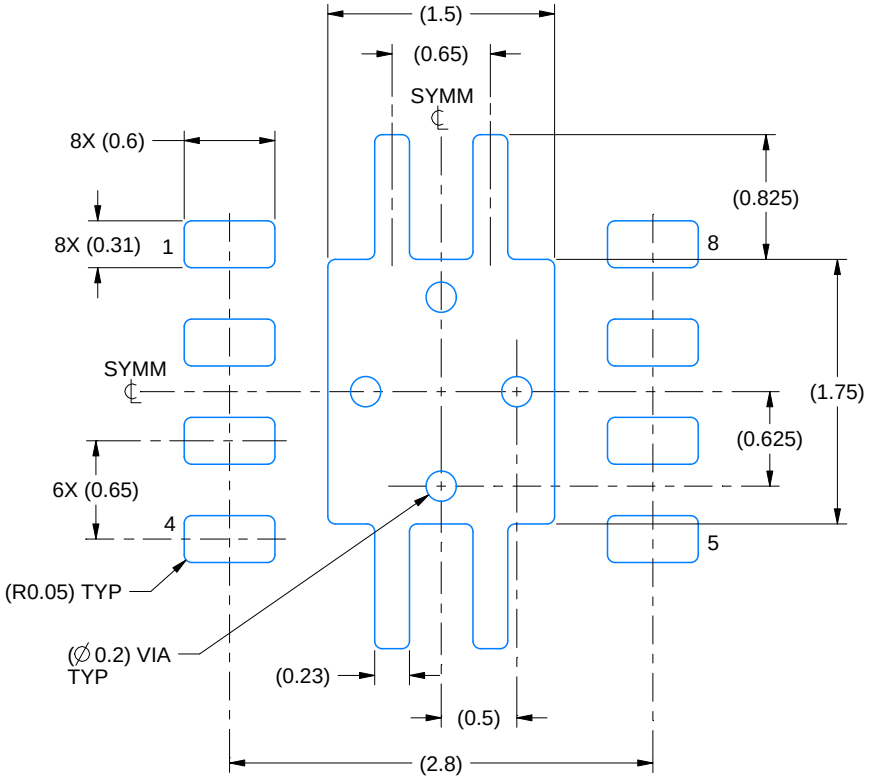
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

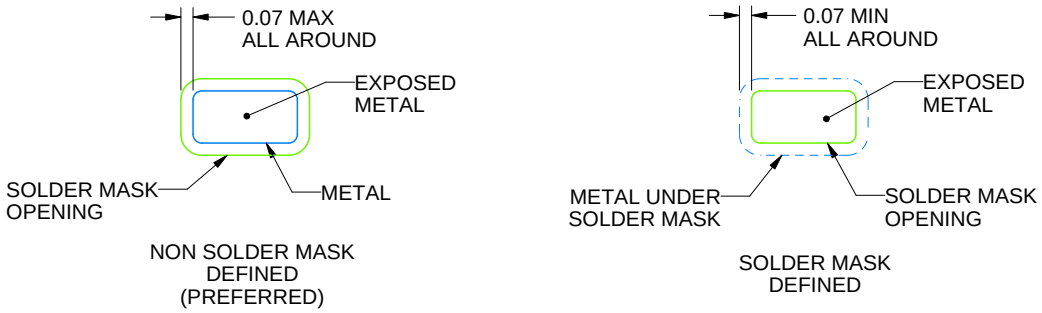
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

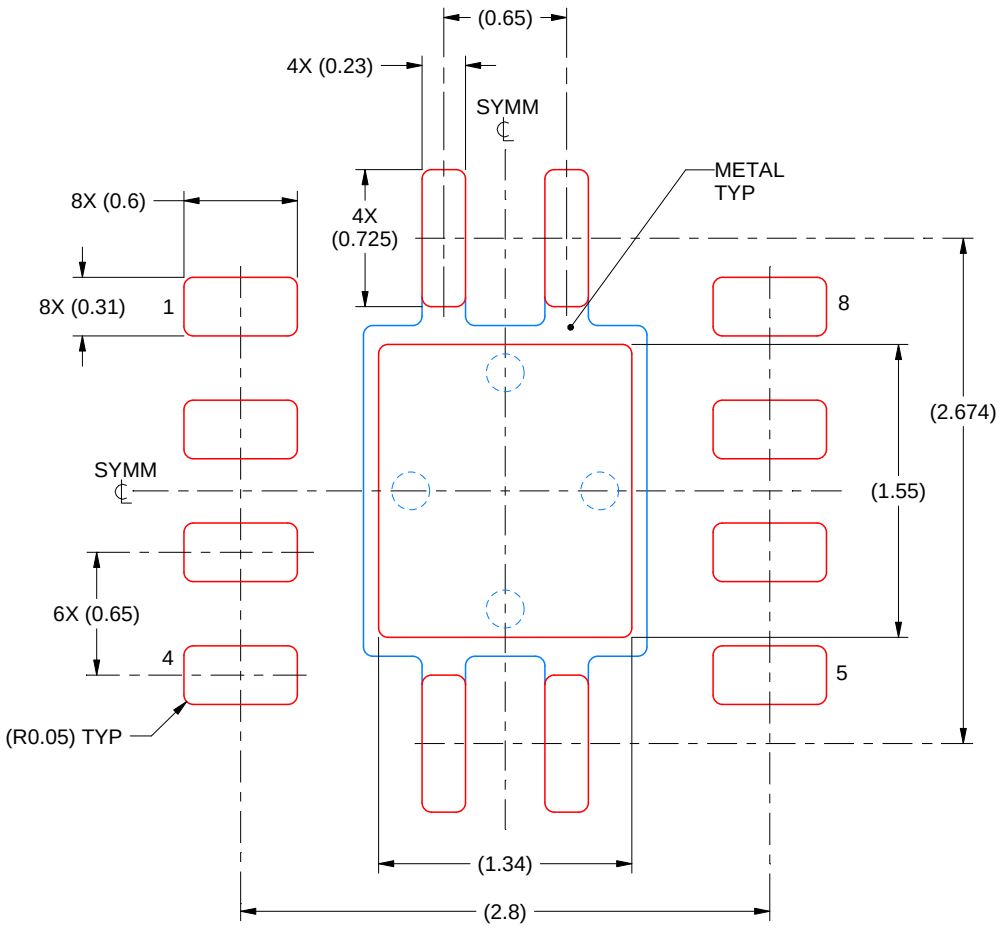


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

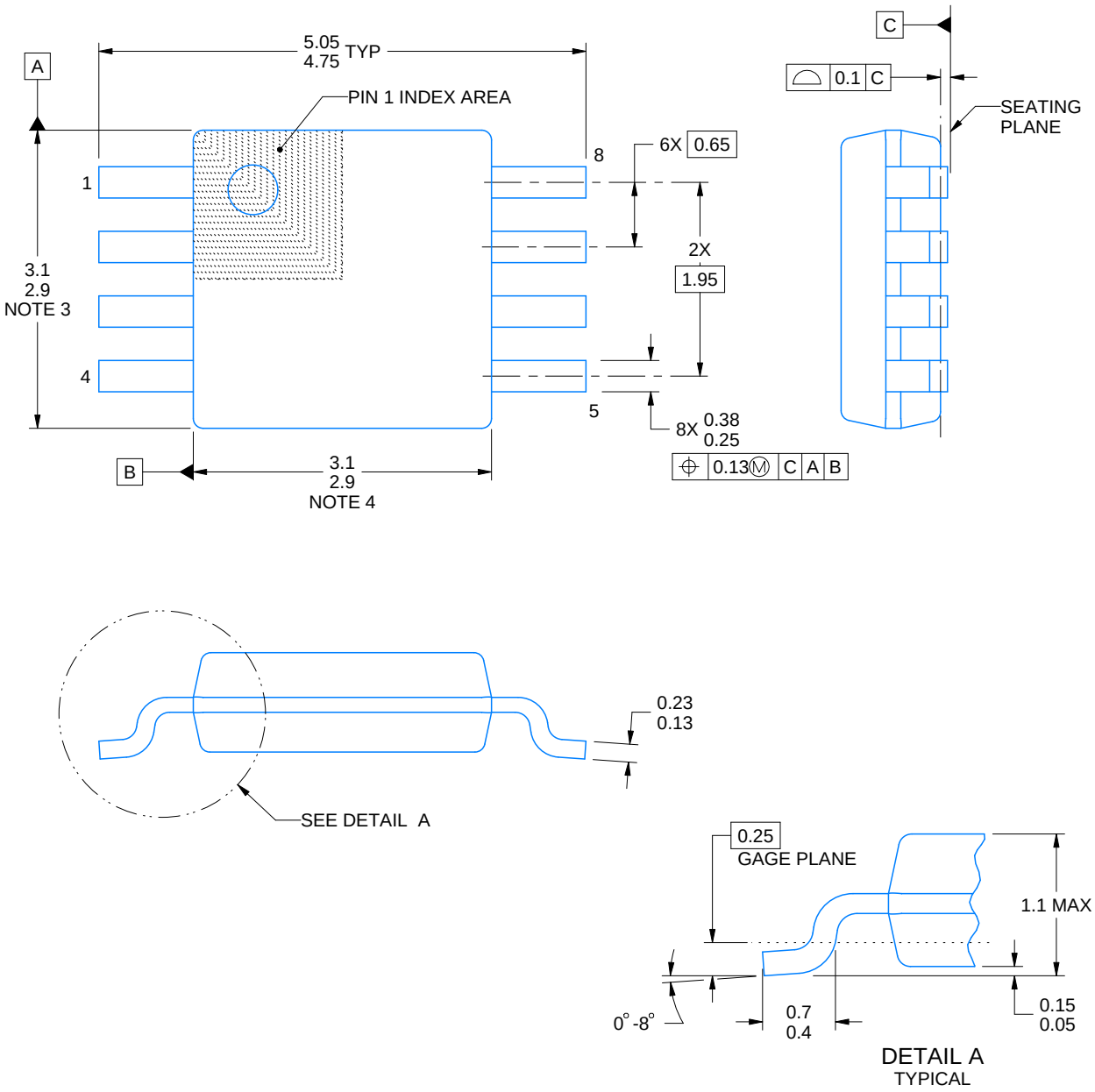
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

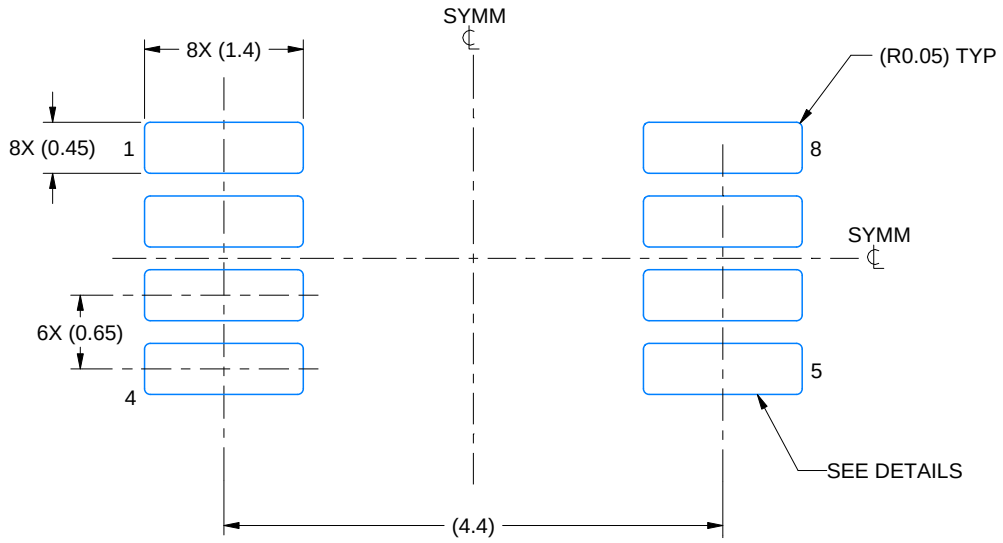
SMALL OUTLINE PACKAGE



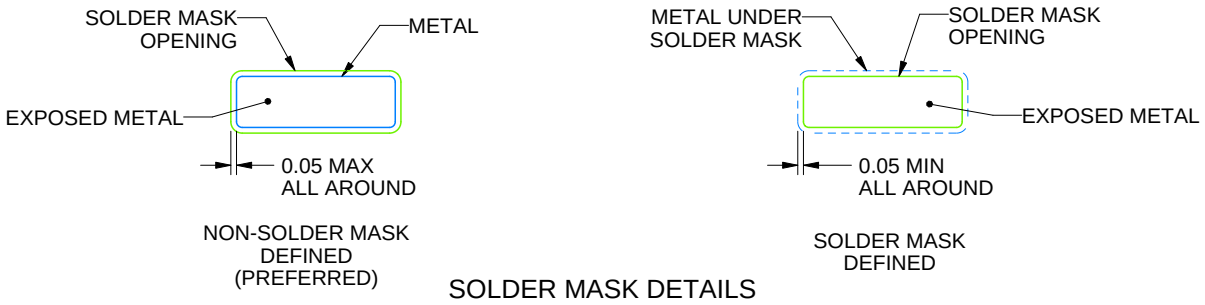
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

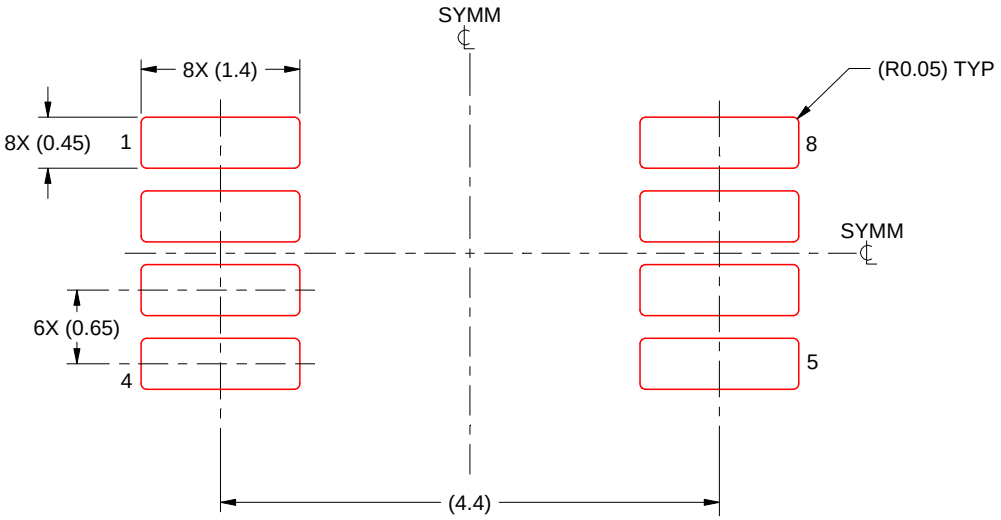


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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