DAC8551-Q1 汽车类 16 位、超低毛刺脉冲、电压输出 DAC

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 相对精度：16 最低有效位 (LSB) 积分非线性 (INL)
- 超低毛刺脉冲：0.1nV-s
- 稳定时间：8μs 达到 ±0.003% 满量程范围 (FSR)
- 电源：3.2V 至 5.5V
- 上电复位为零量程
- 微功耗运行：5V 时为 160μA
- 具有施密特触发输入的低功耗串口
- 支持轨至轨运行的片上输出缓冲放大器
- 掉电能力
- 二进制输入
- SYNC 中断功能
- 采用微型超薄小外形尺寸封装 (VSSOP)-8 封装

2 应用

- 汽车雷达
- 车用传感器

3 说明

DAC8551-Q1 是一款小型、低功耗、电压输出、16 位数模转换器 (DAC)，符合汽车类 应用的需求。DAC8551-Q1 具有出色的线性度，并且最大限度减少了意外的码间瞬态电压。DAC8551-Q1 器件采用时钟速率达 30MHz 的通用三线制串口，并且兼容标准的 SPI、QSPI、Microwire 和数字信号处理器 (DSP) 接口。

DAC8551-Q1 需要使用一个外部基准电压来设置其输出范围。DAC8551-Q1 包含一个上电复位电路，可确保 DAC 输出在 0V 时上电，并在器件被执行有效写操作之前一直保持此状态。DAC8551-Q1 包含一个由串口访问的掉电特性，可将器件在 5V 电压下的电流消耗降低至 800μA。

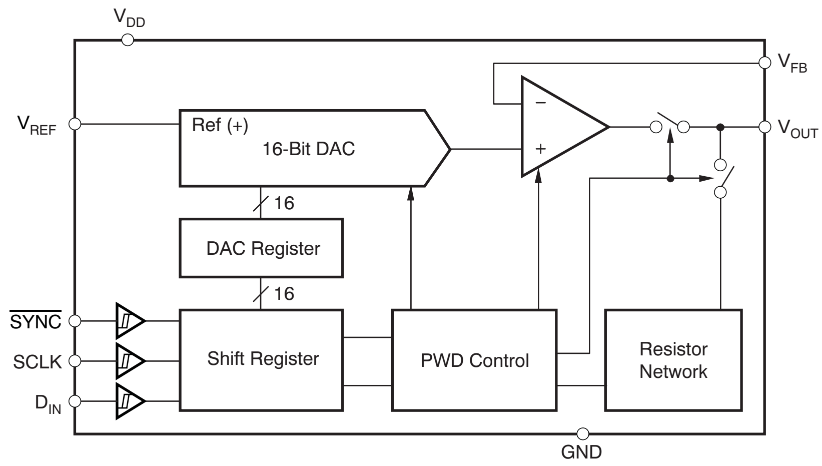
DAC8551-Q1 在 5V 电压下的功耗仅为 800μW，在掉电模式下的功耗降至 4μW 以下。DAC8551-Q1 采用 VSSOP-8 封装。

表 **1.** 器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC8551-Q1	超薄小外形尺寸封装 (VSSOP) (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

DAC8551-Q1 功能框图



目录

4 修订历史记录

Changes from Original (February 2016) to Revision A	Page
• 已将数据表从“产品预览”更改为“量产数据”	1

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View

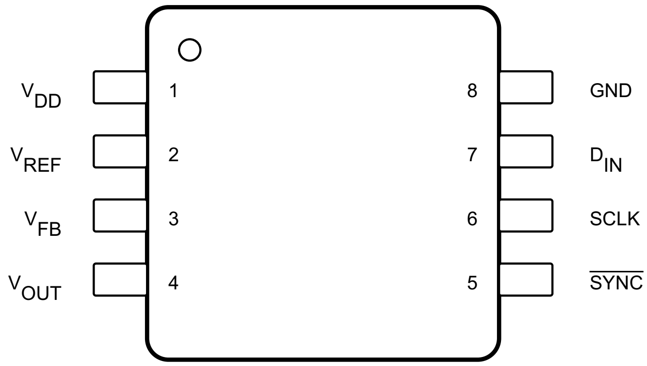


Table 2. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D_{IN}	7	I	Serial data input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-trigger logic input.
GND	8	GND	Ground reference point for all circuitry on the device
SCLK	6	I	Serial clock input. Data can be transferred at rates up to 3 0MHz. Schmitt-trigger logic input.
$\overline{SYNC}$	5	I	Level-triggered control input (active-low). This is the frame synchronization signal for the input data. $\overline{SYNC}$ going low enables the input shift register, and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock (unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the DAC8551-Q1). Schmitt-trigger logic input.
V_{DD}	1	PWR	Power supply input, 3.2 V to 5.5 V.
V_{FB}	3	I	Feedback connection for the output amplifier. For voltage output operation, tie to V_{OUT} externally.
V_{OUT}	4	O	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
V_{REF}	2	I	Reference voltage input.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to GND		–0.3	6	V
Digital input voltage to GND	D_{IN}, SCLK and $\overline{SYNC}$	–0.3	V_{DD} + 0.3	V
V_{OUT} to GND		–0.3	V_{DD} + 0.3	V
V_{REF} to GND		–0.3	V_{DD} + 0.3	V
V_{FB} to GND		–0.3	V_{DD} + 0.3	V
Junction temperature range, T_J max		–65	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Supply voltage	V_{DD} to GND	3.2		5.5	V
DIGITAL INPUTS						
	Digital input voltage	D_{IN}, SCLK and $\overline{SYNC}$	0		V_{DD}	V
REFERENCE INPUT						
V_{REF}	Reference input voltage		0		V_{DD}	V
AMPLIFIER FEEDBACK INPUT						
V_{FB}	Output amplifier feedback input			V_{OUT}		V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		DAC8551-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	173.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{DD} = 3.2 V to 5.5 V, V_{REF} = V_{DD} and T_A = –40°C to 125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE[1]						
	Resolution		16			Bits
	Relative accuracy			±4	±16	LSB
	Differential nonlinearity			±0.35	±2	LSB
	Offset error			±1	±15	mV
	Full-scale error			±0.05	±0.5	% of FSR
	Gain error			±0.02	±0.2	% of FSR
	Offset error drift			±5		μV/°C
	Gain temperature coefficient			±1		ppm of FSR/°C
PSRR	Power-supply rejection ratio	R_L = 2 kΩ, C_L = 200 pF		0.75		mV/V

(1) Linearity calculated using a reduced code range of 485 to 64,741; output unloaded.

Electrical Characteristics (continued)

V_{DD} = 3.2 V to 5.5 V, V_{REF} = V_{DD} and T_A = –40°C to 125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS(2)						
	Output voltage range		0		V_{REF}	V
	Output voltage settling time	To ±0.003% FSR, 0200h to FD00h R_L = 2 kΩ, 0 pF < C_L < 200 pF		8		μs
	Slew rate			1.4		V/μs
	Capacitive load stability	R_L = ∞		470		pF
		R_L = 2 kΩ		1000		pF
	Code change glitch impulse	1 LSB change around major carry		0.1		nV-s
	Digital feedthrough	50 kΩ series resistance on digital lines		0.1		nV-s
	DC output impedance	At mid-code input		1		Ω
	Short-circuit current	V_{DD} = 3.2 V to 5.5 V		35		mA
AC PERFORMANCE						
SNR	Signal-to-noise ratio	BW = 20 kHz, V_{DD} = 5 V, V_{REF} = 4.5 V, f_{OUT} = 1 kHz First 19 harmonics removed for SNR calculation		84		dB
THD	Total harmonic distortion			–80		dB
SFDR	Spurious-free dynamic range			84		dB
SINAD	Signal to noise and distortion			76		dB
REFERENCE INPUT						
	Reference current	V_{REF} = V_{DD} = 5.5 V		50		μA
		V_{REF} = V_{DD} = 3.6 V		25		
	Reference input range		0		V_{DD}	V
	Reference input impedance			125		kΩ
LOGIC INPUTS(2)						
Input current				±1		μA
$V_{IN}L$	Input low voltage	V_{DD} = 5 V			0.3×V_{DD}	V
		V_{DD} = 3.3 V			0.1×V_{DD}	
$V_{IN}H$	Input high voltage	V_{DD} = 5 V	0.7×V_{DD}			V
		V_{DD} = 3.3 V	0.9×V_{DD}			
	Pin capacitance			3		pF
POWER REQUIREMENTS						
V_{DD}	Supply voltage		3.2		5.5	V
I_{DD}	Supply current	Normal mode, input code = 32,768, no load, does not include reference current. V_{IH} = V_{DD} and V_{IL} = GND, V_{DD} = 3.6 V to 5.5 V		160	250	μA
		Normal mode, input code = 32,768, no load, does not include reference current. V_{IH} = V_{DD} and V_{IL} = GND, V_{DD} = 3.2 V to 3.6 V		110	240	
		All power-down modes, V_{IH} = V_{DD} and V_{IL} = GND, V_{DD} = 3.6 V to 5.5 V		0.8	3	
		All power-down modes, V_{IH} = V_{DD} and V_{IL} = GND, V_{DD} = 3.2 V to 3.6 V		0.5	3	
POWER EFFICIENCY						
	I_{OUT} / I_{DD}	I_{LOAD} = 2 mA, V_{DD} = 5 V		89%		
TEMPERATURE RANGE						
T_A	Ambient temperature		–40		125	°C

(2) Specified by design and characterization; not production tested.

6.6 Timing Requirements[(1)(2)]

V_{DD} = 3.2 V to 5.5 V and T_A = –40°C to 125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency	V_{DD} = 3.2 V to 3.6 V			25	MHz
		V_{DD} = 3.6 V to 5.5 V			30	
t_1	SCLK cycle time	V_{DD} = 3.2 V to 3.6 V	40			ns
		V_{DD} = 3.6 V to 5.5 V	34			
t_2	SCLK high time	V_{DD} = 3.2 V to 3.6 V	13			ns
		V_{DD} = 3.6 V to 5.5 V	13			
t_3	SCLK low time	V_{DD} = 3.2 V to 3.6 V	22.5			ns
		V_{DD} = 3.6 V to 5.5 V	13			
t_4	$\overline{\text{SYNC}}$ to SCLK rising edge setup time	V_{DD} = 3.2 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_5	Data setup time	V_{DD} = 3.2 V to 3.6 V	5			ns
		V_{DD} = 3.6 V to 5.5 V	5			
t_6	Data hold time	V_{DD} = 3.2 V to 3.6 V	5			ns
		V_{DD} = 3.6 V to 5.5 V	5			
t_7	24th SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	V_{DD} = 3.2 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_8	Minimum $\overline{\text{SYNC}}$ high time	V_{DD} = 3.2 V to 3.6 V	50			ns
		V_{DD} = 3.6 V to 5.5 V	34			
t_9	24th SCLK falling edge to $\overline{\text{SYNC}}$ falling edge	V_{DD} = 3.2 V to 5.5 V	50			ns

(1) All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
(2) See the *Serial-Write-Operation Timing Diagram*.

6.7 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time	Coming out of power-down mode, V_{DD} = 5 V		2.5		µs
	Coming out of power-down mode, V_{DD} = 3.3 V		5		

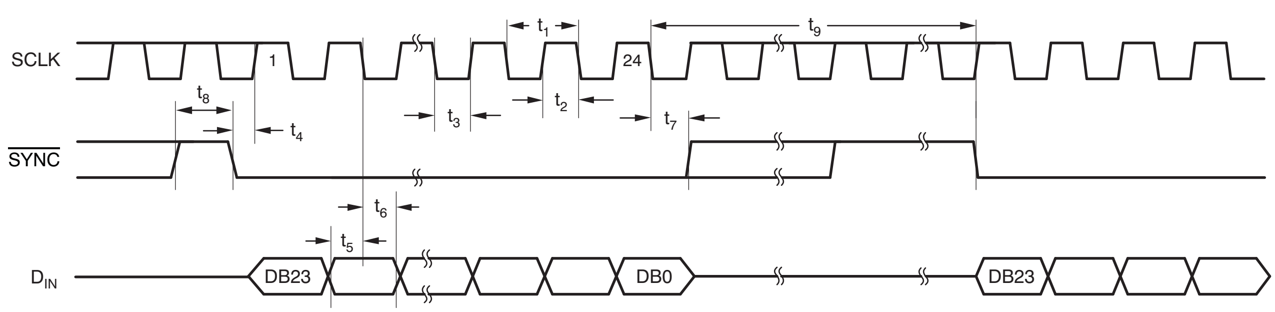


Figure 1. Serial-Write-Operation Timing Diagram

6.8 Typical Characteristics

At T_A = 25°C, V_{DD} = 5 V unless otherwise noted.

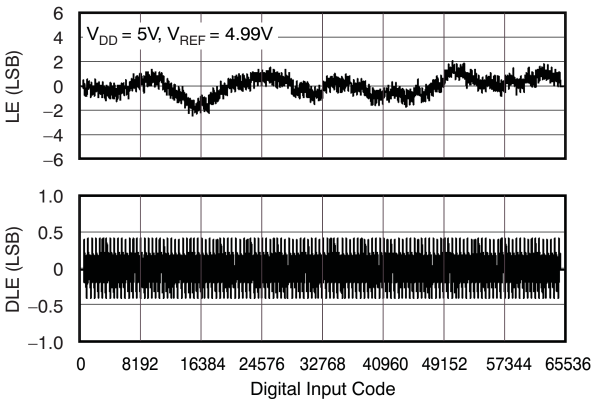


Figure 2. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

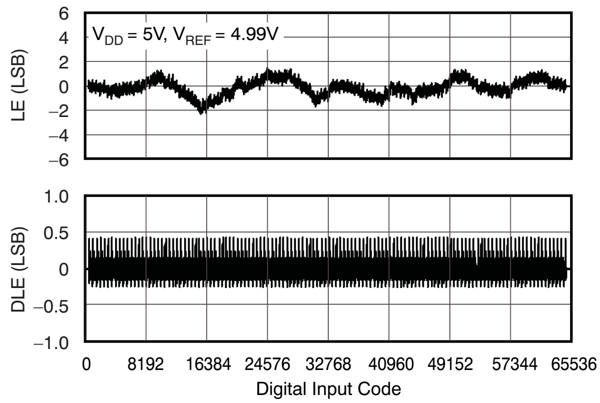


Figure 3. Linearity Error and Differential Linearity Error vs Digital Input Code (25°C)

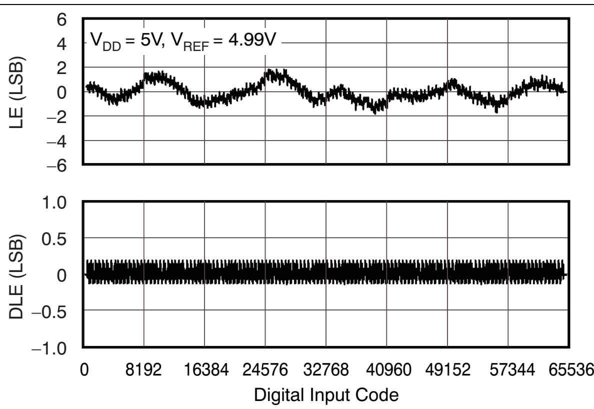


Figure 4. Linearity Error and Differential Linearity Error vs Digital Input Code (125°C)

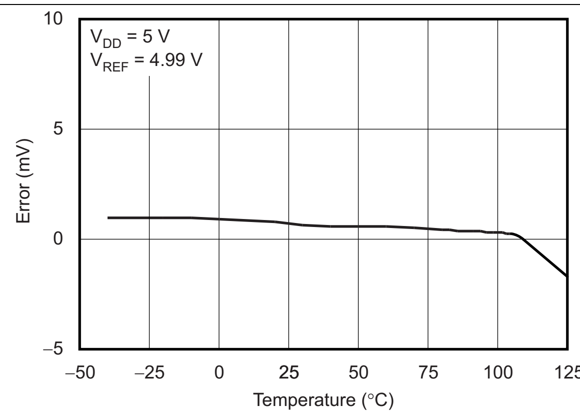


Figure 5. Offset Error vs Temperature

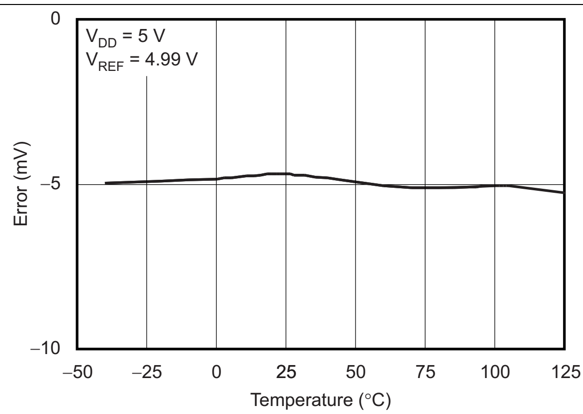


Figure 6. Full-Scale Error vs Temperature

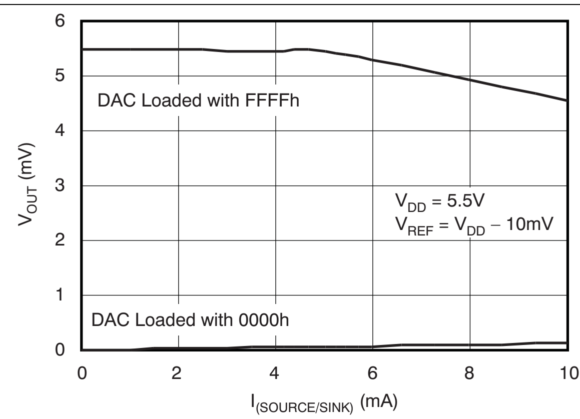


Figure 7. Source and Sink Current Capability

Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 5 V unless otherwise noted.

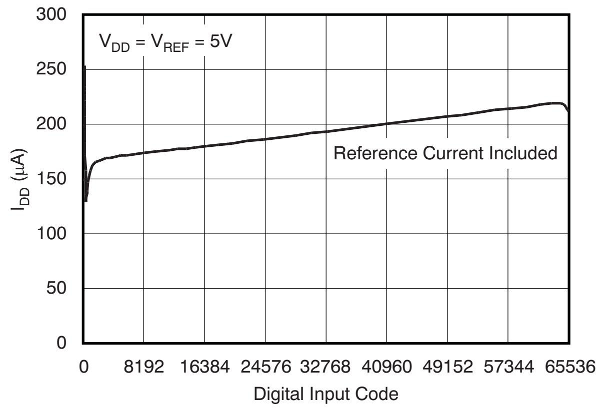


Figure 8. Supply Current vs Digital Input Code

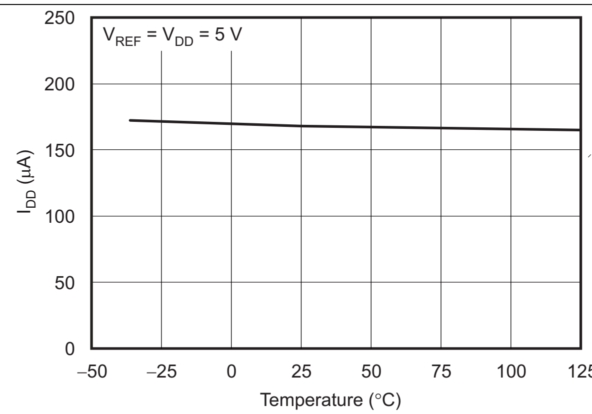


Figure 9. Power-Supply Current vs Temperature

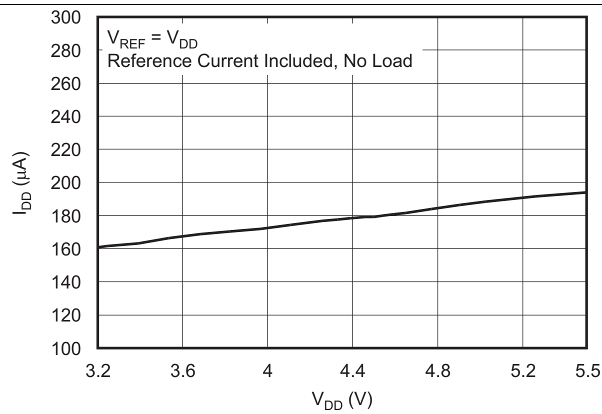


Figure 10. Supply Current vs Supply Voltage

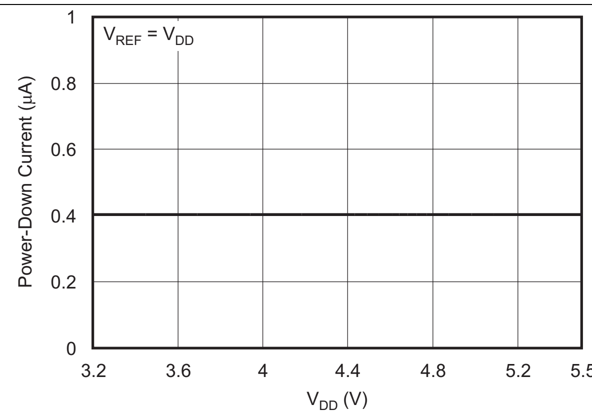


Figure 11. Power-Down Current vs Supply Voltage

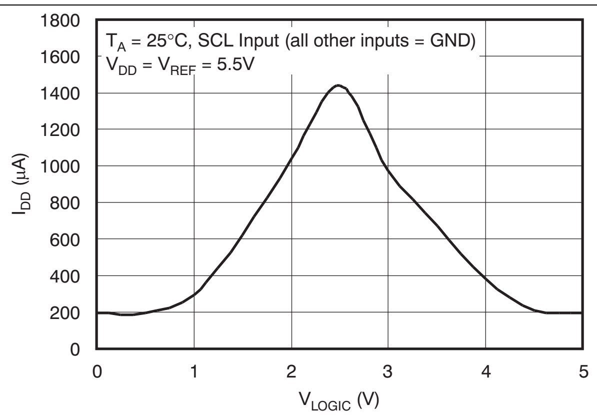


Figure 12. Supply Current vs Logic Input Voltage

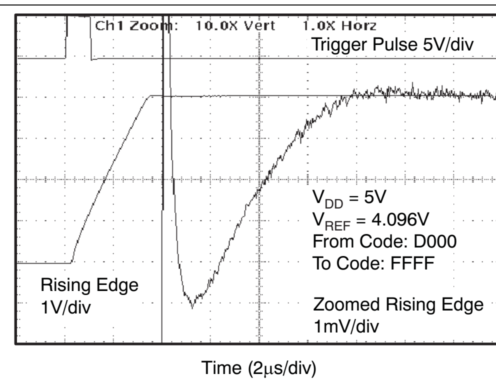


Figure 13. Full-Scale Settling Time: 5-V Rising Edge

Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 5 V unless otherwise noted.

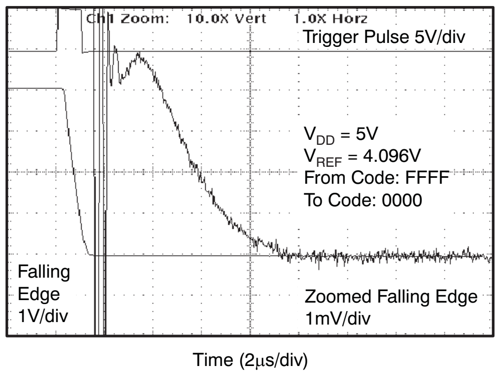


Figure 14. Full-Scale Settling Time: 5-V Falling Edge

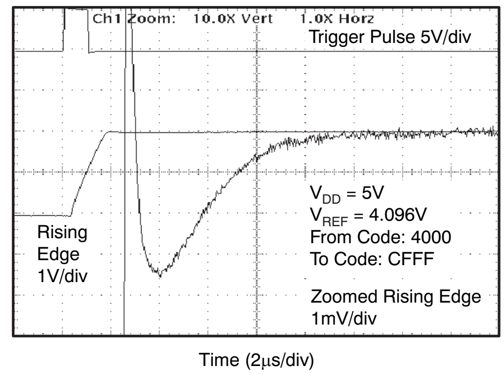


Figure 15. Half-Scale Settling Time: 5-V Rising Edge

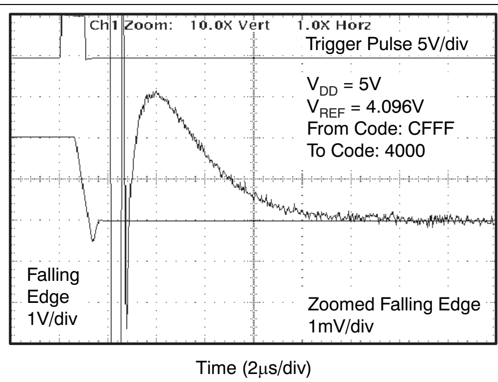


Figure 16. Half-Scale Settling Time: 5-V Falling Edge

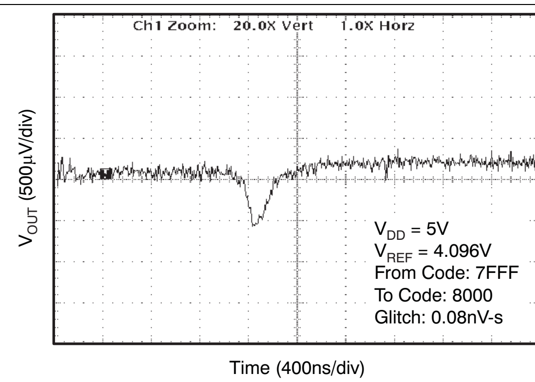


Figure 17. Glitch Impulse: 5 V, 1-LSB Step, Rising Edge

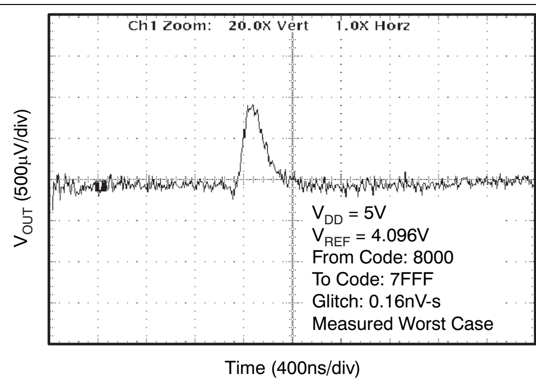


Figure 18. Glitch Impulse: 5 V, 1-LSB Step, Falling Edge

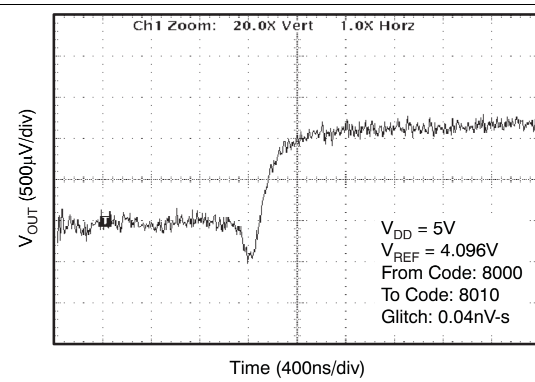


Figure 19. Glitch Impulse: 5 V, 16-LSB Step, Rising Edge

Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 5 V unless otherwise noted.

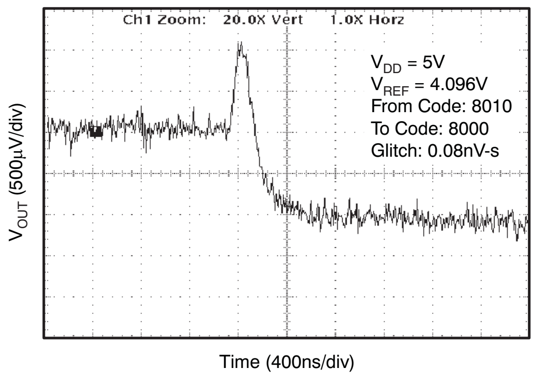


Figure 20. Glitch Impulse: 5 V, 16-LSB Step, Falling Edge

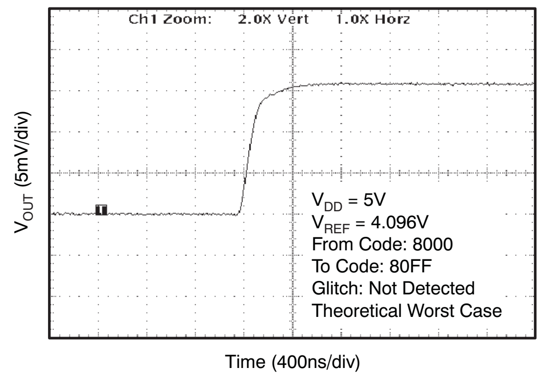


Figure 21. Glitch Impulse: 5 V, 256-LSB Step, Rising Edge

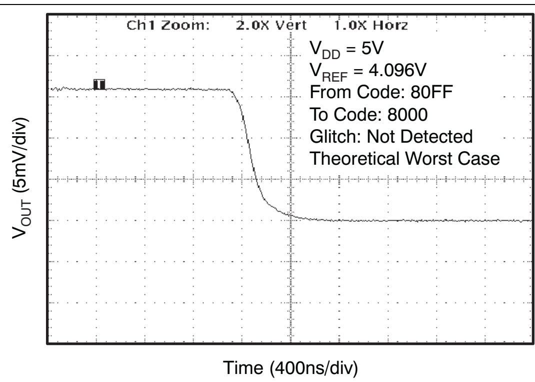


Figure 22. Glitch Impulse: 5 V, 256-LSB Step, Falling Edge

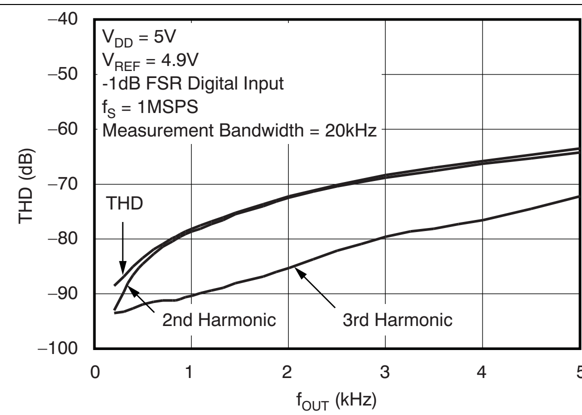


Figure 23. Total Harmonic Distortion vs Output Frequency

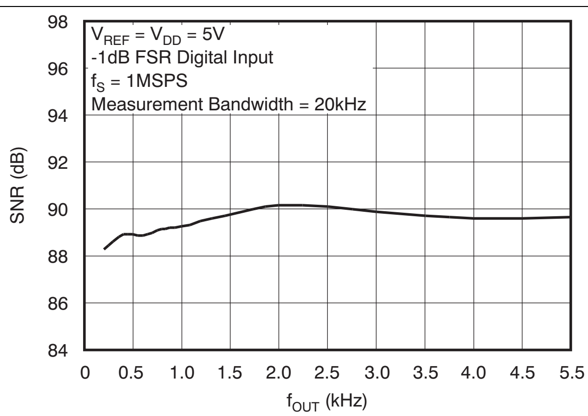


Figure 24. Signal-to-Noise Ratio vs Output Frequency

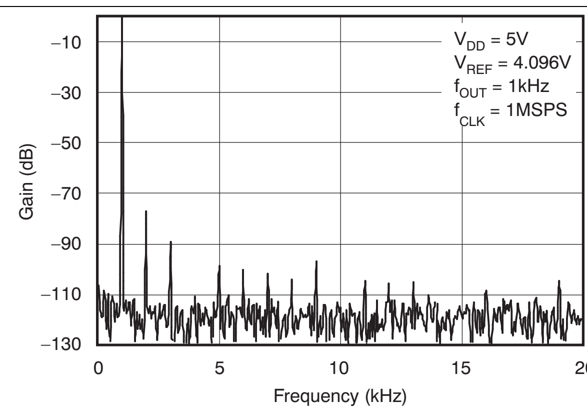


Figure 25. Power Spectral Density

Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 5 V unless otherwise noted.

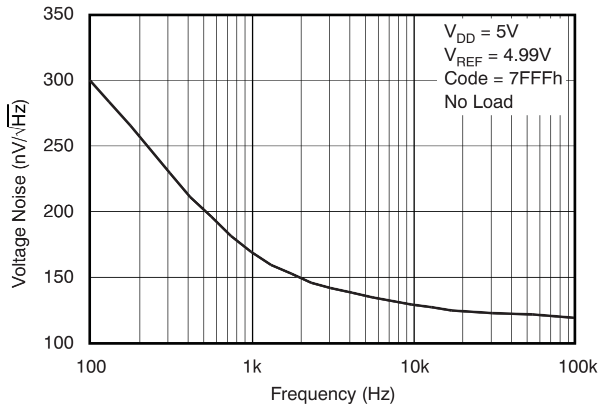


Figure 26. Output Noise Density

7 Detailed Description

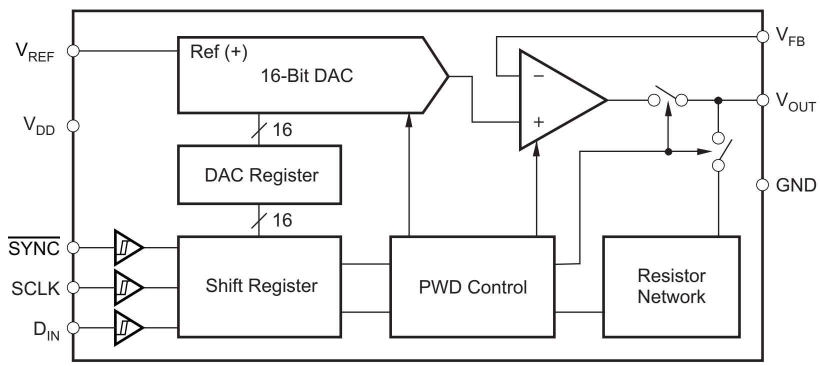
7.1 Overview

The DAC8551-Q1 is a small, low-power, voltage-output, 16-bit digital-to-analog converters (DACs) qualified for automotive applications. The DAC8551-Q1 provides good linearity, and minimizes undesired code-to-code transient voltages. The DAC8551-Q1 devices use a versatile 3-wire serial interface that operates at clock rates to 30 MHz and is compatible with standard SPI, QSPI, Microwire, and digital signal processor (DSP) interfaces.

The DAC8551-Q1 requires an external reference voltage to set its output range. The DAC8551-Q1 incorporates a power-on-reset circuit that ensures the DAC output powers up at 0 V and remains there until a valid write to the device takes place. The DAC8551-Q1 contain a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 800 nA at 5 V.

The DAC8551-Q1 power consumption is only 800 µW at 5 V, reducing to less than 4 µW in power-down mode. The DAC8551-Q1 is available in a VSSOP-8 package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DAC Section

The DAC8551-Q1 architecture consists of a string DAC followed by an output buffer amplifier. Figure 27 shows a block diagram of the DAC architecture.

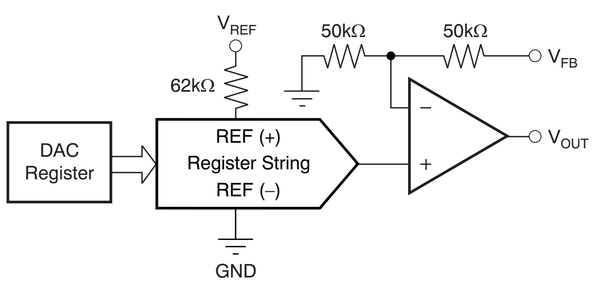


Figure 27. DAC8551-Q1 Architecture

The input coding to the DAC8551-Q1 device is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = \frac{D_{IN}}{65536} \times V_{REF} \quad (1)$$

where D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65 535.

Feature Description (continued)

7.3.1.1 Resistor String

The resistor string section is shown in Figure 28. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Monotonicity is ensured because of the string resistor architecture.

7.3.1.2 Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 1.4 V/µs with a full-scale setting time of 8 µs with the output unloaded.

The inverting input of the output amplifier is brought out to the V_{FB} pin. This configuration allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

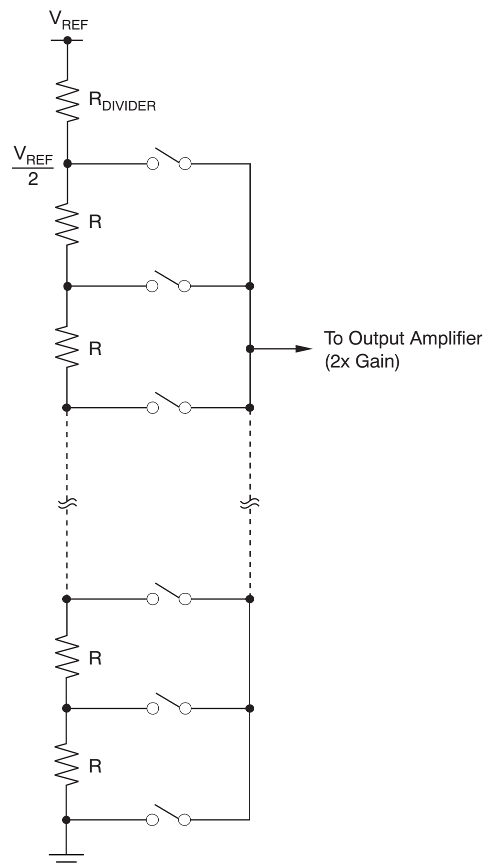


Figure 28. Resistor String

7.3.2 Power-On Reset

The DAC8551-Q1 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC registers are filled with zeros and the output voltages are 0 V; they remain that way until a valid write sequence is made to the DAC. The power-on reset is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

7.4 Device Functional Modes

7.4.1 Power-Down Modes

The DAC8551-Q1 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 3 shows how the state of the bits corresponds to the mode of operation of the device.

Table 3. Operating Modes

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal operation
—	—	Power-down modes
0	1	Output typically 1 kΩ to GND
1	0	Output typically 100 kΩ to GND
1	1	High-Z

When both bits are set to 0, the device works normally with its typical current consumption of 160 µA at 5 V. However, for the three power-down modes, the supply current falls to 800 nA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This configuration has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 29.

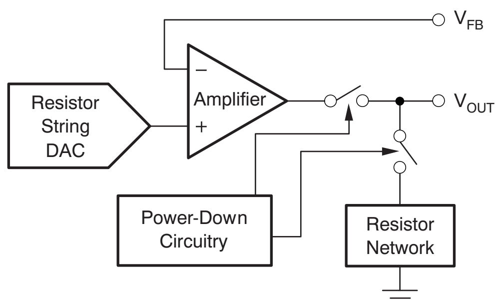


Figure 29. Output Stage During Power Down

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V, and 5 µs for V_{DD} = 3.3 V. See the Typical Characteristics for more information.

7.5 Programming

The DAC8551-Q1 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and D_{IN}), which is compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the *Serial Write Operation Timing Diagram* section for an example of a typical write sequence.

The input shift register is 24 bits wide, as shown in Figure 30. The first six bits are *don't care* bits. The next two bits (PD1 andPD0) are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). A more complete description of the various modes is located in the Power-Down Modes section. The next 16 bits are the data bits. These bits are transferred to the DAC register on the 24th falling edge of SCLK.

DB23																							DB0
X	X	X	X	X	X	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 30. DAC8551-Q1 Data-Input Register Format

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the DAC8551-Q1 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed (that is, a change in DAC register contents and/or a change in the mode of operation).

At this point, the $\overline{\text{SYNC}}$ line may be kept low or brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. As previously mentioned, it must be brought high again just before the next write sequence.

7.5.1 $\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 24th falling edge, it acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 31.

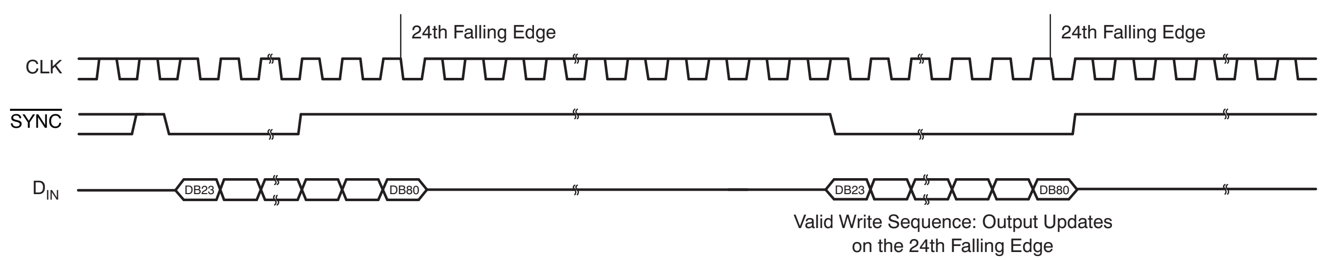


Figure 31. $\overline{\text{SYNC}}$ Interrupt Facility

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Applications

8.2.1 Loop-Powered 2-Wire 4-mA to 20-mA Transmitter With XTR116

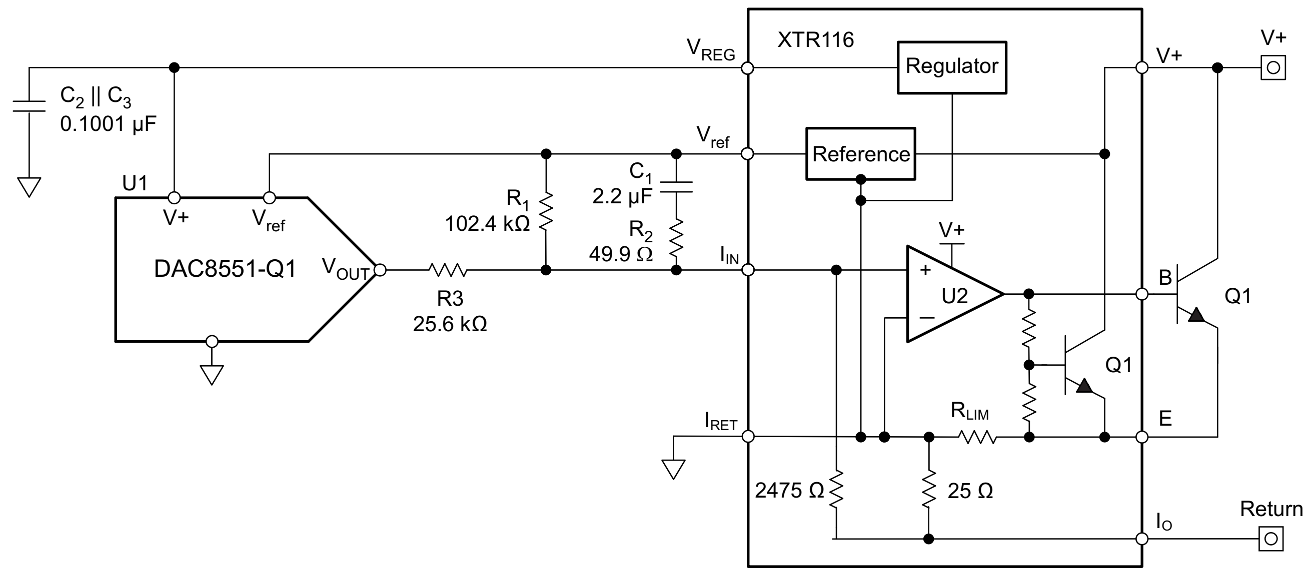


Figure 32. Loop-Powered Transmitter

8.2.1.1 Design Requirements

This design is commonly referred to as a loop-powered, or 2-wire, 4 mA to 20 mA transmitter. The transmitter has only two external input terminals: a supply connection and an output, or return, connection. The transmitter communicates back to its host, typically a PLC analog input module, by precisely controlling the magnitude of its return current. In order to conform to the 4 mA to 20 mA communication standard, the complete transmitter must consume less than 4 mA of current. The DAC8551-Q1 enables the accurate control of the loop current from 4 mA to 20 mA in 16-bit steps.

8.2.1.2 Detailed Design Procedure

Although it is possible to recreate the loop-powered circuit using discrete components, the XTR116 provides simplicity and improved performance due to the matched internal resistors. The output current can be modified if necessary by looking using Equation 2.

$$I_{OUT}(\text{Code}) = \left(\frac{V_{ref} \times \text{Code}}{2^N \times R_3} + \frac{V_{REG}}{R_1} \right) \times \left(1 + \frac{2475\ \Omega}{25\ \Omega} \right) \tag{2}$$

For more details of this application, see *2-wire, 4-20mA Transmitter, EMC/EMI Tested Reference Design* (TIDUAO7). It covers in detail the design of this circuit as well as how to protect it from EMC/EMI tests.

Typical Applications (continued)

8.2.1.3 Application Curves

Total unadjusted error (TUE) is a good estimate for the performance of the output as shown in Figure 33. The linearity of the output or INL is in Figure 34.

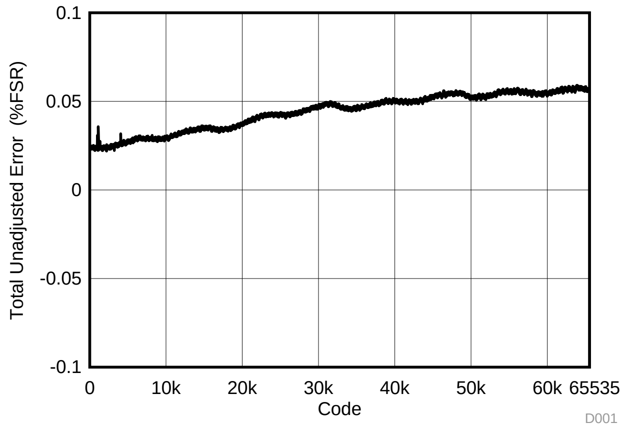


Figure 33. Total Unadjusted Error

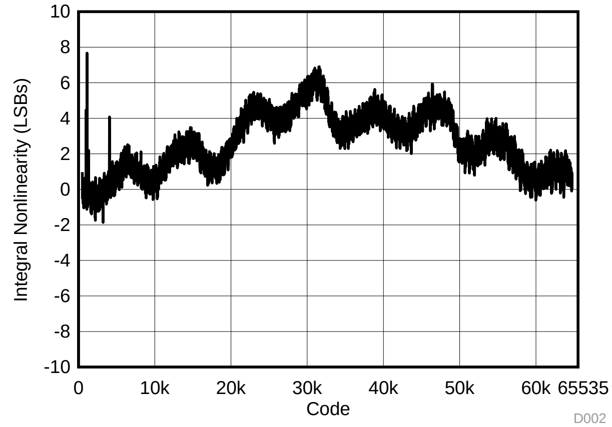


Figure 34. Integral Nonlineareity

8.2.2 Bipolar Operation Using the DAC8551-Q1

The DAC8551-Q1 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 35. The circuit shown gives an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

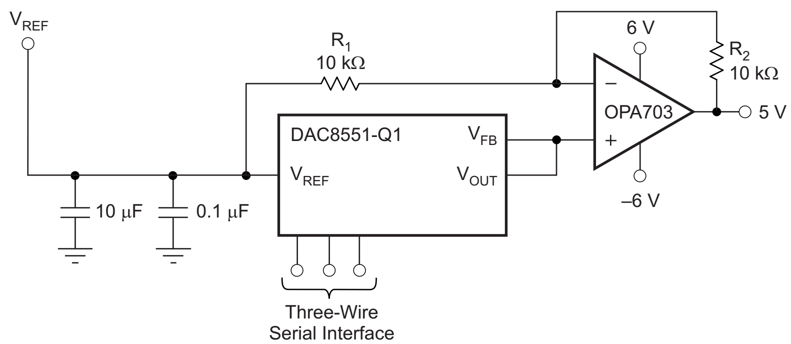


Figure 35. Bipolar Output Range

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{REF} \times \left(\frac{D}{65536} \right) \times \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_2}{R_1} \right) \right] \quad (3)$$

where D represents the input code in decimal (0–65 535)

with V_{REF} = 5V, $R_1 = R_2$ = 10 kΩ.

$$V_O = \left(\frac{10 \times D}{65536} \right) - 5V \quad (4)$$

Using this example, an output voltage range of ±5 V with 0000h corresponding to a –5 V output and FFFFh corresponding to a 5 V output can be achieved. Similarly, using V_{REF} = 2.5 V, a ±2.5 V output voltage range can be achieved.

8.2.3 Using the REF02 As a Power Supply for the DAC8551-Q1

Due to the extremely low supply current required by the DAC8551-Q1, an alternative option is to use a precision reference such as the REF02 device to supply the required voltage to the device, as illustrated in Figure 36.

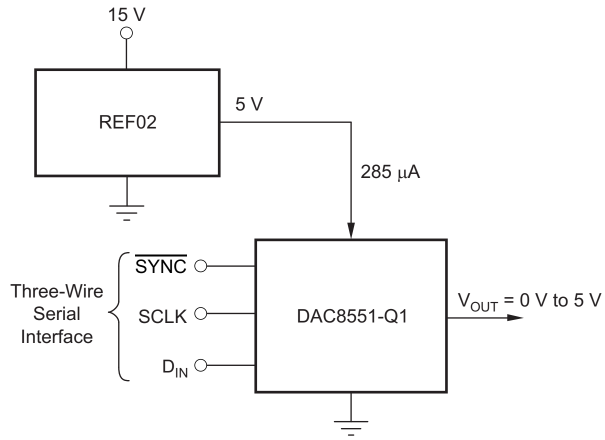


Figure 36. REF02 As a Power Supply to the DAC8551-Q1

This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 device outputs a steady supply voltage for the DAC8551-Q1. If the REF02 device is used, the current it must supply to the DAC8551-Q1 is 200 µA. This configuration is with no load on the output of the DAC. When a DAC output is loaded, the REF02 also must supply the current to the load.

The total current required (with a 5 kΩ load on the DAC output) is:

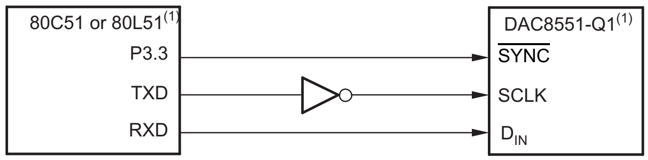
$$200\mu A + \frac{5V}{5k\Omega} = 1.2mA \tag{5}$$

The load regulation of the REF02 is typically 0.005%/mA, resulting in an error of 299 µV for the 1.2 mA current drawn from it. This value corresponds to a 3.9 LSB error.

8.3 System Examples

8.3.1 Interface from DAC8551-Q1 to 8051

See Figure 37 for a serial interface between the DAC8551-Q1 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8551-Q1, while RXD drives the serial data line of the device. The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data are to be transmitted to the DAC8551-Q1, P3.3 is taken low. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, then a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The DAC8551-Q1 requires data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed.

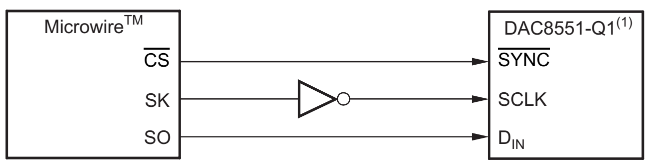


NOTE: (1) Additional pins omitted for clarity.

Figure 37. Interface from DAC8551-Q1 Devices to 80C51 or 80L51

8.3.2 Interface from DAC8551-Q1 to Microwire

Figure 38 shows an interface between the DAC8551-Q1 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and is clocked into the DAC8551-Q1 on the rising edge of the SK signal.

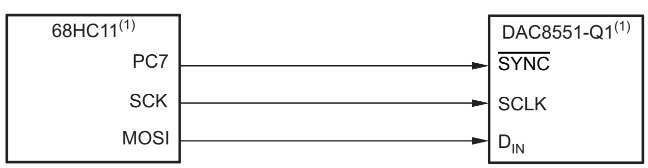


NOTE: (1) Additional pins omitted for clarity.

Figure 38. Interface from DAC8551-Q1 Devices to Microwire

8.3.3 Interface from DAC8551-Q1 to 68HC11

Figure 39 shows a serial interface between the DAC8551-Q1 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8551-Q1, whereas the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7), similar to the 8051 diagram.



NOTE: (1) Additional pins omitted for clarity.

Figure 39. Interface from DAC8551-Q1 Devices to 68HC11

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is held low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC88551-Q1, PC7 is left low after the first eight bits are transferred, then a second and third serial write operation are performed to the DAC. PC7 is taken high at the end of this procedure.

9 Power Supply Recommendations

The DAC8551-Q1 can operate within the specified supply voltage range of 3.2 V to 5.5 V. The power applied to V_{DD} should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. In order to further minimize noise from the power supply, a strong recommendation is to include a 1 µF to 10 µF capacitor and 0.1 µF bypass capacitor. The current consumption on the V_{DD} pin, the short-circuit current limit, and the load current for the device is listed in the Electrical Characteristics table. The power supply must meet the aforementioned current requirements.

10 Layout

10.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8551-Q1 offers single-supply operation, and are often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8551-Q1, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

As with the GND connection, V_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1 µF to 10 µF capacitor and 0.1 µF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100 µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5 V supply, removing the high-frequency noise.

10.2 Layout Example

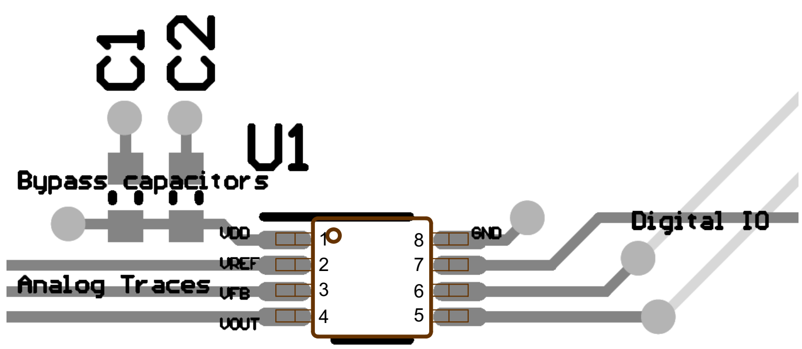


Figure 40. Layout Diagram

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

《通过 EMC/EMI 测试的双线制 4mA-20mA 发送器参考设计》（文献编号：TIDUAO7）

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。本数据随时可能发生变更并且不对本文档进行修订，恕不另行通知。要获得这份数据表的浏览器版本，请查阅左侧的导航窗格。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC6551AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D61Q
DAC6551AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D61Q
DAC6551AQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D61Q
DAC8551AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D81Q
DAC8551AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D81Q
DAC8551AQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D81Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF DAC8551-Q1 :

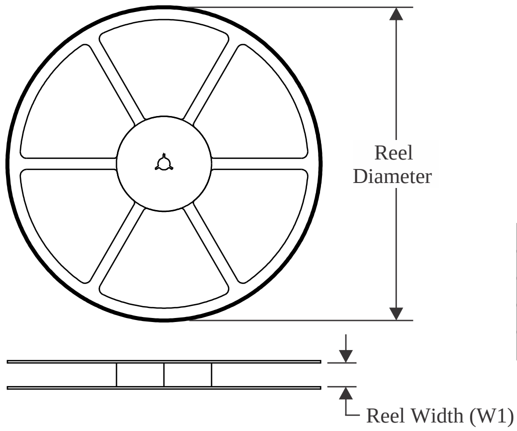
- Catalog : DAC8551

NOTE: Qualified Version Definitions:

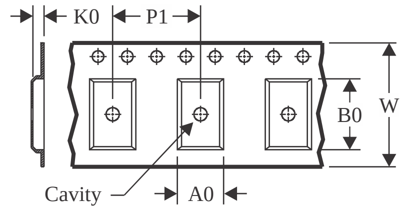
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

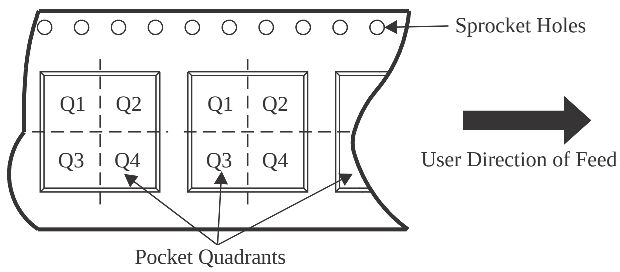


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

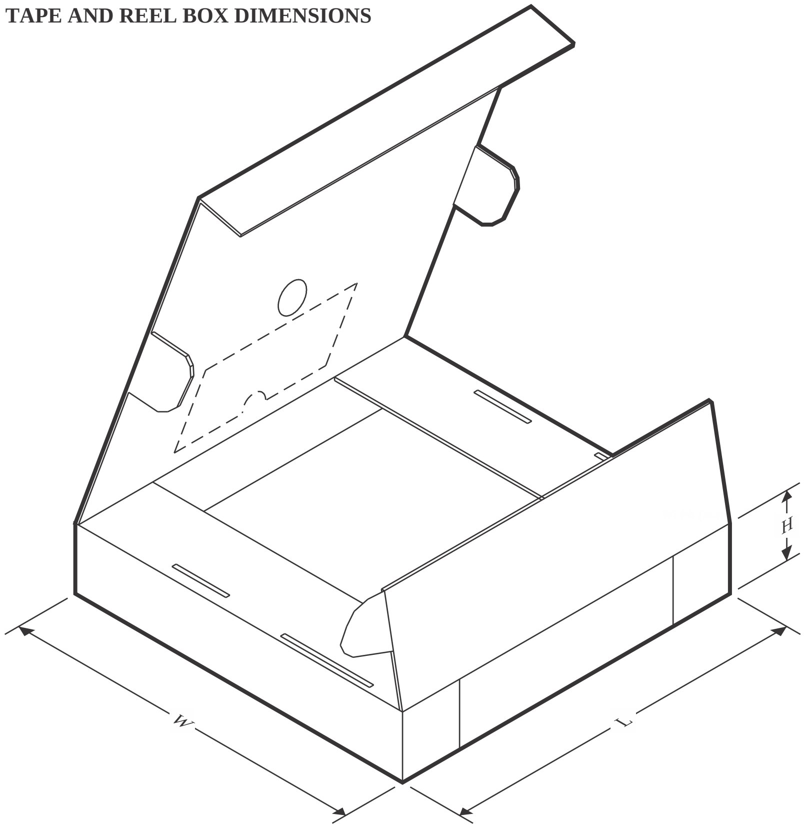
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

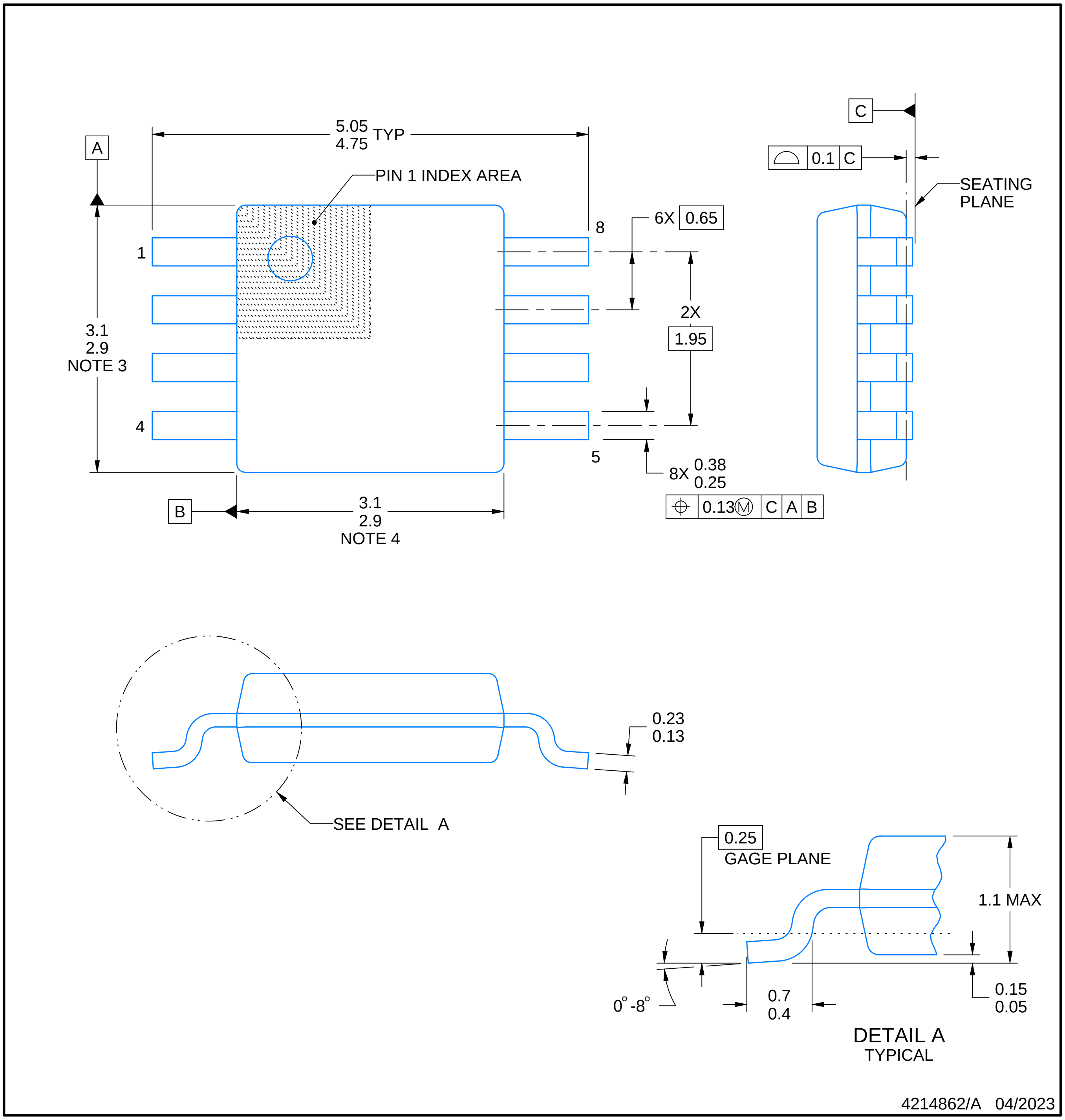
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC6551AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8551AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC6551AQDGKRQ1	VSSOP	DGK	8	2500	350.0	350.0	43.0
DAC8551AQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0



4214862/A 04/2023

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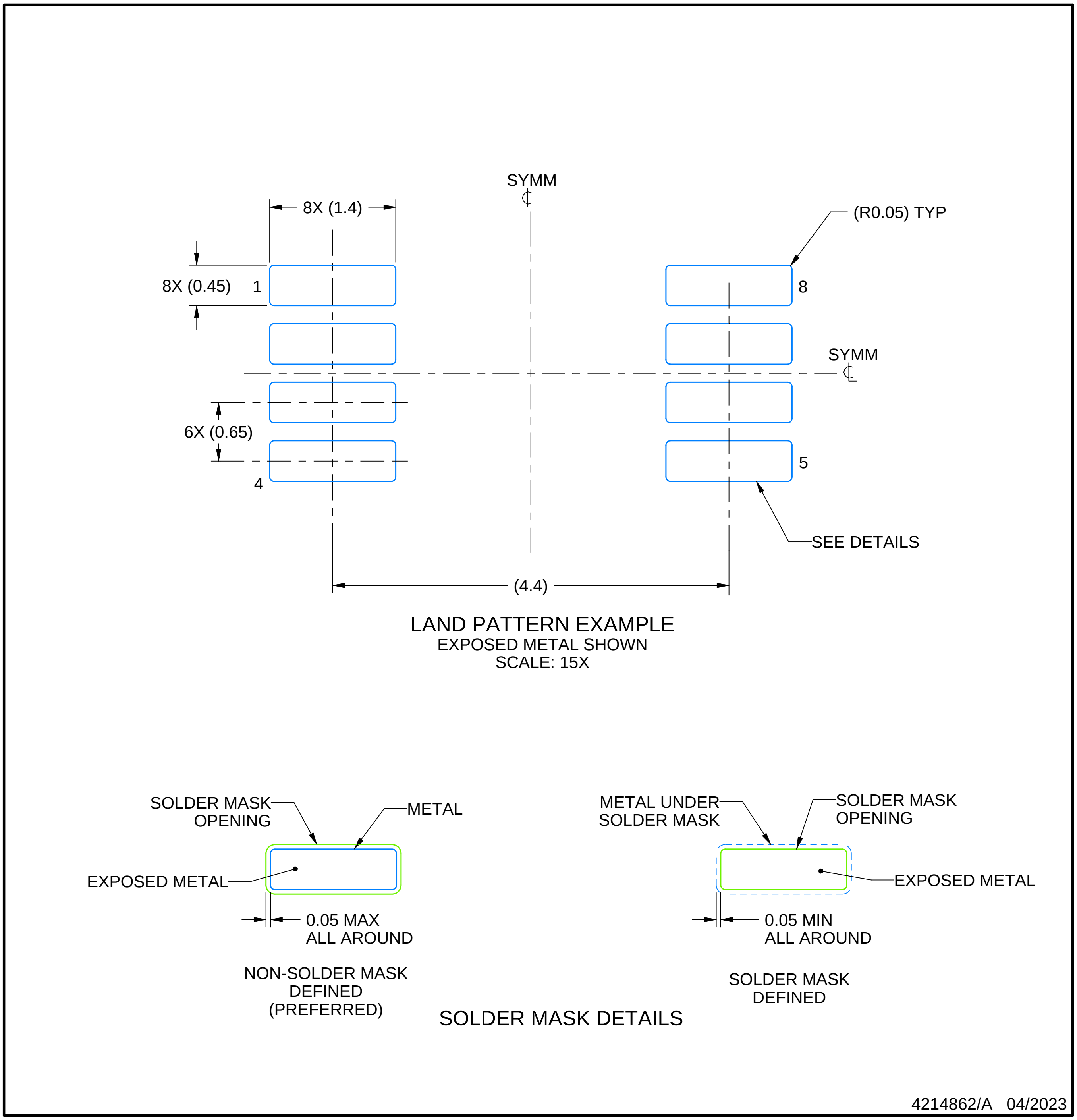
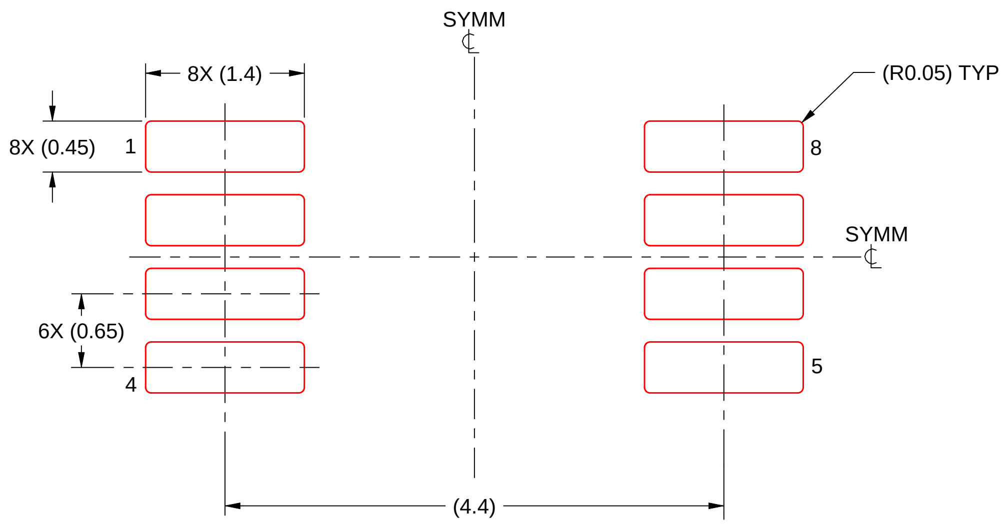
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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