DACx0004 四通道 16 位、14 位、12 位 1LSB INL 缓冲电压输出数模转换器

1 特性

- 真正的 16 位性能：1 LSB 积分非线性 (INL)/微分非线性 (DNL)（最大值）
- 超低毛刺脉冲能量：1nV-s
- 宽电源电压范围：2.7V 至 5.5V
- 支持轨到轨运行的输出缓冲器
- 电流消耗：1mA/通道
- 50Mhz、四线制或三线制串行外设接口 (SPI) 兼容接口
- 用于回读和菊花链连接的 SDO 引脚
- 上电复位至零量程或量程中点
- 温度范围：-40°C 至 +125°C
- 多种封装：
  - 微型 14 引脚超薄小外形尺寸无引线 (VSON) 封装
  - 14 引脚薄型小外形尺寸 (TSSOP) 封装

2 应用

- 便携式仪表
- 可编程逻辑控制器 (PLC) 模拟输出模块(4mA-20mA)
- 闭环伺服器控制
- 数据采集系统

3 说明

DAC80004/70004/60004 (DACx0004) 分别为 16 位、14 位和 12 位高精度、低功耗、电压输出、四通道数模转换器 (DAC)。DACx0004 器件通过设计可保证单调性，拥有低于 1 LSB（最大值）的出色线性度。DAC 的基准输入在内部通过专用基准缓冲器进行缓冲。

DACx0004 器件配有上电复位电路，用于确保 DAC 输出在零量程或量程中点处上电（具体取决于 POR 引脚的状态）并保持该状态直到器件中写入有效编码为止。这些器件的电流消耗非常低（1mA/通道），是便携式、电池供电类设备的理想选择。这些器件还包含一种掉电特性。该特性可将 5V 电压下的流耗降至 3μA（典型值）。

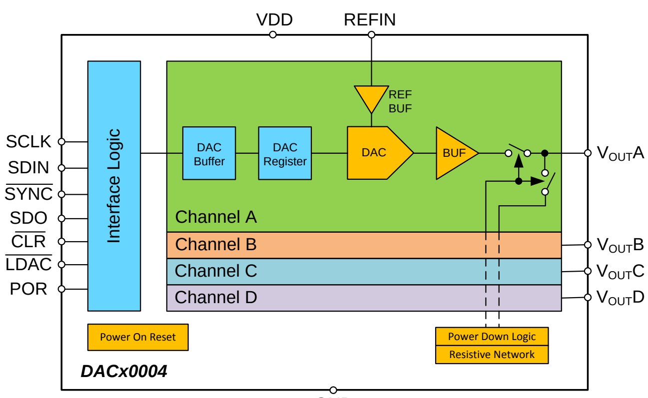
DACx0004 器件使用一个运行时钟速率高达 50MHz 的通用三线制串口。DACx0004 器件还包含一个 SDO 引脚，该引脚能够以菊花链形式连接多个器件。此接口与标准 SPI™， QSPI™、Microwire 以及数字信号处理器 (DSP) 接口兼容。DACx0004 器件采用易于装配的 14 引脚 TSSOP 封装或超小型 14 引脚 VSON 封装，在 -40°C 至 +125°C 的扩展工业级温度范围内完全额定运行.

器件信息(1)

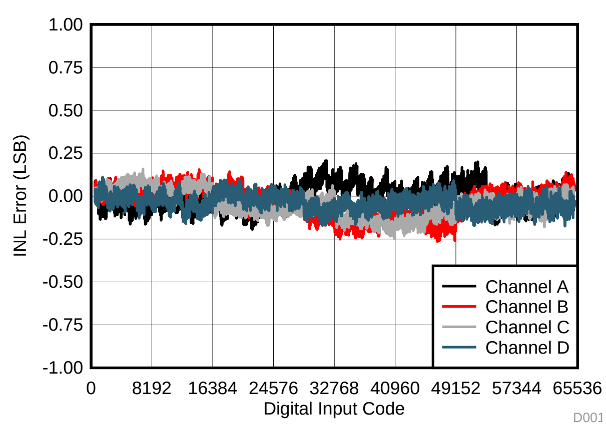
器件型号	封装	封装尺寸（标称值）
DACx0004	VSON (14)	3.00mm x 4.00mm
DACx0004	TSSOP (14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

DACx0004 框图



线性误差与数字输入编码间的关系



目录

4 修订历史记录

Changes from Revision C (August 2016) to Revision D — **Page**

- Changed 2.4 µs From MAX to MIN value for t_{20} in the *DACx0004 Timing Requirements* table 8
- Changed From: t_{19} To: t_{20} in Figure 1 8

Changes from Revision B (June 2016) to Revision C — **Page**

- Deleted thermal pad from PW-TSSOP pin configuration 3

Changes from Revision A (June 2016) to Revision B — **Page**

- 已添加 将 DAC80004IPW 器件标识附录添加到了*机械、封装和可订购信息* 31

Changes from Original (April 2016) to Revision A — **Page**

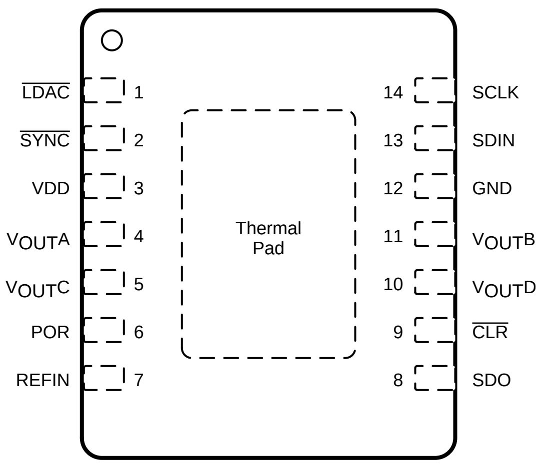
- 已更改 产品预览至量产数据 1

5 Device Comparison Table

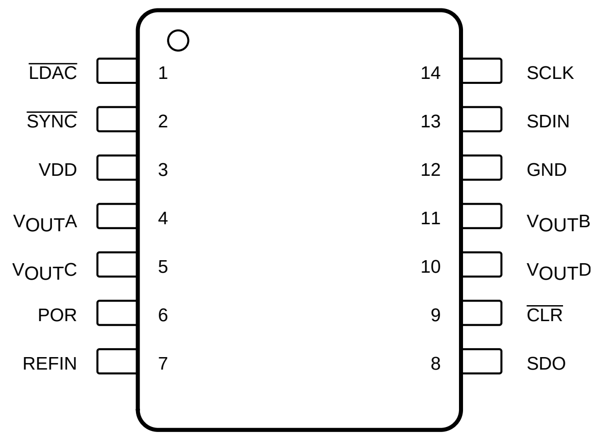
DEVICE	RESOLUTION
DAC80004	16
DAC70004	14
DAC60004	12

6 Pin Configuration and Functions

14-Pin VSON
DMD Package
Top View



14-Pin TSSOP
PW Package
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
$\overline{CLR}$	9	Digital Input	Clear DAC pin, falling edge sensitive
GND	12	Power	Ground
$\overline{LDAC}$	1	Digital Input	Load DAC pin, active low
POR	6	Digital Input	Power-on-reset configuration, Connecting the POR pin to GND powers up all four DACs to zero scale. Connecting this pin to VDD powers up all four DACs to midscale.
REFIN	7	Analog Input	Voltage reference input for all channels
SCLK	14	Digital Input	Serial interface shift clock
SDIN	13	Digital Input	Serial interface digital input
SDO	8	Digital Output	Serial interface digital output for readback and daisy chaining
$\overline{SYNC}$	2	Digital Input	Serial interface synchronization, active low
VDD	3	Power	Positive power supply (2.7 V to 5.5 V)
$V_{OUT}A$	4	Analog Output	DAC A output
$V_{OUT}B$	11	Analog Output	DAC B output
$V_{OUT}C$	5	Analog Output	DAC C output
$V_{OUT}D$	10	Analog Output	DAC D output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Voltage, VDD to GND	–0.3	7	V
Voltage, digital input or output to GND	–0.3	V_{DD} + 0.3	V
Voltage, analog input (REFIN) or output (V_{OUT}x) to GND	–0.3	V_{DD} + 0.3	V
Input current to any pin except supply pins	–10	10	mA
Maximum junction temperature		150	°C
Storage temperature range, T_{stg}	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage, VDD to GND		2.7		5.5	V
Voltage, analog input (REFIN) or output (V_{OUT}x) to GND	2.7 V ≤ V_{DD} ≤ 4.5 V	2.2		V_{DD} – 0.2	V
	4.5 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
Ambient Operating Temperature, T_A		-40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		DACx0004		UNIT
		DMD (VSON)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.6	99.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.3	23.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.0	42.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.9	42.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

All minimum/maximum specifications at T_A = -40°C to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, 2.5 V ≤ REFIN[1] ≤ VDD, R_{load} = 5 kΩ to GND, C_{load} = 200 pF to GND (unless otherwise noted), Digital inputs held at 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE[2]						
	Resolution	DAC80004	16			Bits
		DAC70004	14			
		DAC60004	12			
INL	Relative accuracy[3]				±1	LSB
DNL	Differential nonlinearity[3]	Ensured monotonic			±1	LSB
TUE	Total unadjusted error[3]	T_A = +20°C to +40°C			1.5	mV
		T_A = –40°C to +125°C			2	
ZCE	Zero code error	T_A = –40°C to +125°C, Code 0d into DAC		±0.2	±2	mV
		T_A = +25°C, Code 0d into DAC		±0.1		
ZCE-TC	Zero code error TC	T_A = –40°C to +125°C		±5		µV/°C
OE	Offset error[3]	T_A = +20°C to +40°C			±1.2	mV
		T_A = –40°C to +125°C		±0.2	±1.8	
		T_A = +25°C		±0.2		
OE-TC	Offset error drift	T_A = –40°C to +125°C		±4		µV/°C
FSE	Full-scale error[4]	T_A = +20°C to +40°C, Code 65535d into DAC			±0.05	%FSR
		T_A = –40°C to +125°C, Code 65535d into DAC		±0.01	±0.07	%FSR
		T_A = +25°C		±0.01		
FSE-TC	Full-scale error drift[4]	T_A = –40°C to +125°C		±2		ppm FSR/°C
GE	Gain error[3]	T_A = –40°C to +125°C		±0.005	±0.05	%FSR
		T_A = +25°C		±0.005		
GE-TC	Gain drift	T_A = –40°C to +125°C		±2		ppm FSR/°C
	Output voltage drift vs.Time	T_A = +25°C, Vout = ¾ of full scale, 1900 hr		20		ppm FSR
	Load Regulation	T_A = +25°C, Vout =Mid Scale		0.003%		
PSRR	DC Power supply rejection ratio[4]	T_A = +25°C, Vout = full scale		–92		dB

(1) 200 mV headroom is required between REFIN and VDD when 2.7 V ≤ V_{DD} ≤ 4.5 V.
(2) Output unloaded
(3) End point fit between codes Code 512 to Code 65,024 - DAC80004, Code 128 to Code 16,256 - DAC70004, Code 32 to Code 4064 - DAC60004, Output unloaded.
(4) With 100 mV headroom between DAC output and VDD.

Electrical Characteristics (continued)

All minimum/maximum specifications at T_A = -40°C to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, 2.5 V ≤ REFIN(1) ≤ VDD, R_{load} = 5 kΩ to GND, C_{load} = 200 pF to GND (unless otherwise noted), Digital inputs held at 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
	Output voltage settling time	¼ to ¾ scale and ¾ to ¼ scale settling to ±1 LSB, R_L = 5 kΩ, C_{load} = 200 pF to GND		5.8	8	µs
	Slew rate			1.5		V/µs
	Power-up time(5)			100		µs
	Power-on glitch energy	Supply slew rate <5 V/msec		8		mV
	Power-off glitch energy	DAC in power down mode (1 kΩ-GND), Supply slew rate <5 V/msec		7		mV
	Output noise	0.1 Hz to 10 Hz		5		µVpp
		100 kHz BW		100		µVRMS
	Output noise density	Measured at 1 kHz		60		nV/√Hz
		Measured at 10 kHz		55		
THD	Total harmonic distortion	REFIN = 3 V ± 0.2 V_{pp}, Frequency = 10 kHz, DAC at mid scale, specified by design		–80		dB
PSRR	AC power supply rejection ratio	200 mV 50 Hz and 60 Hz sine wave superimposed on power supply voltage (AC analysis)		-90		dB
	Code change glitch impulse	1 LSB change around major carry, Software LDAC mode		1		nV-s
	Channel-to-channel AC (analog) crosstalk	Full-scale swing on adjacent channel, Hardware LDAC mode		1		nV-s
	Channel-to-channel DC crosstalk	Full-scale swing on adjacent channels, Measured channel at zero scale		1		LSB
		Full-scale swing on all channel, Measured channel at zero scale		1		
	Digital crosstalk	DAC code mid scale, Adjacent input buffer change from 0000h to FFFFh or vice versa		0.2		nV-S
	Reference feedthrough	REFIN = 3 V ± 0.86 V_{pp}, Frequency = 100 Hz to 100 kHz, DAC at zero scale		–85		dB
	Digital feedthrough	At SCLK = 1 MHz, DAC output static at mid scale		0.2		nV-s
OUTPUT CHARACTERISTICS						
	Voltage range		0		V_{DD}	V
	Headroom	Output loaded 5 kΩ, DAC code FFFFh		0.1		V
		Output loaded 0.5 kΩ, DAC code FFFFh		10		%FSR
RL	Resistive load		0.5			kΩ
CL	Capacitive load	R_L = ∞		1		nF
		R_L = 5 kΩ		2		
RO	DC output impedance	Normal mode		0.5		Ω
		Power down with 100 kΩ network		100		kΩ
		Power down with 1 kΩ network		1		kΩ
	Short circuit current			36		mA

(5) Time to exit power-down mode into normal mode. Measured from 32nd falling edge SCLK to 90% of DAC final value, Characterized at mid scale.

Electrical Characteristics (continued)

All minimum/maximum specifications at T_A = -40°C to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, 2.5 V ≤ REFIN(1) ≤ VDD, R_{load} = 5 kΩ to GND, C_{load} = 200 pF to GND (unless otherwise noted), Digital inputs held at 0 V

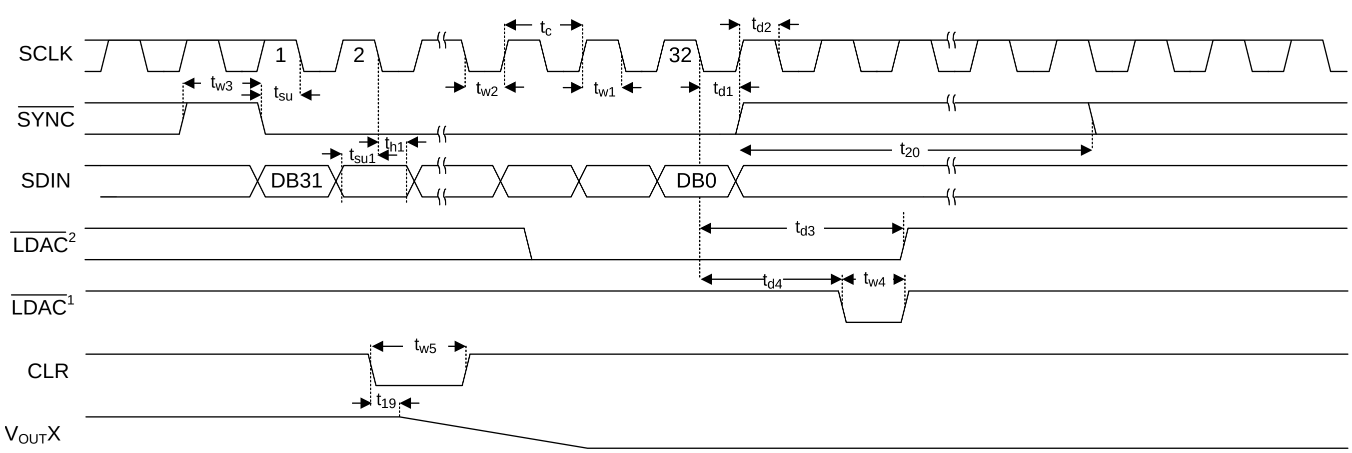
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE INPUT						
	Reference input range	2.7 V ≤ V_{DD} ≤ 4.5 V	2.2		V_{DD} – 0.2	V
		4.5 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	
	Reference input current				450	µA
	Reference input impedance			15		kΩ
	Reference input capacitance			10		pF
MBW	Multiplying bandwidth			340		kHz
DIGITAL INPUTS						
V_{IH}	High-level input voltage		2.3			V
V_{IL}	Low-level input voltage				0.7	V
	Input leakage	0 < $V_{DIGITAL\ INPUT}$ < V_{DD}			±1	µA
	Pin capacitance			4		pF
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	I_{OH} = 2 mA	V_{DD} – 1			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.7	V
	Pin capacitance			7		pF
POWER SUPPLY REQUIREMENTS						
V_{DD}	Supply voltage		2.7		5.5	V
I_{VDD}	Supply current	T_A = –40°C to +125°C, Normal mode		4	5.5	mA
		T_A = –40°C to +125°C, Power-down mode		3	7	µA
	Power dissipation	T_A = –40°C to +125°C, Normal mode		20		mW
TEMPERATURE RANGE						
T_A	Specified performance		–40		125	°C

7.6 DACx0004 Timing Requirements

At T_A = -40°C to +125°C, T_{rise} = T_{fall} = 1 nV/sec (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2, SDO pin loaded with 10 pF

		4.5 V ≤ V_{DD} ≤ 5.5 V			2.7 V ≤ V_{DD} ≤ 4.5 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SERIAL WRITE and READ								
t_c	SCLK cycle time	20			40			ns
t_{w1}	SCLK high pulse duration	10			20			ns
t_{w2}	SCLK low pulse duration	10			20			ns
t_{su}	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	15			30			ns
t_{su1}	Data setup time	5			10			ns
t_{h1}	Data hold time	5			10			ns
t_{d1}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge delay time	5			10			ns
t_{w3}	Minimum $\overline{\text{SYNC}}$ high pulse duration(1)	25			35			ns
t_{d2}	$\overline{\text{SYNC}}$ rising edge to SCLK fall ignore delay time	15			20			ns
t_{w4}	$\overline{\text{LDAC}}$ pulse duration low	20			30			ns
t_{d3}	SCLK falling edge to $\overline{\text{LDAC}}$ rising edge delay time	10			20			ns
t_{w5}	$\overline{\text{CLR}}$ minimum pulse duration low	10			20			ns
t_{d4}	SCLK falling edge to $\overline{\text{LDAC}}$ falling edge delay time	10			20			ns
t_v	SCLK rising edge to SDO valid time			18			18	ns
t_{d5}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge delay time	5			10			ns
t_{d6}	$\overline{\text{SYNC}}$ rising edge to SCLK rising edge delay time	5			10			ns
t_{d7}	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ falling edge delay time	20			40			ns
t_{19}	$\overline{\text{CLR}}$ pulse activation time	20			20			ns
t_{20}	Successive DAC Update	2.4			2.4			µs

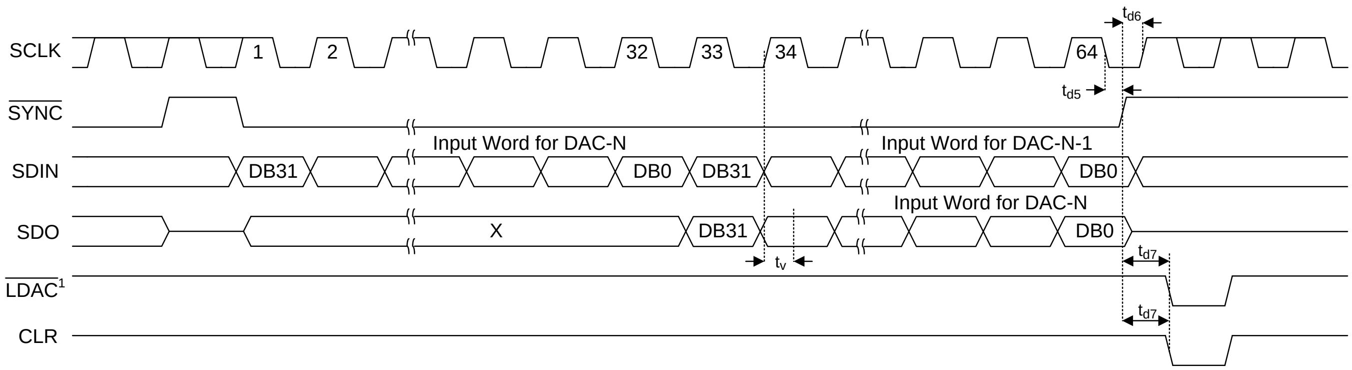
(1) Does not include output settling tiime



(1) Asynchronous $\overline{\text{LDAC}}$ update

(2) Synchronous $\overline{\text{LDAC}}$ update

Figure 1. Stand-Alone Timing



(1) Asynchronous LDAC update

Figure 2. Daisy-Chain Timing

7.7 Typical Characteristics

At T_A = 25°C, VDD = 5.5 V, REFIN = 5.45 V, DAC outputs unloaded, unless otherwise noted.

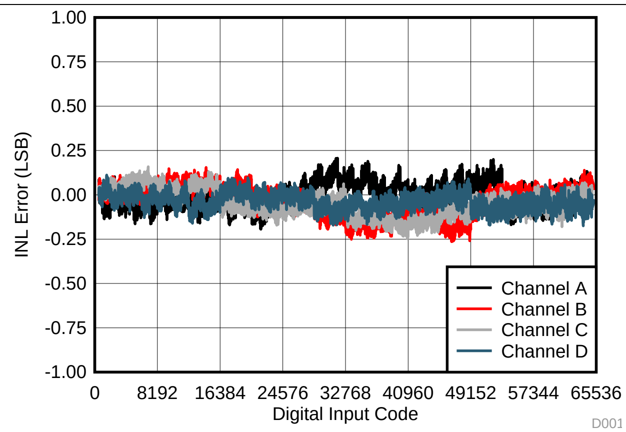


Figure 3. Linearity Error vs Digital Input Code

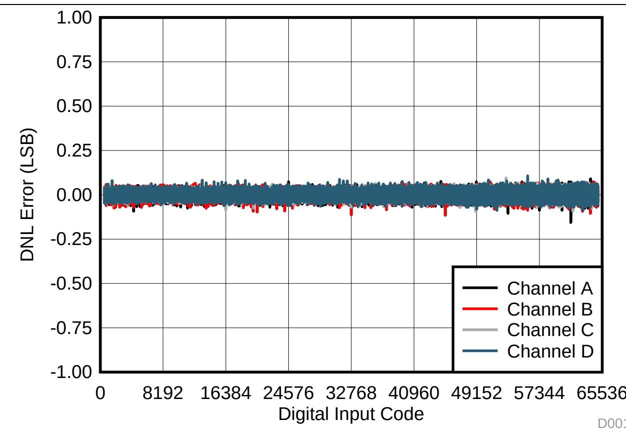
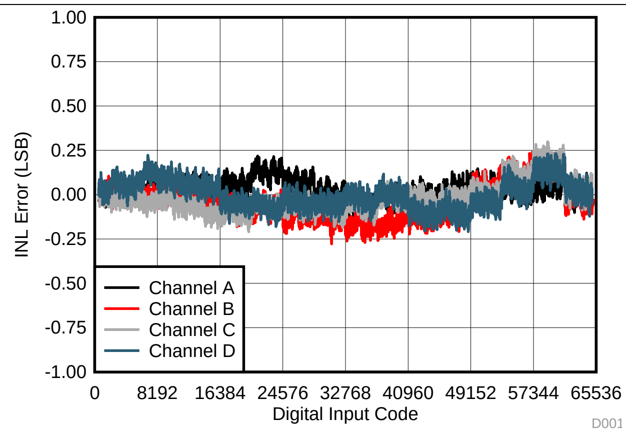
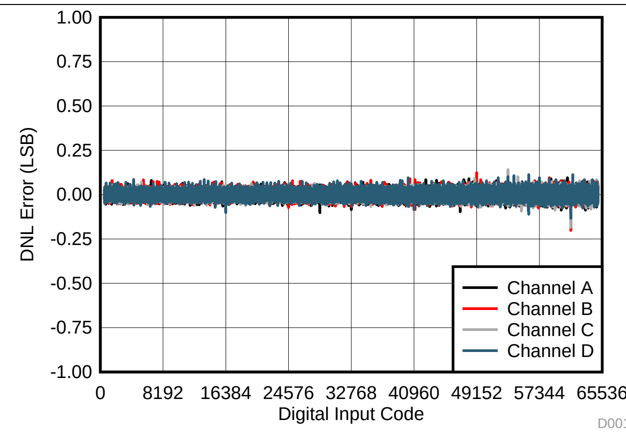


Figure 4. Differential Linearity Error vs Digital Input Code



DAC load 5 kΩ//200 pF

Figure 5. Linearity Error vs Digital Input Code



DAC load 5 kΩ//200 pF

Figure 6. Differential Linearity Error vs Digital Input Code

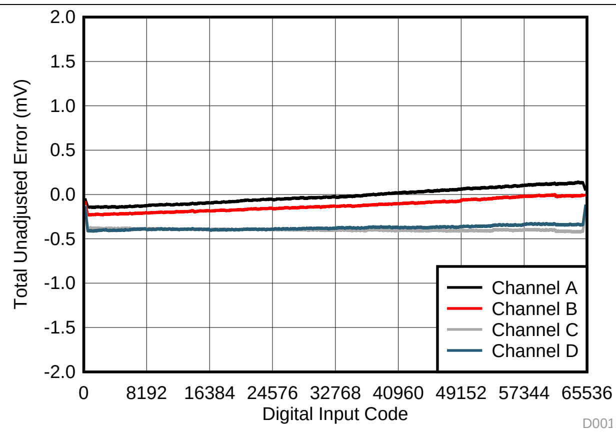
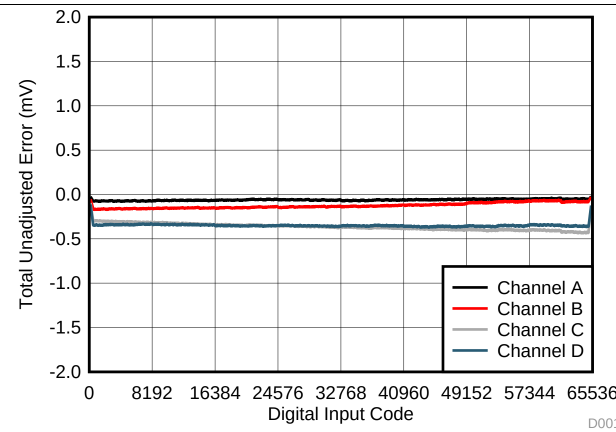


Figure 7. Total Unadjusted Error vs Digital Input Code

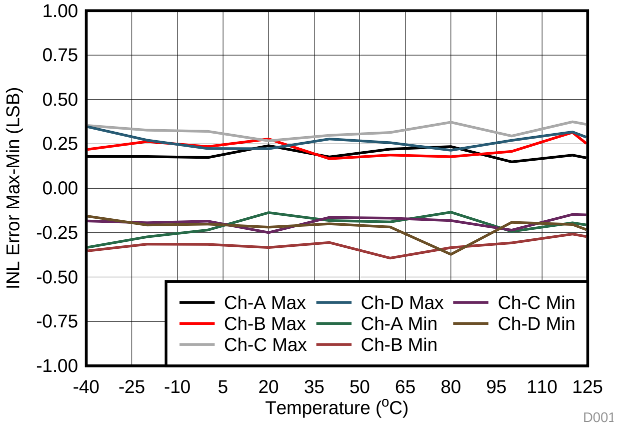


DAC load 5 kΩ//200 pF

Figure 8. Total Unadjusted Error vs Digital Input Code

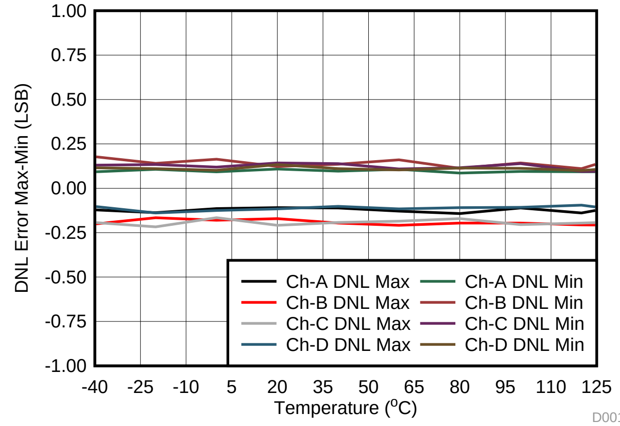
Typical Characteristics (continued)

At T_A = 25°C, VDD = 5.5 V, REFIN = 5.45 V, DAC outputs unloaded, unless otherwise noted.



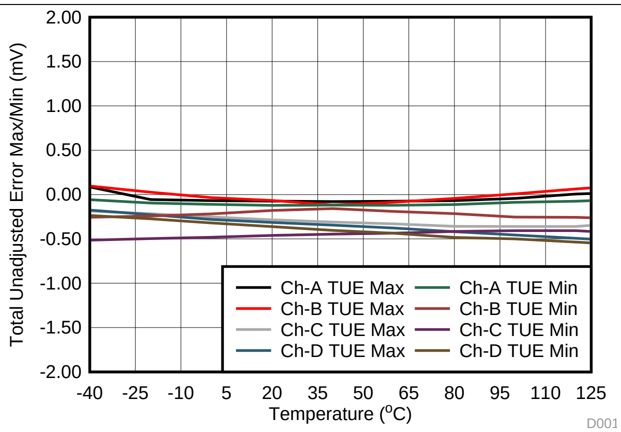
DAC load 5 kΩ//200 pF

Figure 9. Linearity Error (Max-Min) vs Temperature



DAC load 5 kΩ//200 pF

Figure 10. Differential Linearity Error (Max-Min) vs Temperature



DAC load 5 kΩ//200 pF

Figure 11. Total Unadjusted Error Max/Min vs Temperature

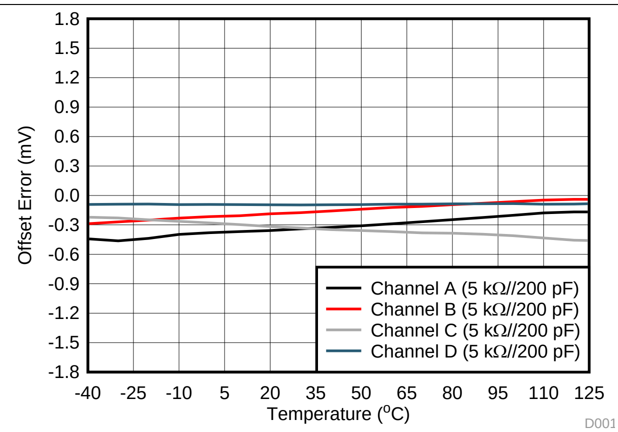


Figure 12. Offset Error vs Temperature

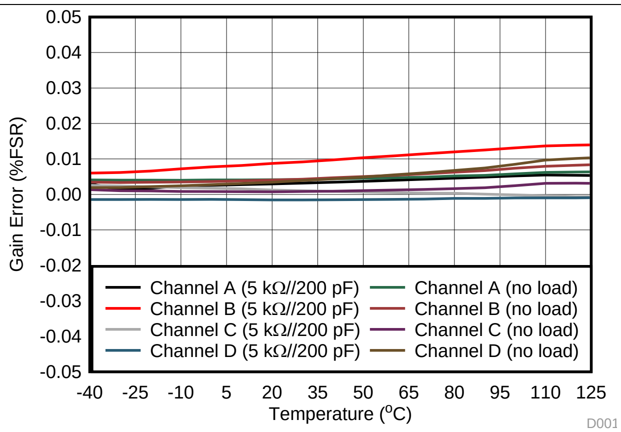


Figure 13. Gain Error vs Temperature

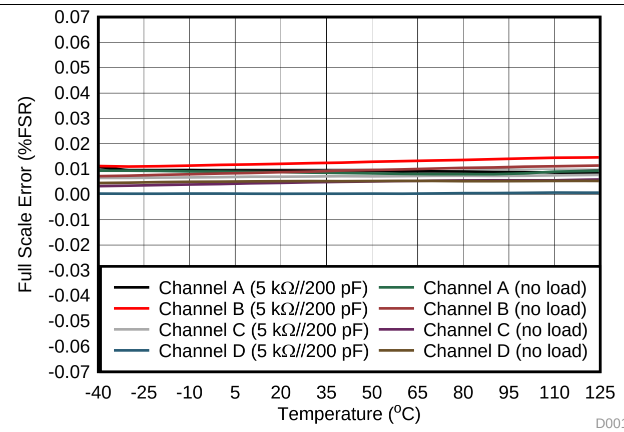


Figure 14. Full Scale Error vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, VDD = 2.7 V, REFIN = 2.5 V, DAC outputs unloaded, unless otherwise noted.

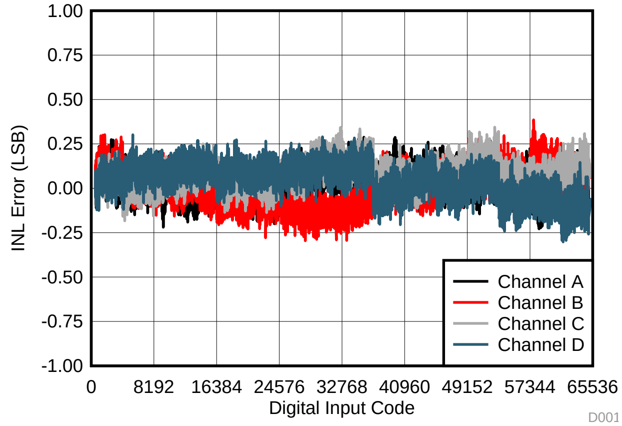


Figure 15. Linearity Error vs Digital Input Code

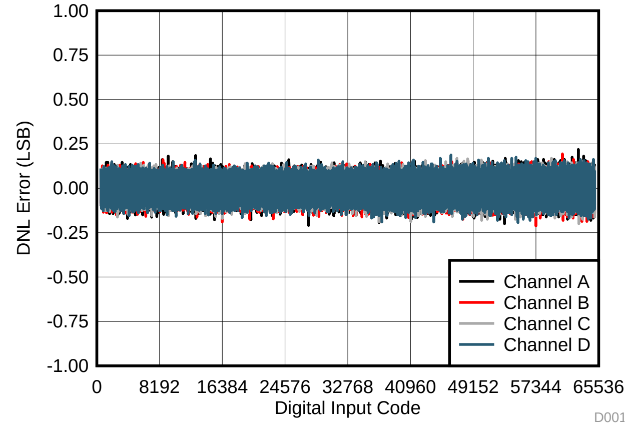
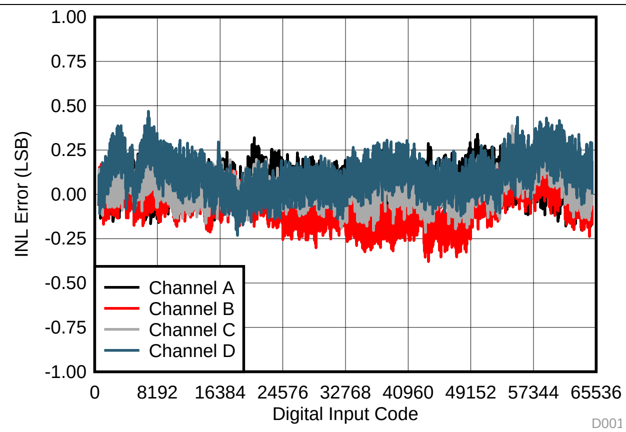
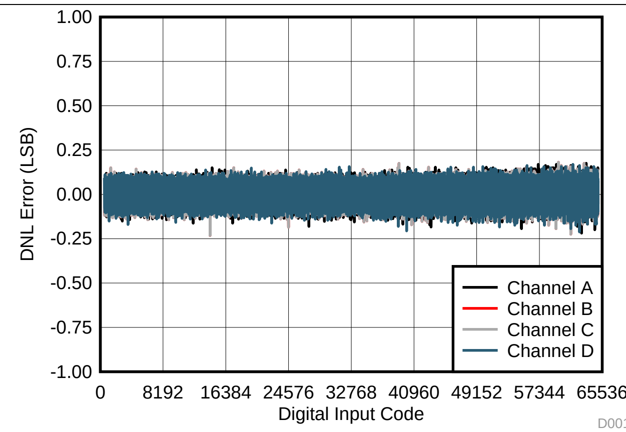


Figure 16. Differential Linearity Error vs Digital Input Code



DAC load 5 kΩ//200 pF

Figure 17. Linearity Error vs Digital Input Code



DAC load 5 kΩ//200 pF

Figure 18. Differential Linearity Error vs Digital Input Code

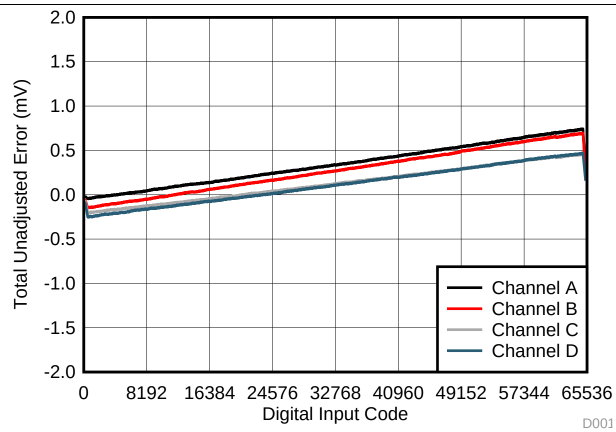
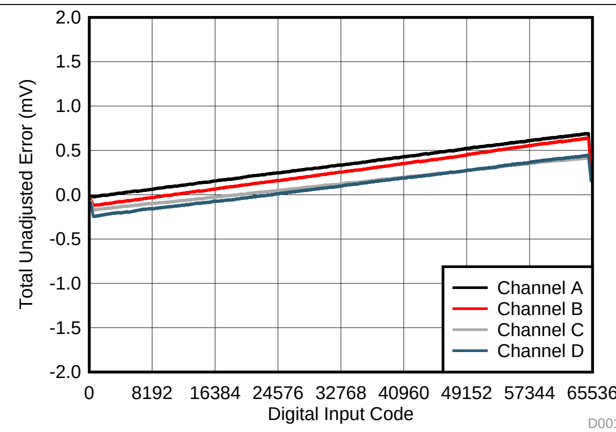


Figure 19. Total Unadjusted Error vs Digital Input Code



DAC load 5 kΩ//200 pF

Figure 20. Total Unadjusted Error vs Digital Input Code

Typical Characteristics (continued)

At T_A = 25°C, VDD = 2.7 V, REFIN = 2.5 V, DAC output unloaded, unless otherwise noted.

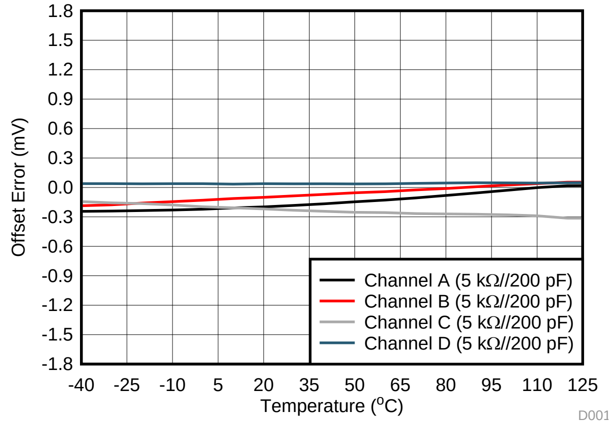


Figure 21. Offset Error vs Temperature

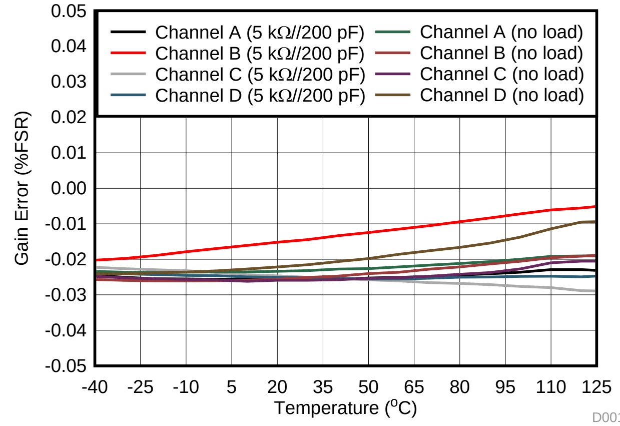


Figure 22. Gain Error vs Temperature

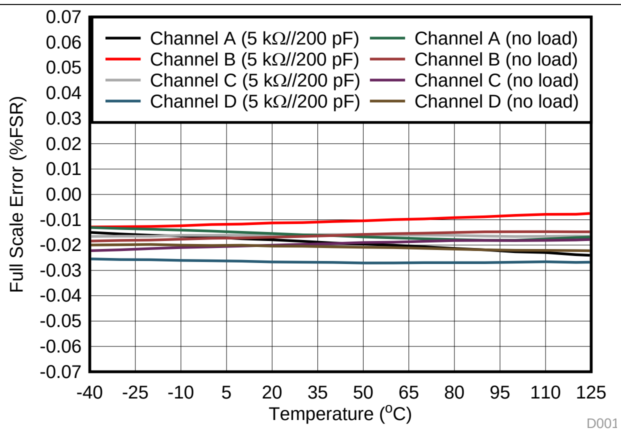
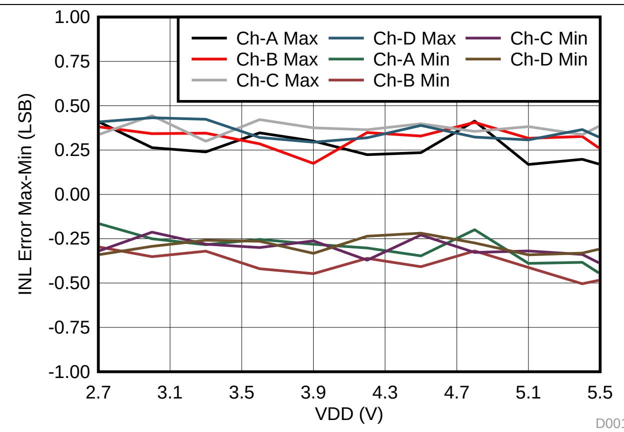
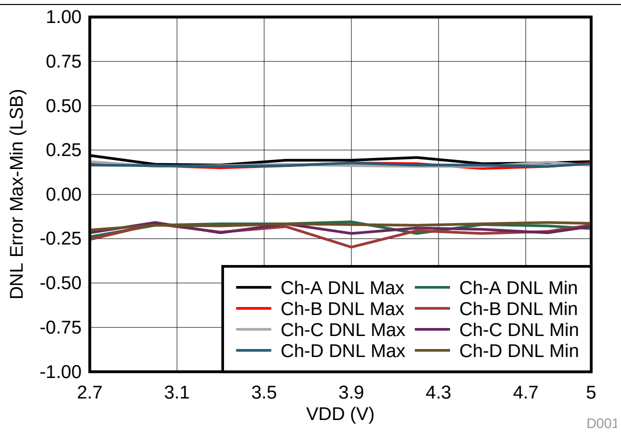


Figure 23. Full Scale Error vs Temperature



DAC load 5 kΩ/200 pF

Figure 24. Linearity Error (Max-Min) vs Power Supply Voltage



DAC load 5 kΩ/200 pF

Figure 25. Differential Linearity Error (Max-Min) vs Power Supply Voltage

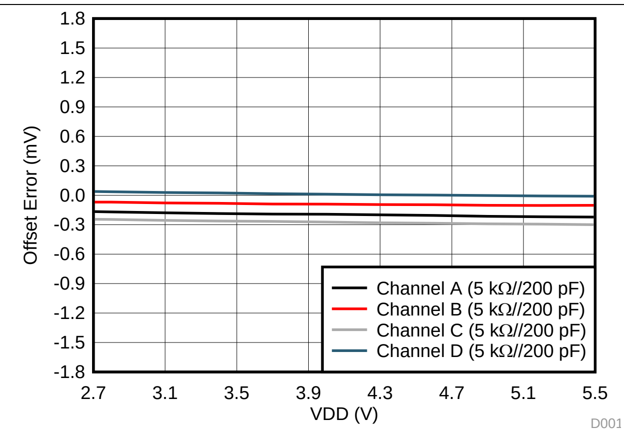


Figure 26. Offset Error vs Power Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, VDD = 5.5 V, REFIN = 2.5 V, DAC output load = 5 kΩ||200 pF, unless otherwise noted.

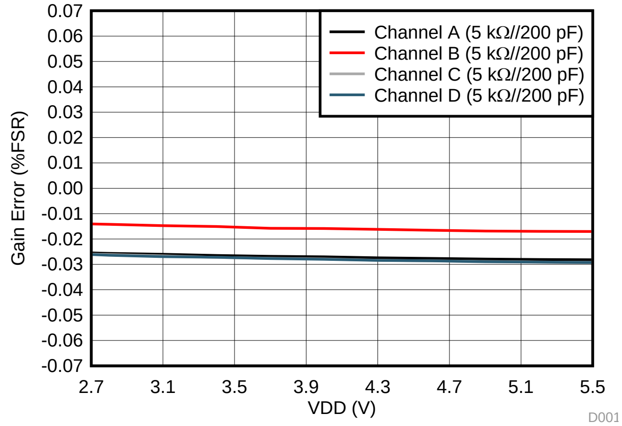


Figure 27. Gain Error vs Power Supply Voltage

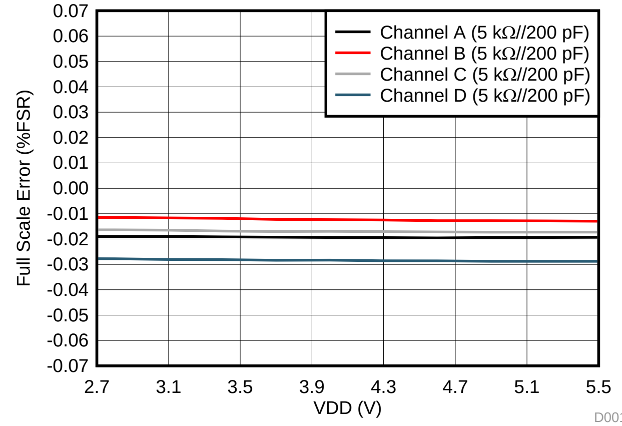


Figure 28. Full Scale Error vs Power Supply Voltage

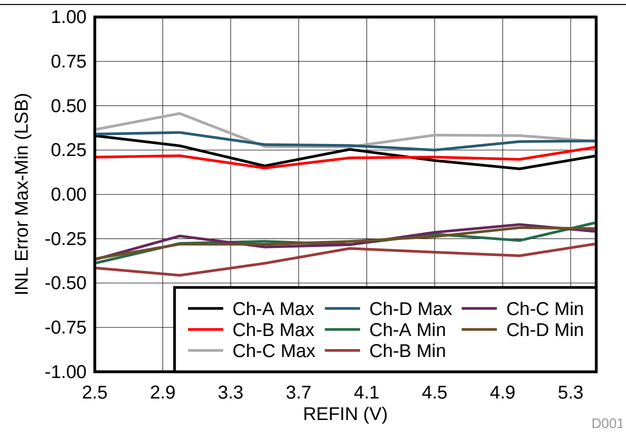


Figure 29. Linearity Error (Max-Min) vs Reference Voltage

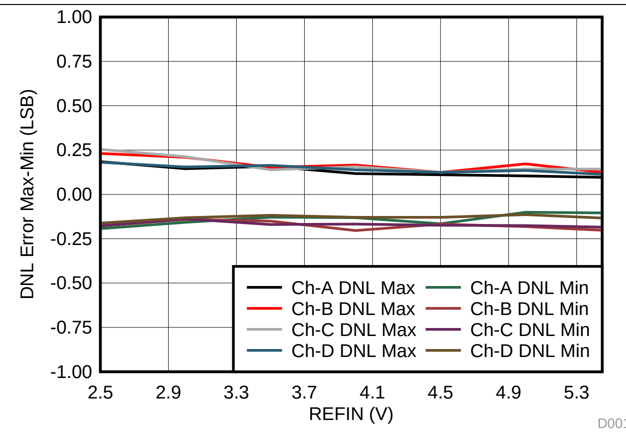


Figure 30. Differential Linearity Error (Max-Min) vs Reference Voltage

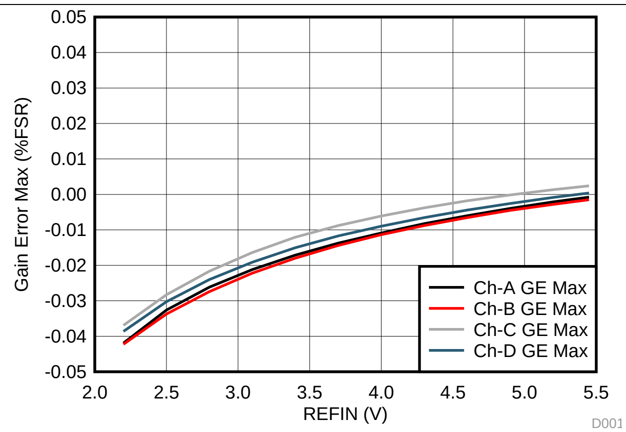


Figure 31. Gain Error (Max) vs Reference Voltage

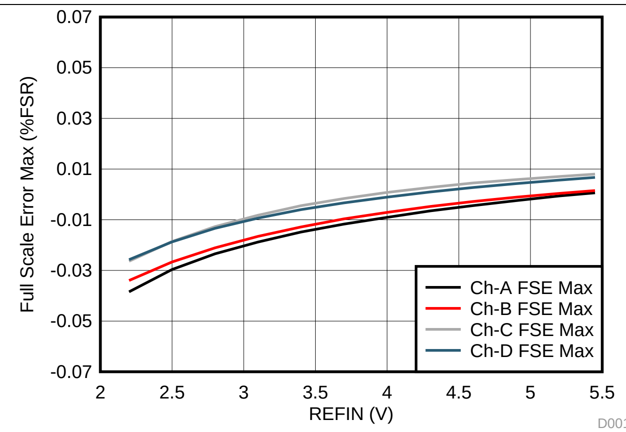


Figure 32. Full Scale Error (Max) vs Reference Voltage

Typical Characteristics (continued)

At T_A = 25°C, VDD = 5.5 V, REFIN = 5.45 V, DAC outputs unloaded, All channels active, unless otherwise noted.

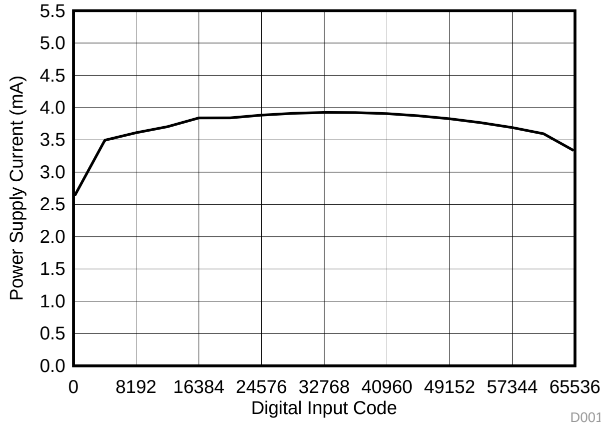
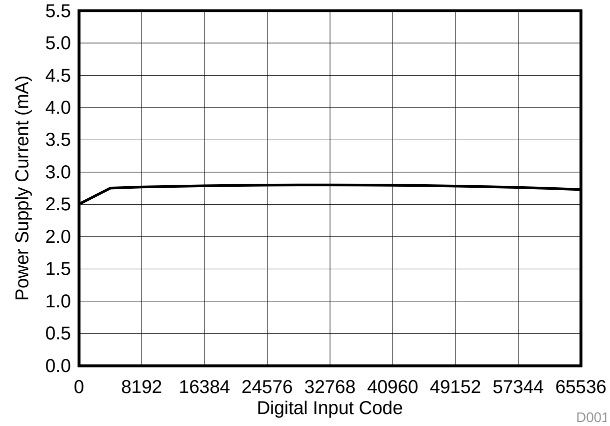
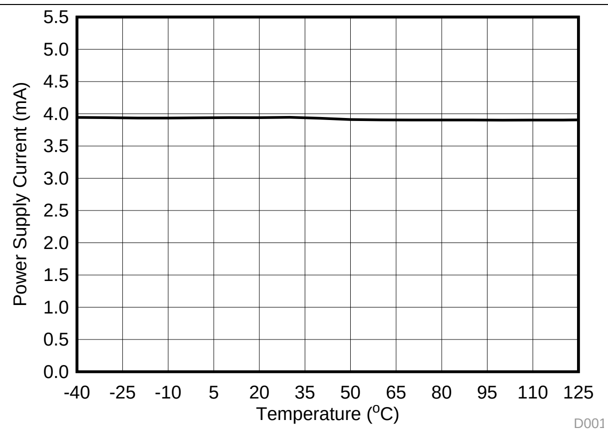


Figure 33. Power Supply Current vs Digital Input Code



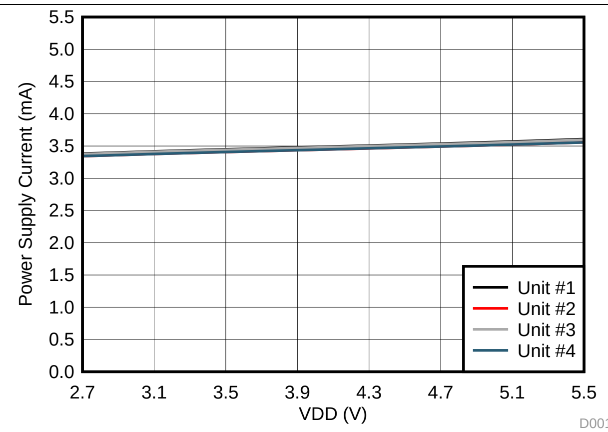
VDD = 2.7 V, REFIN = 2.5 V

Figure 34. Power Supply Current vs Digital Input Code



DAC code = mid-scale code

Figure 35. Power Supply Current vs Temperature



REFIN = 2.5 V, DAC code = mid-scale code

Figure 36. Power Supply Current vs Power Supply Voltage

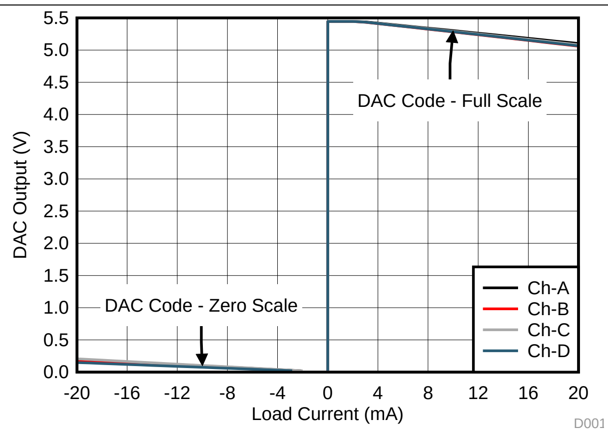
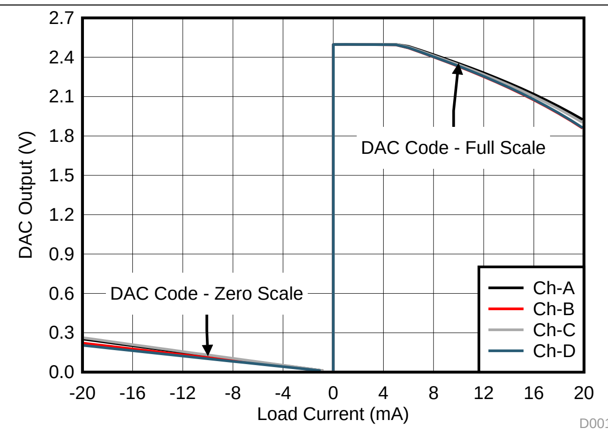


Figure 37. DAC Output Voltage vs Load Current

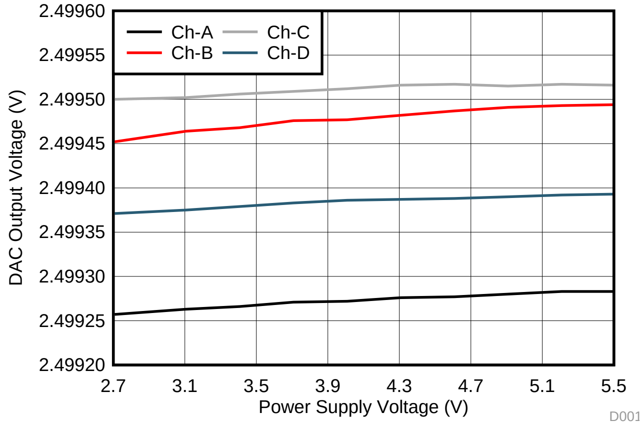


VDD = 2.7 V, REFIN = 2.5 V

Figure 38. DAC Output Voltage vs Load Current

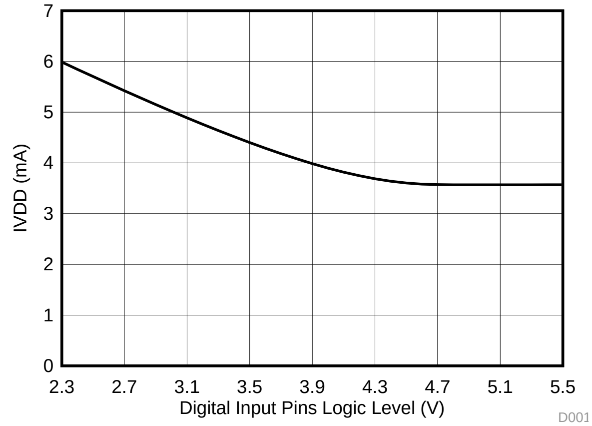
Typical Characteristics (continued)

At T_A = 25°C, VDD = 5.5 V, REFIN = 5.45 V, DAC output load = 5 kΩ||200 pF, unless otherwise noted.



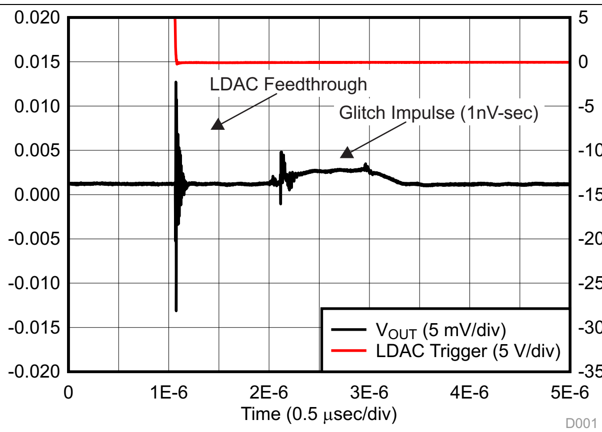
REFIN = 2.5 V, All channels active with full-scale code, DAC unloaded

Figure 39. DAC Output Voltage vs Power Supply Voltage



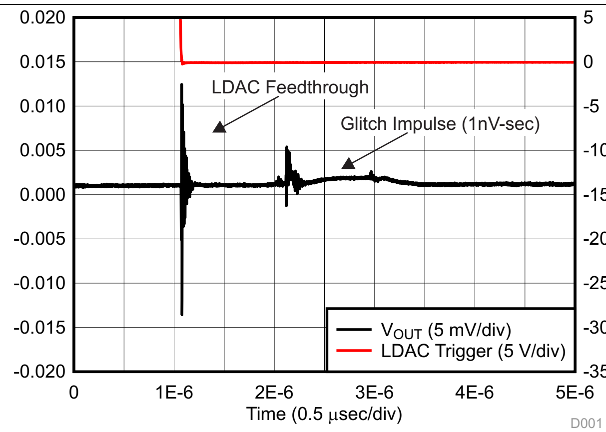
DAC unloaded, All channels to mid-scale

Figure 40. Power Supply Current vs Digital Input Pins Logic Level



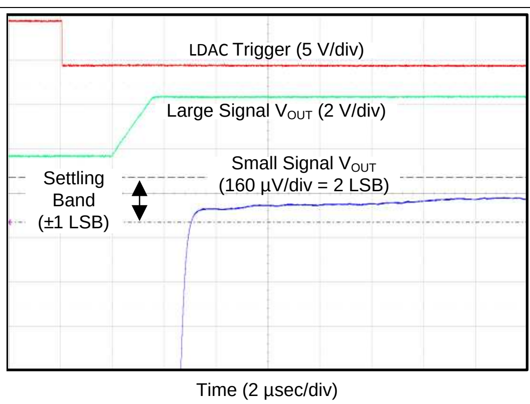
DAC code transition from 8000h to 7FFFh

Figure 41. Glitch Impulse, Falling Edge, 1LSB Step



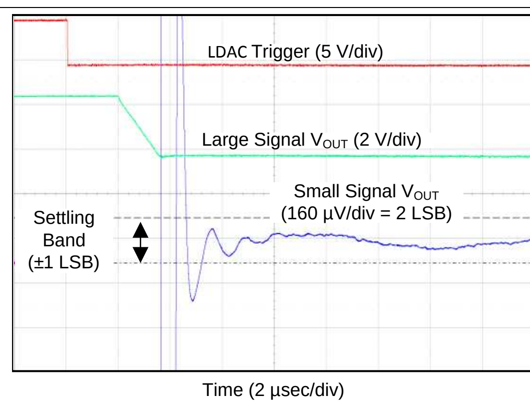
DAC code transition from 7FFFh to 8000h

Figure 42. Glitch Impulse, Rising Edge, 1LSB Step



From code 512d to 65024d, Typical channel shown

Figure 43. Full-Scale Settling Time, Rising Edge

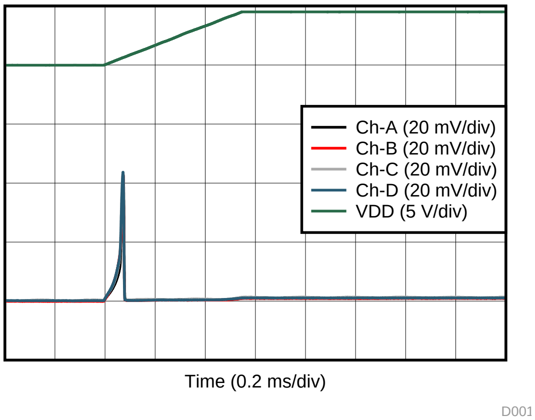


From code 65024d to 512d, Typical channel shown

Figure 44. Full-Scale Settling Time, Falling Edge

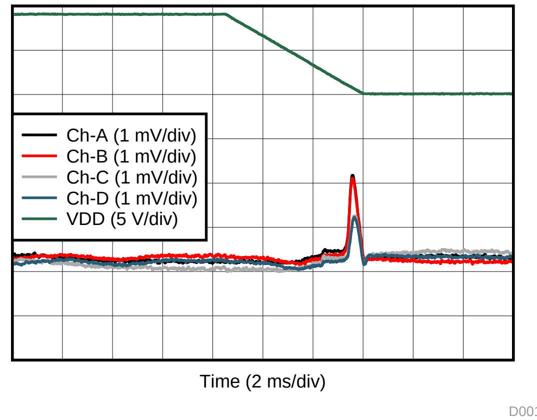
Typical Characteristics (continued)

At T_A = 25°C, VDD = 5.5 V, REFIN = 5.45 V, DAC output load = 5 kΩ||200 pF, unless otherwise noted.



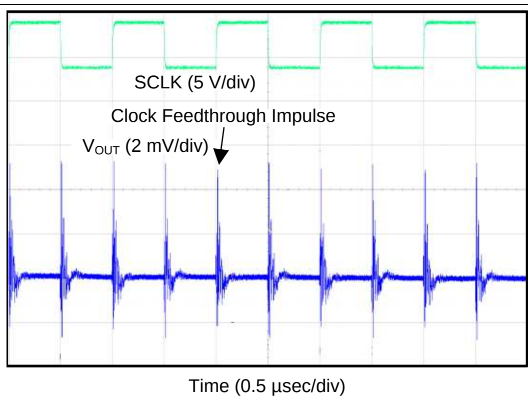
DAC unloaded

Figure 45. Power-On Glitch, Reset to Zero Scale



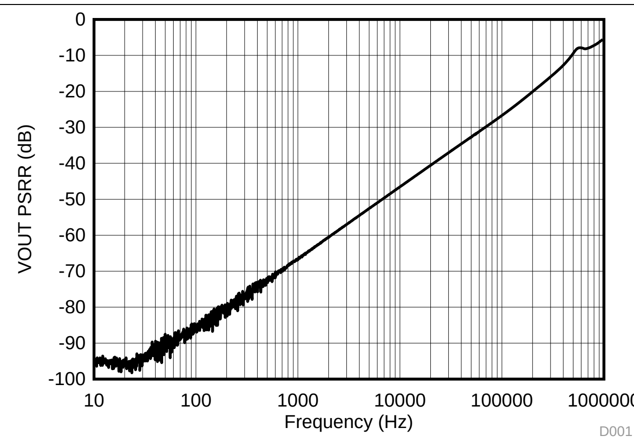
DAC in power down mode (1 kΩ-GND)

Figure 46. Power-Off Glitch, Reset to Zero Scale



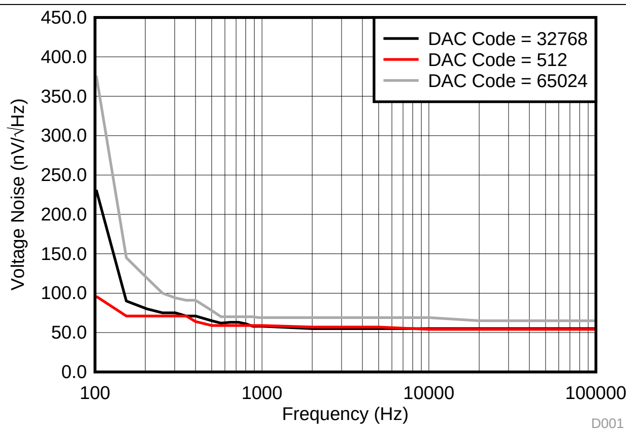
DAC unloaded, DAC code mid-scale, Typical channel shown

Figure 47. Clock Feedthrough, 1MHz Midscale



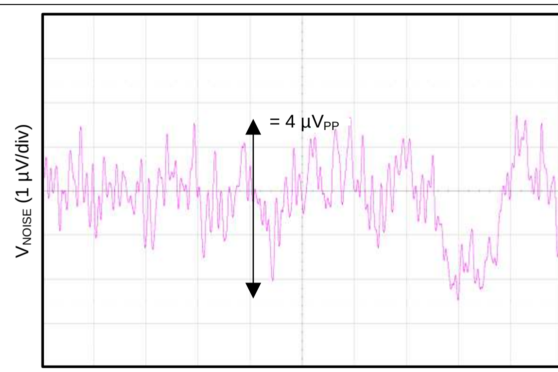
VDD = 5.0 + 1 VPP (Sinusoid), REFIN = 2.5 V, DAC code full-scale, Typical channel shown

Figure 48. DAC Output AC PSRR vs VDD



DAC unloaded, Typical channel shown

Figure 49. DAC Output Noise Density vs Frequency



DAC unloaded, DAC code mid-scale, Typical channel shown

Figure 50. DAC Output Noise, 0.1 Hz to 10 Hz

8 Detailed Description

8.1 Overview

The DAC80004, DAC70004, and DAC60004 are quad-channel, 16-bit, voltage-output DACs with internal reference buffers and output buffers. Each channel consists of an R-2R ladder configuration with the 4 MSBs segmented, followed by an operational amplifier, as shown in Figure 51. The DACx0004 devices have a constant impedance (30 kΩ typical), buffered reference input. The output of the reference buffers drives the R-2R ladders. With the production trim process these devices have excellent dc accuracy and ac performance.

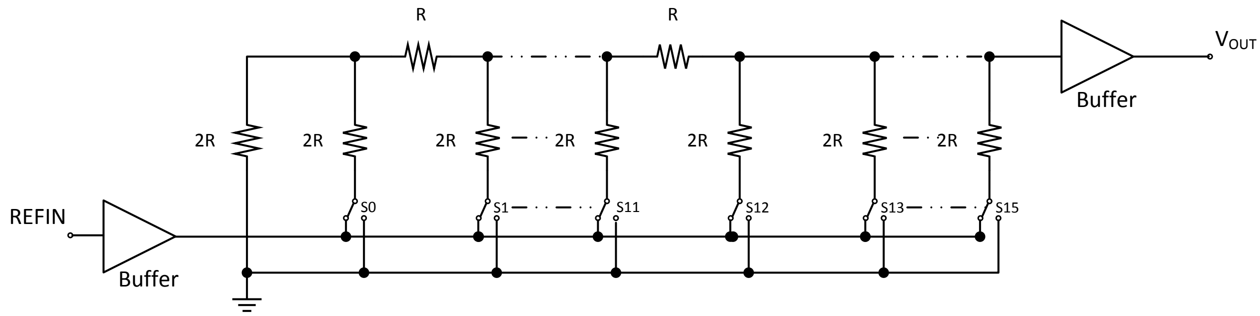


Figure 51. DACx0004 Architecture

The input coding to the DACx0004 is straight binary, so the ideal output voltage is given by Equation 1:

$$V_{OUT} = \left(\frac{D_{IN}}{2^N}\right) \text{ x REFIN} \quad (1)$$

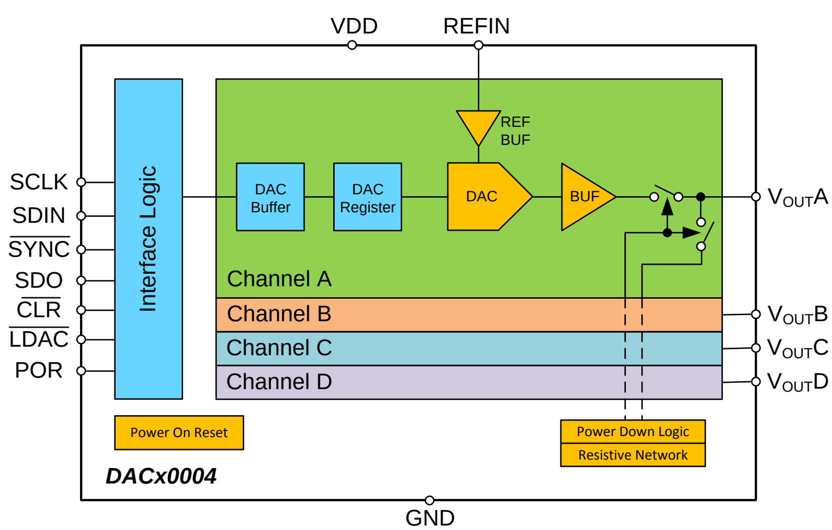
Where:

N = resolution in bits; either 16 (DAC80004), 14 (DAC70004) or 12 (DAC60004)

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. D_{IN} ranges from 0 to 2^N –1

REFIN = DAC reference voltage

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Amplifier

The DACx0004 output buffer amplifier is capable of generating near rail-to-rail voltages on its output, giving a maximum output range of 0 V to REFIN. It is capable of driving a load of 5 kΩ in parallel with 2 nF to GND. The typical slew rate of this amplifier while driving no load is 1.5 V/µs, with a full-scale settling time of 8 µs to 1 LSB of the final value as shown in Figure 43 and Figure 44. The current consumption of the amplifier (unloaded) is 1 mA/channel (typical). The DACx0004 output amplifier also implements a short circuit current limiting circuit. The default value of short circuit limit is 40 mA, however this can be reduced to 30 mA using dedicated bits (1 per channel) via SPI command 1010 (see Table 2).

8.3.2 Reference Buffer

The DACx0004 requires an external reference to operate. The reference input pin has the following input range:

2.2 V to (V_{DD} – 0.2) for 2.7 V ≤ V_{DD} ≤ 4.5 V

2.2 V to V_{DD} for 4.5 V ≤ V_{DD} ≤ 5.5 V

The DACx0004 contains a dedicated reference buffer for each DAC channel. The REFIN pin drives the input of these buffers. The integrated reference buffers offers constant impedance of 30 kΩ (typical) at the REFIN pin. This simplifies the external reference drive circuit for the device.

8.3.3 Power-On Reset

The DACx0004 contain a power-on-reset circuit that controls the output voltage during power up. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. At power up all DAC registers are filled with power-on reset code (see Table 1).

8.3.3.1 POR Pin Feature

The DAC power-on reset code for all of the channels depends on the state of the POR pin at power up (see *Pin Configuration and Functions*).

Each DAC channel remains that way until a valid load command is written to it. All device registers are reset at power up as shown in Table 1.

Table 1. DACx0004 Power-On Reset Values

REGISTER NAME	DACx0004 - POWER-ON RESET VALUE
	TSSOP-/VSON-14
DAC latches (per channel)	If POR pin = '0' then Zero Scale else Mid scale
DAC buffers (per channel)	If POR pin= '0' then Zero Scale else Mid scale
Power down (per channel)	00 – Normal mode
Clear mode	00 – Clear to Zero
Ignore LDAC (per channel)	0000 – Do not ignore
Daisy chain	0 – Daisy chain disabled, DAC update at 32nd SCLK falling edge
Short circuit limit (per channel)	0000 – all DACs 40 mA

8.3.3.2 Internal Power-On Reset (IPOR) Levels

When the device powers up, an IPOR circuit sets the device in default mode as shown in Table 1. The IPOR circuit requires specific V_{DD} levels, as indicated in Figure 52, to ensure discharging of internal capacitors and to reset the device on power up. In order to ensure a power-on reset, V_{DD} must be below 0.7 V for at least 1 ms. When V_{DD} drops below 2.4 V but remains above 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power supply conditions. In this case, In this case a power-down reset is recommended. When V_{DD} remains above 2.4 V, a power-on reset does not occur.

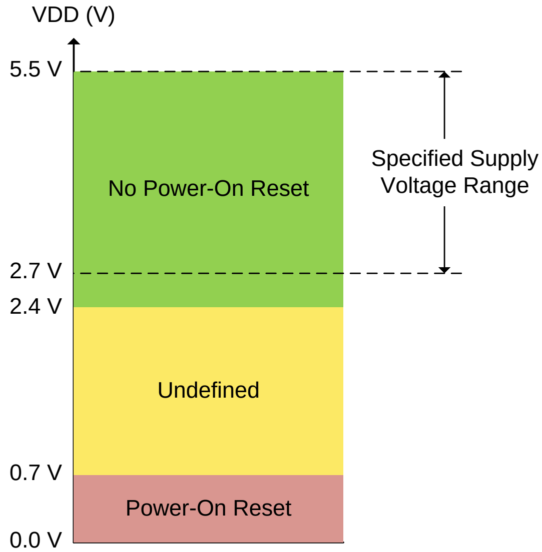


Figure 52. Relevant Voltage Levels for IPOR Circuit

8.4 Device Functional Modes

8.4.1 Serial Interface

The DACx0004 devices have a 4-wire serial interface: $\overline{\text{SYNC}}$, SCLK, SDIN, and SDO (see *Pin Configuration and Functions*). The serial interface (3-wire and 4-wire) is compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs and it operates up to 50 MHz. See the Write Mode Stand-Alone Timing and Write Mode Daisy-Chain Timing diagrams (see Figure 1 and Figure 2) for examples of typical write and read sequences. The input shift register is 32 bits wide.

8.4.1.1 Stand-Alone Mode

The serial clock SCLK can be a continuous or a gated clock. The first falling edge of $\overline{\text{SYNC}}$ starts the operation cycle. When $\overline{\text{SYNC}}$ is high, the SCLK and SDIN signals are blocked and the SDO pin (TSSOP-14 and VSON-14 packages) is in a Hi-Z state. The device internal registers are updated from the shift register on the 32nd falling edge of SCLK.

8.4.1.1.1 $\overline{\text{SYNC}}$ Interrupt – Stand-Alone Mode

For stand-alone operation, the $\overline{\text{SYNC}}$ line stays low for at least 32 falling edges of SCLK and the addressed DAC register updates on the 32nd SCLK falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd SCLK falling edge, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (as shown in Figure 53).

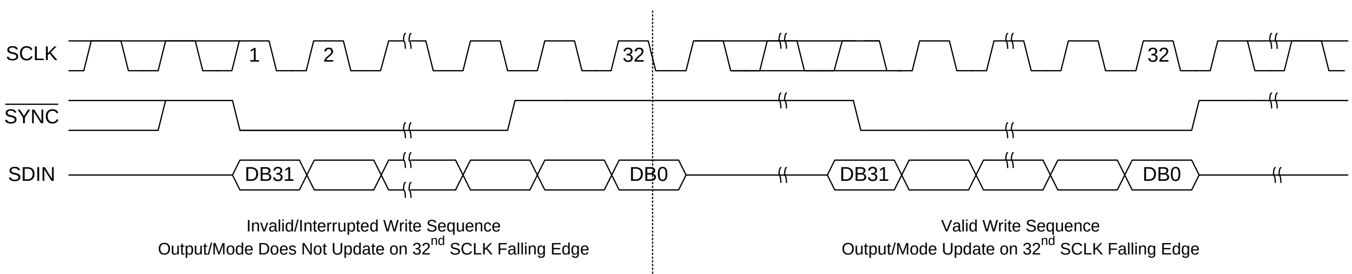


Figure 53. $\overline{\text{SYNC}}$ Interrupt – Stand Alone Operation

Device Functional Modes (continued)

8.4.1.1.2 Read-Back Mode

The READ command is used to start read-back operation. However, before read-back operation can be initiated, the SDO pin must be enabled by setting the DSDO bit to '1'; this bit is disabled by default. Read-back operation is then started by executing a READ command (R/W bit = '1', see Table 3). Bits C3 to C0 select the register to be read. The remaining data in the command are don't care bits. During the next SPI operation, the data appearing on the SDO output are from the previously addressed register. For a read of a single register, a NOP (No Operation) command (1110) can be used to clock out the data from the selected register on SDO. Multiple registers can be read if multiple READ commands are issued (see Figure 54).

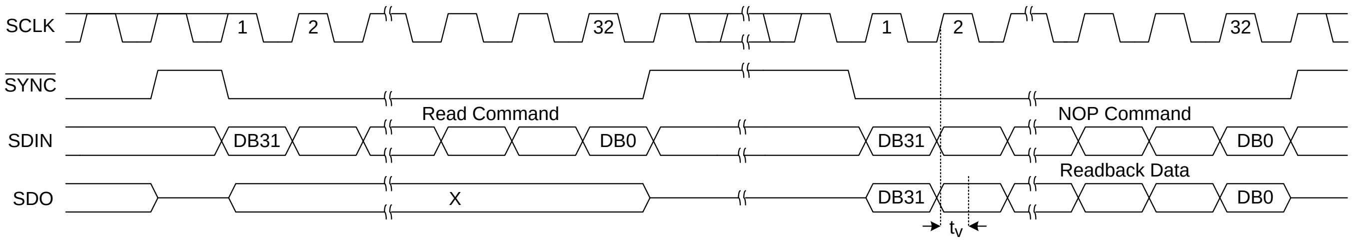


Figure 54. Read-Back Operation

8.4.1.2 Daisy-Chain Mode

For systems that contain more than one device, the SDO pin can be used to daisy-chain multiple devices together (see Figure 55). Daisy-chain operation can be useful in system diagnostics and in reducing the number of serial interface lines. The daisy-chain feature can be enabled by writing a logic '1' to the DSDO bit (see Table 3); the SDO pin is set to HIZ when the DSDO bit is set to 0.

The first falling edge of $\overline{\text{SYNC}}$ starts the operating cycle. SCLK is continuously applied to the SPI shift register when $\overline{\text{SYNC}}$ is low. If more than 32 clock pulses are applied, the data ripples out of the shift register and appear on the SDO line. The data bits are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO pin of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed (see Figure 2). Each device in the system requires 32 clock pulses. Therefore, the total number of clock cycles must equal 32 × N, where N is the total number of DACx0004s in the chain. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This action latches the data from the SPI shift registers to the device internal registers for each device in the daisy-chain and prevents any further data from being clocked in. The serial clock can be a continuous or a gated clock. Note that a continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. For gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ must be taken high after the final clock in order to latch the data.

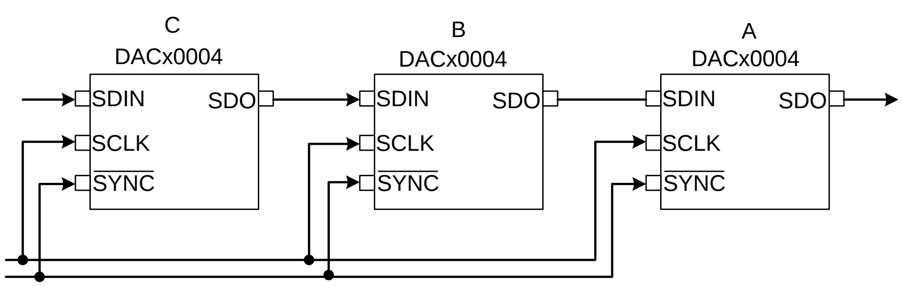


Figure 55. DACx0004 in Daisy Chain Mode

8.4.1.2.1 $\overline{\text{SYNC}}$ Interrupt – Daisy-Chain Mode

For daisy-chain operation, the $\overline{\text{SYNC}}$ line stays low for at least 32 × N SCLK cycles, where N is the number of DACx0004s in the daisy chain. If $\overline{\text{SYNC}}$ is brought high before a multiple 32 SCLKs, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (see Figure 56).

Device Functional Modes (continued)

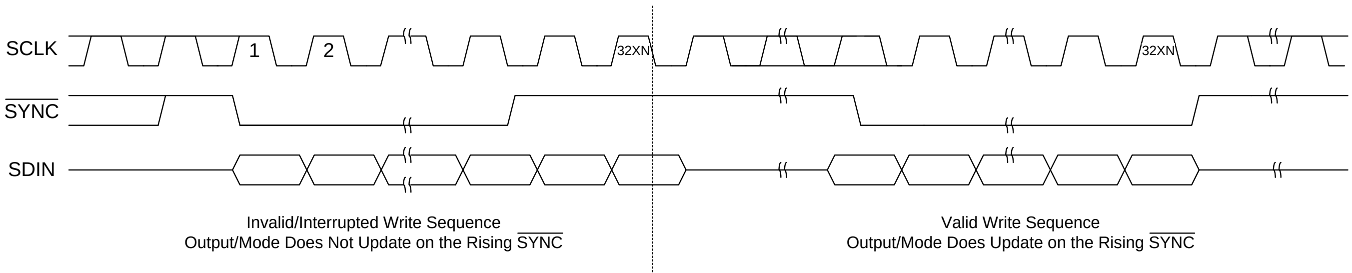


Figure 56. $\overline{\text{SYNC}}$ Interrupt – Daisy-Chain Operation

8.4.2 SPI Shift Register

The SPI shift register is 32 bits wide, as shown in Table 2. The shift register command mapping is shown in Table 3. The DACx0004 accepts DAC code in straight binary format. Note that, the DAC data is left alligned from MSB (D19) to LSB (D4 - 16 bits, D6 - 14 bits, D8 - 12 bits).

Table 2. DACx0004 SPI Shift Register Format

D31	D30	D29	D28	D27-D24	D23-D20	D19-D04	D03-D00
Don't Cares			R/W	Command Bits	Channel Address Bits	16/14/12-Bit DAC Data left alligned/Power Down Bits/Device Ready bit	Mode Bits

Table 3. DAC Commands

D31 - D28		D27 - D24				D23 - D20	D19 - D16	D15 - D12	D11 - D08			D07 - D04		D03 - D00				Commands
X	$\overline{\text{W}}$/R	0	0	0	0	Channel Address	DAC Data	DAC Data	DAC Data			DAC Data		X				Write to buffer n
X	$\overline{\text{W}}$	0	0	0	1	Channel Address	X	X	X			X		X				Update DAC n
X	$\overline{\text{W}}$	0	0	1	0	Channel Address	DAC Data	DAC Data	DAC Data			DAC Data		X				Write to buffer n and update all DACs (Software $\overline{\text{LDAC}}$)
X	$\overline{\text{W}}$	0	0	1	1	Channel Address	DAC Data	DAC Data	DAC Data			DAC Data		X				Write to buffer and update DAC n
X	$\overline{\text{W}}$/R	0	1	0	0	X	X	X	X	PD1	PD0			Ch-D	Ch-C	Ch-B	Ch-A	Power up/down DAC n
X	$\overline{\text{W}}$/R	0	1	0	1	X	X	X	X			X		X	X	CM1	CM0	Clear mode register
X	$\overline{\text{W}}$/R	0	1	1	0	X	X	X	X			X		Ch-D	Ch-C	Ch-B	Ch-A	LDAC register
X	$\overline{\text{W}}$	0	1	1	1	X	X	X	X			X		X				Software reset
X	$\overline{\text{W}}$/R	1	0	0	0	X	X	X	X			X		X		DSD 0	X	Disable SDO register
X	X	1	0	0	1	X	X	X	X			X		X				Reserved
X	$\overline{\text{W}}$/R	1	0	1	0	X	X	X	X			X		Ch-D	Ch-C	Ch-B	Ch-A	Short circuit limit register
X	$\overline{\text{W}}$	1	0	1	1	X	X	X	X			X		X				Software clear
X	X	1	1	0	0	X	X	X	X			X		X				Reserved
X	R	1	1	0	1	X	X	X	X			X	DRDY	X				Status register
X	$\overline{\text{W}}$	1	1	1	0	X	X	X	X			X		X				No operation (NOP)
X	X	1	1	1	1	X	X	X	X			X		X				Reserved

Table 4. Channel Address Bits

CHANNEL ADDRESS BITS				DESCRIPTION
D23	D22	D21	D20	
0	0	0	0	Select channel A
0	0	0	1	Select channel B
0	0	1	0	Select channel C
0	0	1	1	Select channel D
1	1	1	1	Select all channel

8.4.3 DAC Power-Down Modes

The DACx0004 use four modes of operation. These modes are accessed by setting command bits D28 – D24 and power-down register bits D09 and D08. The command bits must be set to 0100 (see Table 3). Once the command bits are set correctly, the four different power-down modes are software programmable by setting bits D09 and D08 in the shift register. Table 5 shows how to control the operating mode with data bits PD1 (D09), PD0 (D08).

Table 5. Power-Down Bits

POWER DOWN BITS		DESCRIPTION
D09	D08	
0	0	Normal operation/power up selected channel(s) (Default)
0	1	Power down selected channel(s) 1 kΩ-GND
1	0	Power down selected channel(s) 100 kΩ-GND
1	1	Power down selected channel(s) Hi-Z

It is possible to write to the DAC register/buffer of the DAC channel that is powered down. When the DAC channel is then powered up, it powers up to this new value.

The advantage of the available power-down modes is that the output impedance of the device is known while it is in power-down mode. As described in Table 5, there are three different power-down options. $V_{OUT}X$ can be connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor, or open-circuited (Hi-Z). The DAC power-down circuitry is shown in Figure 57.

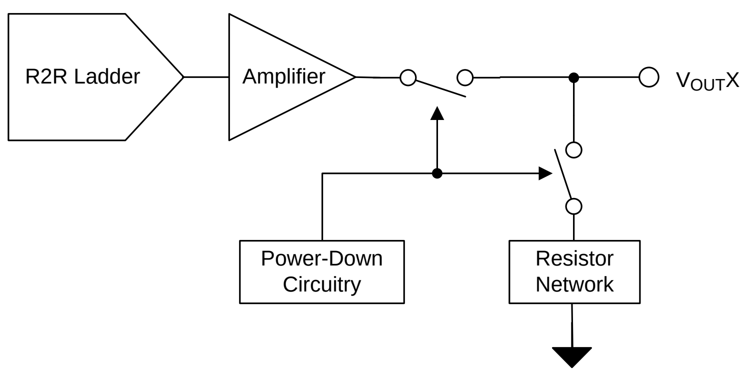


Figure 57. DACx0004 Power Down

8.4.4 $\overline{\text{CLR}}$ Pin Functionality and Software CLEAR Mode

The $\overline{\text{CLR}}$ pin is an asynchronous input pin to the DAC. When activated, this falling edge sensitive pin clears the DAC buffers and the DAC latches to zero, mid, full or user programmed code depending on the clear mode register (see Table 6). The default setting for clear operation is clear to 0 V. The device exits clear mode on the 32nd falling edge of the next write to the device. If the $\overline{\text{CLR}}$ pin receives a falling edge signal during a write sequence in normal operation, the clear mode is activated and changes the input and DAC registers immediately. Additionally, all DAC registers can also be cleared via SPI command 1011. Note that the clear mode bits determine the clear code for all the DACs upon clear operation.

8.4.4.1 DAC Clear Mode Registers

The DACx0004 implement four different clear modes. These modes are accessed by setting command bits D28 – D24 and clear mode register bits D01 and D00. The command bits must be set to 0101 (see Table 3). Based on the value of clear mode register (see Table 6), all of the DAC and the buffers are cleared to zero, mid, or full-scale code, when the $\overline{\text{CLR}}$ pin sees a falling edge or after a software clear command is issued.

The user defined clear scale can be set by writing 16-/14-/12- data to 1001 to bits D28 – D24.

Table 6. Clear Mode Bits

CLEAR MODE BITS		DESCRIPTION
D01	D00	
0	0	All DACs clear to zero scale (default)
0	1	All DACs clear to mid scale
1	0	All DACs clear to full scale

8.4.5 $\overline{\text{LDAC}}$ Pin Functionality

The DACx0004 devices offer both a software and hardware simultaneous update and control function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. Data updates can be performed either in synchronous or in asynchronous mode.

In asynchronous mode, the $\overline{\text{LDAC}}$ pin is used as an active low signal for simultaneous DAC updates. Multiple single-channel writes can be done in order to set different channel buffers to desired values and then pulse the $\overline{\text{LDAC}}$ pin low to simultaneously update the DAC output registers. Data buffers of all channels must be loaded with desired data before an $\overline{\text{LDAC}}$ low pulse. After a $\overline{\text{LDAC}}$ low pulse, all DACs are simultaneously updated with the last contents of the corresponding data buffers. If the content of a data buffer is not changed, the corresponding DAC output remains unchanged after the $\overline{\text{LDAC}}$ pin is pulsed low.

In synchronous mode, data are updated with the falling edge of the 32nd SCLK cycle, which follows a falling edge of $\overline{\text{SYNC}}$. For such synchronous updates, the $\overline{\text{LDAC}}$ pin is not required, and it must be connected to GND permanently or asserted and held low before sending commands to the device.

8.4.5.1 Software $\overline{\text{LDAC}}$ Mode Registers

Alternatively, all DAC outputs can be updated simultaneously using the built-in software function of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ register offers additional flexibility and control by allowing the selection of which DAC channel(s) should be updated simultaneously when the $\overline{\text{LDAC}}$ pin is being brought low. The $\overline{\text{LDAC}}$ register is loaded with a 4-bit word (D03 and D00) using command bits D28 – D24 (see Table 3). The default value for each bit, and therefore for each DAC channel, is zero. If the $\overline{\text{LDAC}}$ register bit is set to 1, it overrides the $\overline{\text{LDAC}}$ pin (the $\overline{\text{LDAC}}$ pin is internally tied low for that particular DAC channel), and this DAC channel updates synchronously after the falling edge of the 32nd SCLK cycle. However, if the $\overline{\text{LDAC}}$ register bit is set to 0, the DAC channel is controlled by the $\overline{\text{LDAC}}$ pin.

See Table 7 for more information.

Table 7. $\overline{\text{LDAC}}$ Register

$\overline{\text{LDAC}}$ REGISTER BITS (D03 – D00)	DAC UPDATE
0	Determined by $\overline{\text{LDAC}}$ pin (Default)
1	DAC channel ignores $\overline{\text{LDAC}}$ pin, DAC updates on 32nd falling edge of SCLK, DAC channels see $\overline{\text{LDAC}}$ as 0

8.4.6 Software Reset Mode

The DACx0004 implements a software reset feature. The software reset function uses command bits D28 – D24 (see Table 3). Table 1 shows the reset values for different registers.

8.4.7 Output Short Circuit Limit Register

The DACx0004 output amplifier has a default short circuit limit of 40 mA. However, this limit can be reduced to 30 mA by using command 1010 on bits D28 – D24 and selecting channel(s) (D03 – D00). Please note that DACx0004 has a dedicated bit per channel, this allows the user to set different short circuit limit for different DAC output channels.

Table 8. Short Circuit Limit Register

SHORT CIRCUIT LIMIT REGISTER BITS (D03 – D00)	DAC SHORT CIRCUIT LIMIT
0	DAC output short circuit limit = 40 mA (Default)
1	DAC output short circuit limit = 30 mA

8.4.8 Status Register

The DACx0004 implements a read-only status register (see Table 3). This register can be read by using command 1101 on bits D28 – D24, followed by a NOP command.

Logic ‘1’ on bit D04 indicates that the device is ready to be used. This feature is useful to check if the device is ready to accept commands after power up.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application - Digitally Controlled Asymmetric Bipolar Output

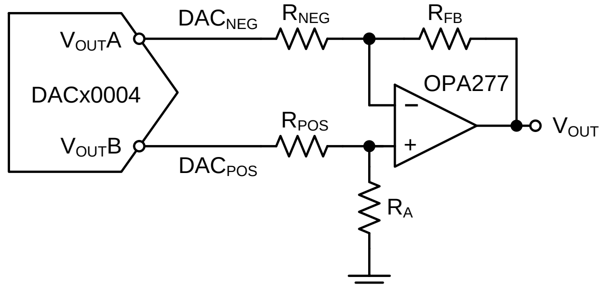


Figure 58. Asymmetric Bipolar Output Block Diagram

9.2.1 Design Requirements

This design requires two channels of the DACx0004 to generate a bipolar output. The design is very flexible and allows for many different configurations. Typically, one channel is used to finely control the output, while the other is used to offset the output. The direction of the offset depends on which channel is used as an offset. DAC_{POS} provides a positive offset and DAC_{NEG} has a negative offset.

9.2.2 Detailed Design Procedure

The output of each DAC can be modified via the digital interface and the gain of each output can be modified independently by changing the external resistors. In order for the gain of each offset to be independent, Equation 2 must be true.

$$R_A = \left(\frac{1}{R_{FB}} + \frac{1}{R_{NEG}} - \frac{1}{R_{POS}} \right)^{-1} \tag{2}$$

The output voltage range, V_{OUT}, is adjusted according to Equation 3. Keep in mind that Equation 3 is only true when Equation 2 is true.

$$V_{OUT} = DAC_{POS} \times \frac{R_{FB}}{R_{POS}} - DAC_{NEG} \times \frac{R_{FB}}{R_{NEG}} \tag{3}$$

Each DAC outputs a voltage from 0 to REFIN. As an example, if DAC_{POS} gain is 1, DAC_{NEG} gain is 2 and R_{FB} = 2 kΩ, then R_{POS} = 2 kΩ, R_{NEG} = 1 kΩ and R_A = 1 kΩ. With the correct digital implementation it gives the output an effective output range of ±15 V, with discrete 16-bit steps.

Typical Application - Digitally Controlled Asymmetric Bipolar Output (continued)

9.2.3 Application Curve

Figure 59 displays two different modes of operation. Mode 1 gains the output of DAC_{Neg} by a factor of 2 and maintains DAC_{POS} at unity gain. Mode 2 reverses the gains of each stage to invert the system. These are just two examples of the types of outputs that can be achieved using this configuration.

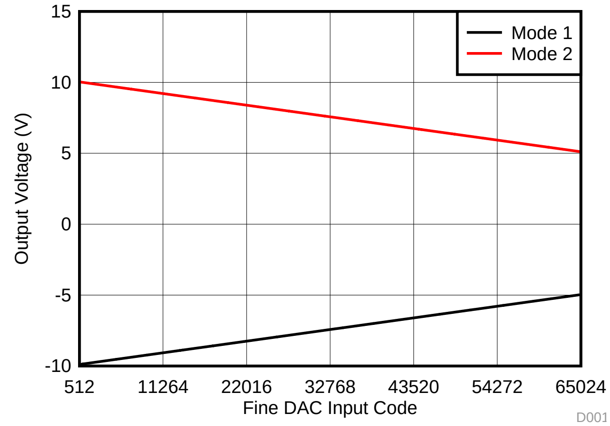


Figure 59. Output Voltage vs Fine DAC Input Code

10 Power Supply Recommendations

The DACx0004 can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to VDD should be well-regulated and have low-noise. Switching power supplies and DC-DC converters often have high frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. A 1 µF to 10 µF capacitor and 0.1 µF bypass capacitor is recommended in order to further minimize noise from the power supply. The current consumption on the VDD pin, the short-circuit current limit, and the load current for the device are listed in the *Electrical Characteristics*. The power supply must meet the aforementioned current requirements.

11 Layout

11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. As a general rule it is important to keep digital traces as far away from analog traces when possible.

The DACx0004 is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

Due to the single ground pin of the DACx0004, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND must be connected directly to an analog ground plane. This plane must be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

As with the GND connection, VDD should be connected to a 5 V power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. It is recommended to have an additional 1 μF to 10 μF capacitor and 0.1 μF bypass capacitor. In some situations, additional bypassing may be required, such as a 100 μF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5 V supply, removing the high-frequency noise. In general it is always a good idea to maintain the digital signals away from analog signals.

11.2 Layout Example

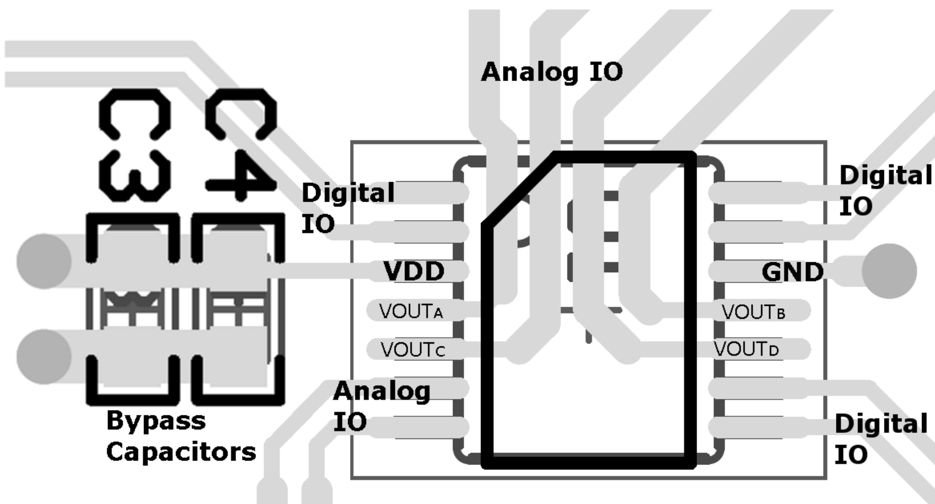


Figure 60. Layout Diagram

12 器件和文档支持

12.1 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **9.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
DAC60004	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DAC70004	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DAC80004	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
SPI, QSPI are trademarks of Motorola.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

DAC80004IPW 器件标识附录：注意，DA80004 和 XDC84 均为 DAC80004IPW 可订购器件的有效器件标识

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC60004IDMDR	Active	Production	VSON (DMD) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA60004
DAC60004IDMDR.B	Active	Production	VSON (DMD) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA60004
DAC60004IDMDT	Active	Production	VSON (DMD) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA60004
DAC60004IDMDT.B	Active	Production	VSON (DMD) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA60004
DAC60004IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA60004
DAC60004IPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA60004
DAC60004IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA60004
DAC60004IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA60004
DAC70004IDMDR	Active	Production	VSON (DMD) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA70004
DAC70004IDMDR.B	Active	Production	VSON (DMD) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA70004
DAC70004IDMDT	Active	Production	VSON (DMD) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA70004
DAC70004IDMDT.B	Active	Production	VSON (DMD) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA70004
DAC70004IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA70004
DAC70004IPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA70004
DAC70004IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA70004
DAC70004IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA70004
DAC80004IDMDR	Active	Production	VSON (DMD) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IDMDR.B	Active	Production	VSON (DMD) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IDMDT	Active	Production	VSON (DMD) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IDMDT.B	Active	Production	VSON (DMD) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IDMDTG4	Active	Production	VSON (DMD) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IDMDTG4.B	Active	Production	VSON (DMD) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004
DAC80004IPWRG4.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA80004

[(1)] **Status:** For more details on status, see our product life cycle.

[(2)] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[(3)] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[(4)] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[(5)] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[(6)] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

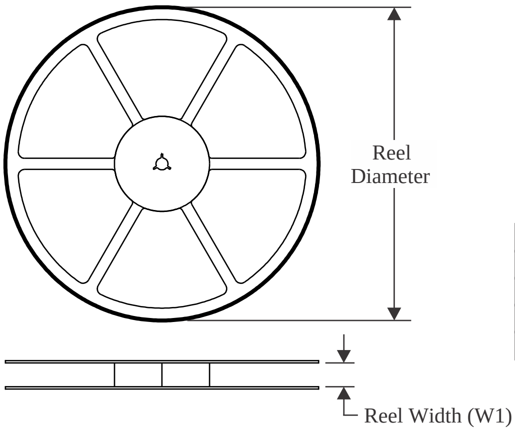
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

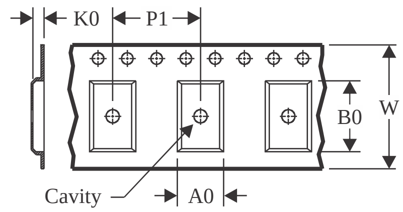
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

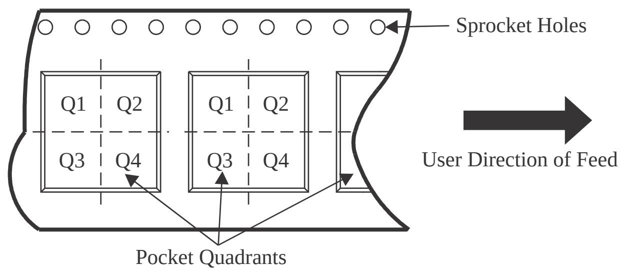


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

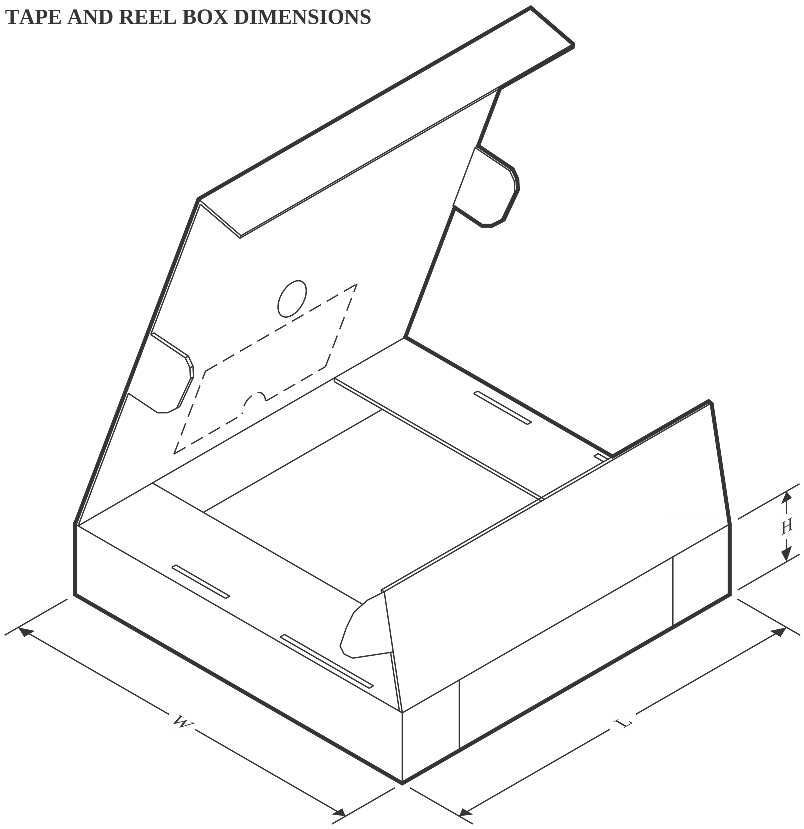
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC60004IDMDR	VSON	DMD	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
DAC60004IDMDT	VSON	DMD	14	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
DAC60004IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC70004IDMDR	VSON	DMD	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
DAC70004IDMDT	VSON	DMD	14	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
DAC70004IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC80004IDMDR	VSON	DMD	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
DAC80004IDMDT	VSON	DMD	14	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
DAC80004IDMDTG4	VSON	DMD	14	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
DAC80004IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC80004IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

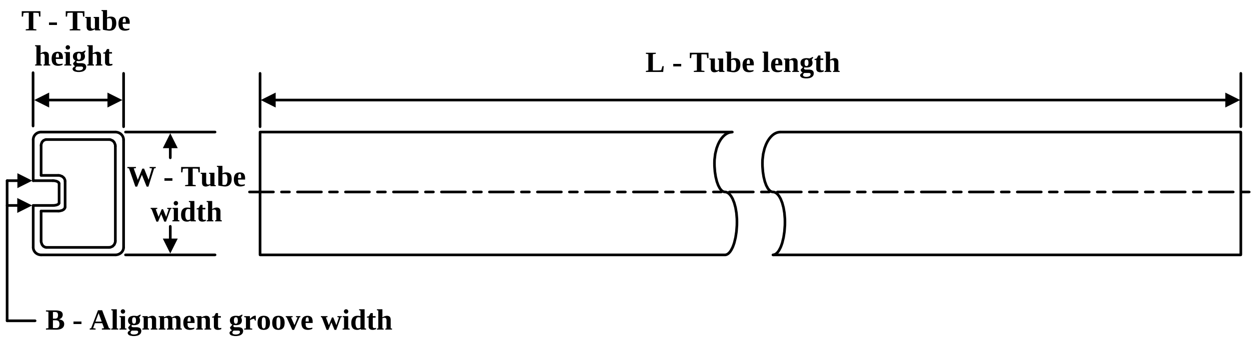
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

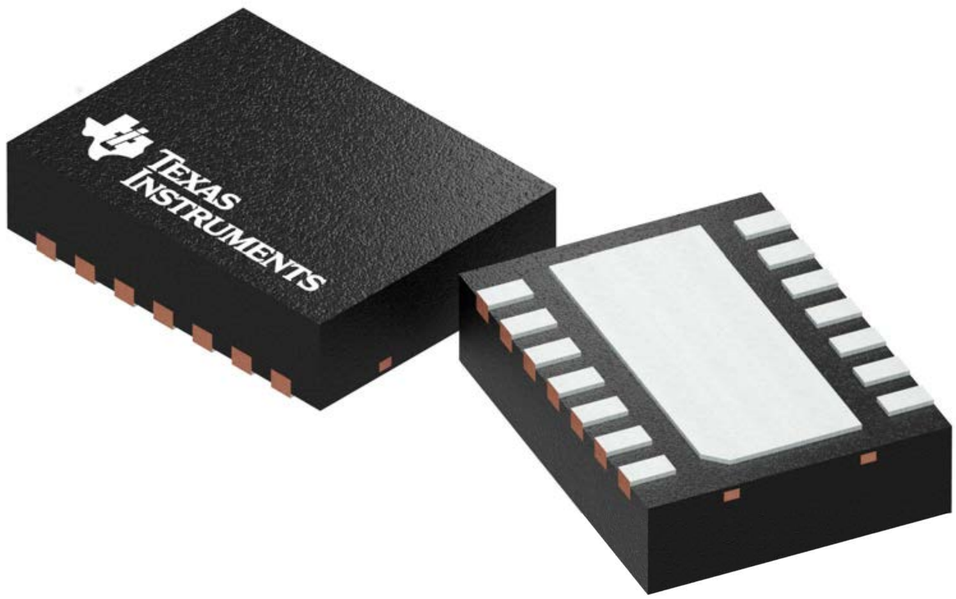
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC60004IDMDR	VSON	DMD	14	3000	367.0	367.0	38.0
DAC60004IDMDT	VSON	DMD	14	250	213.0	191.0	35.0
DAC60004IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
DAC70004IDMDR	VSON	DMD	14	3000	367.0	367.0	38.0
DAC70004IDMDT	VSON	DMD	14	250	213.0	191.0	35.0
DAC70004IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
DAC80004IDMDR	VSON	DMD	14	3000	367.0	367.0	38.0
DAC80004IDMDT	VSON	DMD	14	250	213.0	191.0	35.0
DAC80004IDMDTG4	VSON	DMD	14	250	213.0	191.0	35.0
DAC80004IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
DAC80004IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE

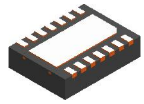


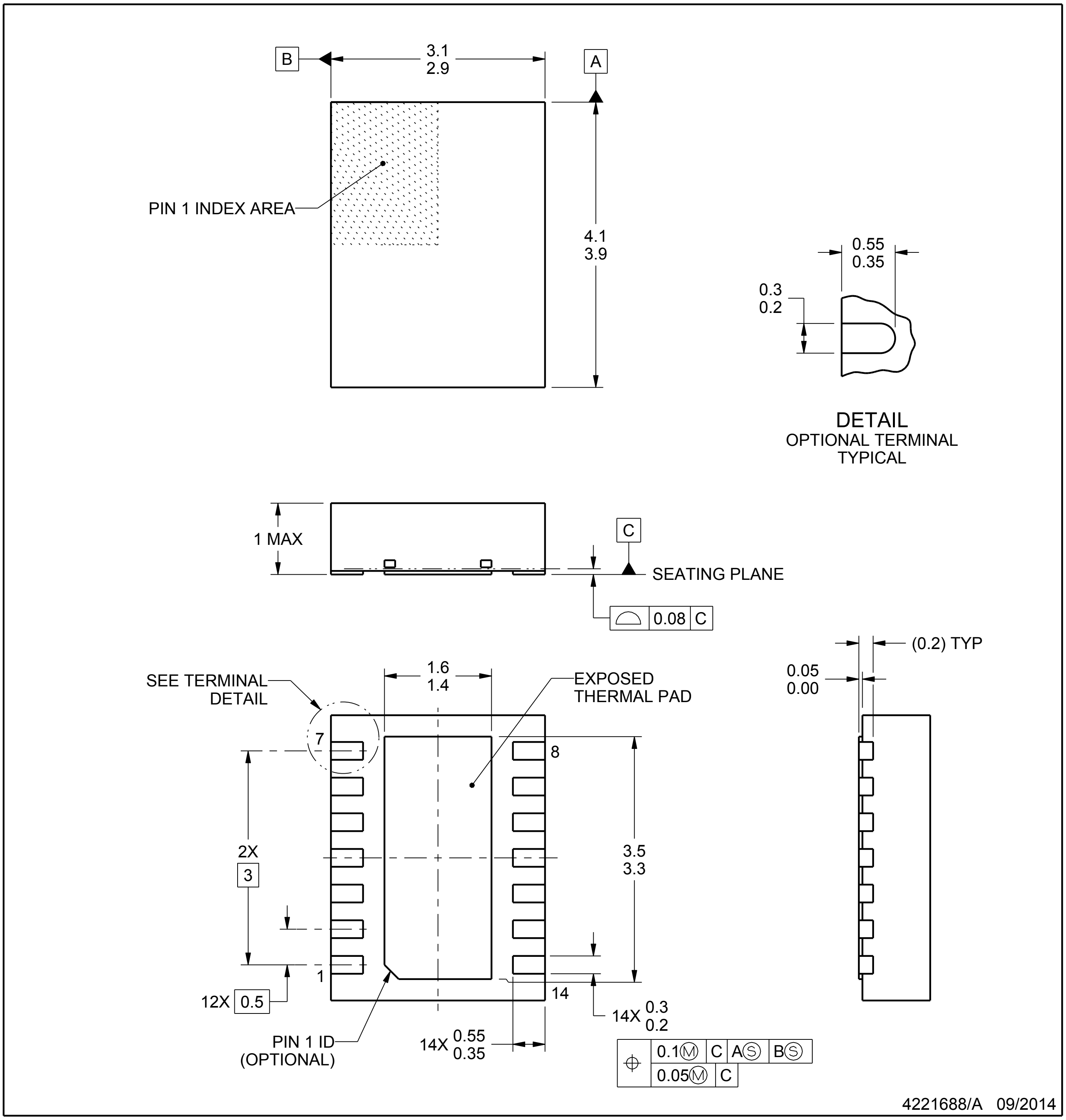
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC60004IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
DAC60004IPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
DAC70004IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
DAC70004IPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
DAC80004IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
DAC80004IPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5



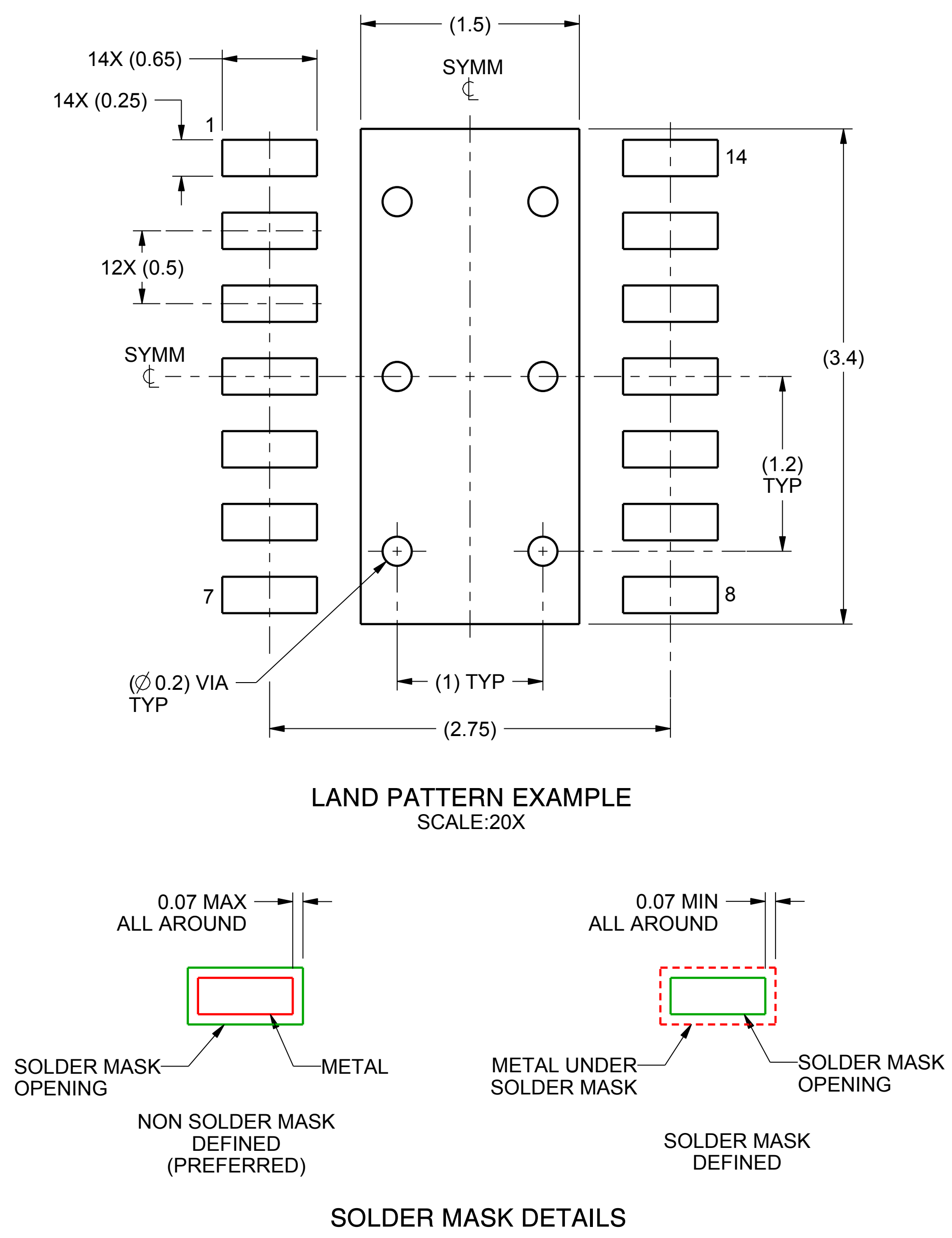
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





NOTES:

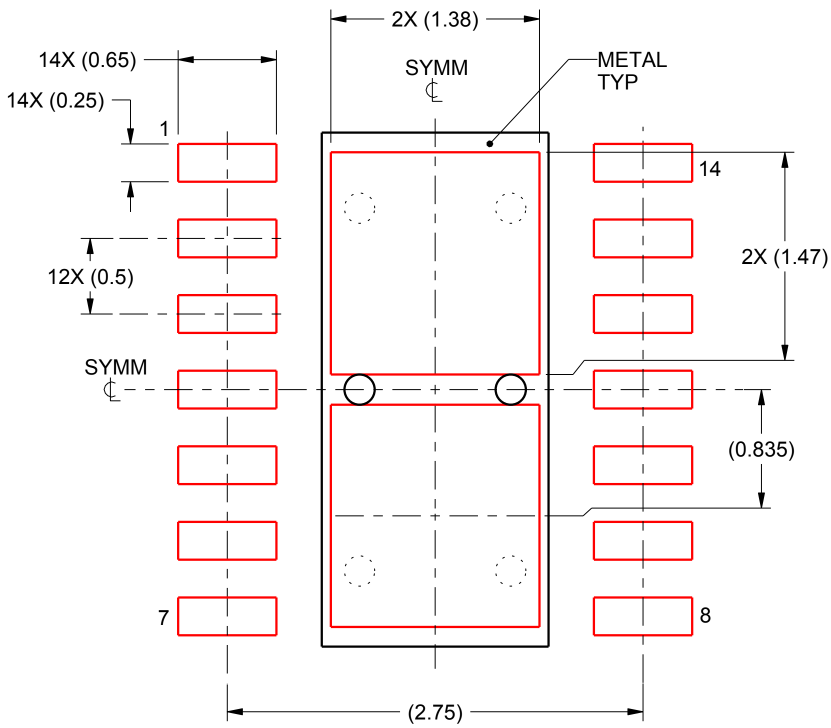
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



4221688/A 09/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



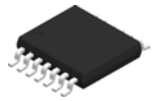
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4221688/A 09/2014

NOTES: (continued)

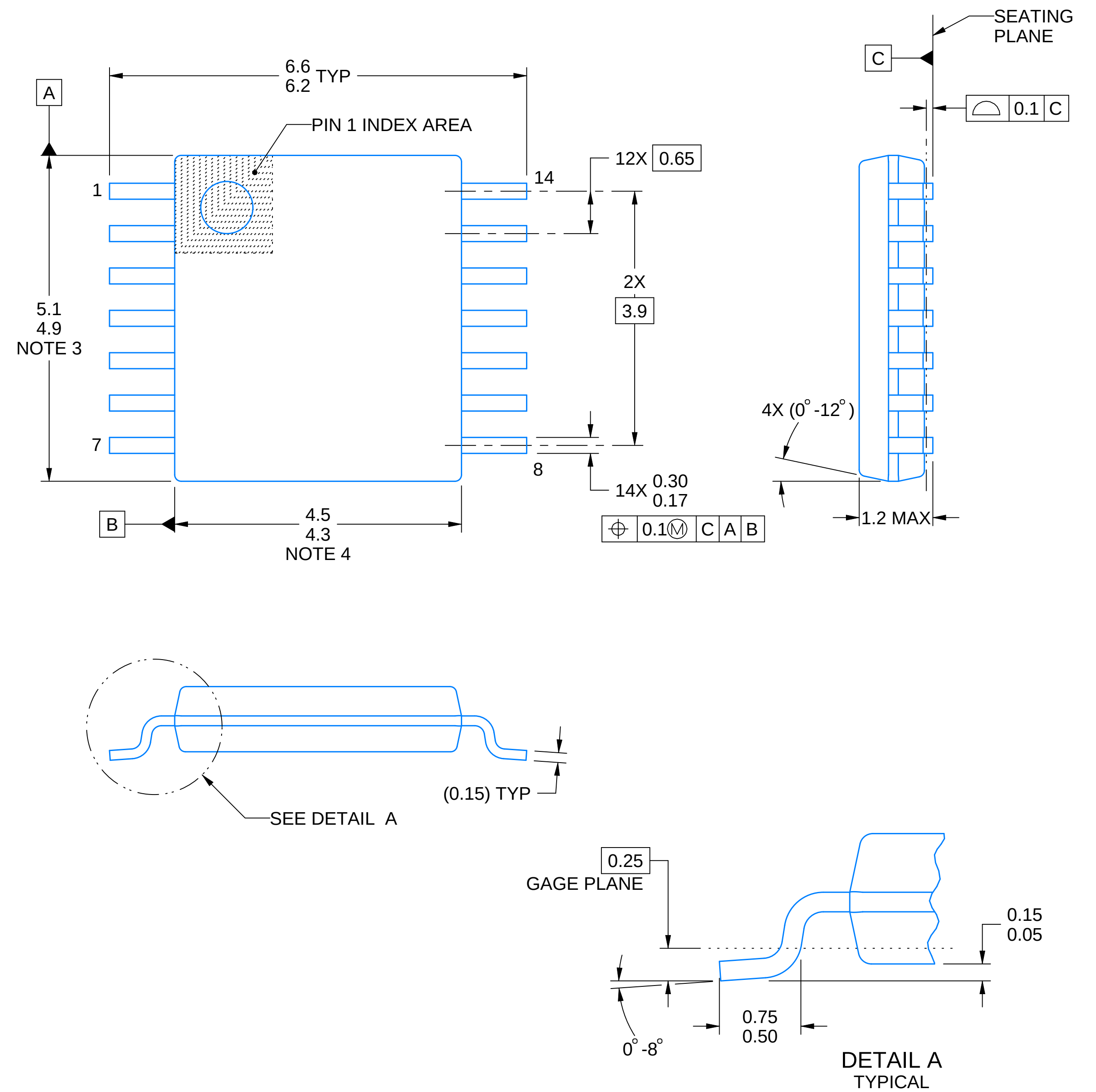
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

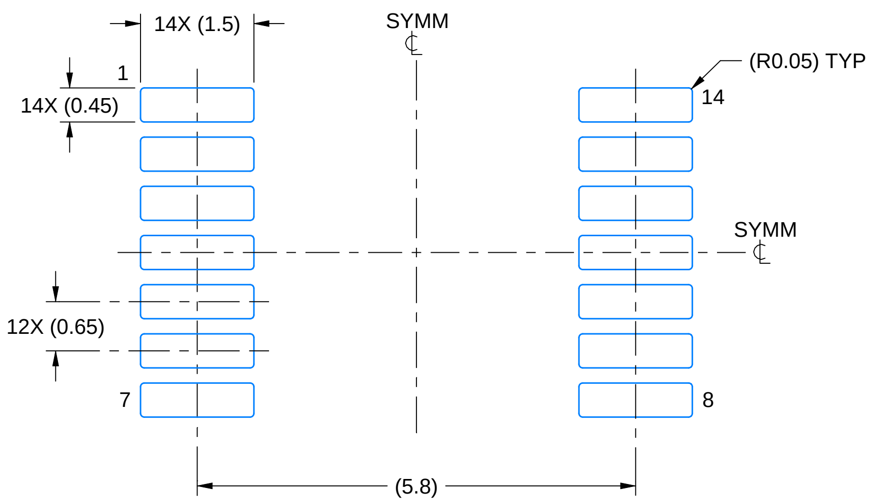
SMALL OUTLINE PACKAGE



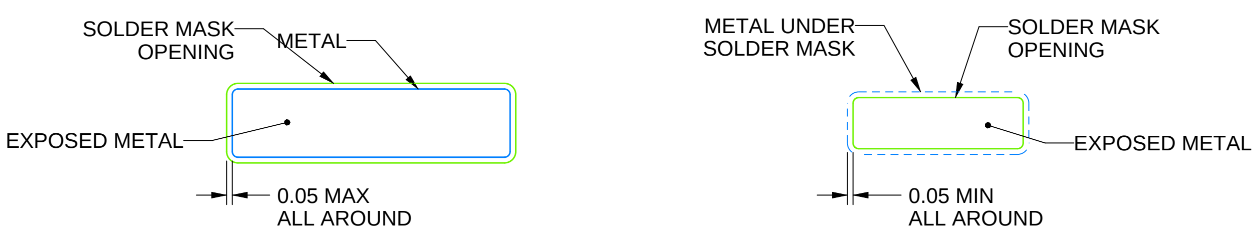
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

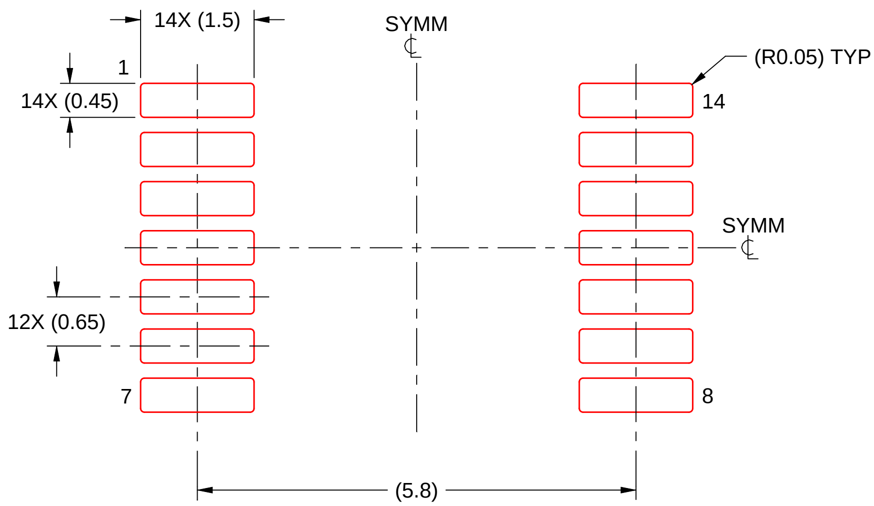


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265