

DAC7811 12 位串行输入乘法数模转换器

1 特性

- 2.7V 至 5.5V 电源供电
- 50MHz 串口
- 10MHz 的乘法带宽
- $\pm 15V$ 基准输入
- 低毛刺脉冲能量: 5 nV-s
- 工作温度范围:
-40°C 至 +125°C
- 10 引脚超薄小外形尺寸 (VSSOP) 封装
- 12 位单调性
- 四象限乘法
- 上电复位 (具有欠压保护功能)
- 菊链模式
- 读回功能
- 工业标准引脚配置

2 应用

- 便携式电池供电仪表
- 波形发生器
- 模拟处理
- 可编程放大器和衰减器
- 数控校准
- 可编程滤波器和振荡器
- 复合视频
- 超声波

3 说明

DAC7811 是一款 CMOS 12 位电流输出数模转换器 (DAC)。该器件由 2.7V 至 5.5V 电源供电, 这使得该器件非常适合电池供电的应用和许多其他应用。

该 DAC 使用与 SPI、QSPI™、MICROWIRE 和大多数 DSP 接口标准相兼容的双缓冲 3 线串行接口。此外, 在使用多个器件时, 可以通过串行数据输出引脚 (SDO) 实现菊链。利用数据读回功能, 用户可以通过 SDO 引脚读取 DAC 寄存器的内容。一旦加电, 内部移位寄存器和锁存器中就会填充零, 并且 DAC 输出将处于零标度。

DAC7811 可提供出色的四象限乘法特性以及 10MHz 的大信号乘法带宽。施加的外部基准输入电压 (V_{REF}) 确定满标量程输出电流。与外部电流到电压精密放大器结合使用时, 集成式反馈电阻器 (R_{FB}) 可提供温度跟踪和满标量程电压输出。

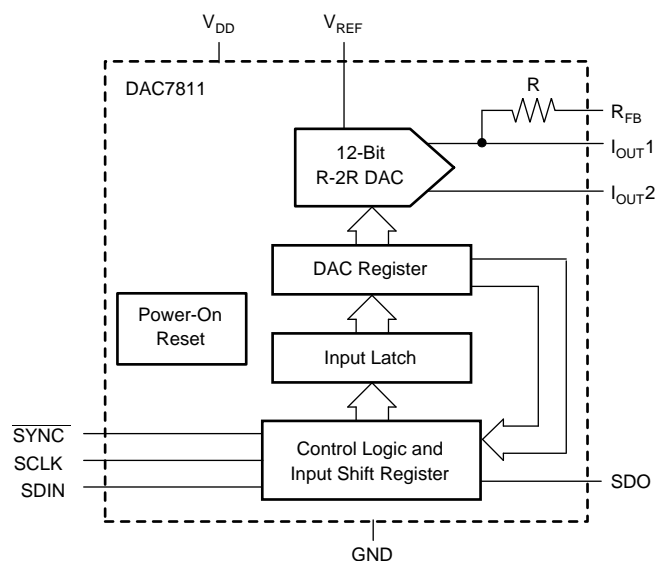
DAC7811 采用 10 引线 VSSOP 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
DAC7811	VSSOP (10)	3.00mm x 3.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的封装选项附录。

框图



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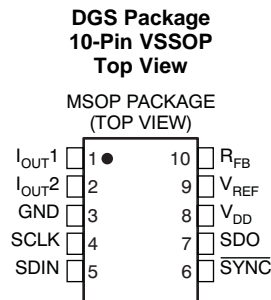
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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (March 2016) to Revision E		Page
•	Changed Figure 28 SDO pin timing to remove Hi-Z	14
Changes from Revision C (July 2007) to Revision D		Page
•	已添加 ESD 额定值 表、特性 说明 部分，器件功能模式，应用和实施 部分，电源建议 部分，布局 部分，器件和文档支持 部分以及机械、封装和可订购信息 部分	1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	I _{OUT1}	O	DAC Current Output
2	I _{OUT2}	O	DAC Analog Ground. This pin is normally tied to the analog ground of the system.
3	GND	G	Ground pin.
4	SCLK	I	Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device may be configured such that data is clocked into the shift register on the rising edge of SCLK.
5	SDIN	I	Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, on power-up, data is clocked into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to the rising edge.
6	$\overline{\text{SYNC}}$	I	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers, and the input shift register is enabled. Data is loaded to the shift register on the active edge of the following clocks (power-on default is falling clock edge). In stand-alone mode, the serial interface counts the clocks and data is latched to the shift register on the 16th active clock edge.
7	SDO	O	Serial Data Output. This allows a number of parts to be daisy-chained. By default, data is clocked into the shift register on the falling edge and out via SDO on the rising edge of SCLK. Data will always be clocked out on the alternate edge to loading data to the shift register. Writing the Readback control word to the shift register makes the DAC register contents available for readback on the SDO pin, clocked out on the opposite edges to the active clock edge.
8	V _{DD}	I	Positive Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
9	V _{REF}	I	DAC Reference Voltage Input
10	R _{FB}	O	DAC Feedback Resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
V_{DD} to GND	−0.3	7	V
Digital input voltage to GND	−0.3	$V_{DD} + 0.3$	V
I_{OUT1} , I_{OUT2} to GND	−0.3	$V_{DD} + 0.3$	V
Operating temperature	−40	125	°C
Junction temperature, (T_J max)		150	°C
Storage temperature, T_{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage to GND	2.7		5.5	V
V_{REF}	Reference voltage	−15		15	V
V_{IL}	Input low voltage	$V_{DD} = 2.7\text{ V}$		0.6	V
		$V_{DD} = 5\text{ V}$		0.8	V
V_{IH}	Input high voltage	$V_{DD} = 2.7\text{ V}$		2.1	V
		$V_{DD} = 5\text{ V}$		2.4	V
T_A	Operating ambient temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DAC7811	UNIT
		DGS (VSSOP)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	84.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

$V_{DD} = 2.7\text{ V}$ to 5.5 V ; $I_{OUT1} = \text{Virtual GND}$; $I_{OUT2} = 0\text{ V}$; $V_{REF} = 10\text{ V}$; $T_A = \text{full operating temperature}$. All specifications -40°C to 125°C , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE					
Resolution		12			Bits
Relative accuracy				± 1	LSB
Differential nonlinearity				± 1	LSB
Output leakage current	Data = 0000h, $T_A = 25^\circ\text{C}$			± 5	nA
Output leakage current	Data = 0000h, $T_A = T_{MAX}$			± 25	nA
Full-scale gain error	All ones loaded to DAC register		± 5	± 10	mV
Full-scale tempco ⁽¹⁾			± 5		ppm/ $^\circ\text{C}$
Output capacitance ⁽¹⁾	Code dependent		5		pF
REFERENCE INPUT					
Input resistance		8	10	12	k Ω
R_{FB} resistance		8	10	12	k Ω
LOGIC INPUTS AND OUTPUT⁽¹⁾					
I_{IL} Input leakage current				10	μA
C_{IL} Input capacitance				10	pF
INTERFACE TIMING (see Figure 28)					
f_{CLK}				50	MHz
t_C Clock period		20			ns
t_{CH} Clock pulse width high		8			ns
t_{CL} Clock pulse width low		8			ns
t_{CSS} $\overline{\text{SYNC}}$ falling edge to SCLK active edge setup time		13			ns
t_{CST} SCLK active edge to $\overline{\text{SYNC}}$ rising edge hold time		5			ns
t_{DS} Data setup time		5			ns
t_{DH} Data hold time		3			ns
t_{SH} $\overline{\text{SYNC}}$ high time		30			ns
t_{DDS} $\overline{\text{SYNC}}$ inactive edge to SDO valid	$V_{DD} = 2.7\text{ V}$		25	35	ns
	$V_{DD} = 5\text{ V}$		20	30	ns
POWER REQUIREMENTS					
I_{DD} (normal operation)	Logic inputs = 0 V			5	μA
$V_{DD} = 4.5\text{ V}$ to 5.5 V	$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$		0.8	5	μA
$V_{DD} = 2.7\text{ V}$ to 3.6 V	$V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$		0.4	2.5	μA
AC CHARACTERISTICS⁽¹⁾					
Output voltage settling time				0.2	μs
Reference multiplying BW	$V_{REF} = 7\text{ V}_{PP}$, Data = FFFh		10		MHz
DAC glitch impulse	$V_{REF} = 0\text{ V}$ to 10 V , Data = 7FFh to 800h to 7FFh		5		nV-s
Feedthrough error V_{OUT}/V_{REF}	Data = 000h, $V_{REF} = 100\text{ kHz}$		-60		dB
Digital feedthrough			2		nV-s
Total harmonic distortion			-105		dB
Output spot noise voltage			18		nV/ $\sqrt{\text{Hz}}$

(1) Specified by design and characterization; not production tested.

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6.6 Typical Characteristics: $V_{DD} = 5\text{ V}$

At $T_A = 25^\circ\text{C}$, unless otherwise noted.

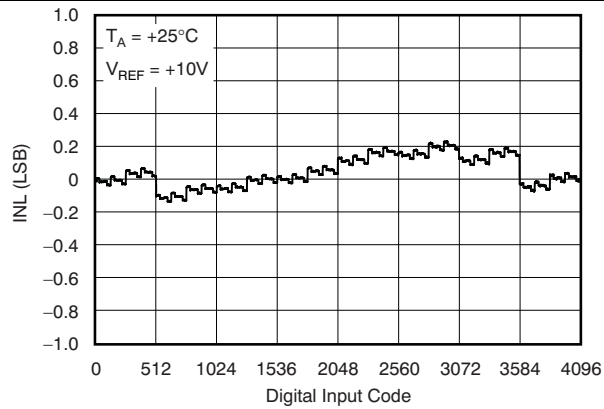


Figure 1. Linearity Error vs Digital Input Code

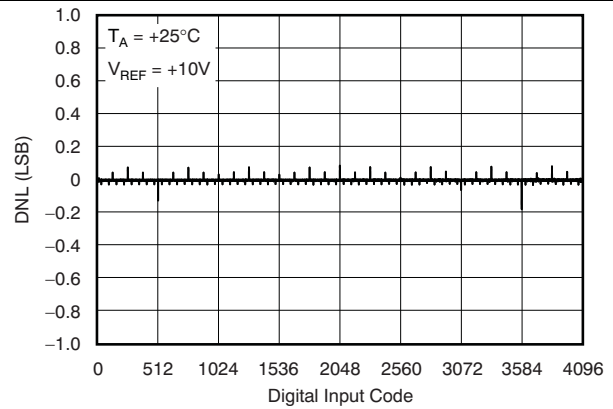


Figure 2. Differential Linearity Error vs Digital Input Code

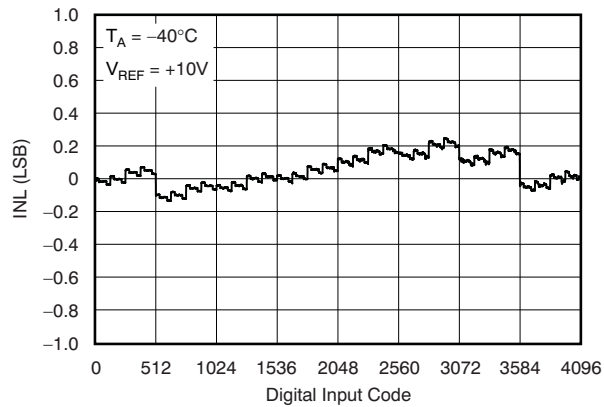


Figure 3. Linearity Error vs Digital Input Code

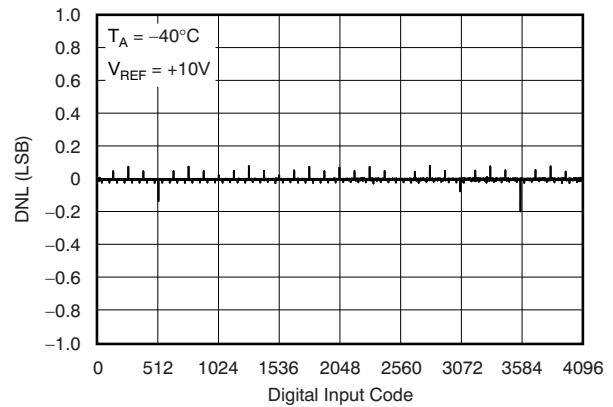


Figure 4. Differential Linearity Error vs Digital Input Code

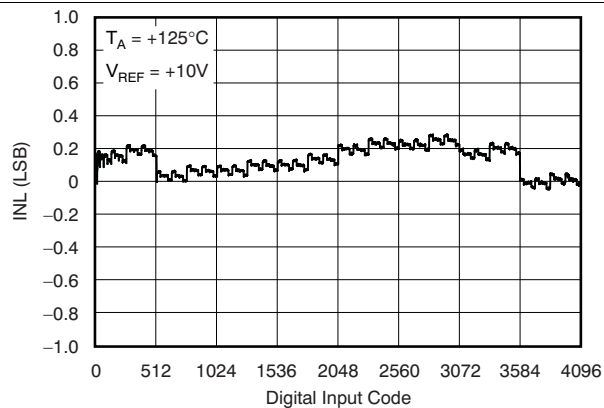


Figure 5. Linearity Error vs Digital Input Code

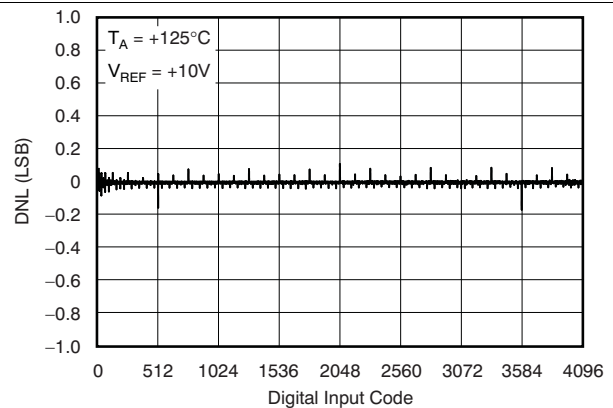


Figure 6. Differential Linearity Error vs Digital Input Code

Typical Characteristics: $V_{DD} = 5\text{ V}$ (continued)

At $T_A = 25^\circ\text{C}$, unless otherwise noted.

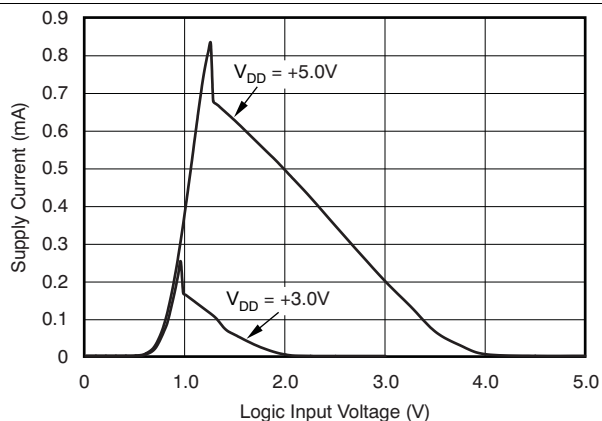


Figure 7. Supply Current vs Logic Input Voltage

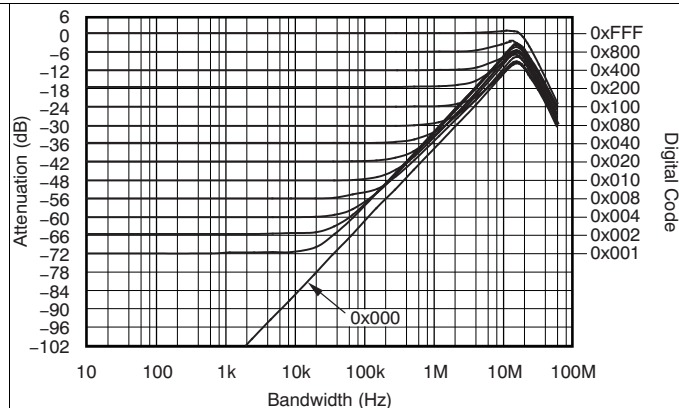


Figure 8. Reference Multiplying Bandwidth

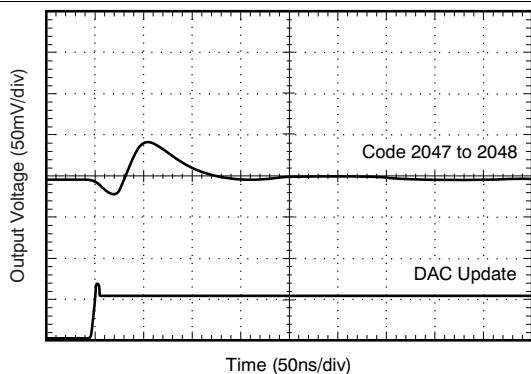


Figure 9. Midscale DAC Glitch

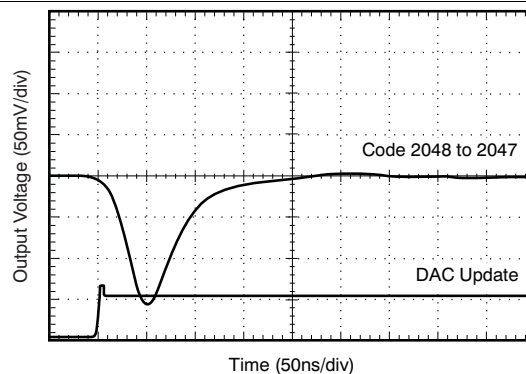


Figure 10. Midscale DAC Glitch

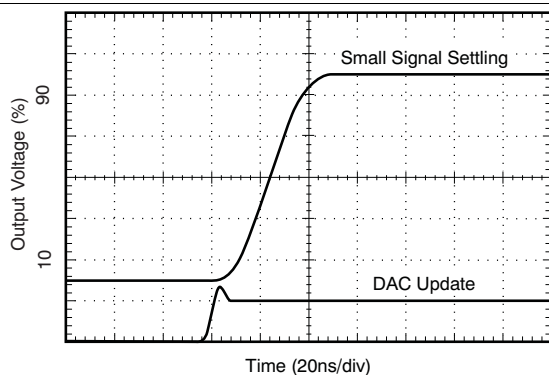


Figure 11. DAC Settling Time

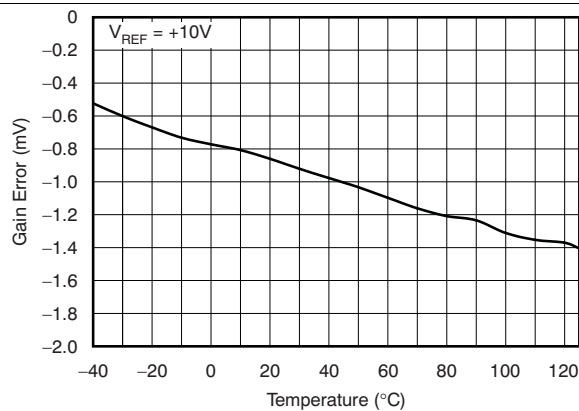
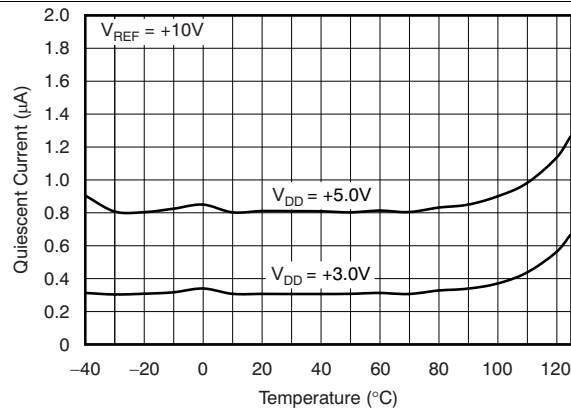
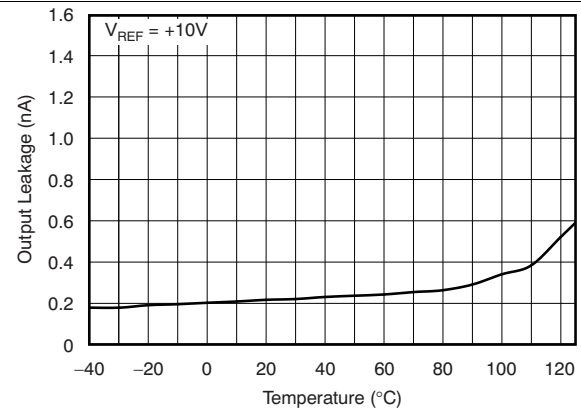


Figure 12. Gain Error vs Temperature

Typical Characteristics: $V_{DD} = 5\text{ V}$ (continued)

 At $T_A = 25^\circ\text{C}$, unless otherwise noted.

Figure 13. Supply Current vs Temperature

Figure 14. Output Leakage vs Temperature

6.7 Typical Characteristics: $V_{DD} = 2.7\text{ V}$

At $T_A = 25^\circ\text{C}$, unless otherwise noted.

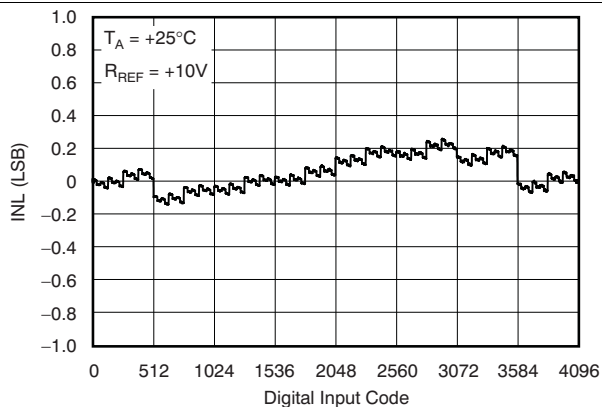


Figure 15. Linearity Error vs Digital Input Code

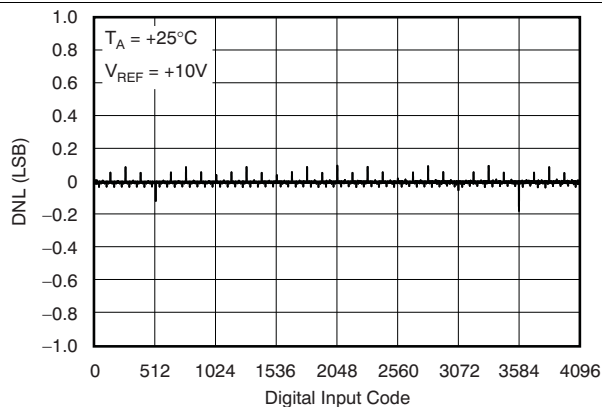


Figure 16. Differential Linearity Error vs Digital Input Code

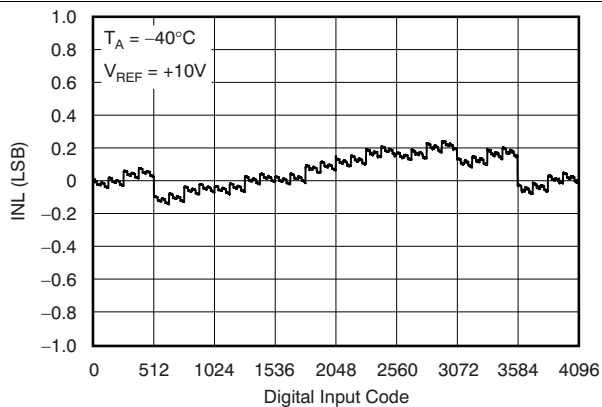


Figure 17. Linearity Error vs Digital Input Code

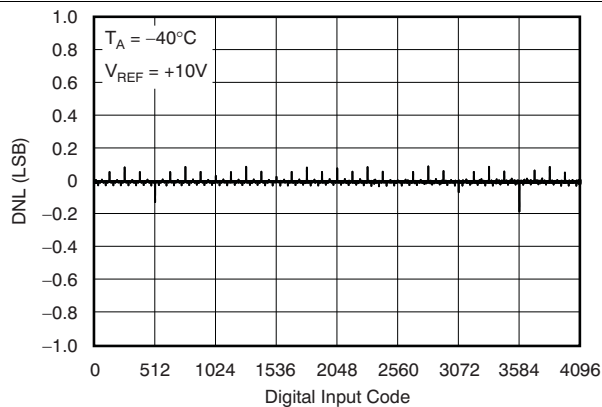


Figure 18. Differential Linearity Error vs Digital Input Code

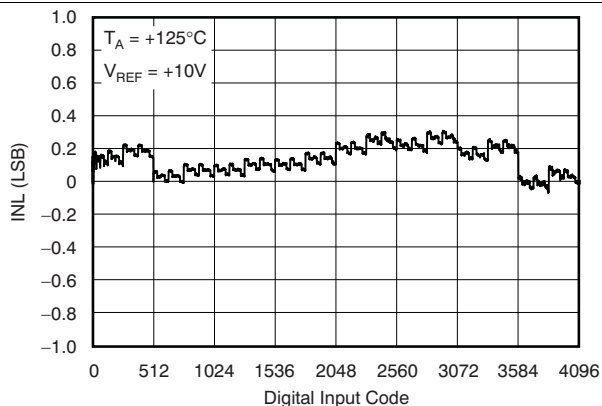


Figure 19. Linearity Error vs Digital Input Code

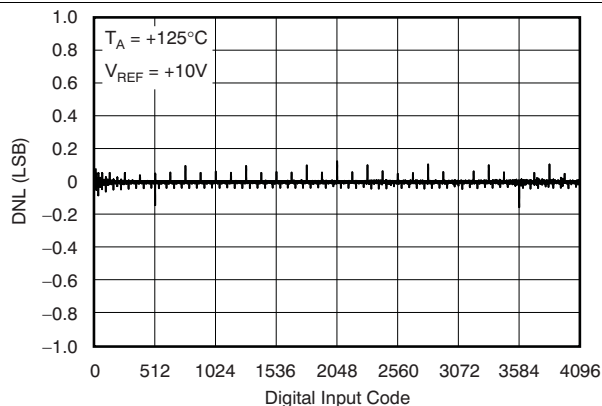


Figure 20. Differential Linearity Error vs Digital Input Code

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Typical Characteristics: $V_{DD} = 2.7\text{ V}$ (continued)

At $T_A = 25^\circ\text{C}$, unless otherwise noted.

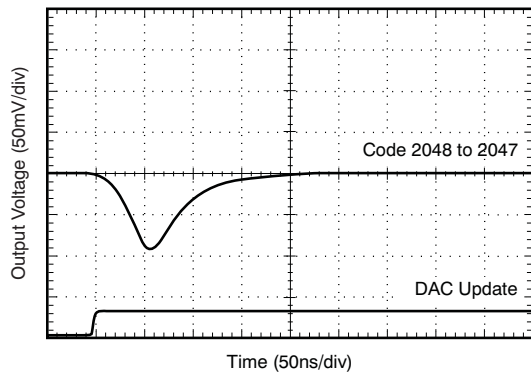


Figure 21. Midscale DAC Glitch

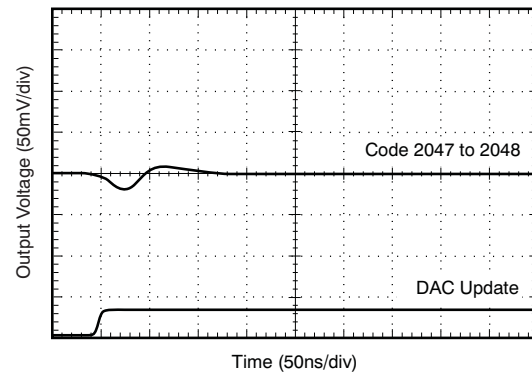


Figure 22. Midscale DAC Glitch

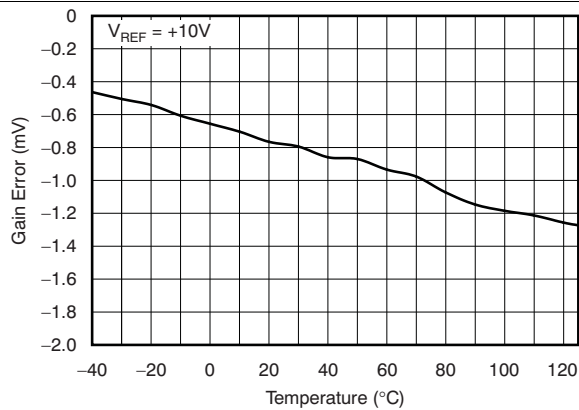


Figure 23. Gain Error vs Temperature

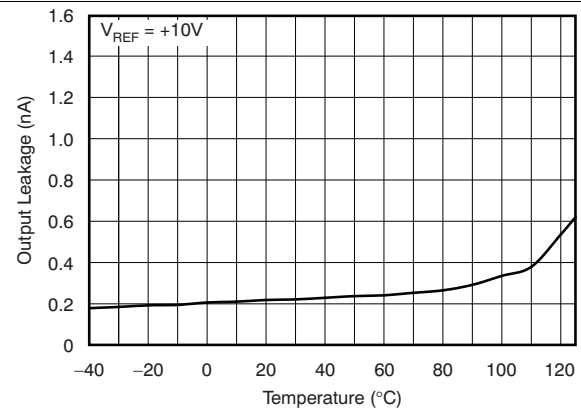


Figure 24. Output Leakage vs Temperature

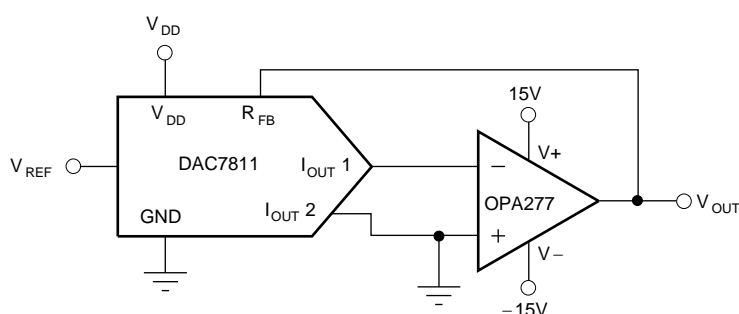
Feature Description (continued)

When using an external I/V converter and the DAC7811 R_{FB} resistor, the DAC output voltage is given by [Equation 1](#):

$$V_{OUT} = -V_{REF} \times \left(\frac{CODE}{4096} \right) \quad (1)$$

Each DAC code determines the 2R leg switch position to either GND or I_{OUT} . Because the DAC output impedance as seen looking into the I_{OUT1} terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT1} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC7811 due to offset modulation versus DAC code.

For best linearity performance of the DAC7811, a low offset voltage op amp (such as the [OPA277](#)) is recommended (see [Figure 26](#)). This circuit allows V_{REF} swinging from -10 V to 10 V .



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Figure 26. Voltage Output Configuration

7.4 Device Functional Modes

7.4.1 Serial Interface

The DAC7811 has a 3-wire serial interface (\overline{SYNC} , SCLK, and SDIN), which is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most Digital Signal Processor (DSP) devices. See the Serial Write Operation timing diagram ([Figure 28](#)) for an example of a typical write sequence. The write sequence begins by bringing the \overline{SYNC} line low. Data from the DIN line are clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DAC7811 compatible with high-speed DSPs. The SDIN and SCLK input buffers are gated off while \overline{SYNC} is high which minimizes the power dissipation of the digital interface. After \overline{SYNC} goes low, the digital interface will respond to the SDIN and SCLK input signals and data can now be shifted into the device. If an inactive clock edge occurs after \overline{SYNC} goes low, but before the first active clock edge, it will be ignored. If the SDO pin is being used then \overline{SYNC} must remain low until after the inactive clock edge that follows the 16th active clock edge.

7.4.2 Input Shift Register

The input shift register is 16 bits wide, as shown in [Figure 27](#). The four MSBs are the control bits C3–C0; these bits determine which function will be executed at the rising edge of \overline{SYNC} in daisy-chain mode or the 16th active clock edge in stand-alone mode. The remaining 12 bits are the data bits. On a load and update command (C3–C0 = 0001) these 12 data bits will be transferred to the DAC register; otherwise, they have no effect. [Table 1](#) shows serial shift register and DAC register operation with CLK and \overline{SYNC} pin settings.

Device Functional Modes (continued)

4 CONTROL BITS				12 DATA BITS											
B15 (MSB)	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
C3	C2	C1	C0	DB11											DB0

Figure 27. Contents of the 16-Bit Input Shift Register

Table 1. Control Logic Truth Table⁽¹⁾

CLK	$\overline{\text{SYNC}}$	SERIAL SHIFT REGISTER	DAC REGISTER
X	H	No effect	Latched
↓−	L	Shift register data advanced one bit	Latched
X	↑+	In daisy-chain mode, the function as determined by C3-C0 is executed.	In daisy-chain mode, the contents may change as determined by C3-C0.

(1) ↓− Negative logic transition, default CLK mode; ↑+ Positive logic transition; X = Do not care.

7.4.3 $\overline{\text{SYNC}}$ Interrupt (Stand-Alone Mode)

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs.

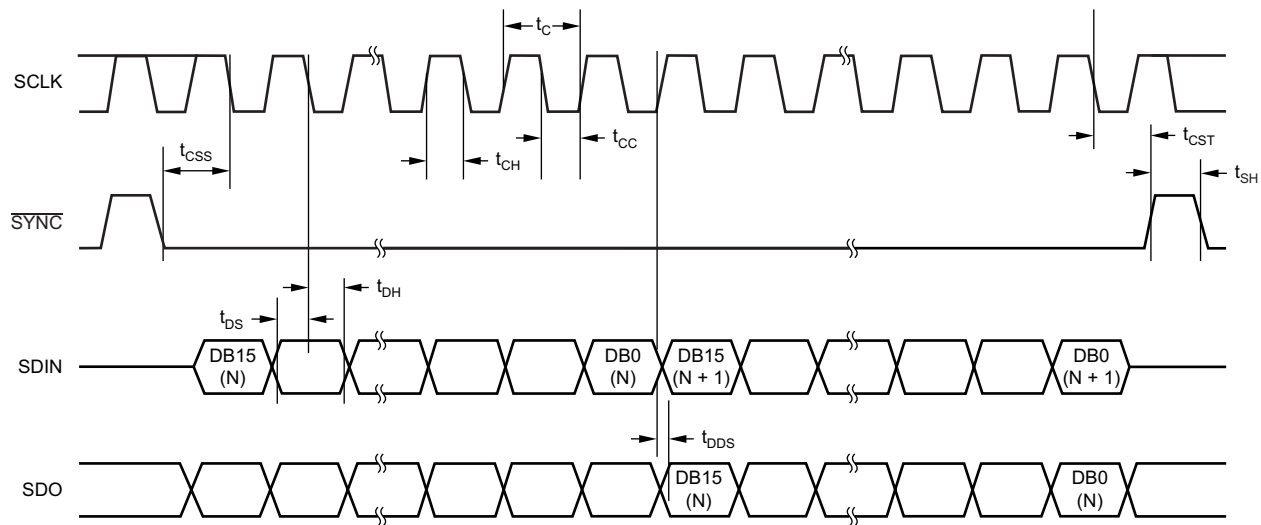
7.4.4 Daisy-Chain

The DAC7811 powers up in the daisy-chain mode which must be used when two or more devices are connected in tandem. The SCLK and $\overline{\text{SYNC}}$ signals are shared across all devices while the SDO output of the first device connects to the SDIN input of the following device, and so forth. In this configuration 16 SCLK cycles for each DAC7811 in the chain are required. Please refer to the timing diagram of [Figure 28](#).

For n devices in a daisy-chain configuration, $16n$ SCLK cycles are required to shift in the entire input data stream. After $16n$ active SCLK edges are received following a falling $\overline{\text{SYNC}}$, the data stream becomes complete, and $\overline{\text{SYNC}}$ can be brought high to update n devices simultaneously.

When $\overline{\text{SYNC}}$ is brought high, each device will execute the function defined by the four DAC control bits C3-C0 in its input shift register. For example, C3-C0 must be **0001** for each DAC in the chain that is to be updated with new data, and C3-C0 must be **0000** for each DAC in the chain whose contents are to remain unchanged.

A continuous stream containing the exact number of SCLK cycles may be sent first while the $\overline{\text{SYNC}}$ signal is held low, and then raise $\overline{\text{SYNC}}$ at a later time. Nothing happens until the rising edge of $\overline{\text{SYNC}}$, and then each DAC7811 in the chain will execute the function defined by the four DAC control bits C3-C0 in its input shift register.


Figure 28. DAC7811 Timing Diagram

7.4.5 Control Bits C3 to C0

Control Bits C3 to C0 allow control of various functions of the DAC; see [Table 2](#). Default settings of the DAC on powering up are as follows: Data clocked into shift register on falling clock edges; daisy-chain mode is enabled. The device powers on with zero-scale loaded into the DAC register and I_{OUT} lines. The DAC control bits allow the user to adjust certain features as part of an initialization sequence; for example, daisy-chaining may be disabled if not in use, active clock edge may be changed to rising edge, and DAC output may be cleared to either zero or midscale. The user may also initiate a readback of the DAC register contents for verification purposes.

Table 2. Serial Input Register Data Format, Data Loaded MSB First

C3	C2	C1	C0	FUNCTION IMPLEMENTED
0	0	0	0	No operation (power-on default)
0	0	0	1	Load and update
0	0	1	0	Initiate readback
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Daisy-chain disable
1	0	1	0	Clock data to shift register on rising edge
1	0	1	1	Clear DAC output to zero
1	1	0	0	Clear DAC output to midscale
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

8 Application and Implementation

NOTE

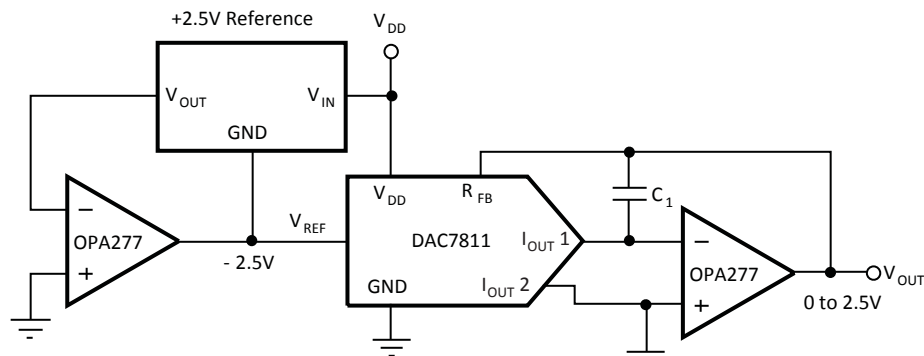
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The 2.7-V to 5.5-V supply operation makes the DAC7811 a viable candidate for battery operated applications, such as waveform generators, programmable amplifiers, and any mobile platforms that may require analog outputs and processing. Additionally, the large signal multiplying bandwidth of the DAC7811 makes it an excellent choice for programmable filters and oscillators.

8.1.1 Unipolar Operation Using DAC7811

To generate a positive voltage output, a negative reference is input to the DAC7811. This design is suggested instead of using an inverting amp to invert the output as a result of resistor tolerance errors. For a negative reference, V_{OUT} and GND of the reference are level-shifted to a virtual ground and a –2.5-V input to the DAC7811 with an op amp.



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Figure 29. Positive Voltage Output Circuit

8.1.2 Bipolar Operation Using the DAC7811

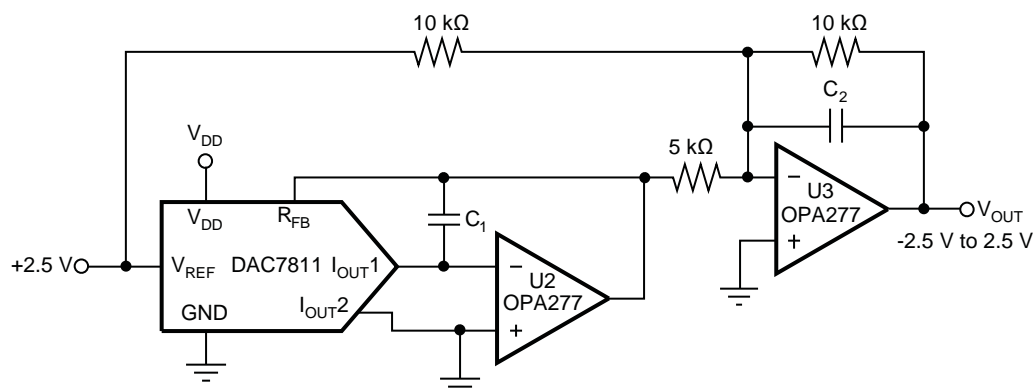
The DAC7811, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 30, external op amp U3 is added as a summing amp and has a gain of 2X that widens the output span to 5 V. A 4-quadrant multiplying circuit is implemented by using a 2.5-V offset of the reference voltage to bias U3. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full-scale produces output voltages of V_{OUT} = –2.5 V to V_{OUT} = +2.5 V

$$V_{OUT} = \left[\left(\frac{D}{2^{11}} \right) - 1 \right] \times V_{REF} \quad (2)$$

External resistance mismatching is the significant error in Figure 30.

Application Information (continued)

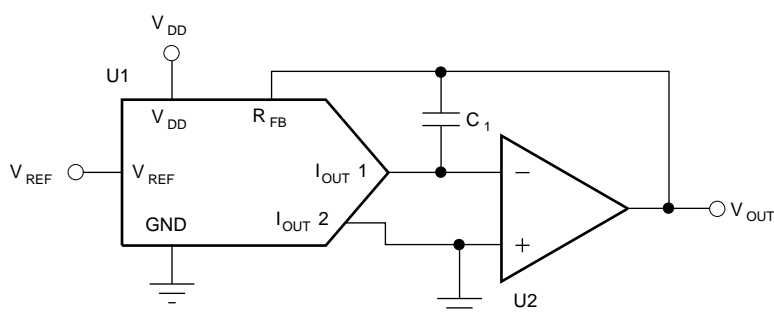


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Figure 30. Bipolar Output Circuit

8.1.3 Stability Circuit

For a current-to-voltage design (see [Figure 31](#)), the DAC7811 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct printed circuit board (PCB) layout design practices. For each code change, there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C_1 (1pF to 5pF typ) can be added to the design, as shown in [Figure 31](#).



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Figure 31. Gain Peaking Prevention Circuit With Compensation Capacitor

8.1.4 Amplifier Selection

There are many choices and many differences in selecting the proper operational amplifier for a multiplying DAC (MDAC). Making the analog signal out of the MDAC is one critical aspect. However, there are also other issues to take into account such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy. [Table 3](#) and [Table 4](#) suggest some suitable operational amplifiers for low power, fast settling, and high-speed applications. A greater selection of operational amplifiers can be found at www.ti.com/amplifier.

Application Information (continued)

Table 3. Suitable Precision Operational Amplifiers from Texas Instruments

PRODUCT	TOTAL SUPPLY VOLTAGE (V) (min)	TOTAL SUPPLY VOLTAGE (V) (max)	I _Q PER CHANNEL (max) (mA)	GBW (typ) (MHz)	SLEW RATE (typ) (V/μs)	OFFSET DRIFT (typ) (μV/°C)	I _B (max) (pA)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
LOW POWER										
OPA703	4	12	0.2	1	0.6	4	10	70	SOT5-23, PDIP-8, SOIC-8	12V, CMOS, Rail-to-Rail I/O, Operational Amplifier
OPA735	2.7	12	0.75	1.6	1.5	0.01	200	115	SOT5-23, SOIC-8	0.05μV/°C (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier
OPA344	2.7	5.5	0.25	1	1	2.5	10	80	SOT5-23, PDIP-8, SOIC-8	Low Power, Single-Supply, Rail-To-Rail Operational Amplifiers MicroAmplifier Series
OPA348	2.1	5.5	0.065	1	0.5	2	10	70	SC5-70, SOT5-23, SOIC-8	1MHz, 45μA, Rail-to-Rail I/O, Single Op Amp
OPA277	4	36	0.825	1	0.8	0.1	1000	130	PDIP-8, SOIC-8, SON-8	High Precision Operational Amplifiers
FAST SETTLING										
OPA350	2.7	5.5	7.5	38	22	4	10	76	MSOP-8, PDIP-8, SOIC-8	High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series
OPA727	4	12	6.5	20	30	0.6	500	86	MSOP-8, SON-8	e-trim 20MHz, High Precision CMOS Operational Amplifier
OPA227	5	36	3.8	8	2.3	0.1	10000	120	PDIP-8, SOIC-8	High Precision, Low Noise Operational Amplifiers

Table 4. Suitable High Speed Operational Amplifiers from Texas Instruments (Multiple Channel Options)

PRODUCT	SUPPLY VOLTAGE (V)	GBW PRODUCT (MHz)	VOLTAGE NOISE nV/√Hz	GBW (typ) (MHz)	SLEW RATE (V/μs)	V _{OS} (typ) (μV)	V _{OS} (max) (μV)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
SINGLE CHANNEL										
THS4281	±2.7 to ±15	38	12.5	35	500	3500	500	1000	SOT5-23, MSOP-8, SOIC-8	Very Low-Power High Speed Rail-To-Rail Input/Output Voltage Feedback Operational Amplifier
THS4031	±4.5 to ±16.5	200	1.6	100	500	3000	3000	8000	CDIP-8, MSOP-8, SOIC-8	100-MHz Low Noise Voltage-Feedback Amplifier
THS4631	±4.5 to ±16.5	210	7	900	260	2000	50pA	2	SOIC-8, MSOP-8	High Speed FET-Input Operational Amplifier
OPA656	±4 to ±6	230	7	290	250	2600	2pA	5pA	SOIC-8, SOT5-23	Wideband, Unity Gain Stable FET-Input Operational Amplifier
OPA820	±2.5 to ±6	280	2.5	240	200	1200	900	23,000	SOIC-8, SOT5-23	Unity Gain Stable, Low Noise, Voltage Feedback Operational Amplifier
DUAL CHANNEL										
THS4032	±4.5 to ±16.5	200	1.6	100	500	3000	3000	8000	SOIC-8, MSOP-8	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
OPA2822	±2 to ±6.3	220	2	170	200	1200	9600	12000	SOIC-8, MSOP-8	SpeedPlus Dual Wideband, Low-Noise Operational Amplifier

8.1.5 Programmable Current Source Circuit

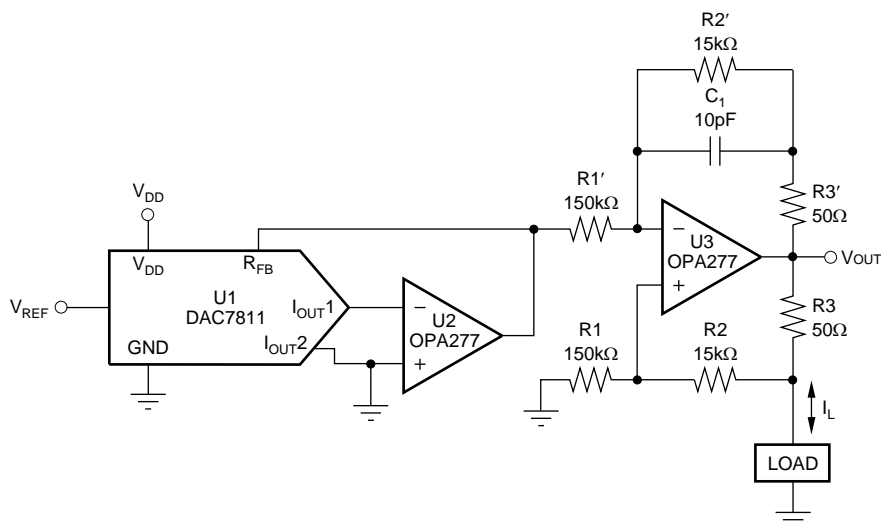
A DAC7811 can be integrated into the circuit in [Figure 32](#) to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by [Equation 3](#):

$$I_L = \frac{(R_2 + R_3)/R_1}{R_3} \times V_{REF} \times \frac{D}{4096} \quad (3)$$

The value of R_3 in [Equation 3](#) can be reduced to increase the output current drive of U_3 . U_3 can drive $\pm 20\text{mA}$ in both directions with voltage compliance limited up to 15V by the U_3 voltage supply. Elimination of the circuit compensation capacitor C_1 in the circuit is not suggested as a result of the change in the output impedance Z_O , according to [Equation 4](#):

$$Z_O = \frac{R_1' R_3 (R_1 + R_2)}{R_1 (R_2' + R_3') - R_1' (R_2 + R_3)} \quad (4)$$

As shown in [Equation 4](#), with matched resistors, Z_O is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C_1 into the circuit, possible oscillation problems are eliminated. The value of C_1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

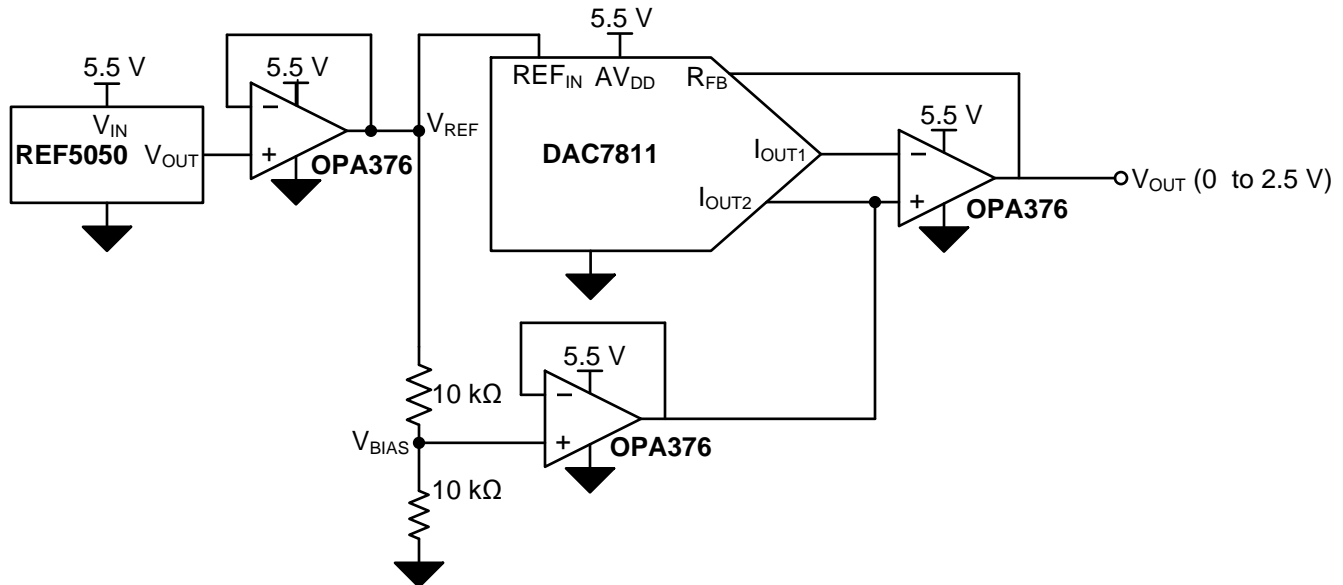


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Figure 32. Programmable Bidirectional Current Source Circuit

8.2 Typical Application

8.2.1 Single Supply Unipolar Multiplying DAC



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Figure 33. Complete Circuit Schematic

8.2.1.1 Design Requirements

This multiplying DAC (MDAC) circuit outputs unipolar voltages from 0 V to 2.5 V. This design does not require dual supplies to realize a unipolar, positive output voltage. This design removes the need for a negative supply rail by applying a bias voltage the output transimpedance stage.

8.2.1.2 Detailed Design Procedure

The DAC7811 output current is converted into a voltage by including an op-amp in a transimpedance configuration at the DAC7811 current output terminal. The transimpedance stage creates an output voltage with opposite polarity to that of V_{REF} and subsequently requires dual supplies. This circuit removes the need of dual power supplies and uses a single supply to power the circuit.

The transfer function from digital code to output voltage is shown in Equation 5.

$$V_{OUT}(Code) = V_{BIAS} - \frac{(V_{REF} - V_{BIAS})}{2^{bits}} \times Code \quad (5)$$

More information regarding this design can be found in [Single-Supply Unipolar Multiplying DAC Reference Design](#) (TIDU300).

8.2.1.3 Application Curve

The Absolute error (TUE) in %FSR is shown the following graph, Figure 34. The plot below represents data ranging from code 30 to 4050. The figure shows the absolute error (TUE) has a maximum value of about 0.05% FSR.

Typical Application (continued)

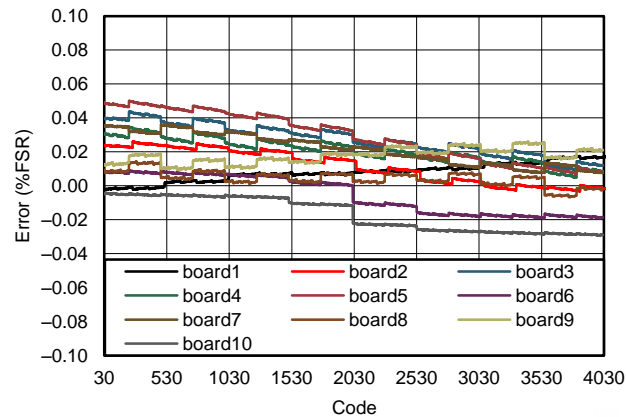


Figure 34. Absolute Error (TUE) in %FSR

9 Power Supply Recommendations

The DAC7811 can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to VDD should be well regulated and low noise. Switching power supplies and DC-DC converters often have high frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. To further minimize noise from the power supply, a strong recommendation is to include a 1- μ F to 10- μ F capacitor and 0.1- μ F bypass capacitor. The required supply current vs Logic Input voltage or temperature is displayed in [Typical Characteristics](#). The power supply must meet the aforementioned current requirements.

10 Layout

10.1 Layout Guidelines

A precision analog component requires careful layout, the list below provides some insight into good layout practices.

- All Power Supply pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 to 0.22- μ F ceramic with a X7R or NP0 dielectric.
- Power supplies and VREF bypass capacitors should be placed close to terminals or planes to minimize inductance and optimize performance.
- A high-quality ceramic type NP0 or X7R is recommended for its optimal performance across temperature, and very low dissipation factor.
- The digital and analog sections should have proper placement with respect to the digital pins and analog pins of the DAC7811 device. The separation of analog and digital blocks will allow for better design and practice as it will ensure less coupling into neighboring blocks, and will minimize the interaction between analog and digital return currents.

10.2 Layout Example

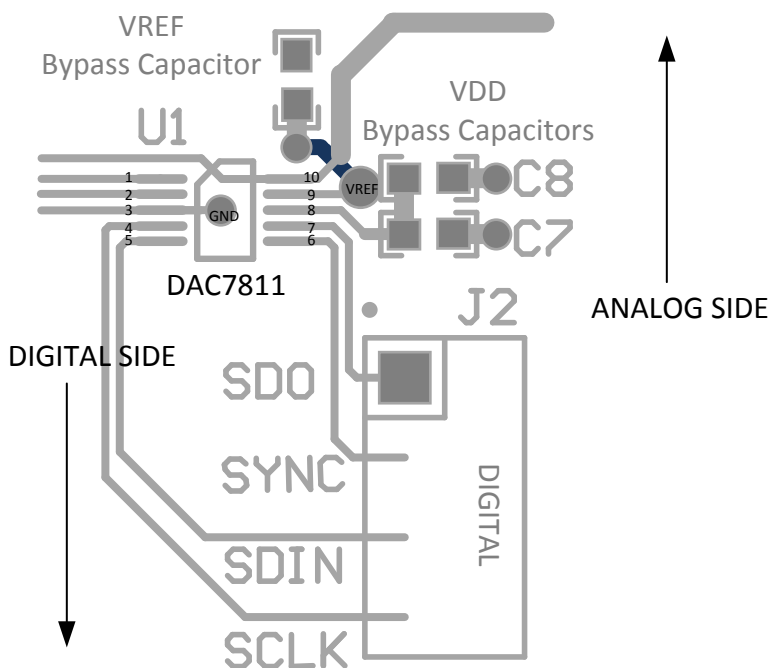


Figure 35. DAC7811 Example Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

如需相关文档，请参阅：

- [《TI Designs – 高精度：验证设计电压模式倍增 DAC 参考设计》\(TIDUAF0\)](#)
- [《TI Designs – 高精度：验证设计单电源单极倍增 DAC 参考设计》\(TIDU300\)](#)
- [《将 DAC7811 连接到 MSP430F449》\(SLAA372\)](#)
- [DAC7811EVM \(SLAU163\)](#)

11.2 接收文档更新通知

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11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC7811IDGS	Active	Production	VSSOP (DGS) 10	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	7811
DAC7811IDGS.A	Active	Production	VSSOP (DGS) 10	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	7811
DAC7811IDGSG4	Active	Production	VSSOP (DGS) 10	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	7811
DAC7811IDGSR	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAUAG SN	Level-2-260C-1 YEAR	-40 to 125	7811
DAC7811IDGSR.A	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7811
DAC7811IDGSRG4	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	7811
DAC7811IDGSRG4.A	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	7811
DAC7811IDGST	Active	Production	VSSOP (DGS) 10	250 SMALL T&R	Yes	NIPDAUAG SN	Level-2-260C-1 YEAR	-40 to 125	7811
DAC7811IDGST.A	Active	Production	VSSOP (DGS) 10	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7811

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7811IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
DAC7811IDGSRG4	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC7811IDGST	VSSOP	DGS	10	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7811IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
DAC7811IDGSRG4	VSSOP	DGS	10	2500	366.0	364.0	50.0
DAC7811IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DAC7811IDGS	DGS	VSSOP	10	80	330	6.55	500	2.88
DAC7811IDGS.A	DGS	VSSOP	10	80	330	6.55	500	2.88
DAC7811IDGSG4	DGS	VSSOP	10	80	330	6.55	500	2.88



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

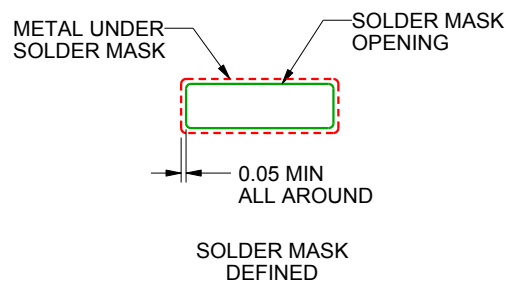
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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