DAC7551-Q1 12 位、超低毛刺脉冲、电压输出数模转换器

1 特性

- 符合汽车应用要求
- 相对精度 (INL)：±0.35 LSB
- 超低毛刺脉冲能量：0.1nV-s
- 低功耗运行：2.7V 时为 100μA
- 上电复位为零量程
- 电源： 2.7V 至 5.5V 单一电源
- 断电：2.7V 时为 0.05μA
- 12 位线性和单调性
- 轨到轨电压输出
- 稳定时间：5μs（最大）
- 具有施密特触发输入的 SPI 兼容串行接口：高达 50MHz
- 菊花链功能
- 异步硬件清除为零量程
- 特定温度范围：
  –40°C 至 +105°C
- 小型 2mm × 3mm 12 引脚 USON 封装
- 名称带 Z 后缀的器件改善了分层现象

2 应用

- 便携式电池供电仪器
- 数字增益和偏移调整
- 可编程电压源和电流源
- 可编程衰减器
- 工业过程控制
- ADAS 雷达应用
- 碰撞预警
- 盲点检测

3 说明

DAC7551-Q1 器件是一款单通道电压输出数模转换器 (DAC)，它具有优异的线性和单调性，并且采用一种专有架构 可以最大限度减小毛刺脉冲能量。 DAC7551-Q1 器件功耗很低，可通过 2.7V 到 5.5V 的单电源供电运行。 DAC7551-Q1 输出放大器可驱动 2kΩ、200pF 的轨到轨负载，稳定时间仅为 5μs。 其输出范围通过外部电压基准进行设置。

3 线串行接口可以高达 50MHz 的时钟速率运行且与 SPI™， QSPI™、microwire 和 DSP 接口标准兼容。该器件集成有上电复位 (POR) 电路，可确保在器件发生有效写入周期之前，将 DAC 输出电压保持为 0V，其包含的断电功能可使器件的电流消耗降至 2μA 以下。

DAC7551-Q1 器件体积小，功耗低，是电池供电便携式应用的理想选择。 其功耗典型值在 5V 时为 0.5mW，在 3V 时为 0.23mW，在断电模式下降至 1μW。

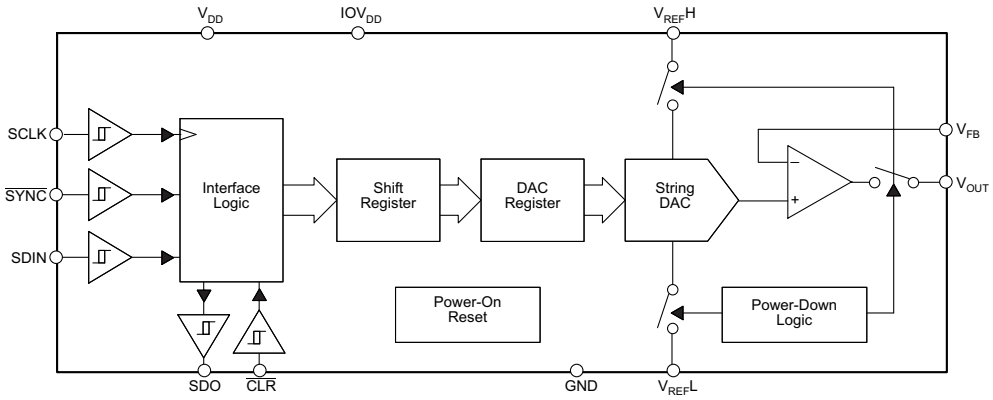
DAC7551-Q1 器件采用 12 引脚 USON 封装，额定工作温度范围为 –40°C 到 +105°C。 名称带有 Z 后缀的器件与标准器件相比，分层现象有所减少。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC7551-Q1	USON (12)	2.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

功能方框图



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4 修订历史记录

Changes from Revision A (February 2015) to Revision B **Page**

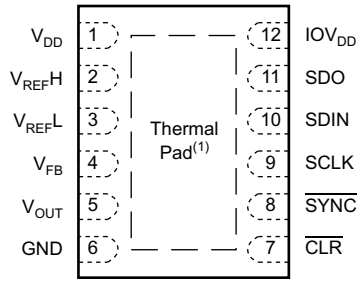
- 已添加 ADAS 雷达、碰撞预警和盲点检测至*应用*列表 ... 1
- Changed the thermal information values for the DRN (USON) package in the *Thermal Information* table ... 4

Changes from Original (June 2011) to Revision A **Page**

- 已添加 *ESD 额定值*表、*建议运行条件*表、*特性描述*部分、*器件功能模式*部分、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 发布了名称带 Z 后缀的可订购器件型号 DAC7551ZTDRNRQ1，该器件改善了分层现象 ... 1

5 Pin Configuration and Functions

DRN Package
12-Pin USON With Exposed Thermal Pad
Top View



(1) The thermal pad should be connected to GND.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{DD}	I	Analog voltage supply input
2	$V_{REF}H$	I	Positive reference voltage input
3	$V_{REF}L$	I	Negative reference voltage input
4	V_{FB}	I	DAC amplifier sense input.
5	V_{OUT}	O	Analog output voltage from DAC
6	GND	—	Ground.
7	$\overline{CLR}$	I	Asynchronous input to clear the DAC registers. When the $\overline{CLR}$ pin is low, the DAC register is set to 000h and the output voltage to 0 V.
8	$\overline{SYNC}$	I	Frame synchronization input. The falling edge of the $\overline{SYNC}$ pulse indicates the start of a serial data frame shifted out to the DAC7551-Q1 device.
9	SCLK	I	Serial clock input
10	SDIN	I	Serial data input
11	SDO	O	Serial data output
12	IOV_{DD}	I	I/O voltage supply input

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

	MIN	MAX	UNIT
V_{DD} , IOV_{DD} to GND	–0.3	6	V
Digital input voltage to GND	–0.3	V_{DD} + 0.3	V
V_{OUT} to GND	–0.3	V_{DD} + 0.3	V
Operating temperature range	–40	105	°C
Junction temperature, T_J max		150	°C
Power dissipation (DRN)	(T_J max – T_A) / $R_{\theta JA}$		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 6, 7, and 12)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	V_{DD}	2.7		5.5	V
		$V_{REF}H$	0.25		V_{DD}	
		$V_{REF}L$	0	GND	V_{DD}	
		V_{FB}	0		V_{DD}	
		IOV_{DD}	1.8		V_{DD}	
		$\overline{CLR}$	0		IOV_{DD}	
		$\overline{SYNC}$	0		IOV_{DD}	
		SCLK	0		IOV_{DD}	
		SDIN	0		IOV_{DD}	
V_O	Output voltage	SDO	0		IOV_{DD}	V
		V_{OUT}	0		V_{DD}	
T_J	Operating junction temperature				150	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRN (USON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	18.2	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	18.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

all specifications at –40°C to +105°C, V_{DD} = 2.7 to 5.5 V, $V_{REF}H$ = V_{DD}, $V_{REF}L$ = GND, R_L = 2 kΩ to GND, and C_L = 200 pF to GND (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)					
Resolution		12			Bits
Relative accuracy			±0.35	±1	LSB
Differential nonlinearity	Specified monotonic by design		±0.08	±0.5	LSB
Offset error				±12	mV
Zero-scale error	All zeroes loaded to DAC register			±12	mV
Gain error				±0.15	%FSR
Full-scale error				±0.5	%FSR
Zero-scale error drift			7		µV/°C
Gain temperature coefficient			3		ppm of FSR/°C

(1) Linearity tested using a reduced code range of 30 to 4065; output unloaded.

Electrical Characteristics (continued)

all specifications at –40°C to +105°C, V_{DD} = 2.7 to 5.5 V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = GND, R_L = 2 kΩ to GND, and C_L = 200 pF to GND (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power-supply rejection ratio		V_{DD} = 5 V		0.75		mV/V
OUTPUT CHARACTERISTICS(2)							
	Output voltage range			2 × $V_{REF}L$		$V_{REF}H$	V
	Output voltage settling time		R_L = 2 kΩ, 0 pF < C_L < 200 pF			5	µs
	Slew rate				1.8		V/µs
	Capacitive load stability		R_L = ∞		470		pF
			R_L = 2 kΩ		1000		
	Digital-to-analog glitch impulse		1 LSB change around major carry		0.1		nV-s
	Digital feedthrough				0.1		nV-s
	Output noise density		10kHz offset frequency		120		nV/√Hz
THD	Total harmonic distortion		f_{OUT} = 1 kHz, f_S = 1 MSPS, BW = 20 kHz		–85		dB
	DC output impedance				1		Ω
	Short-circuit current		V_{DD} = 5 V		50		mA
			V_{DD} = 3 V		20		
	Power-up time		Coming out of power-down mode, V_{DD} = 5 V		15		µs
			Coming out of power-down mode, V_{DD} = 3 V		15		
REFERENCE INPUT							
	$V_{REF}H$ input range			0		V_{DD}	V
	$V_{REF}L$ input range		$V_{REF}L < V_{REF}H$	0	GND	V_{DD}	V
	Reference input impedance				100		kΩ
	Reference current		$V_{REF} = V_{DD}$ = 5 V		50	100	µA
			$V_{REF} = V_{DD}$ = 3 V		30	60	
LOGIC INPUTS(2)							
	Input current					±1	µA
V_{IN_L}	Input low voltage		IOV_{DD} ≥ 2.7 V			0.3 IOV_{DD}	V
V_{IN_H}	Input high voltage		IOV_{DD} ≥ 2.7 V	0.7 IOV_{DD}			V
	Pin capacitance					3	pF
POWER REQUIREMENTS							
V_{DD}	Supply voltage			2.7		5.5	V
IOV_{DD}	I/O supply voltage(3)			1.8		V_{DD}	V
I_{DD}	Supply current(4)	Normal operation (DAC active and excluding load current)	V_{DD} = 3.6 to 5.5 V, $V_{IH} = IOV_{DD}$, V_{IL} = GND		150	200	µA
			V_{DD} = 2.7 to 3.6 V, $V_{IH} = IOV_{DD}$, V_{IL} = GND		100	150	
		All power-down modes	V_{DD} = 3.6 to 5.5 V, $V_{IH} = IOV_{DD}$, V_{IL} = GND		0.2	2	µA
			V_{DD} = 2.7 to 3.6 V, $V_{IH} = IOV_{DD}$, V_{IL} = GND		0.05	2	
POWER EFFICIENCY							
	I_{OUT}/I_{DD}		I_{LOAD} = 2 mA, V_{DD} = 5 V		93%		
TEMPERATURE RANGE							
	Specified performance			–40		105	°C

(2) Specified by design and characterization; not production tested. For 1.8 V < IOV_{DD} < 2.7 V, TI recommends that V_{IH} ≥ 0.8 IOV_{DD}, and V_{IL} ≤ 0.2 IOV_{DD}.
(3) IOV_{DD} operates down to 1.8 V with slightly degraded timing, as long as V_{IH} ≥ 0.8 IOV_{DD} and V_{IL} ≤ 0.2 IOV_{DD}.
(4) I_{DD} tested with digital input code = 0032.

6.6 Timing Requirements(1)

All specifications at –40°C to +105°C, V_{DD} = 2.7 to 5.5 V, and R_L = 2 kΩ to GND (unless otherwise noted). See Figure 1.

			MIN	MAX	UNIT
t_1(2)	SCLK cycle time	V_{DD} = 2.7 V to 3.6 V	20		ns
		V_{DD} = 3.6 V to 5.5 V	20		
t_2	SCLK HIGH time	V_{DD} = 2.7 V to 3.6 V	6.5		ns
		V_{DD} = 3.6 V to 5.5 V	6.5		
t_3	SCLK LOW time	V_{DD} = 2.7 V to 3.6 V	6.5		ns
		V_{DD} = 3.6 V to 5.5 V	6.5		
t_4	$\overline{SYNC}$ falling edge to SCLK falling edge setup time	V_{DD} = 2.7 V to 3.6 V	4		ns
		V_{DD} = 3.6 V to 5.5 V	4		
t_5	Data setup time	V_{DD} = 2.7 V to 3.6 V	3		ns
		V_{DD} = 3.6 V to 5.5 V	3		
t_6	Data hold time	V_{DD} = 2.7 V to 3.6 V	3		ns
		V_{DD} = 3.6 V to 5.5 V	3		
t_7	SCLK falling edge to $\overline{SYNC}$ rising edge	V_{DD} = 2.7 V to 3.6 V	0	t_1 – 10 ns(3)	ns
		V_{DD} = 3.6 V to 5.5 V	0	t_1 – 10 ns(3)	
t_8	Minimum $\overline{SYNC}$ HIGH time	V_{DD} = 2.7 V to 3.6 V	20		ns
		V_{DD} = 3.6 V to 5.5 V	20		
t_9	SCLK falling edge to SDO valid	V_{DD} = 2.7 V to 3.6 V	10		ns
		V_{DD} = 3.6 V to 5.5 V	10		
t_{10}	$\overline{CLR}$ pulse width low	V_{DD} = 2.7 V to 3.6 V	10		ns
		V_{DD} = 3.6 V to 5.5 V	10		

(1) All input signals are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
(2) Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 to 5.5 V.
(3) SCLK falling edge to $\overline{SYNC}$ rising edge time shold not exceed (t_1 – 10 ns) to latch the correct data.

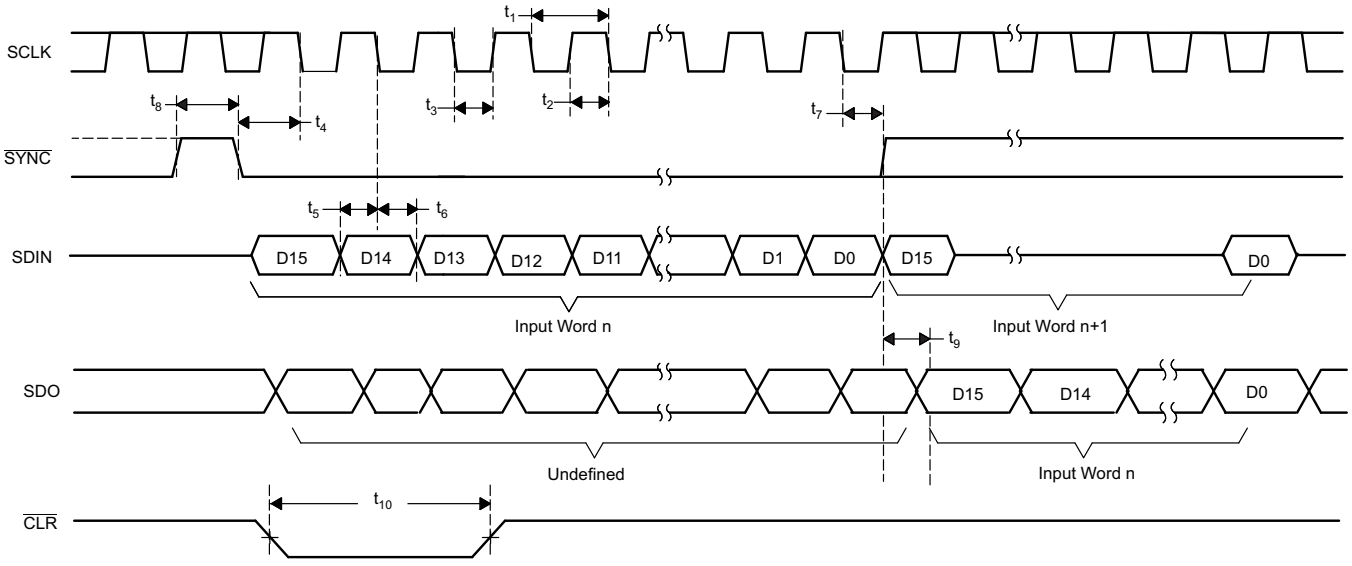
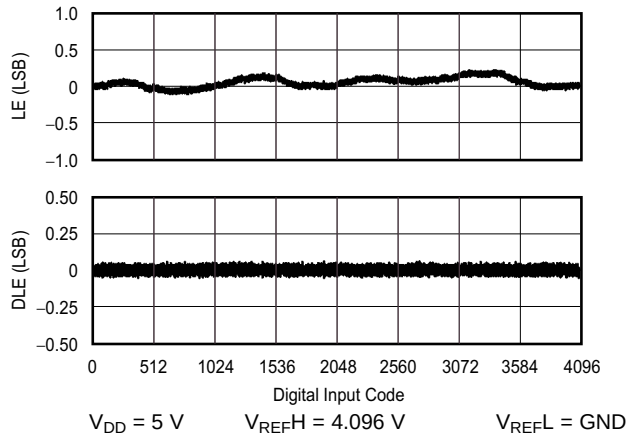


Figure 1. Serial Write Operation Timing Diagram

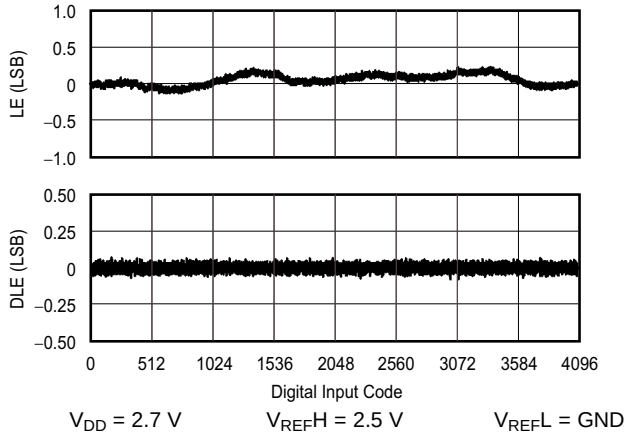
6.7 Typical Characteristics

At T_A = 25°C, unless otherwise noted.



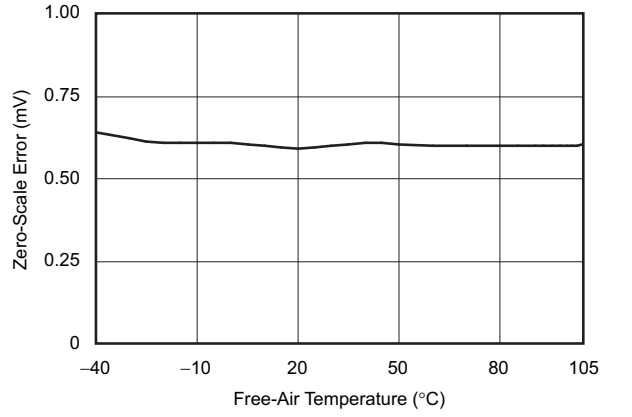
V_{DD} = 5 V $V_{REF}H$ = 4.096 V $V_{REF}L$ = GND

Figure 2. Linearity Error and Differential Linearity Error vs Digital Input Code



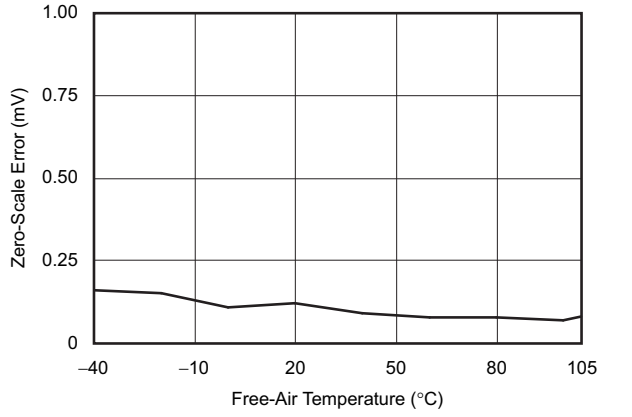
V_{DD} = 2.7 V $V_{REF}H$ = 2.5 V $V_{REF}L$ = GND

Figure 3. Linearity Error and Differential Linearity Error vs Digital Input Code



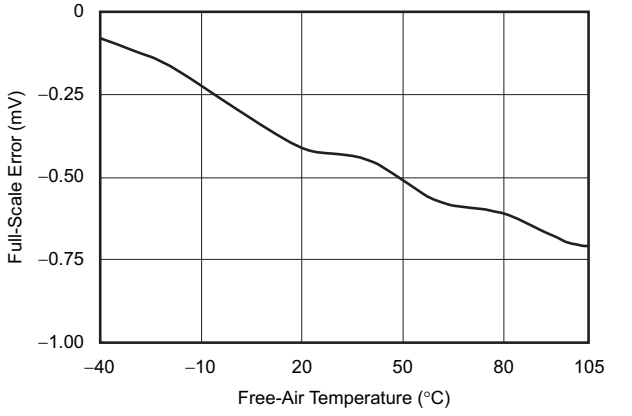
V_{DD} = 5 V $V_{REF}H$ = 4.096 V $V_{REF}L$ = GND

Figure 4. Zero-Scale Error vs Free-Air Temperature



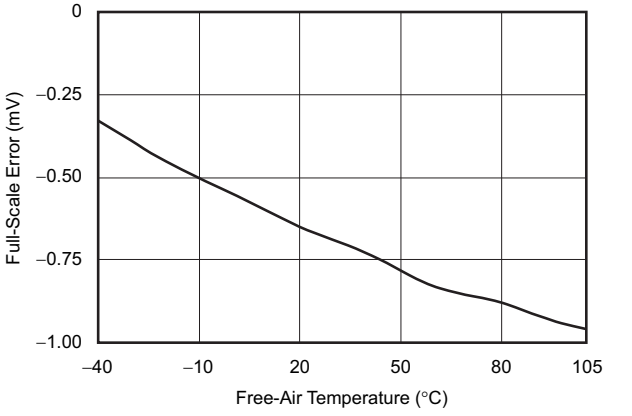
V_{DD} = 2.7 V $V_{REF}H$ = 2.5 V $V_{REF}L$ = GND

Figure 5. Zero-Scale Error vs Free-Air Temperature



V_{DD} = 5 V $V_{REF}H$ = 4.096 V $V_{REF}L$ = GND

Figure 6. Full-Scale Error vs Free-Air Temperature



V_{DD} = 2.7 V $V_{REF}H$ = 2.5 V $V_{REF}L$ = GND

Figure 7. Full-Scale Error vs Free-Air Temperature

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted.

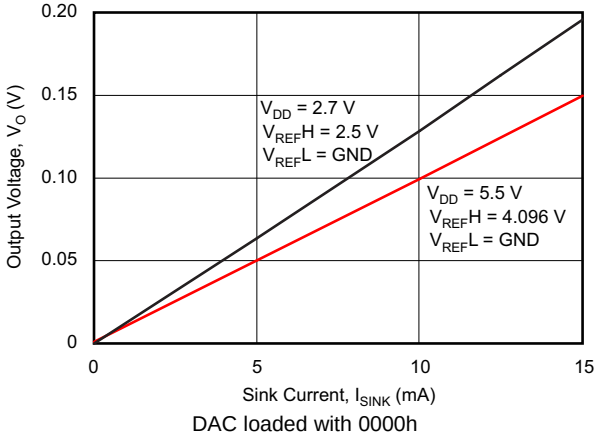


Figure 8. Sink Current at Negative Rail (Typical)

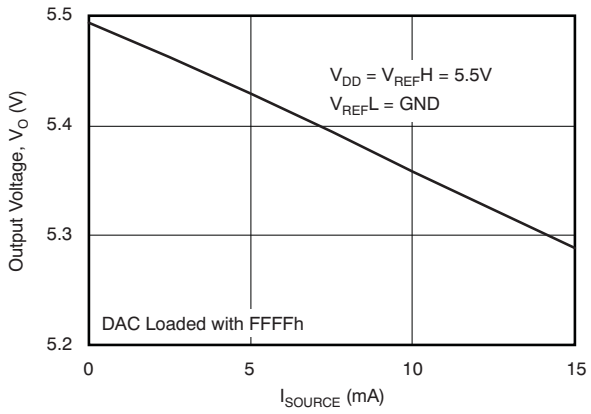


Figure 9. Source Current at Positive Rail

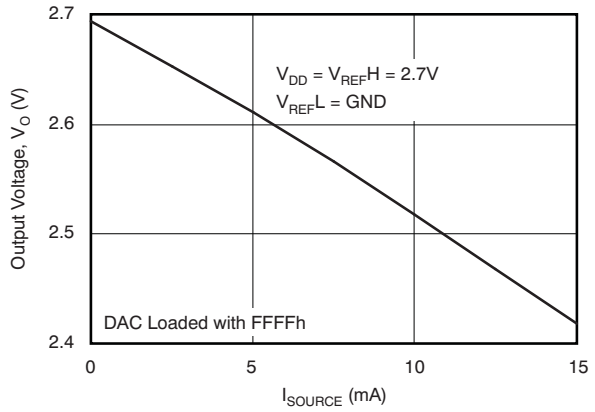


Figure 10. Source Current at Positive Rail

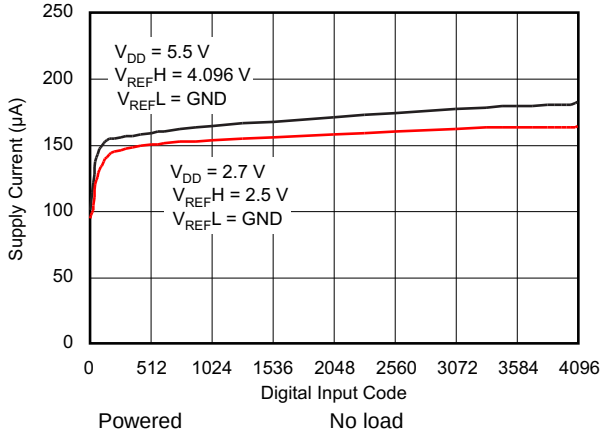


Figure 11. Supply Current vs Digital Input Code

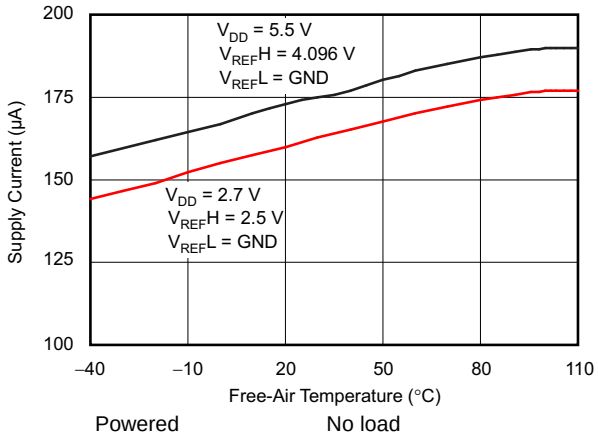


Figure 12. Supply Current vs Free-Air Temperature

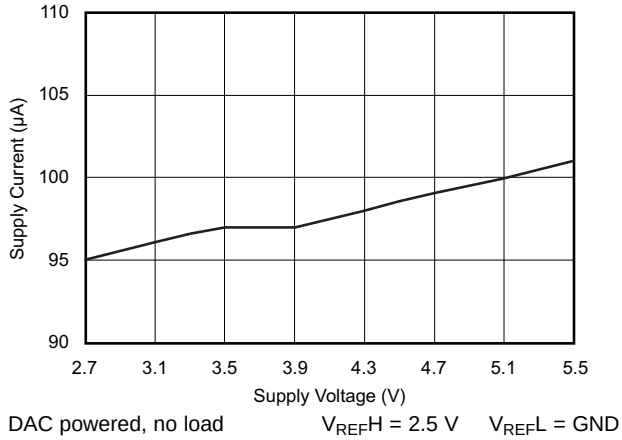
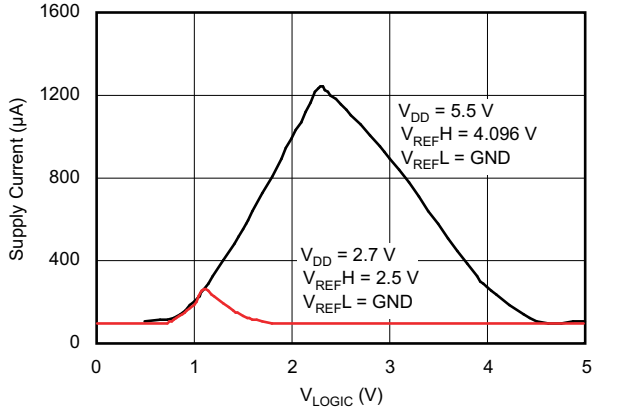


Figure 13. Supply Current vs Supply Voltage

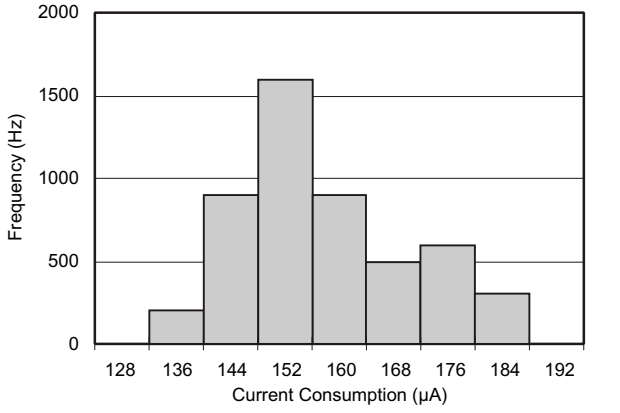
Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted.



T_A = 25°C SCLK input All other inputs = GND

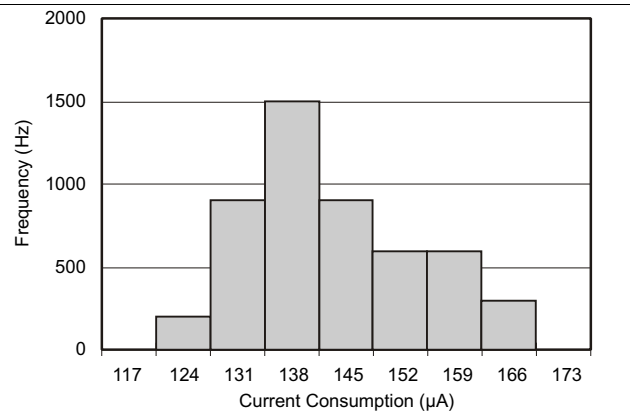
Figure 14. Supply Current vs Logic Input Voltage



Digital input code = 2048

V_{DD} = 5.5 V V_{REF}H = 4.096 V V_{REF}L = GND

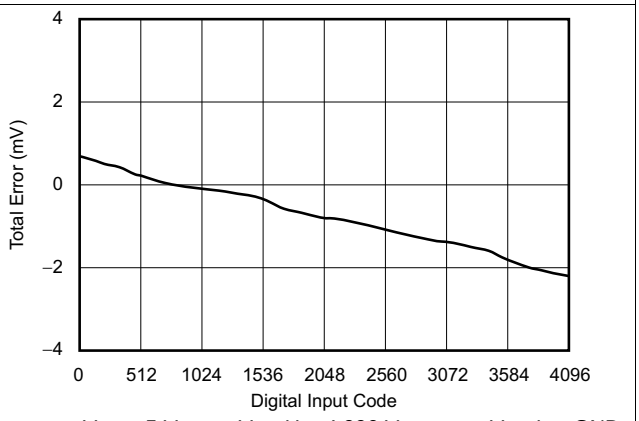
Figure 15. Histogram of Current Consumption, 5.5 V



Digital input code = 2048

V_{DD} = 2.7 V V_{REF}H = 2.5 V V_{REF}L = GND

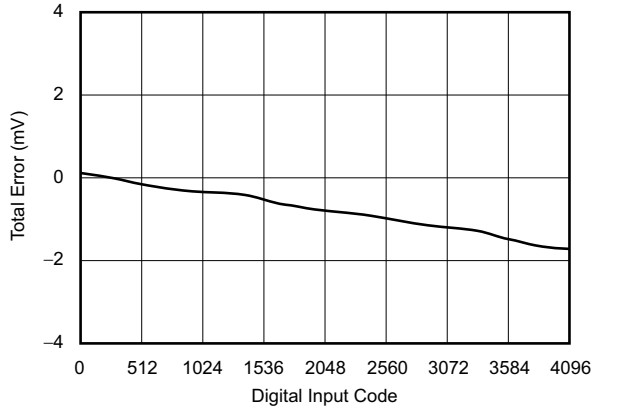
Figure 16. Histogram of Current Consumption, 2.7 V



V_{DD} = 5 V V_{REF}H = 4.096 V V_{REF}L = GND

T_A = 25°C

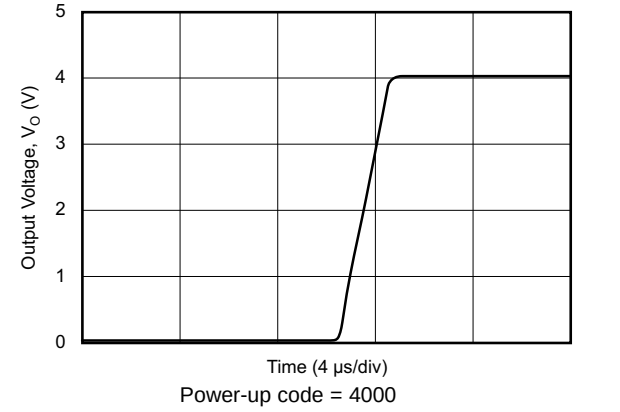
Figure 17. Total Error, 5 V



V_{DD} = 2.7 V V_{REF}H = 2.5 V V_{REF}L = GND

T_A = 25°C

Figure 18. Total Error, 2.7 V



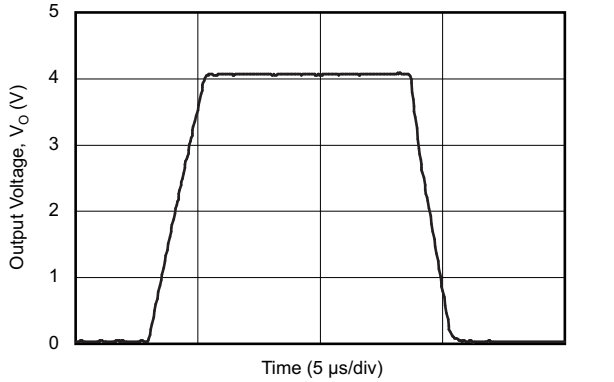
Power-up code = 4000

V_{DD} = 5 V V_{REF}H = 4.096 V V_{REF}L = GND

Figure 19. Exiting Power-Down Mode

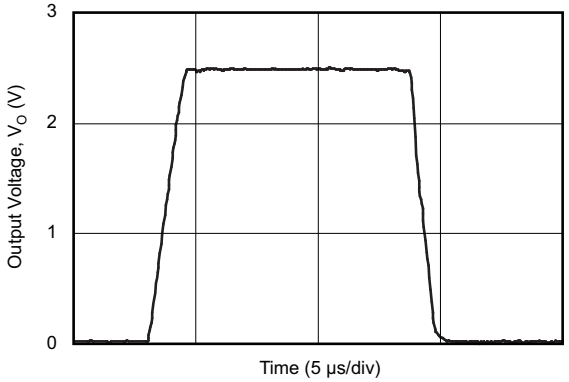
Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted.



Output loaded with 200 pF to GND
Code 0041 to 4055
V_{DD} = 5 V $V_{REF}H$ = 4.096 V $V_{REF}L$ = GND

Figure 20. Large-Signal Settling Time, 5 V



Output loaded with 200 pF to GND
Code 0041 to 4055
V_{DD} = 2.7 V $V_{REF}H$ = 2.5 V $V_{REF}L$ = GND

Figure 21. Large-Signal Settling Time, 2.7 V

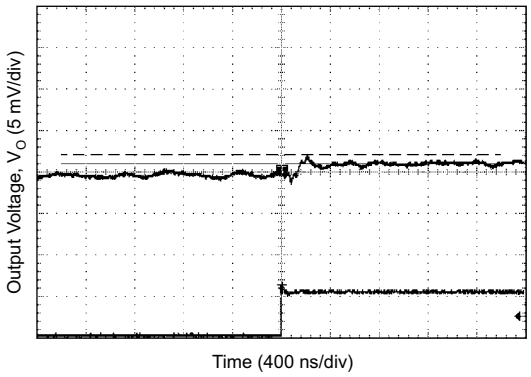


Figure 22. Midscale Glitch

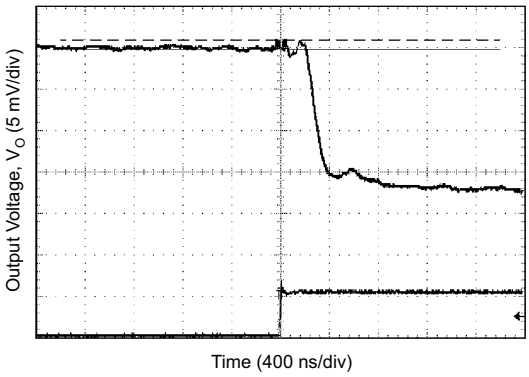


Figure 23. Worst-Case Glitch

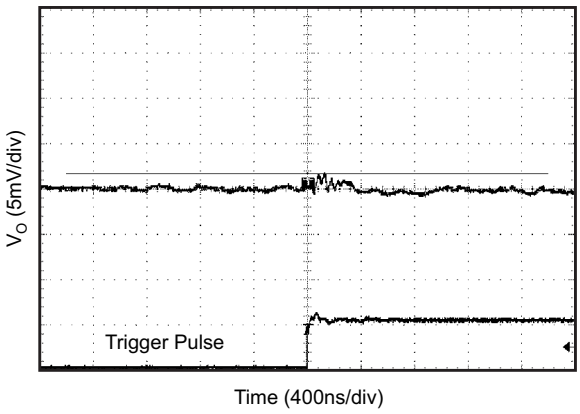
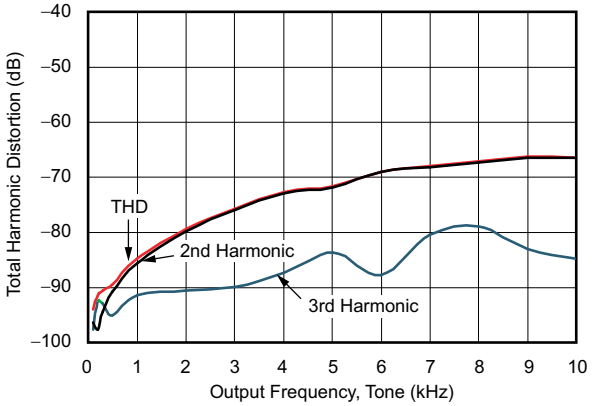


Figure 24. Digital Feedthrough Error



V_{DD} = 5.5 V $V_{REF}H$ = 4.096 V $V_{REF}L$ = GND
f_S = 1 MSPS –1-dB FSR digital input
Measurement bandwidth = 20 kHz

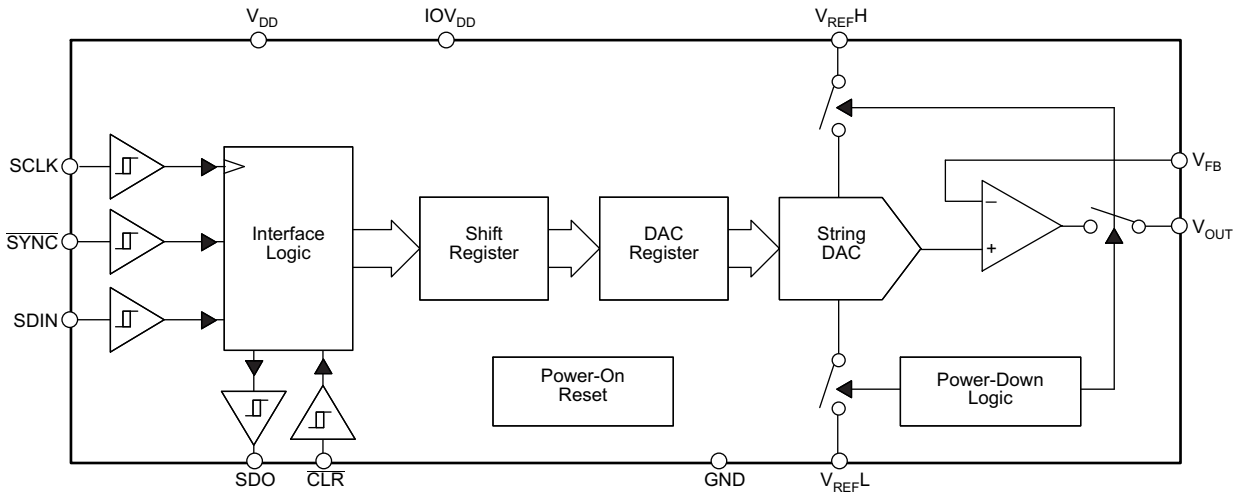
Figure 25. Total Harmonic Distortion vs Output Frequency

7 Detailed Description

7.1 Overview

The DAC7551-Q1 device is a 12-bit resistor-string digital-to-analog converter (DAC). Unbuffered external reference inputs allow for a positive voltage reference as low as 0.25 V and as high as V_{DD}. An amplifier-feedback input is available for better DC accuracy at the load point. The device is controlled over a 16-bit word three-wire serial peripheral interface (SPI) up to 50 MHz with an option to daisy-chain multiple devices. An asynchronous clear function along with power-down features allows for software controlled resets and low-power consumption. A separate logic-supply input means the device can be used with different logic families across a wide range of supply voltages.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital-to-Analog Converter

The architecture of the DAC7551-Q1 device consists of a string DAC followed by an output buffer amplifier. Figure 26 shows a generalized block diagram of the DAC architecture.

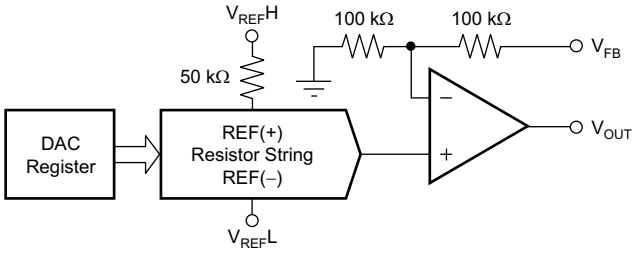


Figure 26. Typical DAC Architecture

The input coding to the DAC7551-Q1 device is unsigned binary, which gives the ideal output voltage as show in Equation 1.

$$V_{OUT} = 2 \times V_{REF}L + (V_{REF}H - V_{REF}L) \times D / 4096 \quad (1)$$

where

- D is the decimal equivalent of the binary code that is loaded to the DAC register, which ranges from 0 to 4095.

Feature Description (continued)

7.3.2 Resistor String

Figure 27 shows the resistor string section. This section is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. The output of the DAC is specified monotonic because it is a string of resistors.

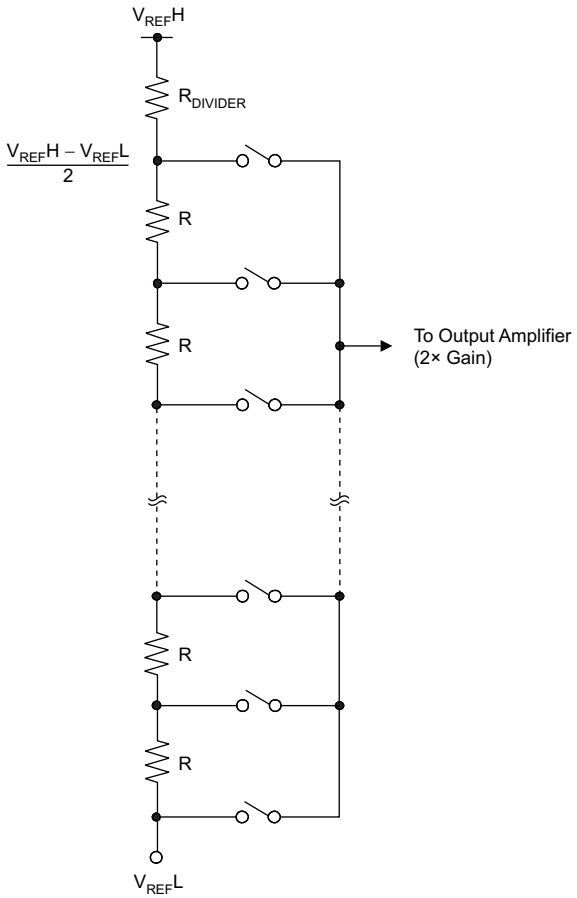


Figure 27. Typical Resistor String

7.3.3 Output Buffer Amplifiers

The output buffer amplifier is capable of generating rail-to-rail voltages on the output, providing an output range of 0 V to V_{DD}. The amplifier is capable of driving a load of 2 kΩ in parallel with up to 1000 pF to ground. Figure 8, Figure 9, and Figure 10 show the sink and source capabilities of the output amplifier. The slew rate is 1.8 V/µs with a half-scale settling time of 3 µs with the output unloaded.

7.3.3.1 DAC External Reference Input

The DAC7551-Q1 device contains $V_{REF}H$ and $V_{REF}L$ reference inputs which are unbuffered. The $V_{REF}H$ reference voltage can be as low as 0.25 V, and as high as V_{DD} because there is no restriction of headroom and footroom from any reference amplifier.

Using a buffered reference in the external circuit is recommended (for example, the REF3140 device). The input impedance is typically 100 kΩ.

Feature Description (continued)

7.3.3.2 Amplifier Sense Input

The DAC7551-Q1 device contains an amplifier-feedback input pin, V_{FB}. For voltage output operation, V_{FB} must be externally connected to V_{OUT}. For better DC accuracy, this connection should be made at load points. The V_{FB} pin is also useful for a variety of applications, including digitally-controlled current sources. The feedback input pin is internally connected to the DAC amplifier negative input terminal through a 100-kΩ resistor. The amplifier negative input terminal internally connects to ground through another 100-kΩ resistor (see Figure 26). These connections form a gain-of-two, noninverting, amplifier configuration. Overall gain remains 1 because the resistor string has a divide-by-two configuration. The resistance seen at the V_{FB} pin is approximately 200 kΩ to ground.

7.3.3.3 Power-On Reset

On power up, all registers are cleared and the DAC channel is updated with zero-scale voltage. The DAC output remains in this state until valid data are written. This setup is particularly useful in applications where knowing the state of the DAC output while the device is powering up is important. To not turn on ESD protection devices, V_{DD} and IOV_{DD} should be applied before any other pin (such as $V_{REF}H$) is brought high. The power-up sequence of V_{DD} and IOV_{DD} is irrelevant. Therefore, IOV_{DD} can be brought up before V_{DD}, or the other way around.

7.3.3.4 Power Down

The DAC7551-Q1 device has a flexible power-down capability. During a power-down condition, the user has flexibility to select the output impedance of the DAC. During power-down operation, the DAC can have either 1kΩ, 100kΩ, or Hi-Z output impedance to ground.

7.3.3.5 Asynchronous Clear

The DAC7551-Q1 output is asynchronously set to zero-scale voltage immediately after the $\overline{CLR}$ pin is brought low. The $\overline{CLR}$ signal resets all internal registers and therefore functions similar to the power-on reset. The DAC7551-Q1 device updates at the first rising edge of the $\overline{SYNC}$ signal that occurs after the $\overline{CLR}$ pin is brought back to high.

7.3.3.6 IOVDD and Level Shifters

The DAC7551-Q1 device can be used with different logic families that require a wide range of supply voltages. To enable this useful feature, the IOV_{DD} pin must be connected to the logic supply voltage of the system. All DAC7551-Q1 digital input and output pins are equipped with level-shifter circuits. Level shifters at the input pins ensure that external logic-high voltages are translated to the internal logic-high voltage, with no additional power dissipation. Similarly, the level shifter for the SDO pin translates the internal logic-high voltage (V_{DD}) to the external logic-high level (IOV_{DD}). For single-supply operation, the IOV_{DD} pin can be tied to the V_{DD} pin.

7.3.4 Integral and Differential Linearity

The DAC7551-Q1 device uses precision thin-film resistors providing exceptional linearity and monotonicity. Integral linearity error is typically within ±0.35 LSBs, and differential linearity error is typically within ±0.08 LSBs.

7.3.5 Glitch Energy

The DAC7551-Q1 device uses a proprietary architecture that minimizes glitch energy. The code-to-code glitches are so low that they are usually buried within the wide-band noise and cannot be easily detected. The DAC7551-Q1 glitch is typically well under 0.1 nV-s. Such low glitch energy provides more than a ten-time improvement over industry alternatives.

7.4 Device Functional Modes

The DAC7551-Q1 device uses four modes of operation. These modes are accessed by setting bit PD0 (DB13) and PD1 (DB14) in the control register. Table 1 shows how to control the operating mode with data bits PD0 (DB13) and PD1 (DB14). The DAC7551-Q1 device treats the power-down condition as data; all the operation modes are still valid for power down. Broadcasting a power-down condition to all the DAC7551-Q1 devices in a system is possible. Powering down a channel and updating data on other channels is also possible. Furthermore, writing to the DAC register or buffer of the DAC channel that is powered down is also possible. When the DAC is the powered on, the DAC contains this new value.

Device Functional Modes (continued)

When both the PD0 and PD1 bits are set to 0, the device works normally with the typical consumption of 100 µA at 2.7 V. For the three power-down modes, the supply current falls to 0.05 µA at 2.7 V. As listed in Table 1, three different power-down options are available. The VOUT pin can be connected internally to GND through a 1-kΩ resistor or a 100-kΩ resistor or can be open circuited (High-Z). In other words, DB14 and DB13 = 11 represent a power-down condition with High-Z output impedance for a selected channel. DB14 and DB13 = 01 and 10 represent a power-down condition with a 1-kΩ and 100-kΩ output impedance respectively.

7.5 Programming

7.5.1 Serial Interface

The DAC7551-Q1 device is controlled over a versatile 3-wire serial interface, which operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire, and DSP interface standards.

Table 1. Serial Interface Programming

CONTROL				DATA BITS	FUNCTION
DB15	DB14	DB13 (PD1)	DB12 (PD0)	DB11–DB0	
X	X	0	0	data	Normal mode
X	X	0	1	X	Powerdown 1kΩ
X	X	1	0	X	Powerdown 100kΩ
X	X	1	1	X	Powerdown Hi-Z

7.5.1.1 16-Bit Word and Input Shift Register

The input shift register is 16 bits wide. DAC data are loaded into the device as a 16-bit word under the control of a serial clock input, SCLK, as shown in Figure 1. The 16-bit word, listed in Table 1, consists of four control bits followed by 12 bits of DAC data. The data format is straight binary with all 0s corresponding to 0-V output and all 1s corresponding to full-scale output (V_{REF} – 1 LSB). Data are loaded MSB first (bit 15) where the first two bits (DB15 and DB14) are *don't care* bits. Bit 13 and bit 12 (DB13 and DB12) determine either normal mode operation or power-down mode (see Table 1).

The $\overline{\text{SYNC}}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while the $\overline{\text{SYNC}}$ pin is low. To begin the serial data transfer, the $\overline{\text{SYNC}}$ pin should be taken low, observing the minimum $\overline{\text{SYNC}}$-to-SCLK falling edge setup time, t_4. After the $\overline{\text{SYNC}}$ pin goes low, serial data is shifted into the device input shift register on the falling edges of SCLK for 16 clock pulses.

The SPI is enabled after the $\overline{\text{SYNC}}$ pin becomes low and the data are continuously shifted into the shift register at each falling edge of the SCLK input. When the $\overline{\text{SYNC}}$ pin is brought high, the last 16 bits stored in the shift register are latched into the DAC register, and the DAC updates.

7.5.1.2 Daisy-Chain Operation

Daisy-chain operation is used for updating serially-connected devices on the rising edge of the $\overline{\text{SYNC}}$ in.

As long as the $\overline{\text{SYNC}}$ pin is high, the SDO pin is in a high-impedance state. When the $\overline{\text{SYNC}}$ pin is brought low the output of the internal shift register is tied to the SDO pin. As long as the $\overline{\text{SYNC}}$ pin is low, the SDO pin duplicates the SDIN signal with a 16-cycle delay. To support multiple devices in a daisy chain, the SCLK and $\overline{\text{SYNC}}$ signals are shared across all devices, and the SDO pin of one DAC7551-Q1 device should be tied to the SDIN pin of the next DAC7551-Q1 device. For *n* devices in such a daisy chain, 16*n* SCLK cycles are required to shift the entire input data stream. After 16*n* SCLK falling edges are received, following a falling $\overline{\text{SYNC}}$ signal, the data stream becomes complete and the $\overline{\text{SYNC}}$ pin can be brought high to update *n* devices simultaneously. SDO operation is specified at a maximum SCLK speed of 10 MHz.

In daisy-chain mode, the use of a weak pulldown resistor on the SDO output pin, which provides the SDIN data for the next device in the chain, is recommended. For standalone operation, the maximum clock speed is 50 MHz. For daisy-chain operation, the maximum clock speed is 10 MHz.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Waveform Generation

As a result of the exceptional linearity and low glitch of the DAC7551-Q1 device, the device is well-suited for waveform generation (from DC to 10kHz). The DAC7551-Q1 large-signal settling time is 5 µs, supporting an update rate of 200 kSPS. However, the update rates can exceed 1 MSPS if the waveform to be generated consists of small voltage steps between consecutive DAC updates. To obtain a high dynamic range, the REF3140 device (4.096 V) or the REF02 device (5 V) is recommended for reference-voltage generation.

8.1.2 Generating ±5-V, ±10-V, and ±12-V Outputs For Precision Industrial Control

Industrial control applications can require multiple feedback loops consisting of sensors, analog-to-digital converters (ADCs), microcontrollers (MCUs), DACs, and actuators. Loop accuracy and loop speed are the two important parameters of such control loops.

8.1.2.1 Loop Accuracy

DAC offset, gain, and the integral linearity errors are not factors in determining the accuracy of the loop. As long as a voltage exists in the transfer curve of a monotonic DAC, the loop can find this voltage and settle to it. On the other hand, DAC resolution and differential linearity do determine the loop accuracy, because each DAC step determines the minimum incremental change the loop can generate. A DNL error less than –1 LSB (non-monotonicity) can create loop instability. A DNL error greater than 1 LSB implies unnecessarily large voltage steps and missed voltage targets. With high DNL errors, the loop loses stability, resolution, and accuracy. Offering 12-bit ensured monotonicity and ±0.08-LSB typical DNL error, the DAC755x devices are great choices for precision control loops.

8.1.2.2 Loop Speed

Many factors determine the control-loop speed, such as ADC conversion time, MCU speed, and DAC settling time. Typically, the ADC conversion time, and the MCU computation time are the two major factors that dominate the time constant of the loop. DAC settling time is rarely a dominant factor because ADC conversion times usually exceed DAC conversion times. DAC offset, gain, and linearity errors can slow the loop down only during the startup. When the loop reaches the steady-state operation, these errors do not affect loop speed any further. Depending on the ringing characteristics of the loop-transfer function, DAC glitches can also slow the loop down. With a 1-MSPS (small-signal) maximum data-update rate, the DAC7551-Q1 device can support high-speed control loops. Ultralow glitch energy of the DAC7551-Q1 device significantly improves loop stability and loop settling time.

8.2 Typical Application

8.2.1 Generating Industrial Voltage Ranges

For control-loop applications, DAC gain and offset errors are not important parameters. This consideration could be exploited to lower trim and calibration costs in a high-voltage control-circuit design. Using a quad operational amplifier (OPA4130), and a voltage reference (REF3140), the DAC7551-Q1 can generate the wide voltage swings required by the control loop.

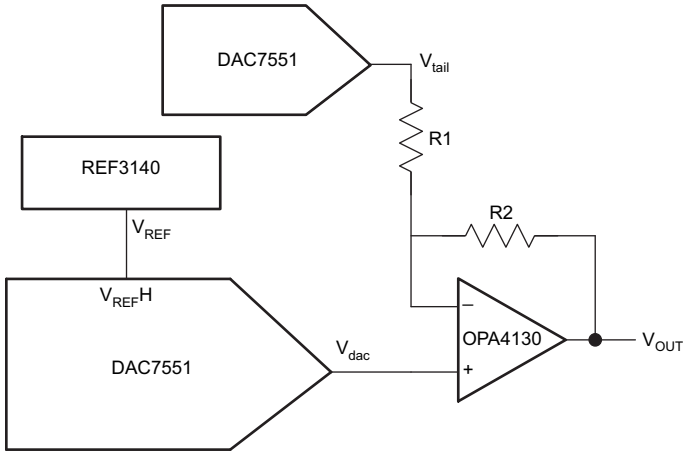


Figure 28. Low-cost, Wide-swing Voltage Generator for Control-Loop Applications

8.2.1.1 Design Requirements

For ±5-V operation:

R1 = 10 kΩ
R2 = 15 kΩ
V_{tail} = 3.33 V
V_{REF} = 4.096 V

For ±10-V operation:

R1 = 10 kΩ
R2 = 39 kΩ
V_{tail} = 2.56 V
V_{REF} = 4.096 V

For ±12-V operation:

R1 = 10 kΩ
R2 = 49 kΩ
V_{tail} = 2.45 V
V_{REF} = 4.096 V

8.2.1.2 Detailed Design Procedure

Use Equation 2 to calculate the output voltage of the configuration.

$$V_{OUT} = V_{REF}\left(\frac{R2}{R1}+1\right)\frac{SDIN}{4096} - V_{tail}\left(\frac{R2}{R1}\right) \quad (2)$$

Fixed R1 and R2 resistors can be used to coarsely set the gain required in the first term of the equation. When R2 and R1 set the gain to include some minimal over-range gain, a single DAC7551-Q1 device can be used to set the required offset voltages. Residual errors are not an issue for loop accuracy because offset and gain errors can be tolerated. One DAC7551-Q1 device can provide the V_{tail} voltages, while four additional DAC7551-Q1 devices can provide the V_{dac} voltages to generate four high-voltage outputs. A single SPI is sufficient to control all five DAC7551-Q1 devices in a daisy-chain configuration.

Typical Application (continued)

8.2.1.3 Application Curves

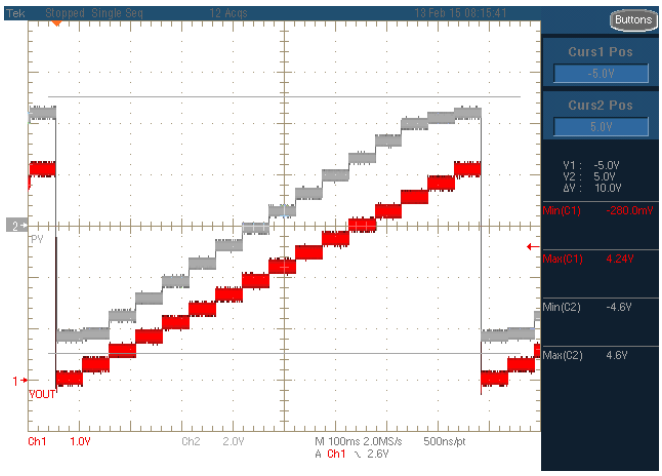


Figure 29. SDIN Step Increments of 273 for ±5-V Operation

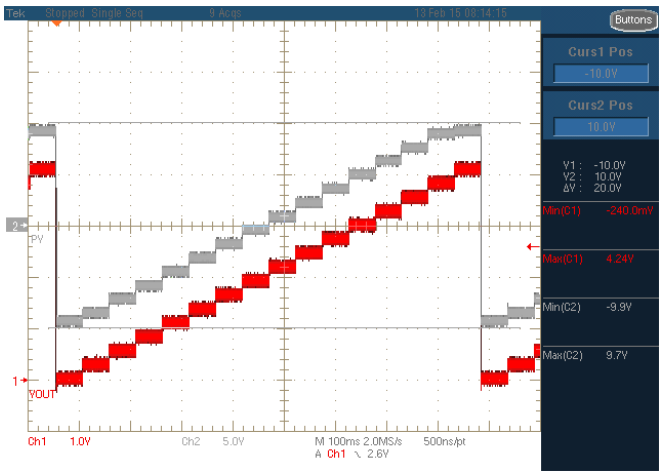


Figure 30. SDIN Step Increments of 273 for ±10-V Operation

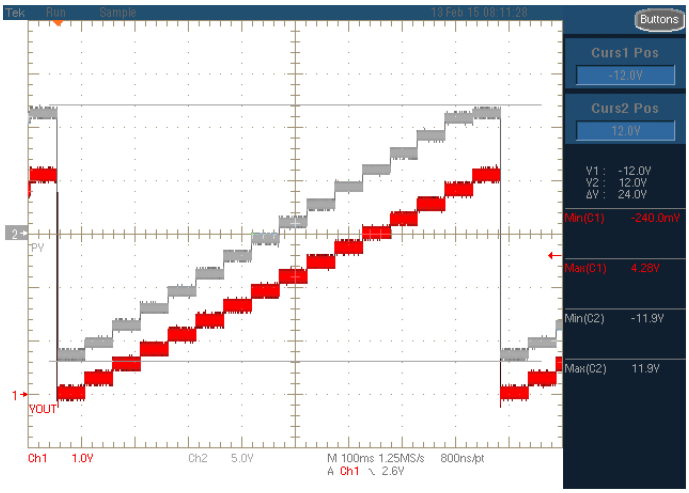


Figure 31. SDIN Step Increments of 273 for ±12-V Operation

9 Power Supply Recommendations

The power applied to the V_{DD} pin should be well regulated and low noise. Switching power supplies and DC-DC converters often have high frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as the internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between power connections and analog output. As with the GND connection, the V_{DD} pin should be connected to a power-supply plane of trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, the use of a 1-µF and 10-µF capacitor and a 0.1-µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors. These bypassing methods are all designed to low-pass filter the supply and remove the high-frequency noise.

10 Layout

10.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC7551-Q1 device offers single-supply operation, and is often used in close proximity with digital logic, microcontrollers, microprocessors, digital signal processors, or a combination. The more digital logic present in the design and the higher the switching speed, the more difficult it is to prevent digital noise from appearing at the output. As a result of the single ground pin of the DAC7551-Q1 device, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, the GND should be connected directly to an analog ground plane. This plane should be separate from the ground connection for the digital components until these components were connected at the power-entry point of the system.

10.2 Layout Example

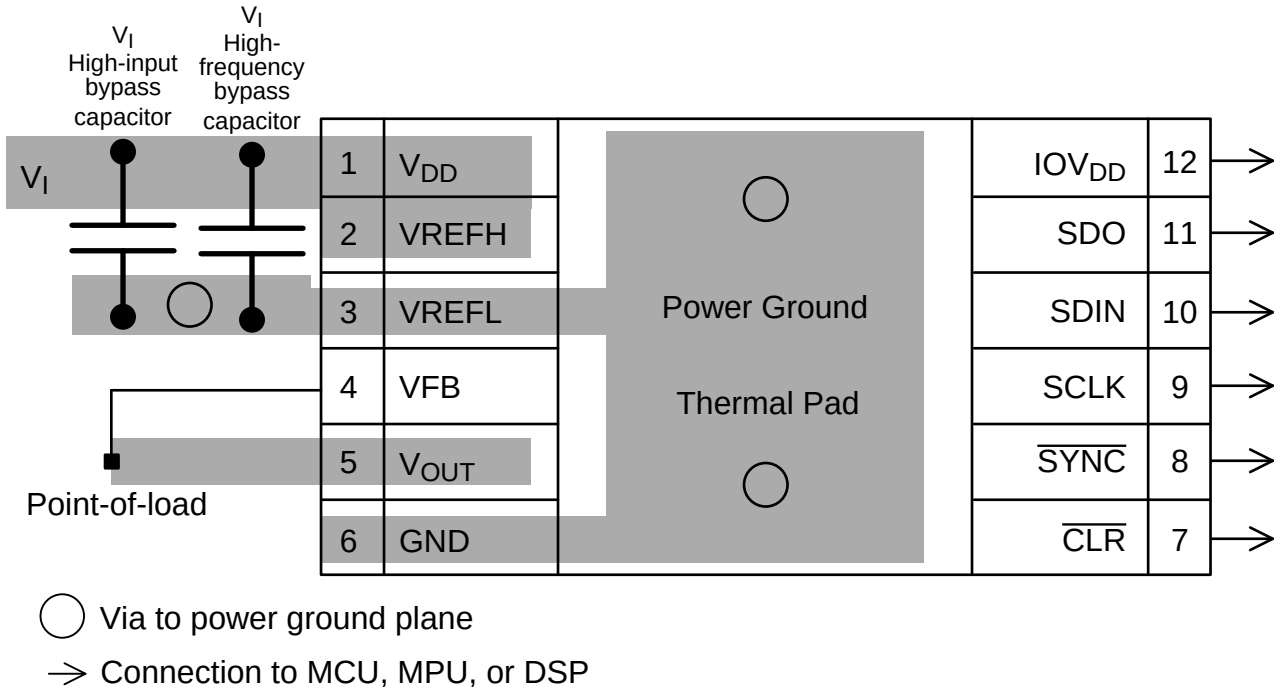


Figure 32. DAC7551-Q1 Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- 《OPA4130 *低功耗、精密 FET 输入运算放大器*》，SBOS053
- 《REF02 *+5V 精密电压基准*》，SBVS003
- 《REF3140 *最大 15ppm/°C、100μA、SOT23-3 串联电压基准*》，SBVS046

11.2 商标

SPI, QSPI are trademarks of Motorola, Inc.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC7551TDRNRQ1	Active	Production	USON (DRN) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RAN
DAC7551TDRNRQ1.A	Active	Production	USON (DRN) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RAN
DAC7551ZTDRNRQ1	Active	Production	USON (DRN) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	SJT
DAC7551ZTDRNRQ1.A	Active	Production	USON (DRN) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	SJT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DAC7551-Q1 :

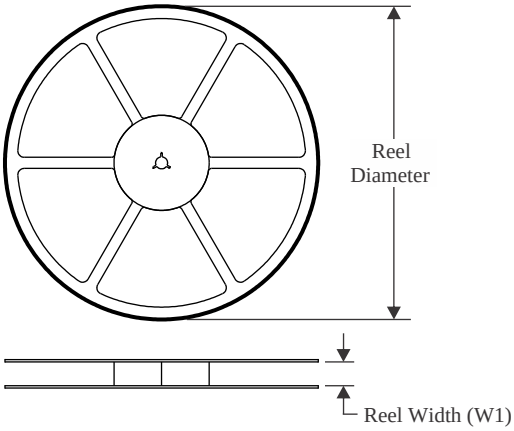
- Catalog : DAC7551

NOTE: Qualified Version Definitions:

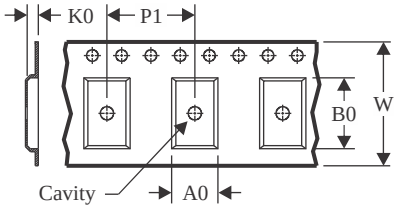
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

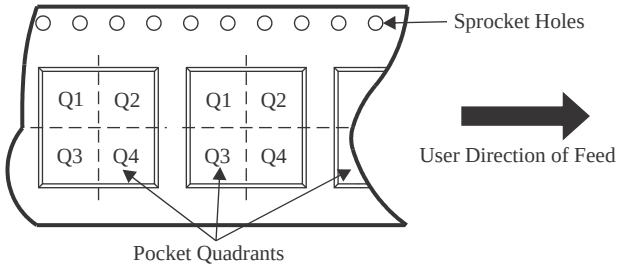


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

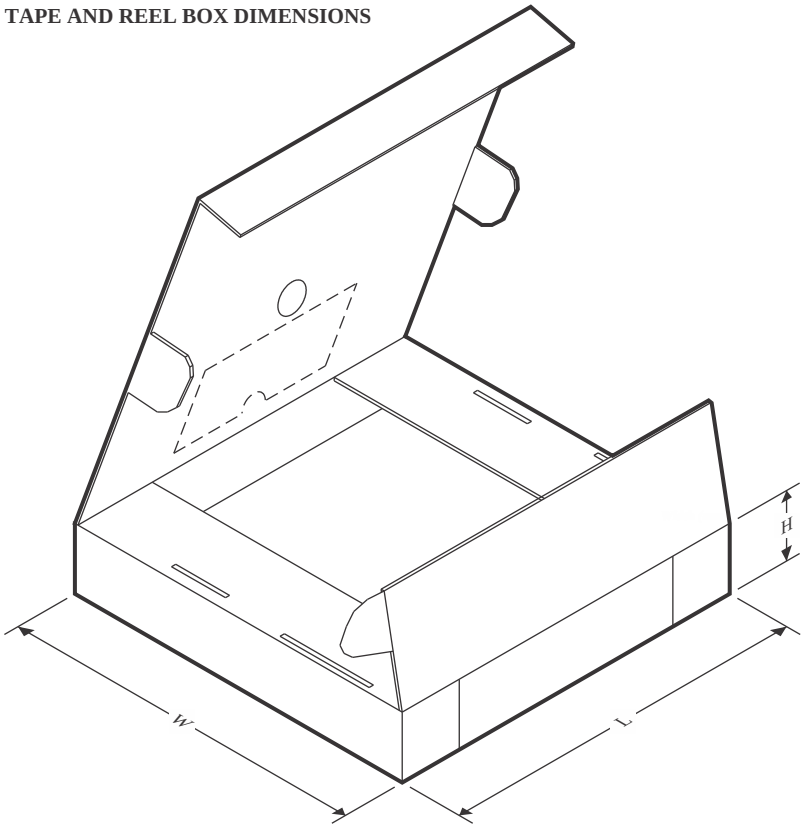
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7551TDRNRQ1	USON	DRN	12	3000	330.0	12.4	2.3	3.3	0.7	4.0	12.0	Q1
DAC7551ZTDRNRQ1	USON	DRN	12	3000	330.0	12.4	2.3	3.3	0.7	4.0	12.0	Q1

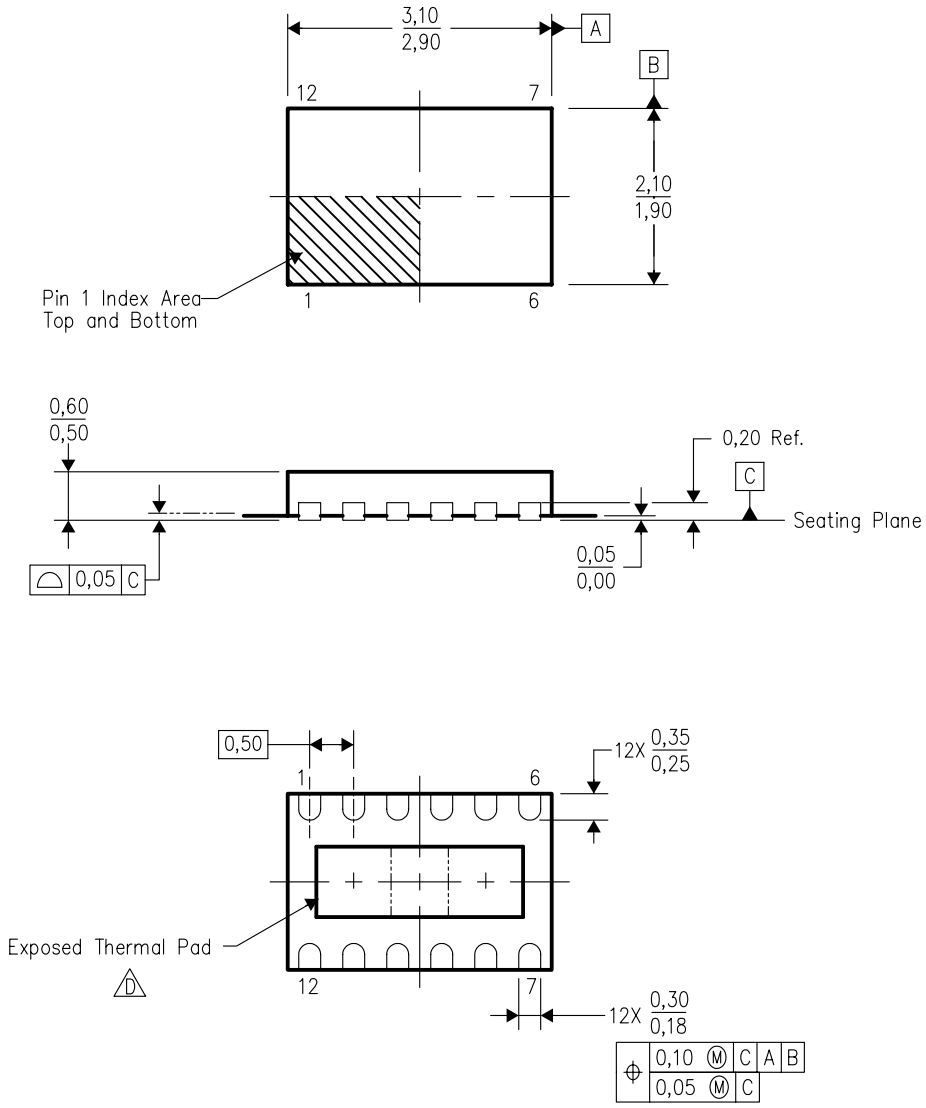
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7551TDRNRQ1	USON	DRN	12	3000	338.0	355.0	50.0
DAC7551ZTDRNRQ1	USON	DRN	12	3000	338.0	355.0	50.0

DRN (R–PDSO–N12) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229.

THERMAL PAD MECHANICAL DATA

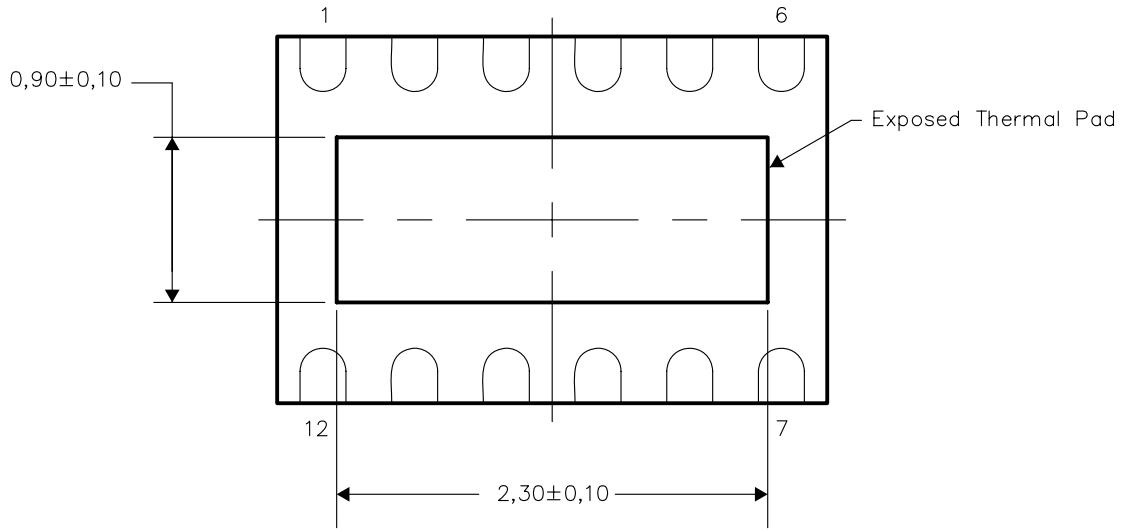
DRN (R–PDSO–N12)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

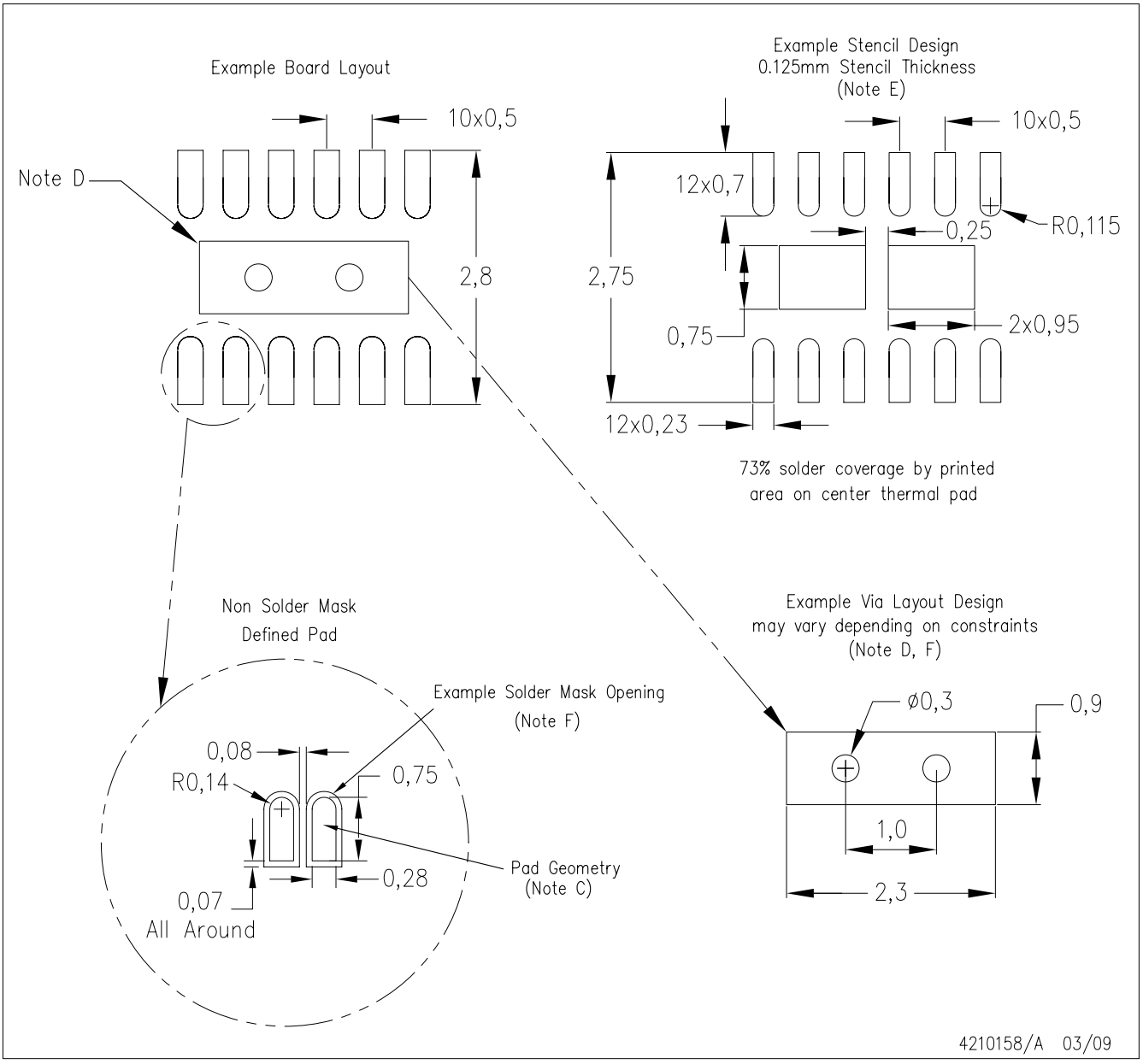


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRN (R–PUSON–N12)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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