DACx300x 带自动检测型 I^{2}C、PMBus™ 或 SPI 接口的 12 位和 10 位超低功率双路和单路电压和电流输出智能 DAC

1 特性

- 具有灵活配置的可编程电压或电流输出：
  - 电压输出：
    - 1LSB INL 和 DNL（10 位）
    - 1x、1.5x、2x、3x 和 4x 增益
  - 电流输出：
    - 1LSB INL 和 DNL（8 位）
    - 25 μA 至 250 μA 的单极和双极输出范围选项
- 电压输出模式具有 35 μA/通道 I_{DD}
- 适合所有通道的可编程比较器模式
- 当 VDD 关闭时提供高阻抗输出
- 高阻抗和电阻下拉断电模式
- 50MHz SPI 兼容型接口
- 自动检测的 I^{2}C、PMBus™ 或 SPI 接口
  - 1.62V V_{IH} (V_{DD} = 5.5V)
- 可配置为多种功能的通用输入/输出 (GPIO)
- 生成预定义的波形：正弦波、余弦波、三角形波、锯齿波
- 用户可编程的非易失性存储器 (NVM)
- 内部、外部或电源作为基准
- 宽工作电压范围：
  - 电源：1.8V 至 5.5V
  - 温度：-40°C 至 +125°C
- 微型封装：16 引脚 WQFN (3mm × 3mm)

2 应用

- 陆地移动无线电
- 脉搏血氧仪
- 光学模块
- 标准笔记本电脑

3 说明

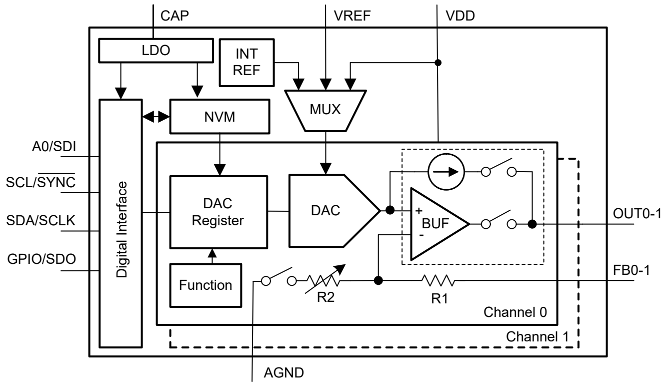
12 位 DAC63001 和 DAC63002 以及 10 - 位 DAC53001 和 DAC53002（统称为 DACx300x）是一系列引脚兼容的超低功耗单通道和双通道缓冲电压输出和电流输出智能数模转换器 (DAC)。这些 DACx300x 器件支持高阻态断电模式，并在断电情况下支持高阻态输出。DAC 输出提供一个强制检测选项，可用作可编程比较器和电流阱。得益于多功能 GPIO、函数生成和 NVM，此类智能 DAC 可用于*无处理器的*应用和设计复用。这些器件自动检测 I^{2}C、PMBus 和 SPI 接口，并包含内部基准。

这些功能集与微型封装和超低功耗相结合，使这些智能 DAC 成为陆地移动无线电、脉搏血氧仪、笔记本电脑和其他电池供电应用的理想选择，以实现偏置、校准和波形生成。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
DACx3001	WQFN (16)	3.00mm x 3.00mm
DACx3002		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版方框图

English Data Sheet: SLASF48

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
May 2022	*	Initial Release

5 Pin Configuration and Functions

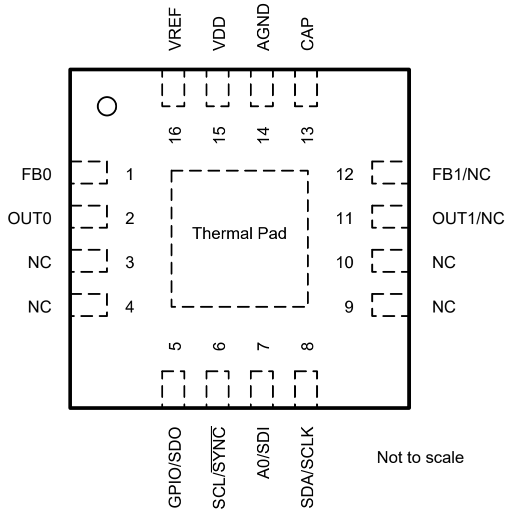


图 5-1. RTE Package, 16-pin WQFN, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	FB0	Input	Voltage feedback pin for channel 0. In voltage-output mode, connect to OUT0 for closed-loop amplifier output. In current-output mode, keep the FB0 pin unconnected to minimize leakage current.
2	OUT0	Output	Analog output voltage from DAC channel 0.
3	NC	NC	No connection. Leave this pin unconnected.
4	NC	NC	No connection. Leave this pin unconnected.
5	GPIO/SDO	Input/Output	General-purpose input/output configurable as $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{PROTECT}}$, $\overline{\text{RESET}}$, SDO, and $\overline{\text{STATUS}}$. For $\overline{\text{STATUS}}$ and SDO, connect the pin to the IO voltage with an external pullup resistor. If unused, connect the GPIO pin to VDD or AGND using an external resistor. This pin can ramp up before VDD.
6	SCL/$\overline{\text{SYNC}}$	Output	I^{2}C serial interface clock or SPI chip select input. This pin must be connected to the IO voltage using an external pullup resistor. This pin can ramp up before VDD.
7	A0/SDI	Input	Address configuration pin for I^{2}C or serial data input for SPI. For A0, connect this pin to VDD, AGND, SDA, or SCL for address configuration (节 7.5.2.2.1). For SDI, this pin need not be pulled up or pulled down. This pin can ramp up before VDD.
8	SDA/SCLK	Input/Output	Bidirectional I^{2}C serial data bus or SPI clock input. This pin must be connected to the IO voltage using an external pullup resistor in the I^{2}C mode. This pin can ramp up before VDD.
9	NC	NC	No connection. Leave this pin unconnected.
10	NC	NC	No connection. Leave this pin unconnected.
11	OUT1/NC	Output/NC	DAC63002 and DAC53002: Analog output voltage from DAC channel 1. DAC63001 and DAC53001: No connection. Leave this pin unconnected.
12	FB1/NC	Input/NC	DAC63002 and DAC53002: Voltage feedback pin for channel 1. In voltage-output mode, connect to OUT1 for closed-loop amplifier output. In current-output mode, keep the FB0 pin unconnected to minimize leakage current. DAC63001 and DAC53001: No-connect. Leave this pin unconnected.
13	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
14	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	Power	Supply voltage.
16	VREF	Power	External reference input. Connect a capacitor (approximately 0.1 µF) between VREF and AGND. Use a pullup resistor to VDD when the external reference is not used. This pin must not ramp up before VDD. In case an external reference is used, make sure the reference ramps up after VDD.

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
Thermal pad	Thermal Pad	Ground	Connect the thermal pad to AGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to A_{GND}	–0.3	6	V
	Digital inputs to A_{GND}	–0.3	V_{DD} + 0.3	V
	CAP to A_{GND}	–0.3	1.65	V
	V_{FBX} to A_{GND}	–0.3	V_{DD} + 0.3	V
	V_{OUTX} to A_{GND}	–0.3	V_{DD} + 0.3	V
V_{REF}	External reference, V_{REF} to A_{GND}	–0.3	V_{DD} + 0.3	V
	Current into any pin except the OUTx pins	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (A_{GND})	1.7		5.5	V
V_{REF}	External reference to ground (A_{GND})	1.7		V_{DD}	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
C_{CAP}	External capacitor on CAP pin	0.5		15	µF
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DACx300x	UNIT
		RTE (WQFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W

THERMAL METRIC(1)		DACx300x	UNIT
		RTE (WQFN)	
		16 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report.*

6.5 Electrical Characteristics: Voltage Output

at 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), digital inputs at VDD or AGND, all minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C, and typical specifications at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC63002, DAC63001	12			Bits
		DAC53002, DAC53001	10			
INL	Integral nonlinearity(1)	DAC63002, DAC63001	–4		4	LSB
		DAC53002, DAC53001	–1		1	
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero-code error(4)	Code 0d into DAC, external reference, V_{DD} = 5.5 V		6	12	mV
		Code 0d into DAC, internal V_{REF}, gain = 4x, V_{DD} = 5.5 V		6	15	
	Zero-code error temperature coefficient(4)	Code 0d into DAC		±10		µV/°C
	Offset error(4) (6)	1.7 V ≤ V_{DD} < 2.7 V, FBx pin shorted to OUTx, DAC code: 32d for 12-bit resolution, 8d for 10-bit resolution	–0.75	0.3	0.75	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, FBx pin shorted to OUTx, DAC code: 32d for 12-bit resolution, 8d for 10-bit resolution	–0.5	0.25	0.5	
	Offset-error temperature coefficient(4)	FBx pin shorted to OUTx, DAC code: 32d for 12-bit resolution, 8d for 10-bit resolution		±0.0003		%FSR/°C
	Gain error(4)	Between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution	–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(4)	Between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution		±0.0008		%FSR/°C
	Full-scale error(4) (6)	1.7 V ≤ V_{DD} < 2.7 V, DAC at full-scale	–1		1	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, DAC at full-scale	–0.5		0.5	
	Full-scale-error temperature coefficient(4)	DAC at full-scale		±0.0008		%FSR/°C
OUTPUT						
	Output voltage	Reference tied to V_{DD}	0		V_{DD}	V
C_L	Capacitive load(2)	R_L = infinite, phase margin = 30°			200	pF
		Phase margin = 30°			1000	
	Short-circuit current	V_{DD} = 1.7 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		15		mA
		V_{DD} = 2.7 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		50		
		V_{DD} = 5.5 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		60		
	Output-voltage headroom(2)	To V_{DD} (DAC output unloaded, internal reference = 1.21 V), V_{DD} ≥ 1.21 V × gain + 0.2 V	0.2			V
		To V_{DD} and A_{GND} (DAC output unloaded, external reference at V_{DD}, gain = 1x, the VREF pin is not shorted to VDD)	0.8			%FSR
		To V_{DD} and A_{GND} (I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V), external reference at V_{DD}, gain = 1x, the VREF pin is not shorted to VDD	10			
Z_O	V_{FB} dc output impedance(3)	DAC output enabled, internal reference (gain = 1.5x or 2x) or external reference at V_{DD} (gain = 1x), the VREF pin is not shorted to VDD	400	500	600	kΩ
		DAC output enabled, internal V_{REF}, gain = 3x or 4x	325	400	485	
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2x, DAC at midscale, V_{DD} = 5 V ±10%		0.25		mV/V

6.5 Electrical Characteristics: Voltage Output (continued)

at 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), digital inputs at VDD or AGND, all minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C, and typical specifications at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		20		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4x		25		
	Slew rate	V_{DD} = 5.5 V		0.3		V/µs
	Power-on glitch magnitude	At startup (DAC output disabled)		75		mV
		At startup (DAC output disabled), R_L = 100 kΩ		200		
	Output-enable glitch magnitude	DAC output disabled to enabled (DAC registers at zero scale), R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		50		μV_{PP}
		Internal V_{REF}, gain = 4x, f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		90		
	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.35		$\mu V/\sqrt{Hz}$
		Internal V_{REF}, gain = 4x, f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.9		
	Power supply rejection ratio (ac)(3)	Internal V_{REF}, gain = 4x, 200-mV 50-Hz or 60-Hz sine wave superimposed on power supply voltage, DAC at midscale		-68		dB
	Code change glitch impulse	±1-LSB change around midscale (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1-LSB change around midscale (including feedthrough)		15		mV
POWER						
I_{DD}	Current flowing into VDD(4) (5)	Normal operation, DACs at full scale, digital pins static, external reference at V_{DD} but the VREF pin is not shorted to VDD		35	50	µA/ch

(1) Measured with DAC output unloaded. For external reference and internal reference V_{DD} ≥ 1.21 x gain + 0.2 V, between end-point codes: 32d to 4064d for 12-bit resolution, 8d to 1016d for 10-bit resolution.
(2) Specified by design and characterization, not production tested.
(3) Specified with 200-mV headroom with respect to reference value when internal reference is used.
(4) Measured with DAC output unloaded.
(5) The total power consumption is calculated by I_{DD} x (total number of channels powered on) + (sleep-mode current).
(6) When a DAC channel is configured in IOUT mode for long term and then switched to VOUT mode, the VOUT mode can show parametric drift.

6.6 Electrical Characteristics: Current Output

at 1.7 V $\leqslant V_{DD} \leqslant$ 5.5 V, ±250-µA output range, digital inputs at VDD or AGND, all minimum and maximum specifications at –40°C $\leqslant T_A \leqslant$ +125°C, and typical specifications at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		8			Bits
INL	Integral nonlinearity	DAC codes between 10d and 255d for current output range of 0 µA to 25 µA, DAC codes between 0d and 255d for other ranges	–1		1	LSB
DNL	Differential nonlinearity	DAC codes between 10d and 255d for current output range of 0 µA to 25 µA, DAC codes between 0d and 255d for other ranges	–1		1	LSB
	Offset error	DAC output range: 0 µA to 25 µA, DAC at code 10d		±1.5		%FSR
		DAC output ranges: 0 µA to 50 µA, 0 µA to 125 µA, and 0 µA to 250 µA; DAC at zero-scale		5		
		all unipolar negative ranges, DAC at zero-scale		-5		
		DAC output ranges: ±25 µA, ±50 µA, ±125 µA, and ±250 µA; DAC at midscale		±1		
	Gain error	DAC output range: 0 µA to 25 µA, DAC codes between 10d and 255d		±1.5		%FSR
		DAC output ranges: 0 µA to 50 µA, 0 µA to 125 µA, and 0 µA to 250 µA; DAC codes between 0d and 255d		±1.5		
		all unipolar negative ranges, DAC codes between 0d and 255d		±5		
		DAC output ranges: ±25 µA, ±50 µA, ±125 µA, and ±250 µA; DAC codes between 0d and 255d		±1.3		
OUTPUT						
	Output compliance voltage(1)	DAC output range: 0 µA to 25 µA, to V_{DD} and to A_{GND}	200			mV
		DAC output ranges: 0 µA to 50 µA, 0 µA to 125 µA, and 0 µA to 250 µA; to V_{DD}	400			
		all unipolar negative ranges, to V_{DD}	400			
		DAC output ranges: ±25 µA, ±50 µA, ±125 µA, and ±250 µA; to V_{DD} and to AGND	400			
Z_O	I_{OUT} dc output impedance(2)	DAC at midscale, DAC output kept at $V_{DD}/2$	60			MΩ
	Power supply rejection ratio (dc)	DAC at midscale, output range: 0 µA to 25 µA, V_{DD} changed from 4.5 V to 5.5 V		0.28		LSB/V
		DAC at midscale, all unipolar positive ranges, V_{DD} changed from 4.5 V to 5.5 V		0.33		
		DAC at midscale, all unipolar negative ranges, V_{DD} changed from 4.5 V to 5.5 V		0.83		
		DAC at midscale, all bipolar ranges, V_{DD} changed from 4.5 V to 5.5 V		0.23		
DYNAMIC PERFORMANCE						
t_{sett}	Output current settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 1 LSB at 8-bit resolution, V_{DD} = 5.5 V, common-mode voltage at OUTx pin is $V_{DD}/2$		60		µs
V_n	Output noise current (peak to peak)	0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V, ±250-µA output range		150		nA_{PP}
	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V, ±250-µA output range		1		$nA/\sqrt{Hz}$
	Power supply rejection ratio (ac)(3)	±250-µA output range, 200-mV 50-Hz or 60-Hz sine wave superimposed on power-supply voltage, DAC at midscale		0.65		LSB/V

6.6 Electrical Characteristics: Current Output (continued)

at 1.7 V ⩽ V_{DD} ⩽ 5.5 V, ±250-μA output range, digital inputs at VDD or AGND, all minimum and maximum specifications at –40°C ⩽ T_A ⩽ +125°C, and typical specifications at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{DD}	Current flowing into VDD(3) (4)	Normal operation, DACs at midscale, all unipolar output ranges, digital pins static		18	24	μA/ch
		Normal operation, DACs at full scale, ±25-μA output range, digital pins static		42	50	
		Normal operation, DACs at full scale, ±50-μA output range, digital pins static		56	70	
		Normal operation, DACs at full scale, ±125-μA output range, digital pins static		98	120	
		Normal operation, DACs at full scale, ±250-μA output range, digital pins static		167	200	

(1) Measured between DAC codes 0d and 255d.
(2) Specified by design and characterization, not production tested.
(3) The current flowing into V_{DD} does not account for the load current sourced or sinked on the OUTx pins. The VREF pin is connected to V_{DD}.
(4) The total power consumption is calculated by I_{DD} x (total number of channels powered on) + (sleep-mode current).

6.7 Electrical Characteristics: Comparator Mode

at 1.7 V ⩽ V_{DD} ⩽ 5.5 V, DAC reference tied to VDD, gain = 1x in voltage output mode, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), digital inputs at VDD or AGND, all minimum and maximum specifications at –40°C ⩽ T_A ⩽ +125°C, and typical specifications at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Offset error(1) (2)	1.7 V ⩽ V_{DD} ⩽ 5.5 V, DAC at midscale, comparator input at Hi-Z, and DAC operating with external reference	–5	0	5	mV
	Offset error time drift(1)	V_{DD} = 5.5 V, external reference, T_A = 125°C, FBx in Hi-Z mode, DAC at full scale and V_{FB} at 0 V or DAC at zero scale and V_{FB} at 1.84 V, drift specified for 10 years of continuous operation		4		mV
OUTPUT						
	Input voltage	VREF connected to VDD, FBx resistor network connected to ground	0		V_{DD}	V
		VREF connected to VDD, FBx resistor network disconnected from ground	0		V_{DD} (1/3 – 1/100)	
V_{OL}	Logic low output voltage	I_{LOAD} = 100 μA, output in open-drain mode		0.1		V
DYNAMIC PERFORMANCE						
t_{resp}	Output response time	DAC at midscale with 10-bit resolution, FBx input at Hi-Z, and transition step at FBx node is (V_{DAC} – 2 LSB) to (V_{DAC} + 2 LSB), transition time measured between 10% and 90% of output, output current of 100 μA, comparator output configured in push-pull mode, load capacitor at DAC output is 25 pF		10		μs

(1) Specified by design and characterization, not production tested.
(2) This specification does not include the total unadjusted error (TUE) of the DAC.

6.8 Electrical Characteristics: General

at 1.7 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x in voltage output mode or ±250-μA output range in current output mode, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) in voltage-output mode and capacitive load (C_L = 200 pF to AGND), digital inputs at VDD or AGND, all minimum and maximum specifications at –40°C ≤ T_A ≤ +125°C, and typical specifications at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	T_A = 25°C	1.1979	1.212	1.224	V
	Reference output temperature coefficient(1) (2)				50	ppm/°C
EXTERNAL REFERENCE						
	V_{REF} input impedance(1) (3)			192		kΩ/ch
EEPROM						
	Endurance(1)	–40°C ≤ T_A ≤ +85°C		20000		Cycles
		T_A = 125°C		1000		
	Data retention(1)	T_A = 25°C		50		Years
	EEPROM programming write cycle time(1)				200	ms
	Device boot-up time(1)	Time taken from power valid (V_{DD} ≥ 1.7 V) to output valid state (output state as programmed in EEPROM), 0.5-μF capacitor on the CAP pin		5		ms
DIGITAL INPUTS						
	Digital feedthrough	Voltage output mode, DAC output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER-DOWN MODE						
I_{DD}	Current flowing into VDD(1)	DAC in sleep mode, internal reference powered down, external reference at 5.5 V			28	μA
		DAC in sleep mode, internal reference enabled, additional current through internal reference		10		
		DAC channels enabled, internal reference enabled, additional current through internal reference per DAC channel in voltage-output mode		12.5		
	Current flowing into VDD	DAC in deep-sleep mode, internal reference powered down, SDO mode disabled		1.5	3	
HIGH-IMPEDANCE OUTPUT						
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	DAC in Hi-Z output mode, 1.7 V ≤ V_{DD} ≤ 5.5 V		10		nA
		V_{DD} = 0 V, V_{OUT} ≤ 1.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 μF		200		
		V_{DD} = 0 V, 1.5 V < V_{OUT} ≤ 5.5 V, decoupling capacitor between V_{DD} and AGND = 0.1 μF		500		
		100 kΩ between V_{DD} and AGND, V_{OUT} ≤ 1.25 V, series resistance of 10 kΩ at OUTx pin		±2		μA

(1) Specified by design and characterization, not production tested.
(2) Measured at –40°C and +125°C and calculated the slope.
(3) Impedances for the DAC channels are connected in parallel.

6.9 Timing Requirements: I^2C Standard Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, –40°C ⩽ T_A ⩽ +125°C, and 1.7 V ⩽ $V_{pull-up}$ ⩽ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			μs
t_{HDSTA}	Hold time after repeated start	4			μs
t_{SUSTA}	Repeated start setup time	4.7			μs
t_{SUSTO}	Stop condition setup time	4			μs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns
t_{VD_DAT}	Data valid time			3.45	μs
t_{VD_ACK}	Data valid acknowledge time			3.45	μs

6.10 Timing Requirements: I^2C Fast Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, –40°C ⩽ T_A ⩽ +125°C, and 1.7 V ⩽ $V_{pull-up}$ ⩽ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			400	kHz
t_{BUF}	Bus free time between stop and start conditions	1.3			μs
t_{HDSTA}	Hold time after repeated start	0.6			μs
t_{SUSTA}	Repeated start setup time	0.6			μs
t_{SUSTO}	Stop condition setup time	0.6			μs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns
t_{VD_DAT}	Data valid time			0.9	μs
t_{VD_ACK}	Data valid acknowledge time			0.9	μs

6.11 Timing Requirements: I^2C Fast Mode Plus

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, –40°C ⩽ T_A ⩽ +125°C, and 1.7 V ⩽ $V_{pull-up}$ ⩽ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			μs
t_{HDSTA}	Hold time after repeated start	0.26			μs
t_{SUSTA}	Repeated start setup time	0.26			μs
t_{SUSTO}	Stop condition setup time	0.26			μs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			μs
t_{HIGH}	SCL clock high period	0.26			μs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns

all input signals are timed from VIL to 70% of $V_{pull-up}$, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, –40°C ⩽ T_A ⩽ +125°C, and 1.7 V ⩽ $V_{pull-up}$ ⩽ V_{DD} V

		MIN	NOM	MAX	UNIT
t_{VD_DAT}	Data valid time			0.45	μs
t_{VD_ACK}	Data valid acknowledge time			0.45	μs

6.12 Timing Requirements: SPI Write Operation

all input signals are specified with t_r = t_f = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ⩽ V_{IO} ⩽ 5.5 V, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, and –40°C ⩽ T_A ⩽ +125°C

		MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	9			ns
$t_{SCLKLOW}$	SCLK low time	9			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{CS}}$ to SCLK falling edge setup time	18			ns
t_{CSH}	SCLK falling edge to $\overline{\text{CS}}$ rising edge	10			ns
t_{CSHIGH}	$\overline{\text{CS}}$ hight time	50			ns
$t_{DACWAIT}$	Sequential DAC update wait time for same channel	2			μs
$t_{BCASTWAIT}$	Broadcast DAC update wait time	2			μs

6.13 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with t_r = t_f = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ⩽ V_{IO} ⩽ 5.5 V, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, –40°C ⩽ T_A ⩽ +125°C, and FSDO = 0

		MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency			1.25	MHz
$t_{SCLKHIGH}$	SCLK high time	350			ns
$t_{SCLKLOW}$	SCLK low time	350			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	400			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	400			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ hight time	1			μs
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ⩽ 5 mA, C_L = 20 pF.			300	ns

6.14 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with t_r = t_f = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ⩽ V_{IO} ⩽ 5.5 V, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, –40°C ⩽ T_A ⩽ +125°C, and FSDO = 1

		MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency			2.5	MHz
$t_{SCLKHIGH}$	SCLK high time	175			ns
$t_{SCLKLOW}$	SCLK low time	175			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	300			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	300			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ hight time	1			μs

all input signals are specified with $t_r = t_f = 1$ V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ≤ V_{IO} ≤ 5.5 V, 1.7 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and FSDO = 1

		MIN	NOM	MAX	UNIT
t_{SDODLY}	SCLK rising edge to SDO falling edge, I_{OL} ≤ 5 mA, C_L = 20 pF.			300	ns

6.15 Timing Requirements: GPIO

all input signals are specified with $t_r = t_f$ = 1 V/ns (10% to 90% of V_{IO}) and timed from a voltage level of (VIL + VIH) / 2, 1.7 V ⩽ V_{IO} ⩽ 5.5 V, 1.7 V ⩽ V_{DD} ⩽ 5.5 V, and –40°C ⩽ T_A ⩽ +125°C

		MIN	NOM	MAX	UNIT
$t_{GPIHIGH}$	GPI high time(1)	2			µs
t_{GPILOW}	GPI low time(1)	2			µs
t_{GPAWGD}	$\overline{\text{LDAC}}$ falling edge to DAC update delay(2)			2	µs
$t_{CS2LDAC}$	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	1			µs
$t_{STP2LDAC}$	I^2C stop bit rising edge to $\overline{\text{LDAC}}$ falling edge	1			µs
t_{LDACW}	$\overline{\text{LDAC}}$ low time	2			µs

(1) The SCL, SDA, A0, and A1 pins can be configured as GPIOs that perform different channel-specific or independent operations. The actual response time of the GPIO is determined by the delay provided by the configured function and the settling time of the DAC.

(2) The GPIOs can be configured as channel-specific or global $\overline{\text{LDAC}}$ function.

6.16 Timing Diagrams

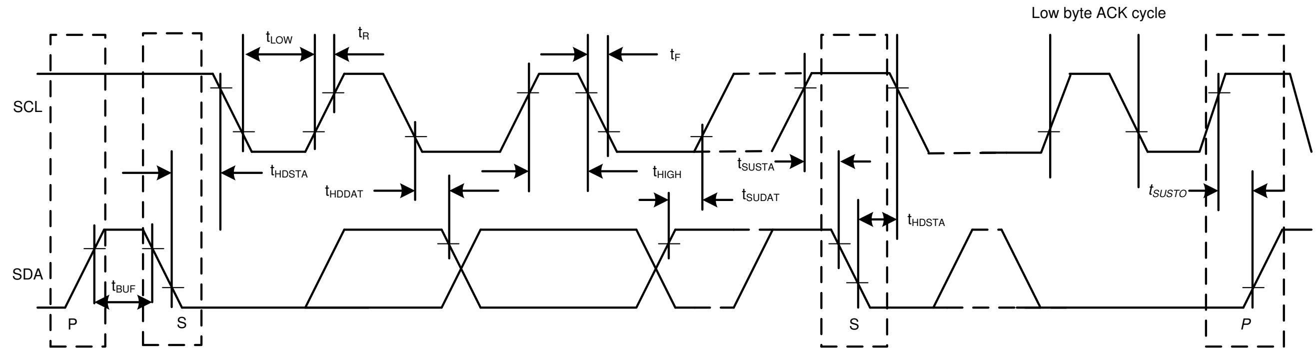


图 6-1. I^2C Timing Diagram

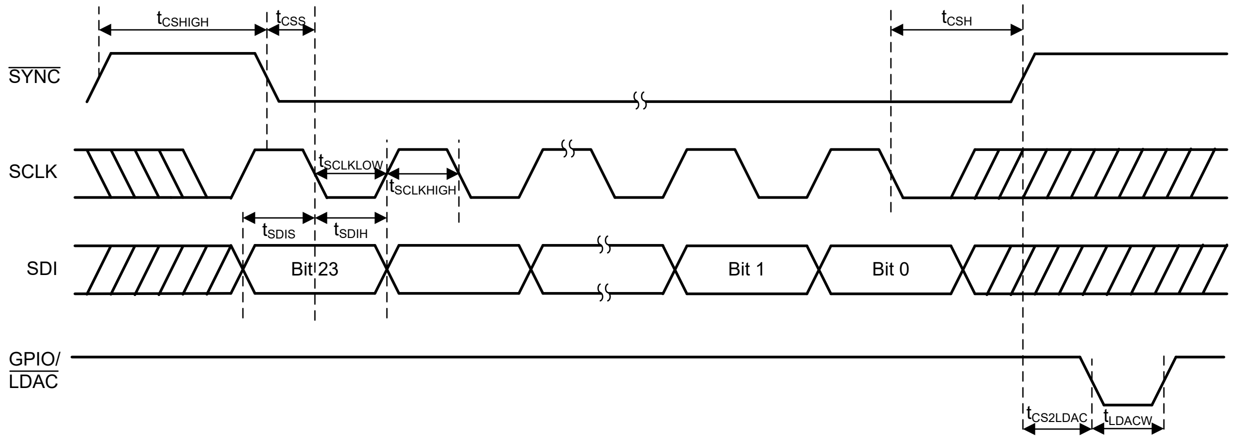


图 6-2. SPI Write Timing Diagram

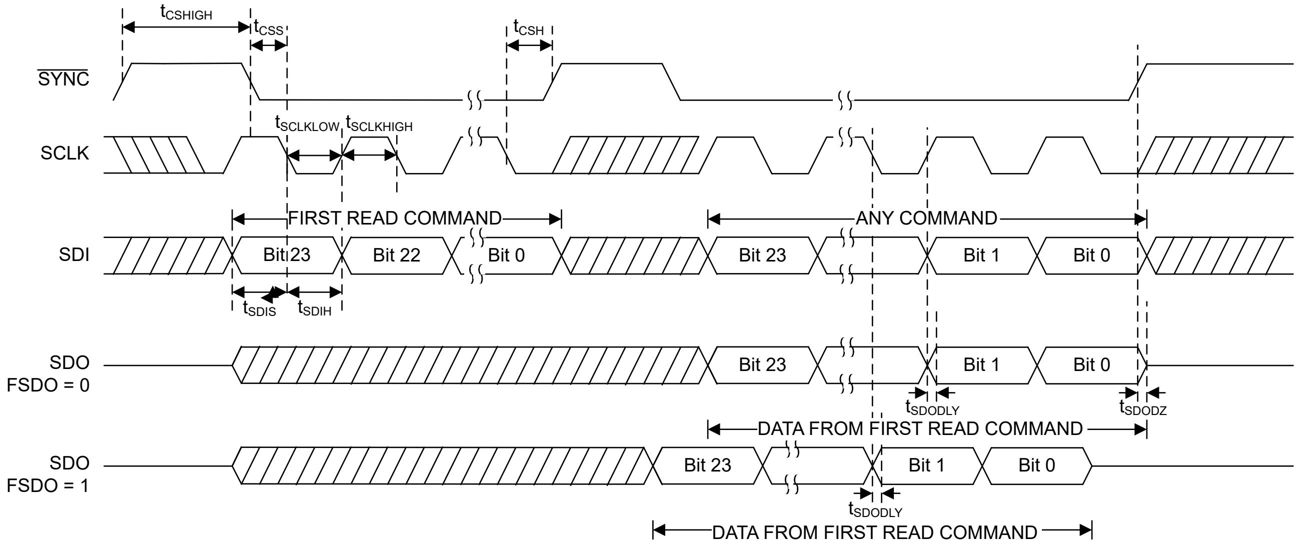
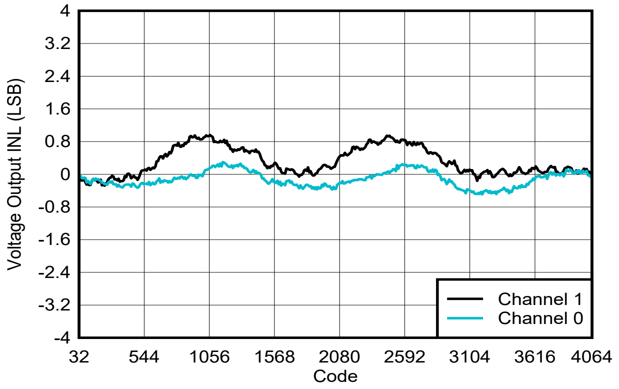


图 6-3. SPI Read Timing Diagram

6.17 Typical Characteristics: Voltage Output

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1x, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



Internal reference, gain = 4x

图 6-4. Voltage Output INL vs Digital Input Code

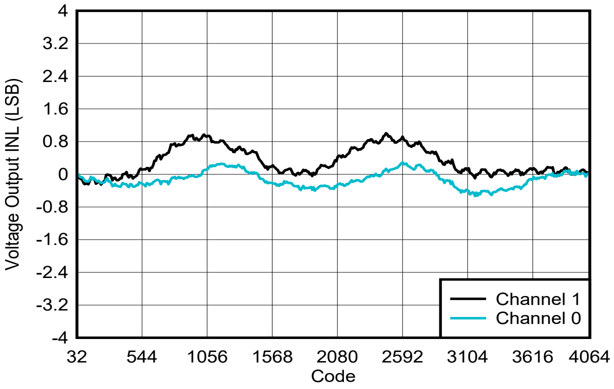


图 6-5. Voltage Output INL vs Digital Input Code

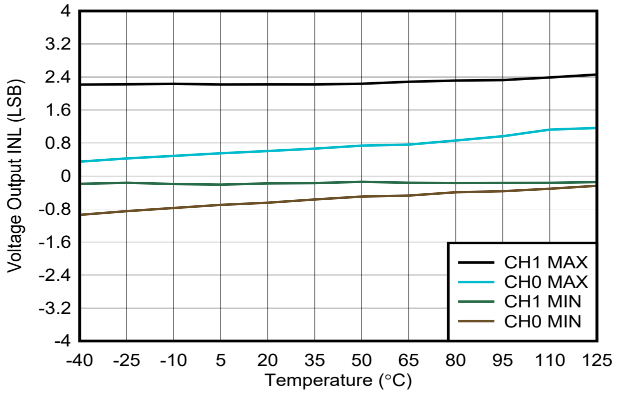


图 6-6. Voltage Output INL vs Temperature

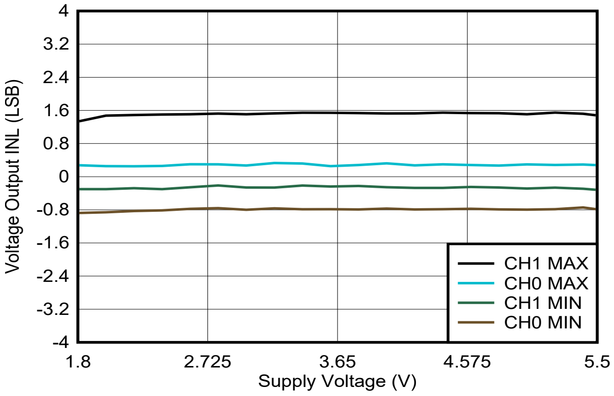
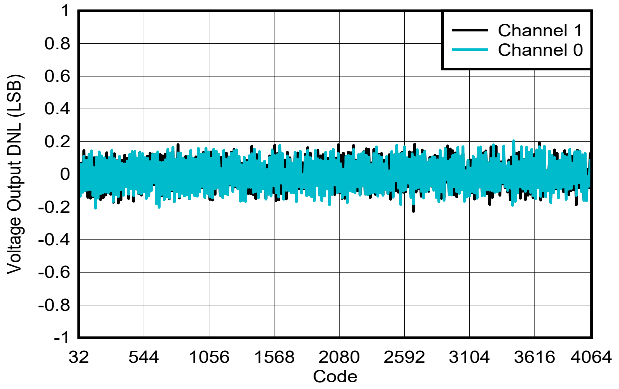


图 6-7. Voltage Output INL vs Supply Voltage



Internal reference, gain = 4x

图 6-8. Voltage Output DNL vs Digital Input Code

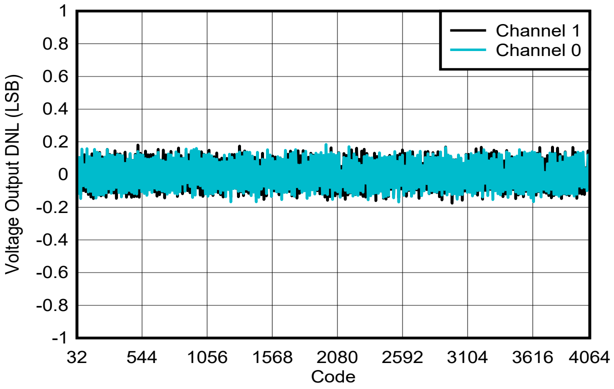


图 6-9. Voltage Output DNL vs Digital Input Code

6.17 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1x, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

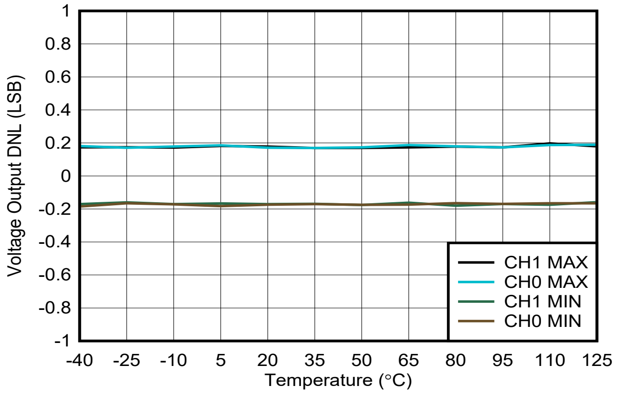


图 6-10. Voltage Output DNL vs Temperature

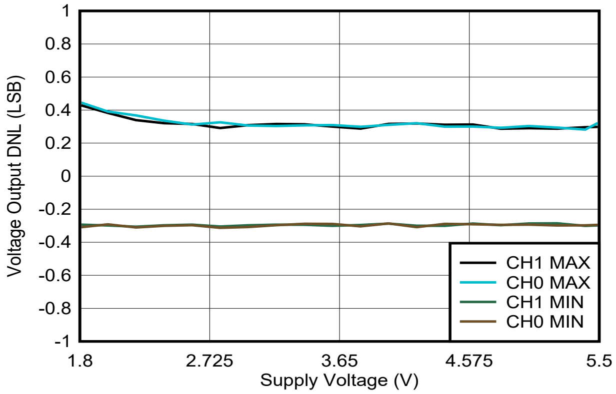
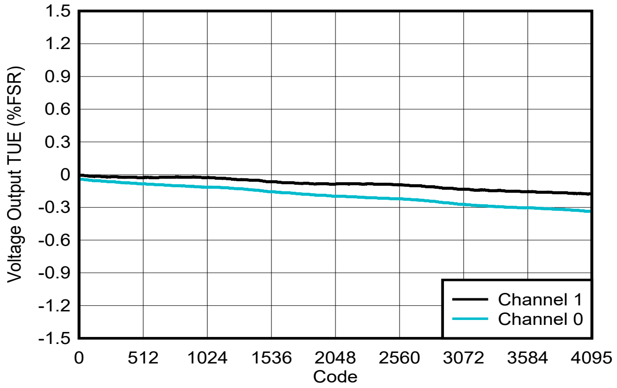


图 6-11. Voltage Output DNL vs Supply Voltage



Internal reference, gain = 4x

图 6-12. Voltage Output TUE vs Digital Input Code

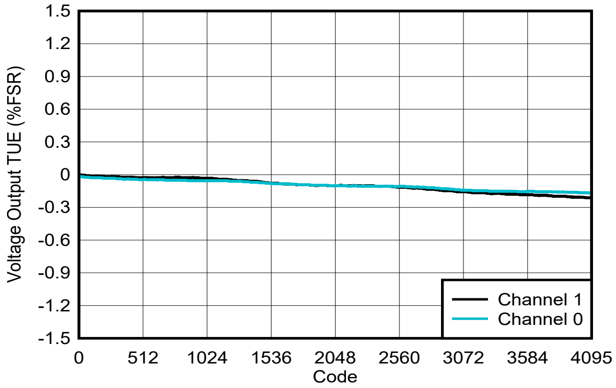
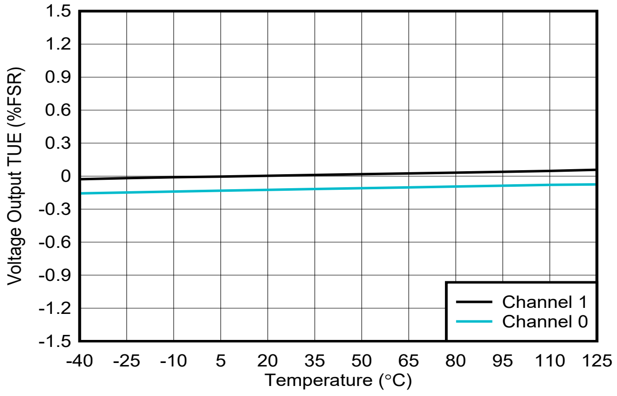
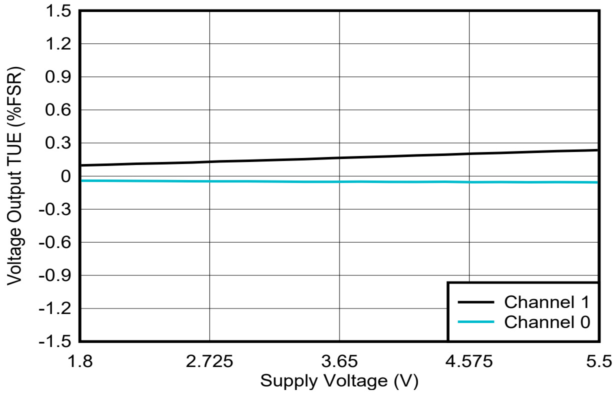


图 6-13. Voltage Output TUE vs Digital Input Code



DAC channels at midscale

图 6-14. Voltage Output TUE vs Temperature



DAC channels at midscale

图 6-15. Voltage Output TUE vs Supply Voltage

6.17 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1x, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)

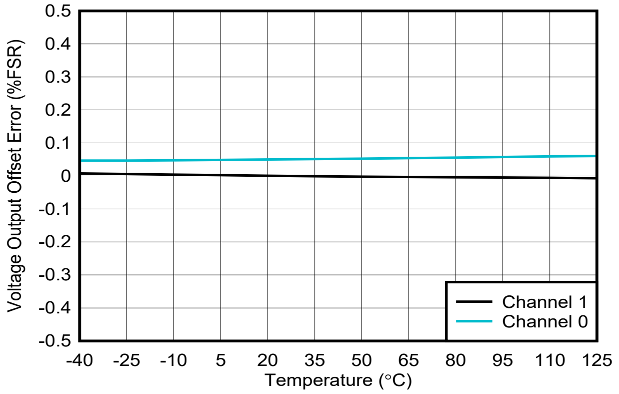


图 6-16. Voltage Output Offset Error vs Temperature

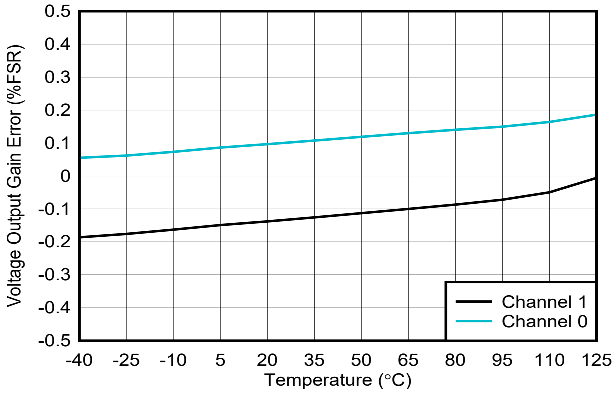
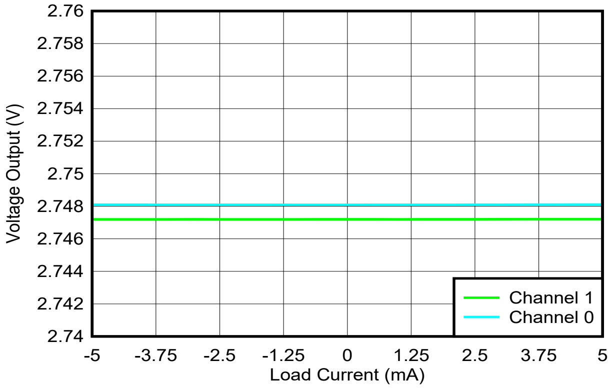


图 6-17. Voltage Output Gain Error vs Temperature



DAC channels at midscale

图 6-18. Voltage Output vs Load Current

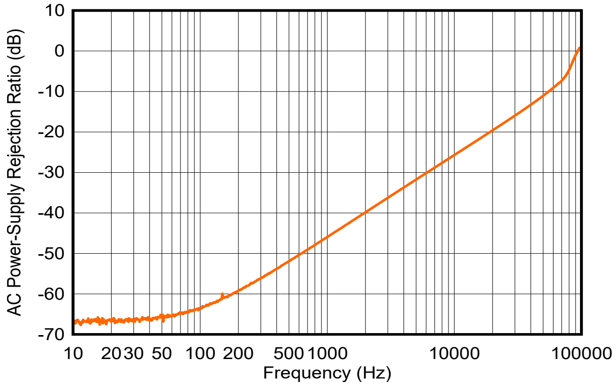


图 6-19. Voltage Output AC PSRR vs Frequency

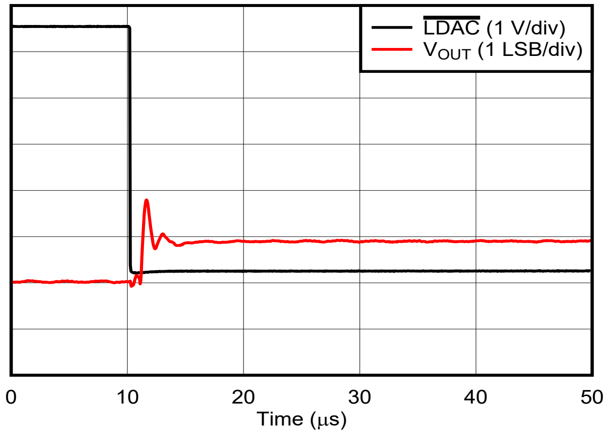


图 6-20. Voltage Output Code-to-Code Glitch - Rising Edge

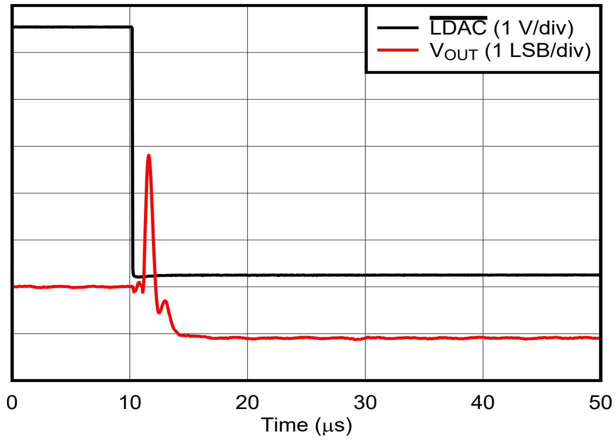
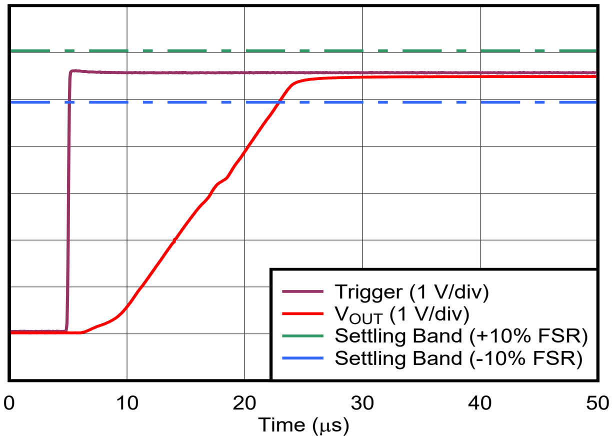


图 6-21. Voltage Output Code-to-Code Glitch - Falling Edge

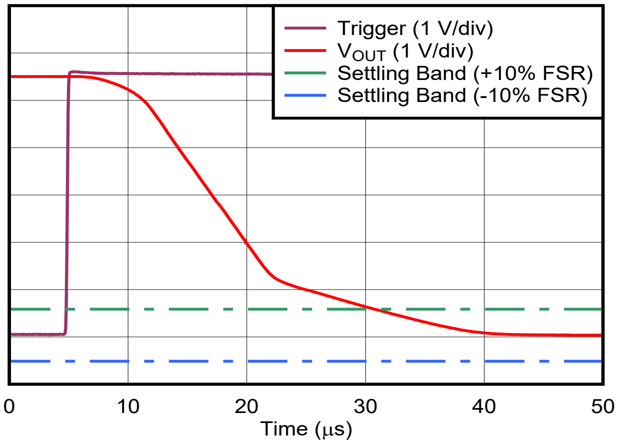
6.17 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1x, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



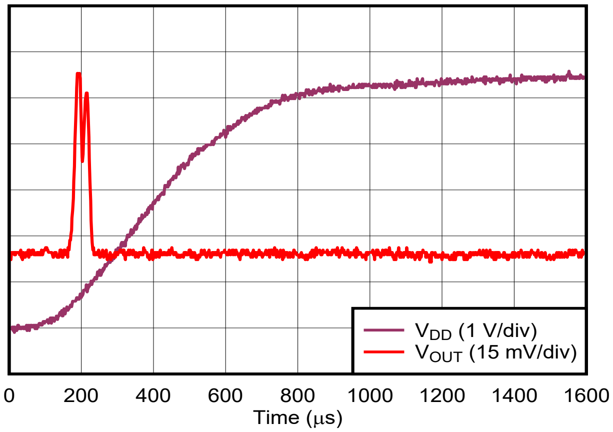
Zero scale to full scale swing

图 6-22. Voltage Output Setting Time - Rising Edge



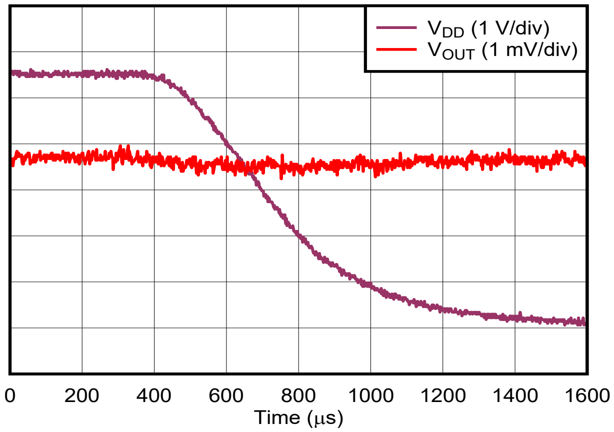
Full scale to zero scale swing

图 6-23. Voltage Output Setting Time - Falling Edge



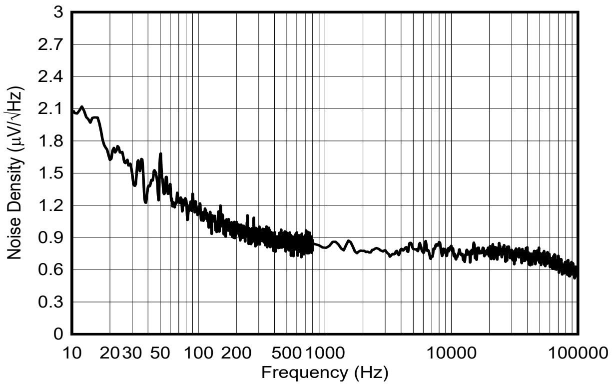
DAC in Hi-Z power-down mode

图 6-24. Voltage Output Power-On Glitch



DAC at zero scale

图 6-25. Voltage Output Power-Off Glitch



Internal reference, gain = 4x

图 6-26. Voltage Output Noise Density

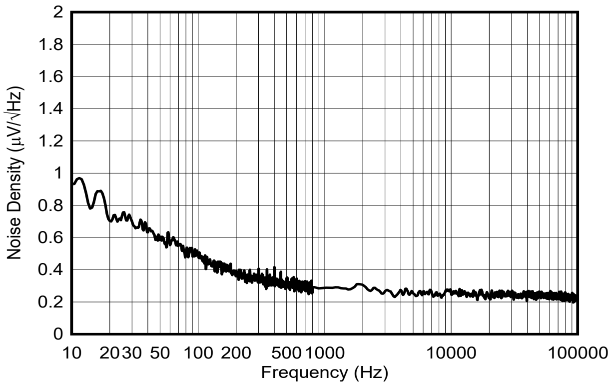
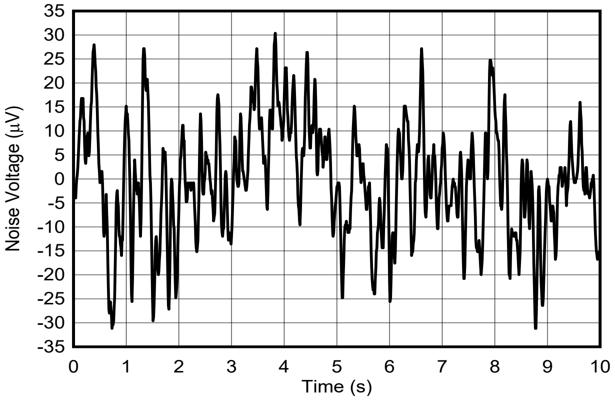


图 6-27. Voltage Output Noise Density

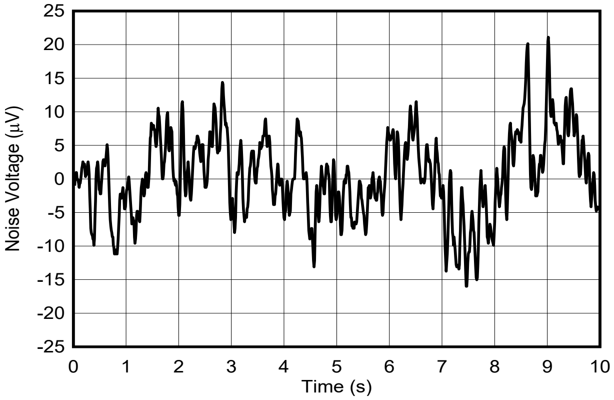
6.17 Typical Characteristics: Voltage Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1x, 12-bit resolution, and DAC outputs unloaded (unless otherwise noted)



Internal reference, gain = 4x, f = 0.1 Hz to 10 Hz

图 6-28. Voltage Output Flicker Noise



f = 0.1 Hz to 10 Hz

图 6-29. Voltage Output Flicker Noise

6.18 Typical Characteristics: Current Output

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 µA (unless otherwise noted)

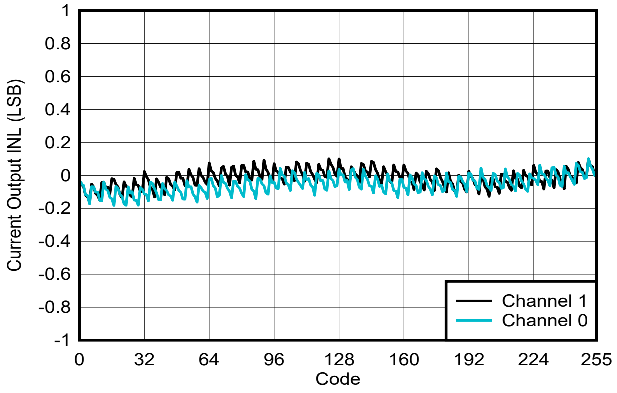
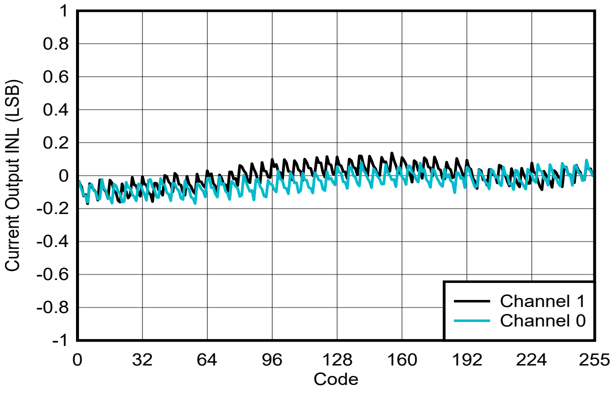
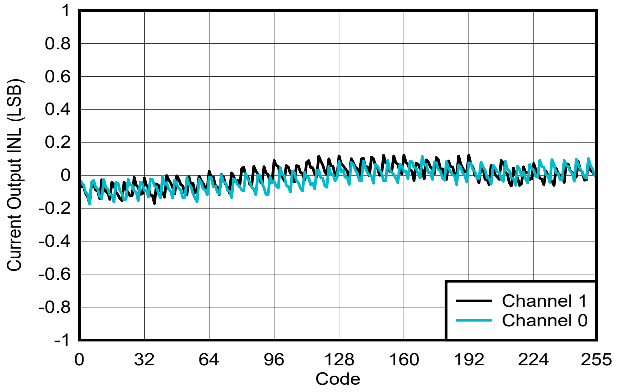


图 6-30. Current Output INL vs Digital Input Code



Output range: 0 µA to 250 µA

图 6-31. Current Output INL vs Digital Input Code



Output range: 0 µA to –240 µA

图 6-32. Current Output INL vs Digital Input Code

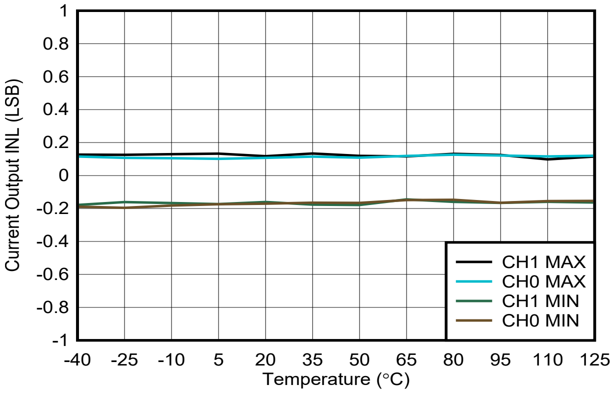


图 6-33. Current Output INL vs Temperature

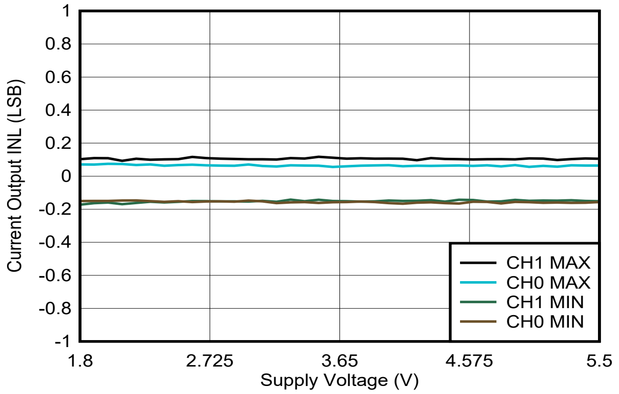


图 6-34. Current Output INL vs Supply Voltage

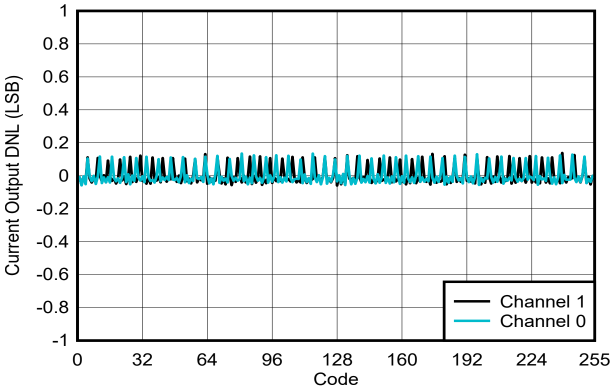
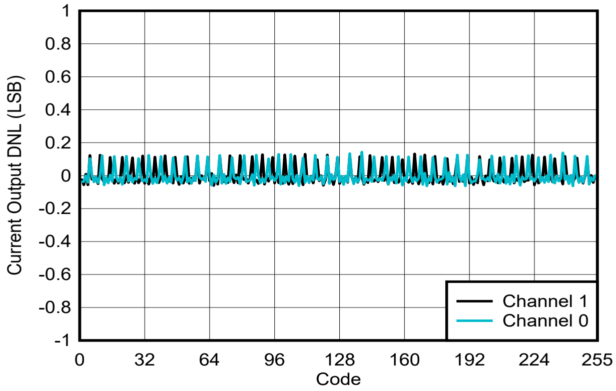


图 6-35. Current Output DNL vs Digital Input Code

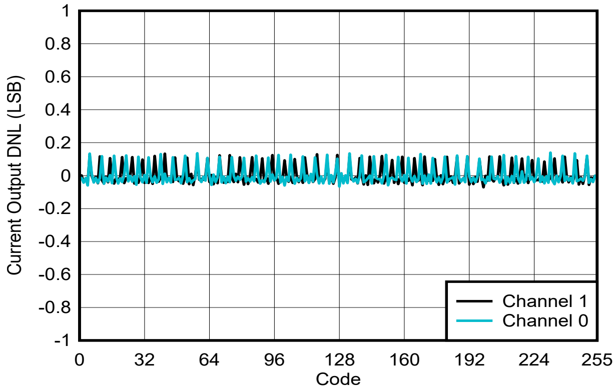
6.18 Typical Characteristics: Current Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 μA (unless otherwise noted)



Output range: 0 μA to 250 μA

图 6-36. Current Output DNL vs Digital Input Code



Output range: 0 μA to – 240 μA

图 6-37. Current Output DNL vs Digital Input Code

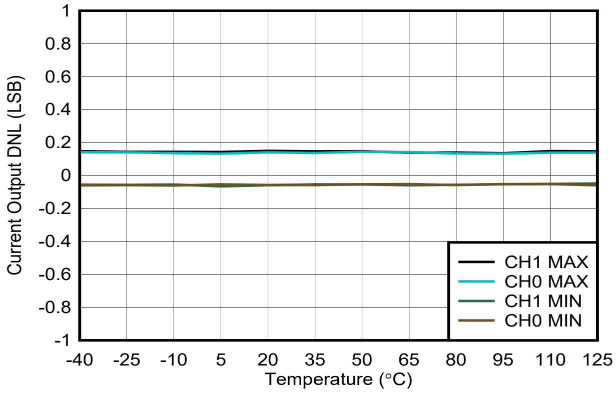


图 6-38. Current Output DNL vs Temperature

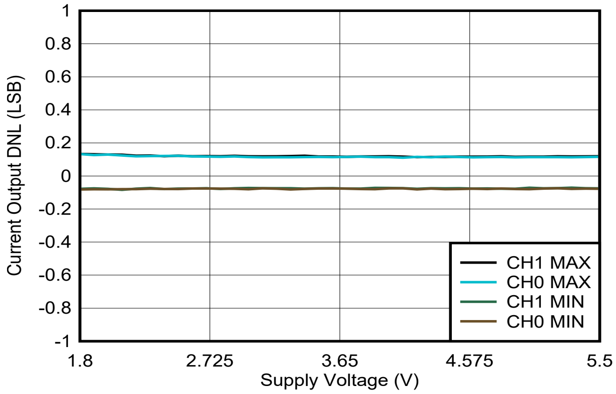


图 6-39. Current Output DNL vs Supply Voltage

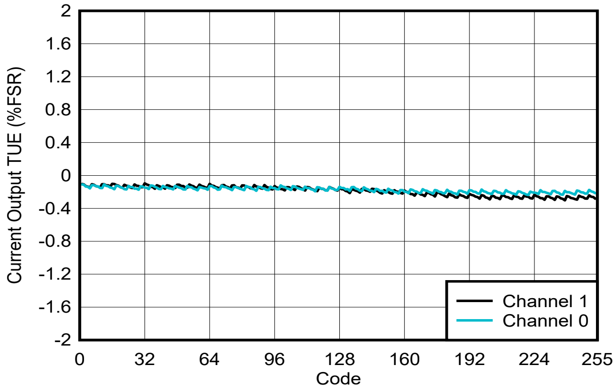
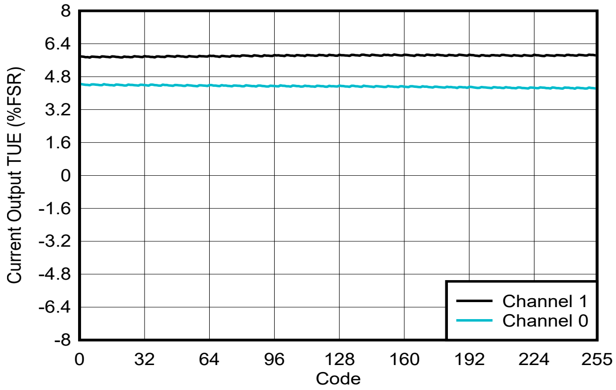


图 6-40. Current Output TUE vs Digital Input Code

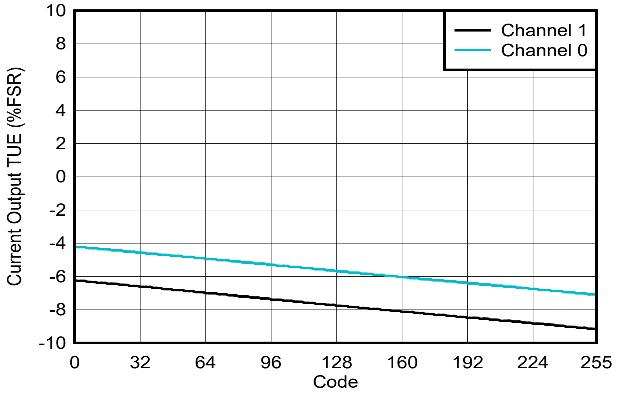


Output range: 0 μA to 250 μA

图 6-41. Current Output TUE vs Digital Input Code

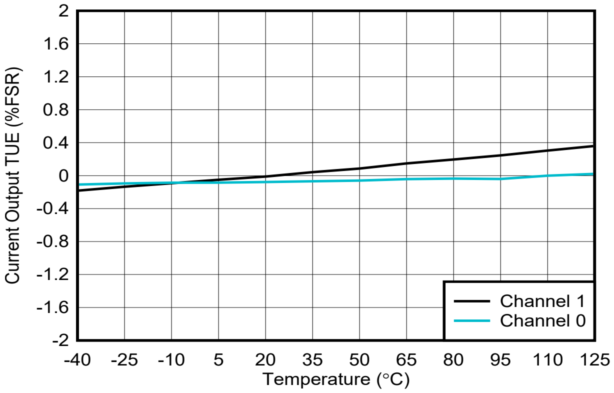
6.18 Typical Characteristics: Current Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 µA (unless otherwise noted)



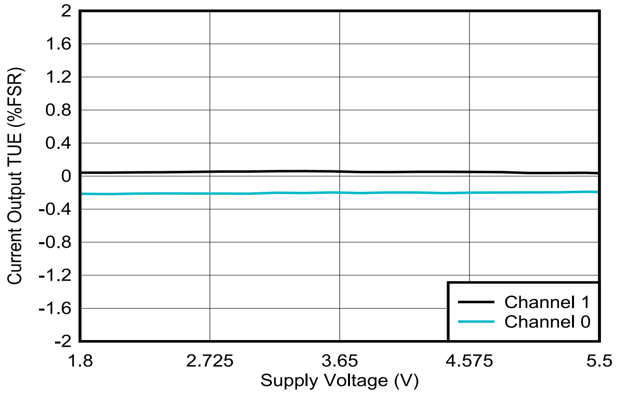
Output range: 0 µA to – 240 µA

图 6-42. Current Output TUE vs Digital Input Code



DAC channels at midscale

图 6-43. Current Output TUE vs Temperature



DAC channels at midscale

图 6-44. Current Output TUE vs Supply Voltage

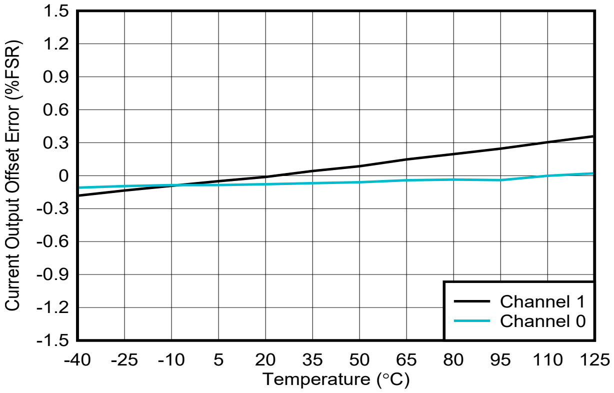


图 6-45. Current Output Offset Error vs Temperature

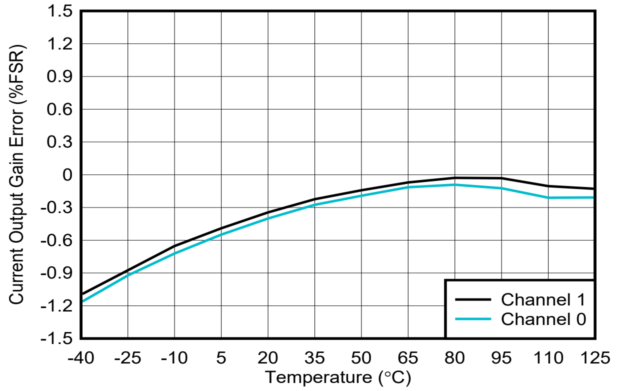


图 6-46. Current Output Gain Error vs Temperature

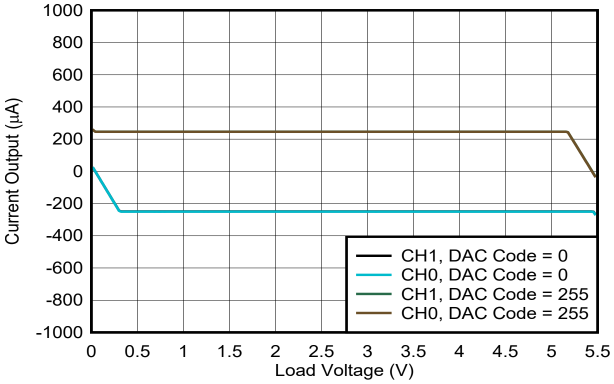


图 6-47. Current Output vs Load Voltage

6.18 Typical Characteristics: Current Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 μA (unless otherwise noted)

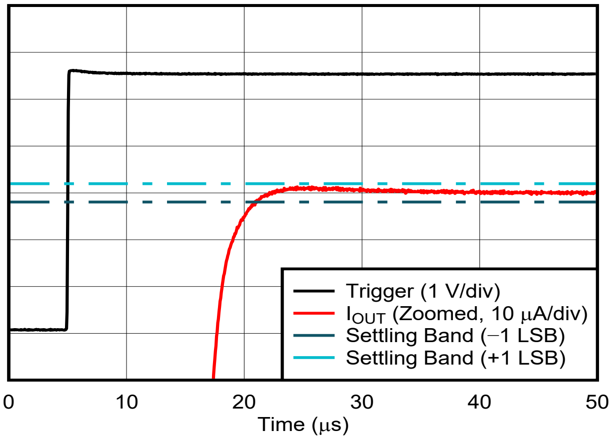


图 6-48. Current Output Setting Time, Rising Edge

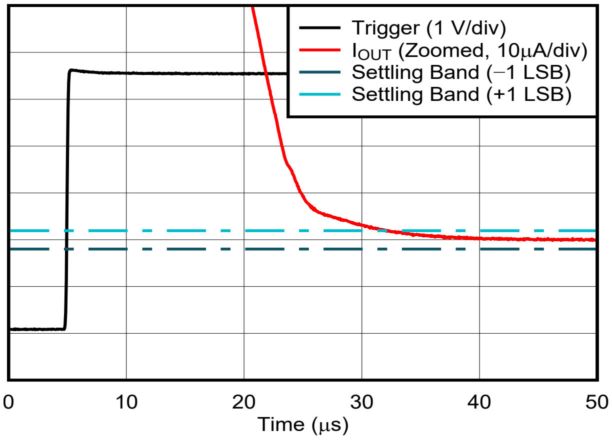
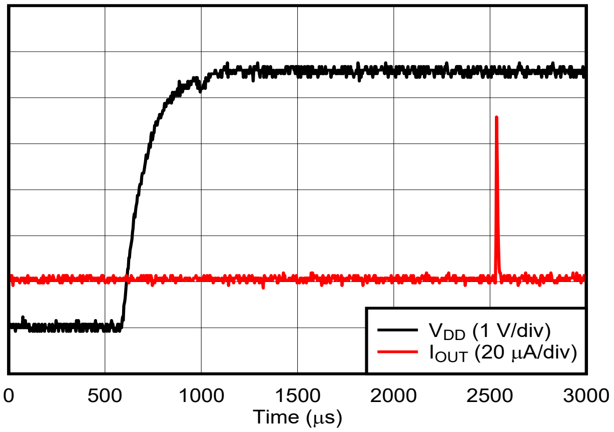
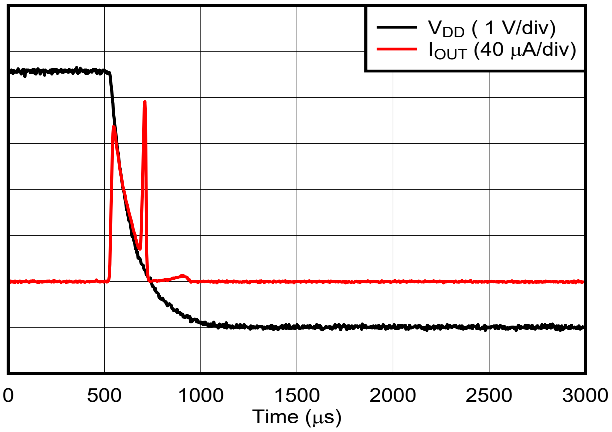


图 6-49. Current Output Setting Time, Falling Edge



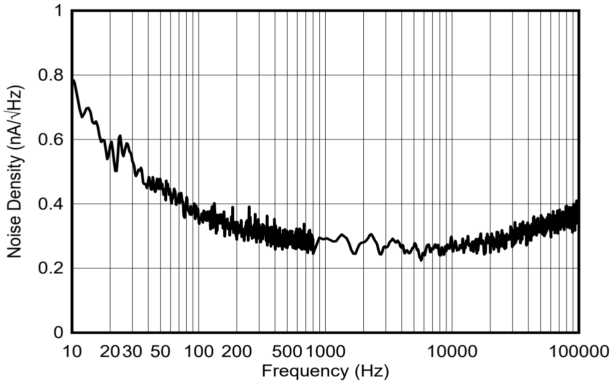
DAC at mid scale (0 μA) stored in EEPROM

图 6-50. Current Output Power-On Glitch



DAC at mid scale (0 μA)

图 6-51. Current Output Power-Off Glitch



Output range: 0 μA to 250 μA

图 6-52. Current Output Noise Density

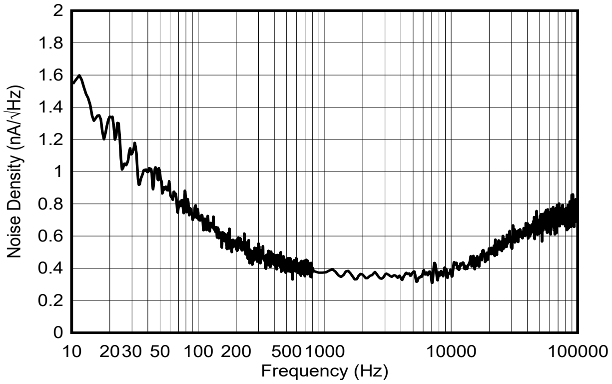
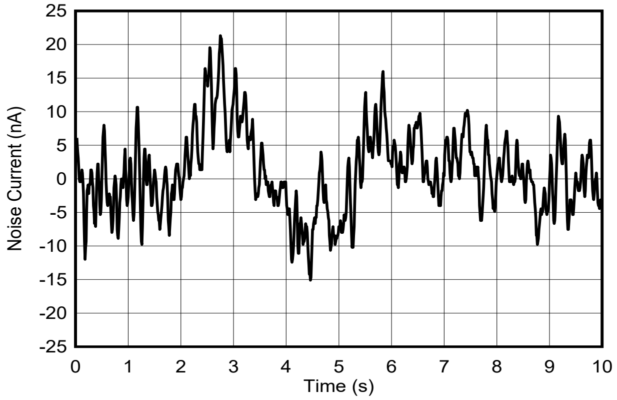


图 6-53. Current Output Noise Density

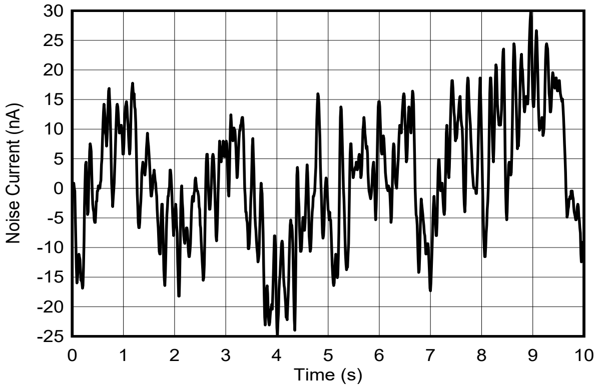
6.18 Typical Characteristics: Current Output (continued)

at T_A = 25°C, V_{DD} = 5.5 V, output range: ±250 µA (unless otherwise noted)



Output range: 0 µA to 250 µA, f = 0.1 Hz to 10 Hz

图 **6-54. Current Output Flicker Noise**



f = 0.1 Hz to 10 Hz

图 **6-55. Current Output Flicker Noise**

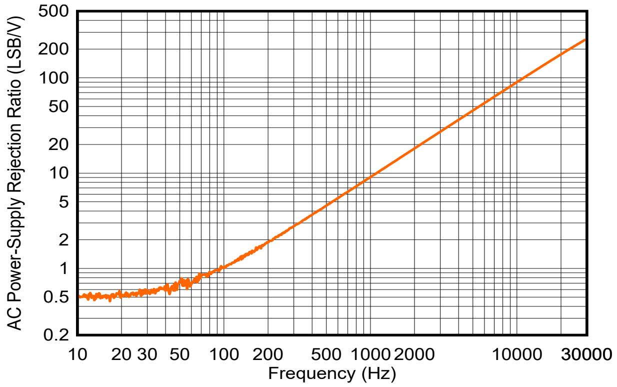
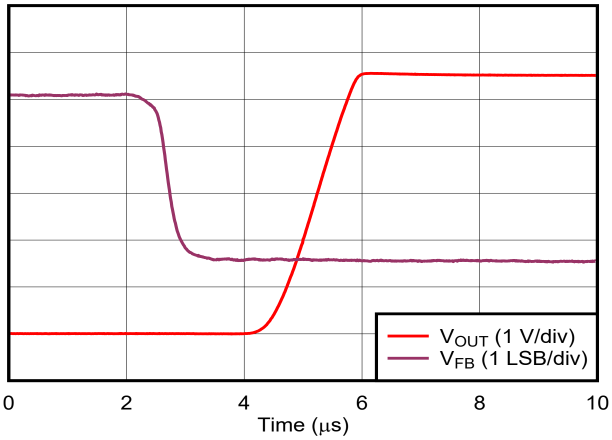


图 **6-56. Current Output AC PSRR vs Frequency**

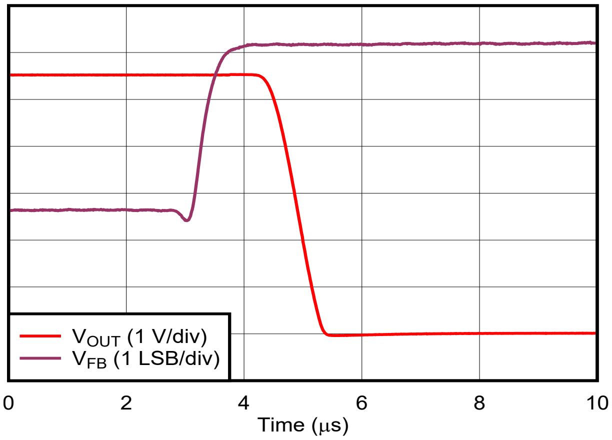
6.19 Typical Characteristics: Comparator

at T_A = 25°C, V_{DD} = 5.5 V, external reference = 5.5 V, gain = 1x, 12-bit resolution, FBx pin in Hi-Z mode, and DAC outputs unloaded (unless otherwise noted)



Comparator output in push-pull mode

图 6-57. Comparator Response Time: Low-to-High Transition



Comparator output in push-pull mode

图 6-58. Comparator Response Time: High-to-Low Transition

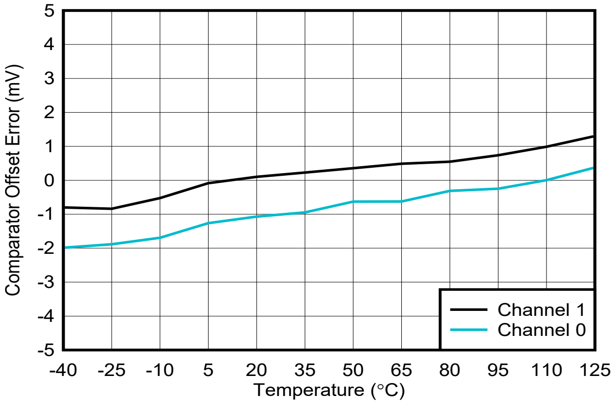
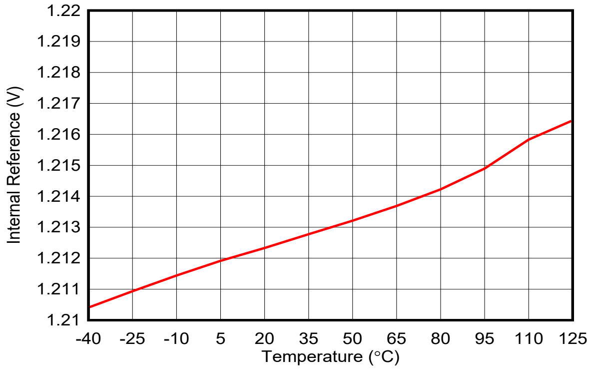


图 6-59. Comparator Offset Error vs Temperature

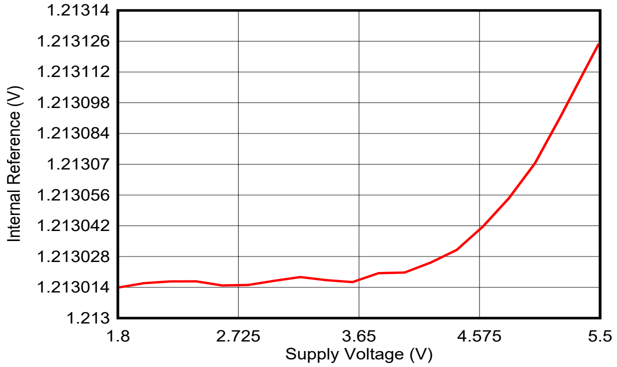
6.20 Typical Characteristics: General

at T_A = 25°C, V_{DD} = 5.5 V, and DAC outputs unloaded (unless otherwise noted)



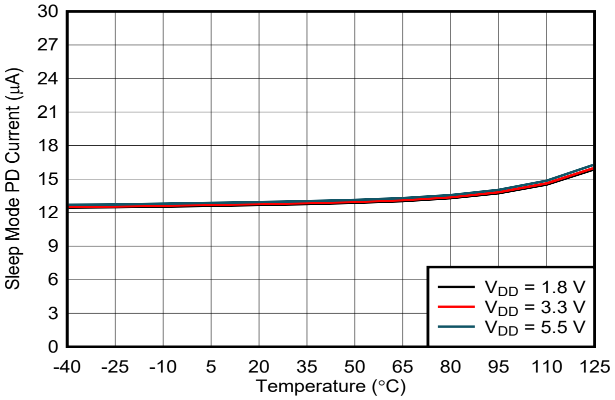
Internal reference

图 6-60. Internal Reference vs Temperature



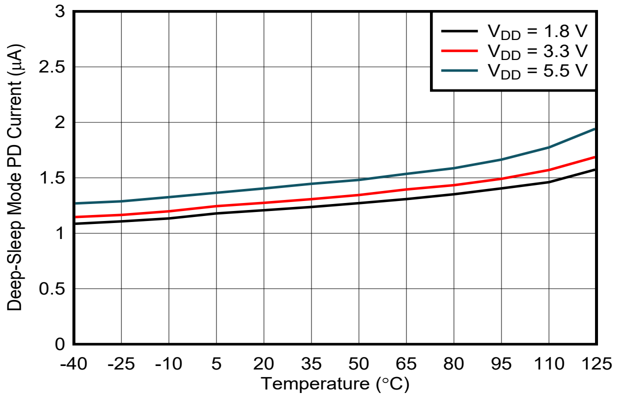
Internal reference

图 6-61. Internal Reference vs Supply Voltage



Sleep mode, internal reference disabled

图 6-62. Power-Down Current vs Temperature



Deep-sleep mode

图 6-63. Power-Down Current vs Temperature

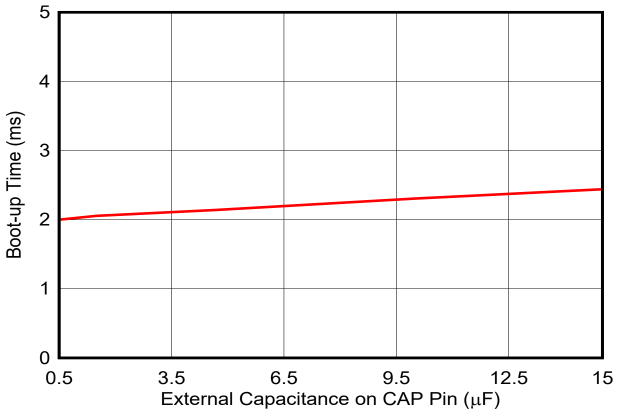


图 6-64. Boot-Up Time vs Capacitance on CAP pin

7 Detailed Description

7.1 Overview

The 12-bit single-channel DAC63001, 12-bit dual-channel DAC63002, 10-bit single-channel DAC53001, and 10-bit dual-channel DAC53002 (collectively referred to as the DACx300x) are a pin-compatible family of ultra-low-power, buffered voltage-output and current-output, smart digital-to-analog converters (DACs). The DAC channels are independently configurable as voltage output or current output. The DAC outputs change to Hi-Z when VDD is off; a feature useful in voltage-margining applications. These smart DACs contain nonvolatile memory (NVM), an internal reference, automatically detectable I^2C or SPI interface, PMBus-compatibility in I^2C mode, a force-sense output, and a general-purpose input/output. These devices support Hi-Z power-down modes by default, which can also be configured to 10 kΩ-GND or 100 kΩ-GND using the NVM. The DACx300x have a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The DACx300x operate with either an internal reference, external reference, or with a power supply as the reference, and provide a full-scale output between 1.8 V and 5.5 V.

The DACx300x devices support I^2C standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). The I^2C interface can be configured with four target addresses using the A0 pin. These devices also support specific PMBus commands such as *turn on/off*, *margin high or low*, and more. SPI mode supports a three-wire interface by default, with up to a 50-MHz SCLK input. The GPIO input can be configured as SDO in the NVM for SPI read capability. The GPIO input can also be configured as $\overline{\text{FAULT-DUMP}}$, $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{PROTECT}}$, $\overline{\text{RESET}}$, and $\overline{\text{STATUS}}$ functions. These devices support deep-sleep mode in addition to sleep (power-down) mode. Deep-sleep mode, in which the device draws a very-low power-down current of 3 μA, uses the GPIO pin for power-down and wake up. Together with ultra-low-power operation, the DACx300x are designed for battery-operated applications, such as land mobile radios, medical pulse oximeters, and laptops.

The DACx300x also include digital slew rate control, and support standard waveform generation such as *sine*, *cosine*, *triangular*, and *sawtooth*. These devices can generate pulse-width modulation (PWM) output with the combination of the triangular or sawtooth waveform and the FB pin. The force-sense outputs of the DAC channels can be used as programmable comparators. Comparator mode allows programmable hysteresis, latching comparator, and window comparator. These features enable the DACx300x to go beyond the limitations of a conventional DAC that depends on a processor to function. As a result of *processor-less* operation and the *smart* feature set, the DACx300x are called smart DACs.

7.2 Functional Block Diagram

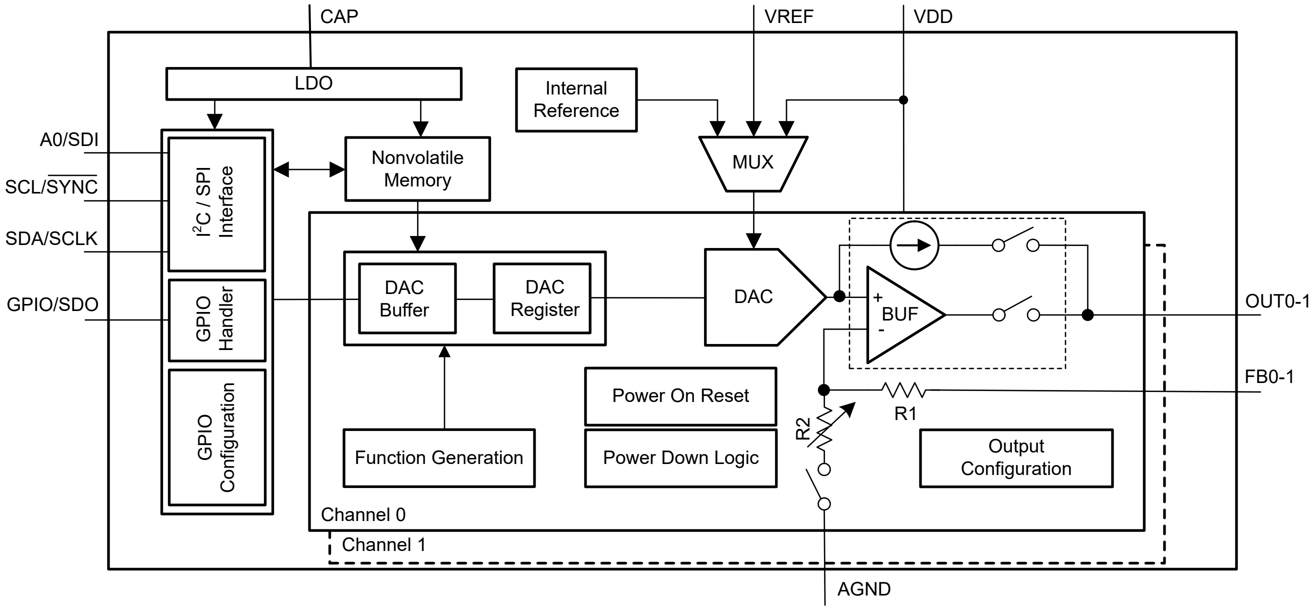


图 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Smart Digital-to-Analog Converter (DAC) Architecture

The DACx300x devices consist of a string architecture with a voltage-output amplifier, as well as an external FB pin and a voltage-to-current converter for each channel. 节 7.2 shows the DAC architecture within the block diagram that operates from a 1.8-V to 5.5-V power supply. The DAC has an internal voltage reference of 1.21 V. Optionally, use an external reference on the VREF pin, or use the power supply as a reference. Voltage output mode uses one of these three reference options. Current output mode uses an internal band gap to generate the current outputs. Both the voltage- and current-output modes support multiple programmable output ranges.

The DACx300x devices support Hi-Z output when VDD is off, maintaining a very low leakage current at the output pins with up to 1.25 V of forced voltage. The DAC output pin also starts up in high-impedance mode by default, making these devices an excellent choice for voltage margining and scaling applications. To change the power-up mode to 10 kΩ-GND or 100 kΩ-GND, program the corresponding VOUT-PDN-X field in the COMMON-CONFIG register and load these bits in the device NVM.

The DACx300x devices support an independent comparator mode for each channel. The respective FBx pin acts as an input for the comparator. The DAC architecture supports inversion of the comparator output using register settings. The comparator outputs can be push-pull or open-drain. Comparator mode supports programmable hysteresis using the *margin-high* and *margin-low* register fields, latching comparator, and window comparator. The comparator outputs are internally accessible by the device.

The DACx300x devices include a *smart* feature set to enable *processor-less* operation and high-integration. The NVM enables a predictable start-up. In the absence of a processor or when the processor or software fails, the GPIO triggers the DAC output without the I^2C interface. The integrated functions and the FBx pin enable PWM output for control applications. The FBx pin enables this device to be used as a programmable comparator. The digital slew-rate control and the Hi-Z power-down modes enable a hassle-free voltage margining and scaling function.

7.3.2 Digital Input/Output

The DACx300x have four digital IO pins that include I^2C, SPI, PMBus, and GPIO interfaces. These devices automatically detect I^2C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I^2C interface uses the A0 pin to select from among four address options. The SPI interface is a 3-wire interface by default. No readback capability is available in this mode. The GPIO pin can be configured in the register map and then programmed in to the NVM as the SDO pin. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I^2C: SCL, SDA, A0
- SPI: SCLK, SDI, $\overline{\text{SYNC}}$, SDO/GPIO

The GPIO can be configured as multiple functions other than SDO. These are $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{STATUS}}$, $\overline{\text{PROTECT}}$, $\overline{\text{FAULT-DUMP}}$, and $\overline{\text{RESET}}$. All the digital pins are open-drain when used as outputs. Therefore, all the output pins must be pulled up to the desired IO voltage using external resistors.

7.3.3 Nonvolatile Memory (NVM)

The DACx300x contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, shown in the highlighted gray cells in 表 7-20, can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. The NVM-PROG is an autoresetting bit. The default values for all the registers in the DACx300x are loaded from NVM as soon as a POR event is issued.

The DACx300x also implement NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 and the device starts an NVM-reload operation. After completion, the device autoresets the NVM-RELOAD bit to 0. During the NVM write or reload operation, all read/write operations to the device are blocked. 节 6.8 provides the timing specification for the NVM write cycle. The processor must wait for the specified duration before resuming any read or write operation on the SPI or I^2C interface.

7.3.4 Power Consumption

The power consumption of the DACx300x in sleep mode and deep-sleep mode are provided in 节 6.20. In normal operation, the total power consumption of the device depends on the number of channels powered on and the output mode of each channel (voltage or current). In current-output mode, the I_{DD} also depends on the output range. The I_{DD} calculation excludes the load current. For example, in the ±250 μA output mode with a DAC setting of +125 μA, the total current drawn through the VDD pin is the total I_{DD} plus 125 μA. The total I_{DD} in normal operation can be calculated using 方程式 1.

$$P_{NORMAL\_MODE} = V_{DD} \times \left(I_{DD\_SLEEP} + I_{DD\_REF}\right) + \sum_{X=0}^{3} \left(V_{DD} \times I_{DD\_X}\right) \tag{1}$$

where:

- I_{DD_SLEEP} is the current through V_{DD} in sleep mode when all the channels and internal reference are powered down.
- I_{DD_REF} is the reference current, which is:
  - either the current drawn by the reference input impedance when V_{DD} is used as reference
  - or the current drawn by the internal reference, if enabled
- I_{DD_X} is the current through V_{DD} for every powered-on channel-*X*.

备注

When an external reference is used, the current is calculated mainly as the current sourced from the external reference, which is equal to the reference voltage divided by the input impedance of the VREF pin.

7.4 Device Functional Modes

7.4.1 Voltage-Output Mode

The voltage-output mode for each DAC channel can be entered by selecting the power-up option in the VOUT-PDN-X fields in the COMMON-CONFIG register and simultaneously powering down the current output option for the respective channels using the IOUT-PDN-X bits in the same register. Short the OUTx and FBx pins of respective channels externally for closed-loop amplifier output. An open FBx pin saturates the amplifier output. To achieve the desired voltage output, select the correct reference option, select the amplifier gain for the required output range, and program the DAC code in the DAC-X-DATA register of the respective channels.

7.4.1.1 Voltage Reference and DAC Transfer Function

图 7-2 shows that there are three voltage reference options possible with the DACx300x: internal reference, external reference, and the power supply as reference. The DAC transfer function in the voltage-output and comparator modes changes based on the voltage reference selection.

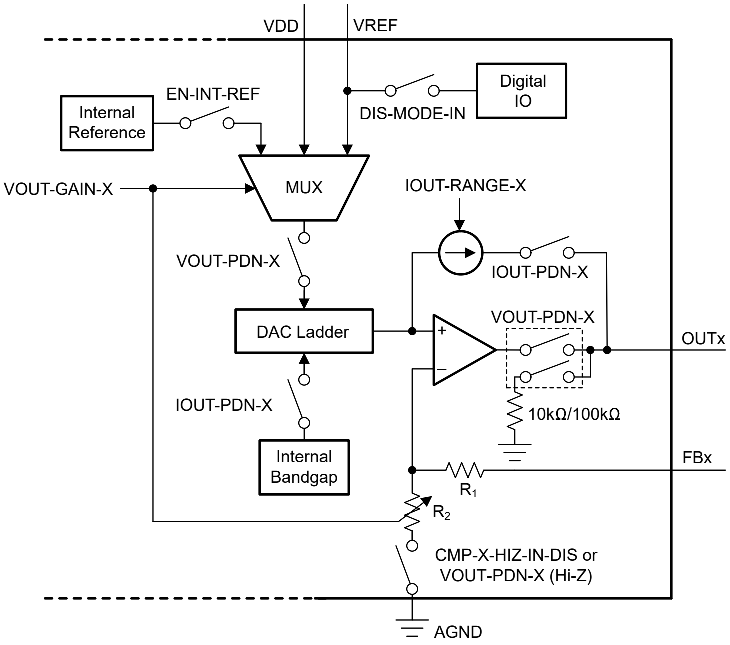


图 7-2. Voltage Reference Selection and Power-Down Logic

7.4.1.1.1 Internal Reference

The DACx300x contain an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the VOUT-GAIN-X bit in the DAC-X-VOUT-CMP-CONFIG register to achieve gains of 1.5x, 2x, 3x, or 4x for the DAC output voltage (V_{OUT}). 方程式 2 shows DAC transfer function using the internal reference.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \tag{2}$$

where:

- N is the resolution in bits, 10 (DAC53001, DAC53002), or 12 (DAC63001, DAC63002).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bit in the DAC-X-DATA register. DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V (typical).
- GAIN = 1.5x, 2x, 3x, or 4x, based on VOUT-X-GAIN bits.

7.4.1.1.2 External Reference

By default, the DACx300x operate from an external reference input. The external reference option can also be selected by configuring the VOUT-GAIN-X field in the DAC-X-VOUT-CMP-CONFIG register appropriately. Write 1 to the DIS-MODE-IN bit in the DEVICE-MODE-CONFIG register to minimize I_{DD}. The external reference can be between 1.7 V and VDD. 方程式 3 shows DAC transfer function when the external reference is used. The gain at the output stage of the DAC is always 1x in the external reference mode.

备注

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \tag{3}$$

where:

- N is the resolution in bits, 10 (DAC53001, DAC53002), or 12 (DAC63001, DAC63002).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA field in the DAC-X-DATA register. DAC_DATA ranges from 0 to $2^N - 1$.
- V_{REF} is the external reference voltage.

7.4.1.1.3 Power-Supply as Reference

The DACx300x can operate with the power-supply pin (VDD) as a reference. 方程式 4 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1x.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{DD} \tag{4}$$

where:

- N is the resolution in bits, either 10 (DAC53001, DAC53002), or 12 (DAC63001, DAC63002).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bit in the DAC-X-DATA register.
- DAC_DATA ranges from 0 to $2^N - 1$.
- V_{DD} is used as the DAC reference voltage.

7.4.2 Current-Output Mode

To enter current-output mode for each DAC channel, disable the respective IOUT-PDN-X bits in the COMMON-CONFIG register, and set the respective VOUT-PDN-X bits in the same register to Hi-Z power-down mode. Select the desired current-output range by writing to the IOUT-RANGE-X bit in the DAC-X-IOUT-MISC-CONFIG register. To minimize leakage in current-output mode, disconnect the FBx pin. For the best power-on glitch performance, program the NVM with IOUT mode using the smallest output range before powering on the output channel, and then immediately program the DAC code and desired output range. The transfer function of the output current is shown in 方程式 5.

$$I_{OUT} = \frac{DAC\_DATA \times (I_{MAX} - I_{MIN})}{2^8} + I_{MIN} \tag{5}$$

where:

- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA bit specified in 节 7.6.8. DAC_DATA ranges from 0 to 255.
- I_{MAX} is the signed maximum current in the IOUT-RANGE-X setting specified in 节 7.6.5.
- I_{MIN} is the signed minimum current in the IOUT-RANGE-X setting specified in 节 7.6.5.

7.4.3 Comparator Mode

All the DAC channels can be configured as programmable comparators in the voltage-output mode. To enter the comparator mode for a channel, write 1 to the CMP-X-EN bit in the respective DAC-X-VOUT-CMP-CONFIG register. The comparator output can be configured as push-pull or open-drain using the CMP-X-OD-EN bit. To enable the comparator output on the output pin, write 1 to the CMP-X-OUT-EN bit. To invert the comparator output, write 1 to the CMP-X-INV-EN bit. The FBx pin has a finite impedance. By default, the FBx pin is in the high-impedance mode. To disable high-impedance on the FBx pin, write 1 to the CMP-X-HIZ-IN-DIS bit. 表 7-1 shows the comparator output at the pin for different bit settings.

备注

In the Hi-Z input mode, the comparator input range is limited to:

- For GAIN = 1x, 1.5x, or 2x: $V_{FB} \leqslant (V_{REF} \times GAIN) / 3$
- For GAIN = 3x, or 4x: $V_{FB} \leqslant (V_{REF} \times GAIN) / 6$

Any higher input voltage is clipped.

表 7-1. Comparator Output Configuration

CMP-X-EN	CMP-X-OUT-EN	CMP-X-OD-EN	CMP-X-INV-EN	CMPX-OUT PIN
0	X	X	X	Comparator not enabled
1	0	X	X	No output
1	1	0	0	Push-pull output
1	1	0	1	Push-pull and inverted output
1	1	1	0	Open-drain output
1	1	1	1	Open-drain and inverted output

图 7-3 shows the interface circuit when all the DAC channels are configured as comparators. The programmable comparator operation is as shown in 图 7-4. Individual comparator channels can be configured in no-hysteresis, with-hysteresis, and window-comparator modes using the CMP-X-MODE bit in the respective DAC-X-CMP-MODE-CONFIG register, as shown in 表 7-2.

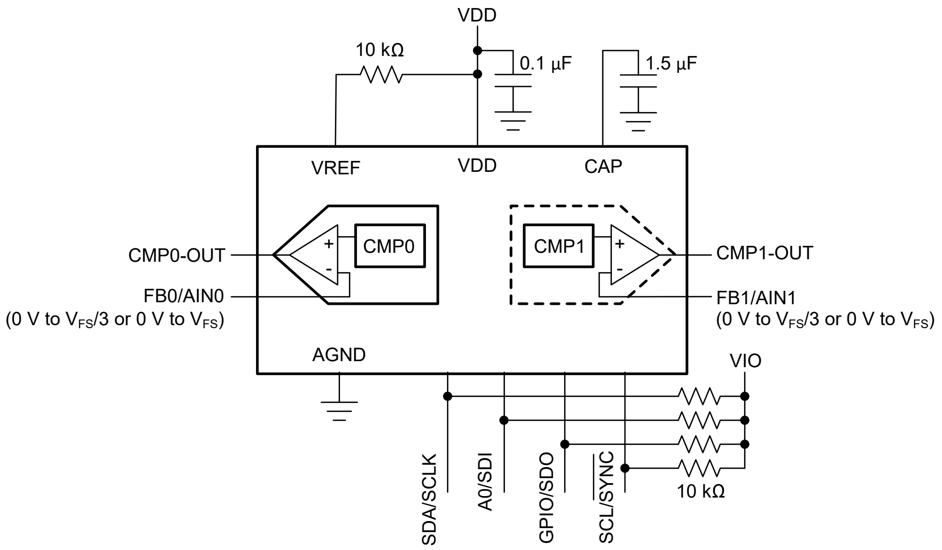


图 7-3. Comparator Interface

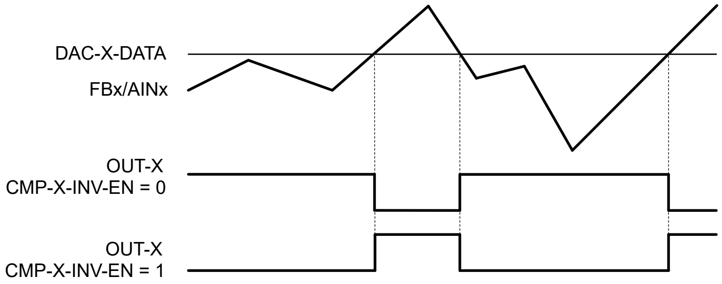


图 7-4. Programmable Comparator Operation

表 7-2. Comparator Mode Selection

CMP-X-MODE BIT FIELD	COMPARATOR CONFIGURATION
00	Normal comparator mode. No hysteresis or window operation.
01	Hysteresis comparator mode. DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers set the hysteresis.
10	Window comparator mode. DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers set the window bounds.
11	Invalid setting

7.4.3.1 Programmable Hysteresis Comparator

表 7-2 shows that comparator mode provides hysteresis when the CMP-X-MODE bit is set to 01b. 图 7-5 shows that the hysteresis is provided by the DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers.

When the DAC-X-MARGIN-HIGH is set to full-code or the DAC-X-MARGIN-LOW is set to zero-code, the comparator works as a latching comparator; that is, the output is latched after the threshold is crossed. The latched output can be reset by writing to the corresponding RST-CMP-FLAG-X bit in the COMMON-DAC-TRIG register. 图 7-6 shows the behavior of a latching comparator with active low output, and 图 7-7 shows the behavior of a latching comparator with active high output.

备注

The value of the DAC-X-MARGIN-HIGH register must be greater than the value of the DAC-X-MARGIN-LOW register. The comparator output in the hysteresis mode can only be noninverting that is, the CMP-X-INV-EN bit in the DAC-X-VOUT-CMP-CONFIG register must be set to 0. For the reset to take effect in latching mode, the input voltage must be within DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW.

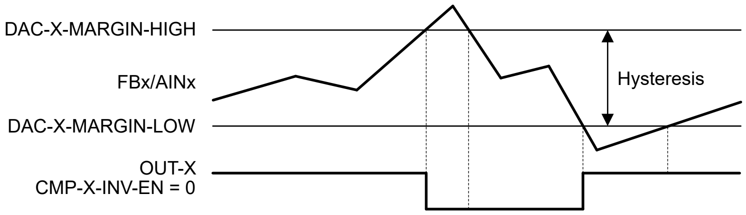


图 7-5. Programmable Hysteresis Without Latching Output

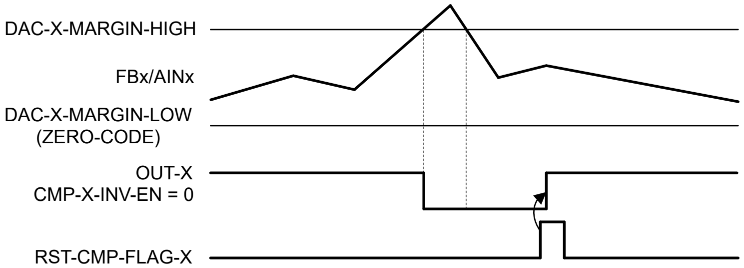


图 7-6. Latching Comparator With Active Low Output

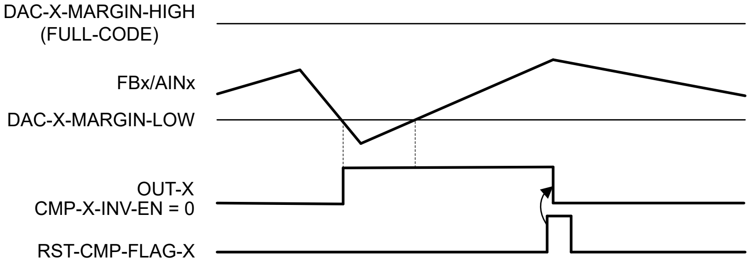


图 7-7. Latching Comparator With Active High Output

7.4.3.2 Programmable Window Comparator

Window comparator mode is enabled by setting the CMP-X-MODE bit to 10b (see also 表 7-2). 图 7-8 shows that the window bounds are set by the DAC-X-MARGIN-HIGH and the DAC-X-MARGIN-LOW registers. The output of the window comparator for a given channel is indicated by the respective WIN-CMP-X bit in the CMP-STATUS register. The comparator output (WIN-CMP-X) is latched by writing 1 to the WIN-LATCH-EN bit in the COMMON-CONFIG register. After being latched, the comparator output is reset using the corresponding RST-CMP-FLAG-X bit in the COMMON-DAC-TRIG register. For the reset to take effect, the input must be within the window bounds.

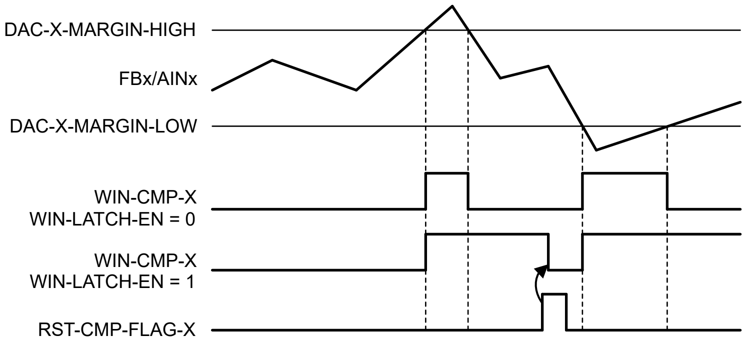


图 7-8. Window Comparator Operation

A single comparator is used per channel to check both the *margin-high* and *margin-low* limits of the window. Therefore, the window comparator function has a finite response time (see also 节 6.7). The static behavior of the WIN-CMP-X bit is not reflected at the output pins. Set the CMP-X-OUT-EN bit to 0. The WIN-CMP-X bit must be read digitally using the communication interface. This bit can also be mapped to the GPIO pin (see also 表 7-19).

备注

- The value of the DAC-X-MARGIN-HIGH register must be greater than that of the DAC-X-MARGIN-LOW register.
- Set the SLEW-RATE-X bit to 0000b (no-slew) and LOG-SLEW-EN-X bit to 0b in the DAC-X-FUNC-CONFIG register to get the best response time from the window comparator.
- The CMP-X-OUT-EN bit in the DAC-X-VOUT-CMP-CONFIG register can be set to 0b to eliminate undesired toggling of the OUT pin.

7.4.4 Fault-Dump Mode

The DACx300x provides a feature to save a few registers into the NVM when the FAULT-DUMP bit is triggered or when the GPIO mapped to fault-dump is triggered (see also 表 7-18). This feature is useful in system-level fault management to capture the state of the device or system just before a fault is triggered, and to allow diagnosis after the fault has occurred. The registers saved when fault-dump is triggered, are:

- CMP-STATUS[7:0]
- DAC-0-DATA[15:8]
- DAC-1-DATA[15:8]

备注

When the fault-dump cycle is in progress, any change in the data can corrupt the final outcome. Make sure the comparator and the DAC codes are stable during the NVM write cycle.

表 7-3 shows the storage format of the registers in the NVM.

表 7-3. Fault-Dump NVM Storage Format

NVM ROWS	B31-B24	B23-B16	B15-B8	B7-B0
Row1	CMP-STATUS[7:0]	Don't care		
Row2	DAC-1-DATA[15:8]	Don't care		DAC-1-DATA[15:8]

The data captured in the NVM after the fault dump can be read in a specific sequence:

1. Set the EE-READ-ADDR bit to 0b in the COMMON-CONFIG register, to select row1 of the NVM.
2. Trigger the read of the selected NVM row by writing 1 to the READ-ONE-TRIG in the COMMON-TRIGGER register; this bit autoresets. This action copies that data from the selected NVM row to SRAM addresses 0x9D (LSB 16 bits from the NVM) and 0x9E (MSB 16 bits from the NVM).
3. To read the SRAM data:
    a. Write 0x009D to the SRAM-CONFIG register.
    b. Read the data from the SRAM-DATA register to get the LSB 16 bits.
    c. Write 0x009E to the SRAM-CONFIG register.
    d. Read the data from the SRAM-DATA register again to get the MSB bits.
4. Set the EE-READ-ADDR bit to 1b in the COMMON-CONFIG register, to select row2 of the NVM. Repeat steps 2 and 3.

7.4.5 Application-Specific Modes

This section provides the details of application-specific functional modes available in the DACx300x.

7.4.5.1 Voltage Margining and Scaling

Voltage margining or scaling is a primary application for the DACx300x. This section provides specific features available for this application such as Hi-Z output, slew-rate control, $\overline{\text{PROTECT}}$ input, and PMBus compatibility.

7.4.5.1.1 High-Impedance Output and $\overline{\text{PROTECT}}$ Input

All the DAC output channels remain in a high-impedance state (Hi-Z) when VDD is off. 图 7-9 shows a simplified schematic of the DACx300x used in a voltage-margining application. Series resistor R_S is required in voltage-output mode, but is optional in current-output mode. Almost all linear regulators and DC/DC converters have a feedback voltage of ⩽ 1.25 V. The low-leakage currents at the outputs are maintained for V_{FB} of ⩽ 1.25 V. Thus, for all practical purposes, the DAC outputs appear as Hi-Z when VDD of the DAC is off in voltage margining and scaling applications. This feature allows for seamless integration of the DACx300x into a system without any need for additional power-supply sequencing for the DAC.

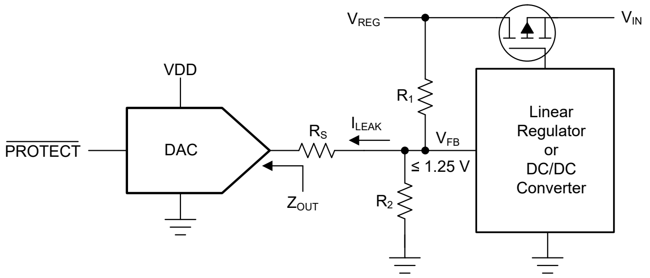


图 7-9. High-Impedance (Hi-Z) Output and $\overline{\text{PROTECT}}$ Input

The DAC channels power down to Hi-Z at boot up. The outputs can power up with a preprogrammed code that corresponds to the nominal output of the DC/DC converter or the linear regulator. This feature allows for smooth power up and power down of the DAC without impacting the feedback loop of the DC/DC converter or the linear regulator.

表 7-18 shows how the GPIO pin of the DACx300x can be configured as a $\overline{\text{PROTECT}}$ function. $\overline{\text{PROTECT}}$ takes the DAC outputs to a predictable state with a slewed or direct transition. This function is useful in systems where a fault condition (such as a brownout), a subsystem failure, or a software crash requires that the DAC outputs reach a predefined state without the involvement of a processor. The detected event can be fed to the GPIO pin that is configured as the $\overline{\text{PROTECT}}$ input. The $\overline{\text{PROTECT}}$ function can also be triggered using the PROTECT bit in the COMMON-TRIGGER register. 表 7-4 shows how to configure the behavior of the $\overline{\text{PROTECT}}$ function in the PROTECT-CONFIG field in the DEVICE-MODE-CONFIG register.

备注

- After the $\overline{\text{PROTECT}}$ function is triggered, the write functionality is disabled on the communication interface until the function is completed.
- The PROTECT-FLAG bit in the CMP-STATUS register is set to 1 when the $\overline{\text{PROTECT}}$ function is triggered. This bit can be polled by reading the CMP-STATUS register. After the $\overline{\text{PROTECT}}$ function is complete, a read command on the CMP-STATUS register resets the PROTECT-FLAG bit.

表 7-4. $\overline{\text{PROTECT}}$ Function Configuration

PROTECT-CONFIG FIELD	FUNCTION
00	Switch to Hi-Z power-down (no slew).
01	Switch to DAC code stored in NVM (no slew) and then switch to Hi-Z power-down.
10	Slew to margin-low code and then switch to Hi-Z power-down.

表 7-4. PROTECT Function Configuration (continued)

PROTECT-CONFIG FIELD	FUNCTION
11	Slew to margin-high code and then switch to Hi-Z power-down.

7.4.5.1.2 Programmable Slew-Rate Control

When the DAC data registers are written, the voltage on DAC output (V_{OUT}) immediately transitions to the new code following the slew rate and settling time specified in the *Electrical Characteristics*.

The slew rate control feature allows the user to control the rate at which the output voltage (V_{OUT}) changes. When this feature is enabled (using the SLEW-RATE-X[3:0] bits), the DAC output changes from the current code to the code in the DAC-X-MARGIN-HIGH or DAC-X-MARGIN-LOW registers (when margin high or low commands are issued to the DAC) using the step size and time-period per step set in CODE-STEP-X and SLEW-RATE-X bits in the DAC-X-FUNC-CONFIG register:

- SLEW-RATE-X defines the time-period per step at which the digital slew updates.
- CODE-STEP-X defines the number of LSBs by which the output value changes at each update, for the corresponding channels.

表 7-5 and 表 7-6 show different settings available for CODE-STEP-X and SLEW-RATE-X. With the default slew rate control setting of no-slew, the output changes immediately at a rate limited by the output drive circuitry and the attached load.

When the slew rate control feature is used, the output changes happen at the programmed slew rate. 图 7-10 shows that this configuration results in a staircase formation at the output. Do not write to CODE-STEP-X, SLEW-RATE-X, or DAC-X-DATA during the output slew operation. 方程式 6 provides the equation for the calculating the slew time (t_{SLEW}).

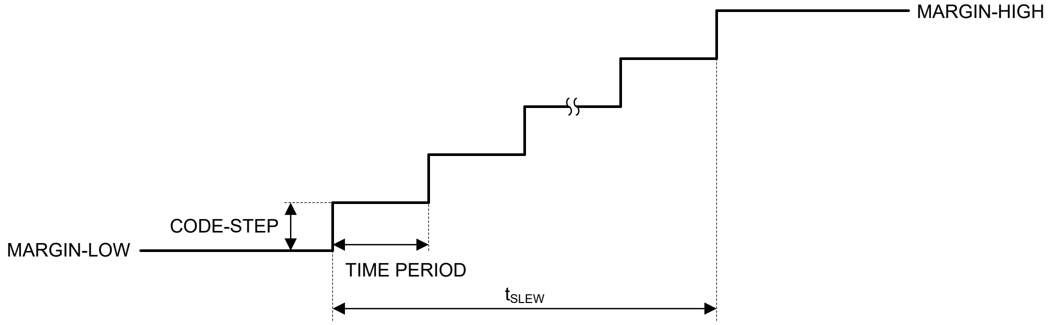


图 7-10. Programmable Slew-Rate Control

$$t_{SLEW} = \frac{\text{SLEW\_RATE} \times (\text{MARGIN\_HIGH} - \text{MARGIN\_LOW} + 1)}{\text{CODE\_STEP}} \quad (6)$$

where:

- SLEW_RATE is the SLEW-RATE-X setting specified in 表 7-6.
- CODE_STEP is the CODE-STEP-X setting specified in 表 7-5.
- MARGIN_HIGH is the DAC-X-MAGIN-HIGH specified in 节 7.6.2.
- MARGIN_LOW is the DAC-X-MAGIN-LOW specified in 节 7.6.3.

表 7-5. Code Step

REGISTER	CODE-STEP-X[2]	CODE-STEP-X[1]	CODE-STEP-X[0]	CODE STEP SIZE
DAC-X-FUNC-CONFIG	0	0	0	1 LSB (default)
	0	0	1	2 LSB
	0	1	0	3 LSB
	0	1	1	4 LSB
	1	0	0	6 LSB
	1	0	1	8 LSB
	1	1	0	16 LSB
	1	1	1	32 LSB

表 7-6. Slew Rate

REGISTER	SLEW-RATE-X[3]	SLEW-RATE-X[2]	SLEW-RATE-X[1]	SLEW-RATE-X[0]	TIME PERIOD (PER STEP)
DAC-X-FUNC-CONFIG	0	0	0	0	No slew (default)
	0	0	0	1	4 µs
	0	0	1	0	8 µs
	0	0	1	1	12 µs
	0	1	0	0	18 µs
	0	1	0	1	27 µs
	0	1	1	0	40.5 µs
	0	1	1	1	60.75 µs
	1	0	0	0	91.13 µs
	1	0	0	1	136.69 µs
	1	0	1	0	239.2 µs
	1	0	1	1	418.61 µs
	1	1	0	0	732.56 µs
	1	1	0	1	1281.98 µs
	1	1	1	0	2563.96 µs
	1	1	1	1	5127.92 µs

7.4.5.1.3 PMBus Compatibility Mode

The PMBus protocol is an I^{2}C-based communication standard for power-supply management. PMBus contains standard command codes tailored to power supply applications. The DACx300x implement some PMBus commands such as *Turn Off*, *Turn On*, *Margin Low*, *Margin High*, *Communication Failure Alert Bit (CML)*, as well as *PMBUS revision*. 图 7-11 shows typical PMBus connections. The EN-PMBUS bit in the INTERFACE-CONFIG register must be set to 1 to enable the PMBus protocol.

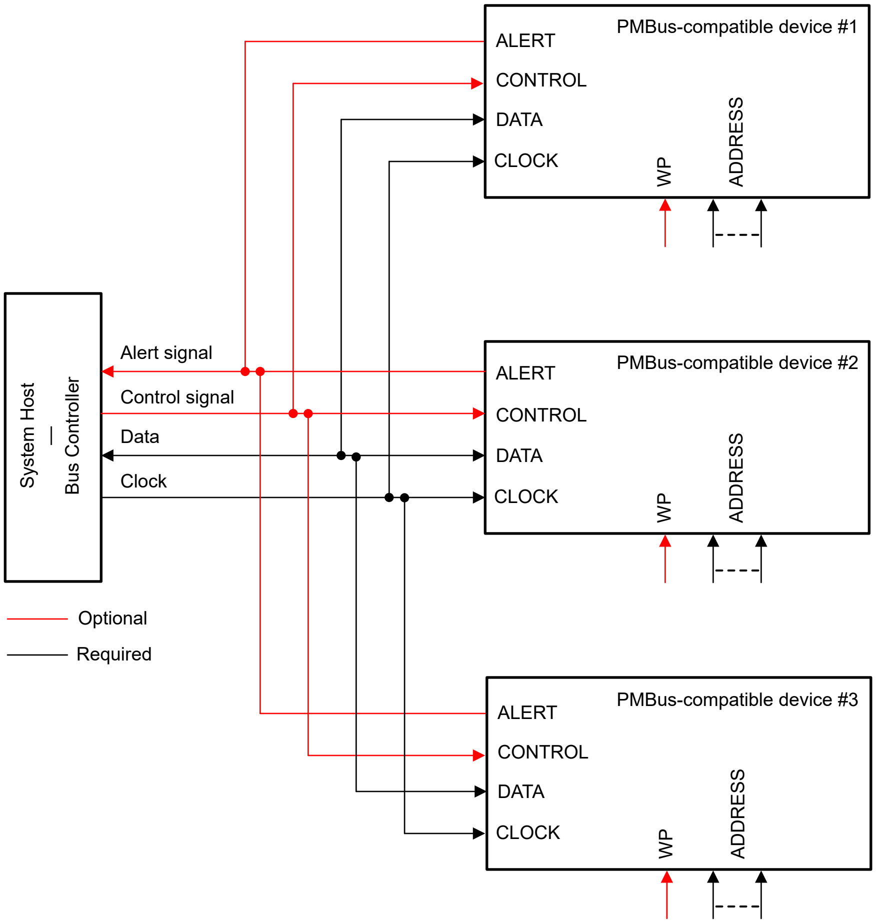


图 7-11. PMBus Connections

Similar to I^2C, PMBus is a variable length packet of 8-bit data bytes, each with a receiver acknowledge, wrapped between a start and stop bit. The first byte is always a 7-bit *target address* followed by a *write* bit, sometimes called the *even address*, that identifies the intended receiver of the packet. The second byte is an 8-bit *command* byte, identifying the PMBus command being transmitted using the respective command code. After the command byte, the transmitter either sends data associated with the command to write to the receiver command register (from least significant byte to most significant byte; see also 表 7-7), or sends a new start bit indicating the desire to read the data associated with the command register from the receiver. Then the receiver transmits the data following the same least significant byte first format; see also 表 7-8.

表 7-7. PMBus Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte 节 7.5.2.2.1				Command byte 节 7.5.2.2.2				Data byte - LSDB				Data byte - MSDB (Optional)			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

表 7-8. PMBus Read Sequence

S	MSB	...	R/$\overline{W}$ (0)	ACK	MSB	...	LSB	ACK	Sr	MSB	...	R/$\overline{W}$ (1)	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
	Address byte 节 7.5.2.2.1				Command byte 节 7.5.2.2.2				Sr	Address byte 节 7.5.2.2.1				LSDB				MSDB (Optional)			
From controller				Target	From controller			Target	From controller				Target	From target			Controller	From target			Controller

The DACx300x I^2C interface implements some of the PMBus commands. 表 7-9 shows the supported PMBus commands that are implemented in DACx300x.The DAC uses DAC-X-MARGIN-LOW, DAC-X-MARGIN-HIGH bits, SLEW-RATE-X, and CODE-STEP-X bits for PMBUS-OPERATION-CMD-X. To access multiple channels, write the PMBus page address specified in 表 7-21 to the PMBUS-PAGE register first, followed by a write to the channel-specific register.

表 7-9. PMBus Operation Commands

REGISTER	PMBUS-OPERATION-CMD-X[15:8]	DESCRIPTION
PMBUS-OP-CMD-X	00h	Turn off
	80h	Turn on
	94h	Margin low
	A4h	Margin high

The DACx300x also implement PMBus features such as group command protocol and communication timeout failure. The CML bit in the PMBUS-CML register indicates a communication fault in the PMBus. This bit is reset by writing 1.

To get the PMBus version, read the PMBUS-VERSION register.

7.4.5.2 Function Generation

The DACx300x implement a continuous function or waveform generation feature. These devices can generate a triangular wave, sawtooth wave, and sine wave independently for every channel.

7.4.5.2.1 Triangular Waveform Generation

The triangular waveform uses the DAC-X-MARGIN-LOW and DAC-X-MARGIN-HIGH registers for minimum and maximum levels, respectively. 方程式 7 shows that the frequency of the waveform depends on the min and max levels, CODE-STEP, and SLEW-RATE settings. An external RC load with a time-constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-X and SLEW-RATE-X settings are available in the DAC-X-FUNC-CONFIG register. Writing 0b000 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register selects triangular waveform.

$$f_{\mathrm{TRIANGLE\_WAVE}} = \frac{1}{2 \times \mathrm{SLEW\_RATE} \times \left(\frac{\mathrm{MARGIN\_HIGH} - \mathrm{MARGIN\_LOW} + 1}{\mathrm{CODE\_STEP}}\right)} \tag{7}$$

where:

- SLEW_RATE is the SLEW-RATE-X setting specified in 表 7-6.
- CODE_STEP is the CODE-STEP-X setting specified in 表 7-5.
- MARGIN_HIGH is the DAC-X-MAGIN-HIGH specified in 节 7.6.2.
- MARGIN_LOW is the DAC-X-MAGIN-LOW specified in 节 7.6.3.

7.4.5.2.2 Sawtooth Waveform Generation

The sawtooth and the inverse sawtooth waveforms use the DAC-X-MARGIN-LOW and DAC-X-MARGIN-HIGH registers for minimum and maximum levels, respectively. 方程式 8 shows that the frequency of the waveform depends on the min and max levels, CODE-STEP, and SLEW-RATE settings. An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-X and SLEW-RATE-X settings are available in the DAC-X-FUNC-CONFIG register. Write 0b001 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register to select sawtooth waveform, and write 0b010 to select inverse sawtooth waveform.

$$f_{\mathrm{SAWTOOTH\_WAVE}} = \frac{1}{\mathrm{SLEW\_RATE} \times \left(\frac{\mathrm{MARGIN\_HIGH} - \mathrm{MARGIN\_LOW} + 1}{\mathrm{CODE\_STEP}}\right)} \tag{8}$$

where:

- SLEW_RATE is the SLEW-RATE-X setting specified in 表 7-6.
- CODE_STEP is the CODE-STEP-X setting specified in 表 7-5.
- MARGIN_HIGH is the DAC-X-MAGIN-HIGH specified in 节 7.6.2.
- MARGIN_LOW is the DAC-X-MAGIN-LOW specified in 节 7.6.3.

7.4.5.2.3 Sine Waveform Generation

The sine wave function uses 24 preprogrammed points per cycle. 方程式 9 shows that the frequency of the sine wave depends on the SLEW-RATE settings:

$$f_{\mathrm{SINE\_WAVE}} = \frac{1}{24 \times \mathrm{SLEW\_RATE}} \tag{9}$$

where SLEW_RATE is the SLEW-RATE-X setting specified in 表 7-6.

An external RC load with a time constant greater than the slew-rate settings can be dominant over the internal frequency calculation. The SLEW-RATE-X setting is available in the DAC-X-FUNC-CONFIG register. Writing 0b100 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register selects sine wave. The codes for the sine wave are fixed. Use the gain settings at the output amplifier for changing the full-scale output using the internal reference option. The gain settings are accessible through the VOUT-GAIN-X bits in the DAC-X-VOUT-CMP-CONFIG register. 表 7-10 shows the list of hard-coded discrete points for the sine wave with 12-bit resolution and 图 7-12 shows the pictorial representation of the sine wave. There are four phase settings available for the sine wave that are selected using the PHASE-SEL-X bit in the DAC-X-FUNC-CONFIG register.

表 7-10. Sine Wave Data Points

SEQUENCE	12-BIT VALUE	SEQUENCE	12-BIT VALUE
0	0x800	12	0x800
1	0x9A8	13	0x658
2	0xB33	14	0x4CD
3	0xC87	15	0x379
4	0xD8B	16	0x275
5	0xE2F	17	0x1D1
6	0xE66	18	0x19A
7	0xE2F	19	0x1D1
8	0xD8B	20	0x275
9	0xC87	21	0x379
10	0xB33	22	0x4CD
11	0x9A8	23	0x658

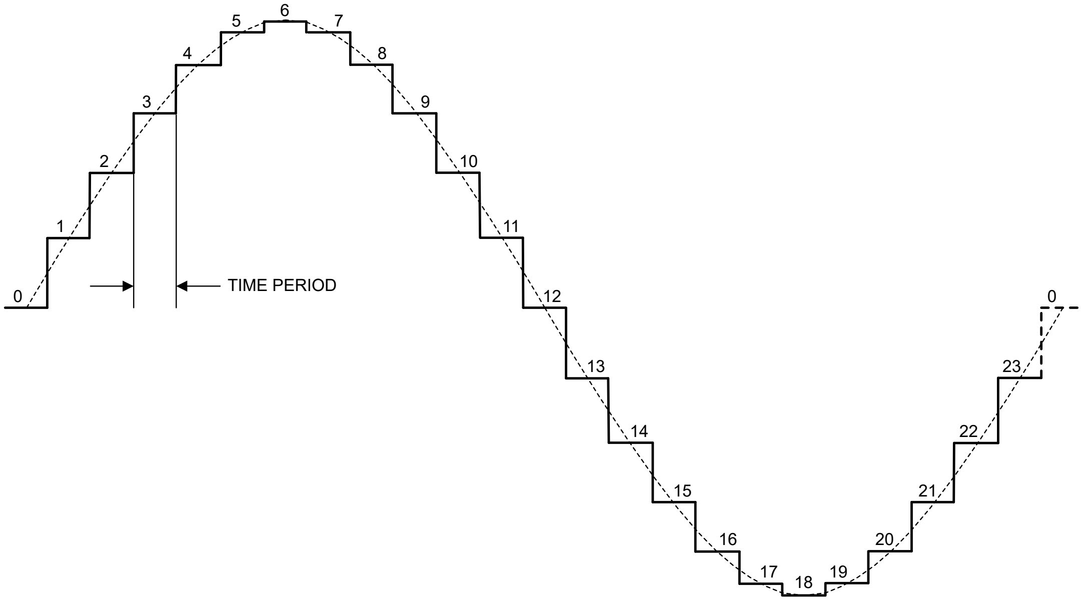


图 7-12. Sine Wave Generation

7.4.6 Device Reset and Fault Management

This section provides the details of power-on-reset (POR), software reset, and other diagnostics and fault-management features of DACx300x.

7.4.6.1 Power-On Reset (POR)

The DACx300x family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the DACx300x is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. 图 7-13 indicates that the POR circuit requires specific V_{DD} levels to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

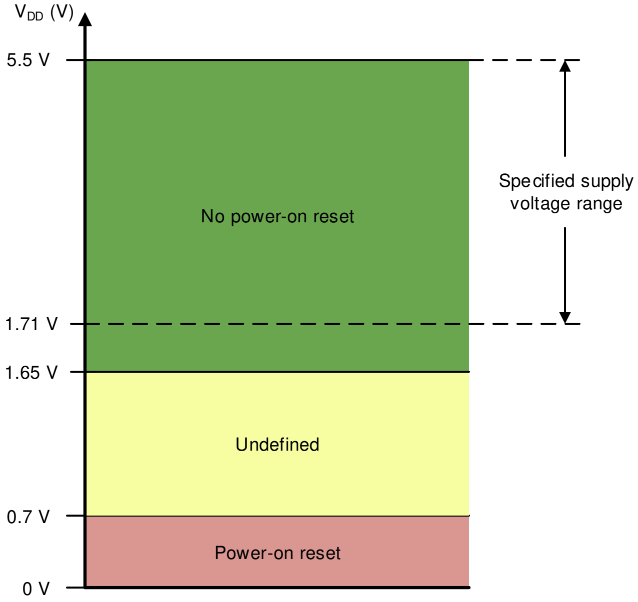


图 7-13. Threshold Levels for V_{DD} POR Circuit

7.4.6.2 External Reset

An external reset to the device can be triggered through the GPIO pin or through the register map. To initiate a device software reset event, write reserved code 1010 to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event. 表 7-18 shows how the GPIO pin can be configured as a $\overline{\text{RESET}}$ pin. This configuration must be programmed into the NVM so that the setting is not cleared after the device reset. The $\overline{\text{RESET}}$ input must be a low pulse. The device starts the boot-up sequence after the falling edge of the $\overline{\text{RESET}}$ input. The rising edge of the $\overline{\text{RESET}}$ input does not have any effect.

7.4.6.3 Register-Map Lock

The DACx300x implement a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using the I^2C interface. To bypass the DEV-LOCK setting, write 0101 to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

7.4.6.4 NVM Cyclic Redundancy Check (CRC)

The DACx300x implement a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in DACx300x:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits The CRC feature is implemented by storing a 16-bit CRC (CRC-16-CCITT) along with the NVM data each time NVM program operation (write or reload) is performed and during the device start-up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot up.

7.4.6.4.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset command (see also *节 7.4.6.2*), or cycle power to the DAC. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

7.4.6.4.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset command (see also *节 7.4.6.2*) or cycle power to the DAC. A permanent failure in the NVM makes the device unusable.

7.4.7 Power-Down Mode

The DACx300x output amplifier and internal reference can be independently powered down through the EN-INT-REF, VOUT-PDN-X, and IOUT-PDN-X bits in the COMMON-CONFIG register (see also 图 7-2). At power up, the DAC output and the internal reference are disabled by default. In power-down mode, the DAC outputs (OUTx pins) are in a high-impedance state. To change this state to 10 kΩ-A_{GND} or 100 kΩ-A_{GND} in voltage-output mode (at power up), use the VOUT-PDN-X bits. The power-down state for current-output mode is always high-impedance.

The DAC power-up state can be programmed to any state (power-down or normal mode) using the NVM. 表 7-11 shows the DAC power-down bits. The individual channel power-down bits can be mapped to the GPIO pin using the GPIO-CONFIG register. This function is called sleep mode. In this mode, the internal low-dropout regulator (LDO) and the common functional blocks are still powered-on, and the device draws a maximum of 28 µA of current through the power supply.

表 7-11. DAC Power-Down Bits

REGISTER	VOUT-PDN-X[1]	VOUT-PDN-X[0]	IOUT-PDN-X	DESCRIPTION
COMMON-CONFIG	0	0	1	Power up VOUT-X
	0	1	1	Power down VOUT-X with 10 kΩ to AGND. Power down IOUT-X to Hi-Z.
	1	0	1	Power down VOUT-X with 100 kΩ to AGND. Power down IOUT-X to Hi-Z.
	1	1	1	Power down VOUT-X to Hi-Z. Power down IOUT-X to Hi-Z (default).
	1	1	0	Power down VOUT-X to Hi-Z. Power up IOUT-X.

7.4.7.1 Deep-Sleep Mode

The DACx300x provide a deep-sleep mode, where the internal LDO and most of the common functional blocks are powered-down. The GPIO pin must be used to enter and exit this mode. The I^2C or SPI interface does not work during the deep-sleep mode. The steps to enter and exit the deep-sleep mode are:

1. Make sure that the GPIO pin is pulled high.
2. Write 1 to the DEEP-SLEEP-EN bit in the GPIO-CONFIG register.
3. Disable GP output and SDO by writing 0 to GPO-EN and SDO-EN bits.
4. Enable GPIO input mode by writing 1 to GPI-EN and 0b0000 to GPI-CONFIG bits.
5. To program these settings into the NVM, write 1 to the NVM-PROG bit in the COMMON-TRIGGER register.
6. A negative-edge trigger on the GPIO puts the device into the deep-sleep mode. The LDO takes approximately 550 µs to switch off. The device remains in this mode as long as the signal is low.
7. To bring the device out of the deep-sleep mode, pull the GPIO pin high. The digital circuitry and the LDO take approximately 550 µs to switch on.

7.5 Programming

The DACx300x are programmed through either a 3-wire SPI or 2-wire I^{2}C interface. A 4-wire SPI mode is enabled by mapping the GPIO pin as SDO. The SPI readback operates at a lower SCLK than the standard SPI write operation. The type of interface is determined based on the first protocol to communicate after device power up. After the interface type is determined, the device ignores any change in the type while the device is on. The interface type can be changed after a power cycle.

7.5.1 SPI Programming Mode

An SPI access cycle for DACx300x is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for DACx300x is 24 bits long. Therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO pin is not enabled (three-wire SPI). In the three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

表 7-12 and 图 7-14 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

表 7-12. SPI Read/Write Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Identifies the communication as a read or write command to the address register: R/$\overline{\text{W}}$ = 0 sets a write operation. R/$\overline{\text{W}}$ = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are *don't care* values.

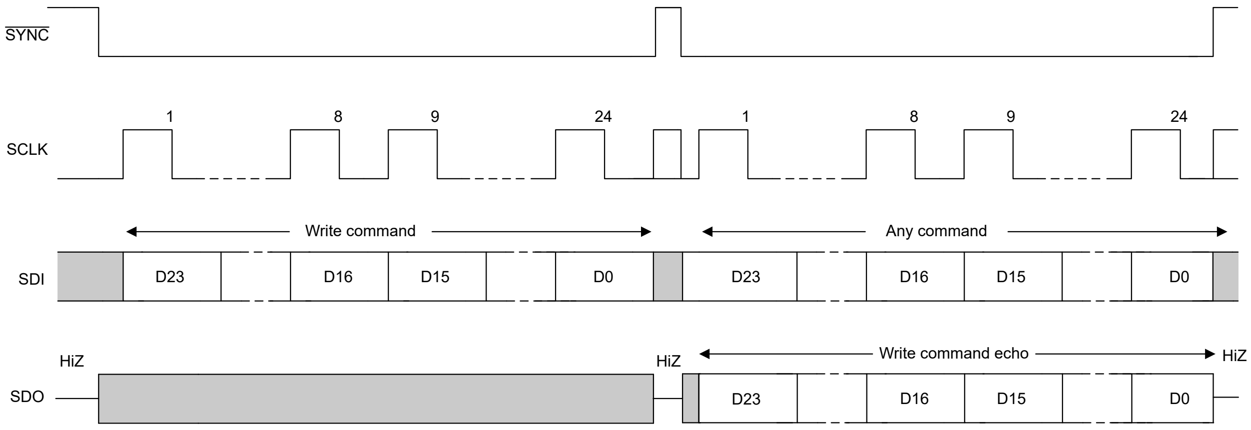


图 7-14. SPI Write Cycle

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. 表 7-13 and 图 7-15 show the output data format. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit (see also 图 6-3).

表 7-13. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Echo R/$\overline{\text{W}}$ from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle

表 7-13. SDO Output Access Cycle (continued)

BIT	FIELD	DESCRIPTION
15-0	DI[15:0]	Readback data requested on previous access cycle

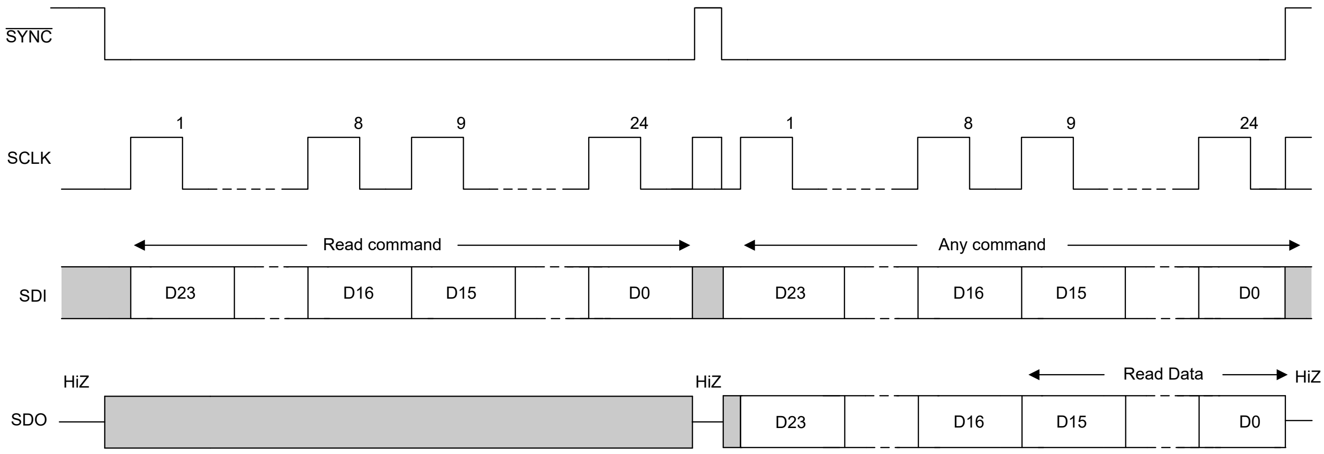


图 7-15. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. 图 7-16 shows that in daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device. The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. 图 7-17 describes the packet format for the daisy-chain write cycle.

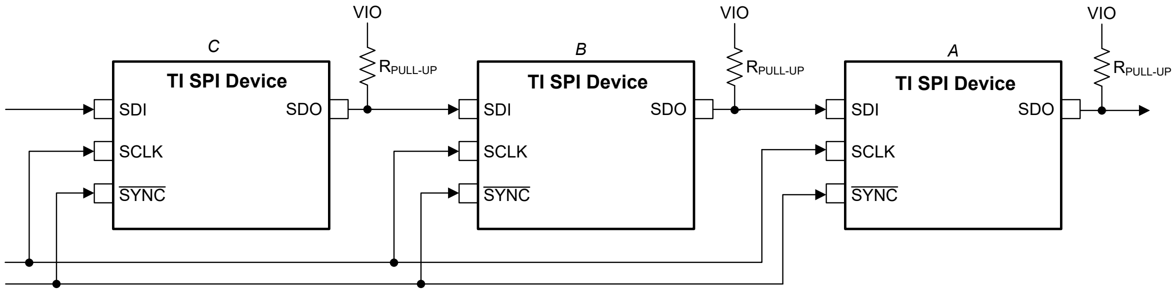


图 7-16. SPI Daisy-Chain Connection

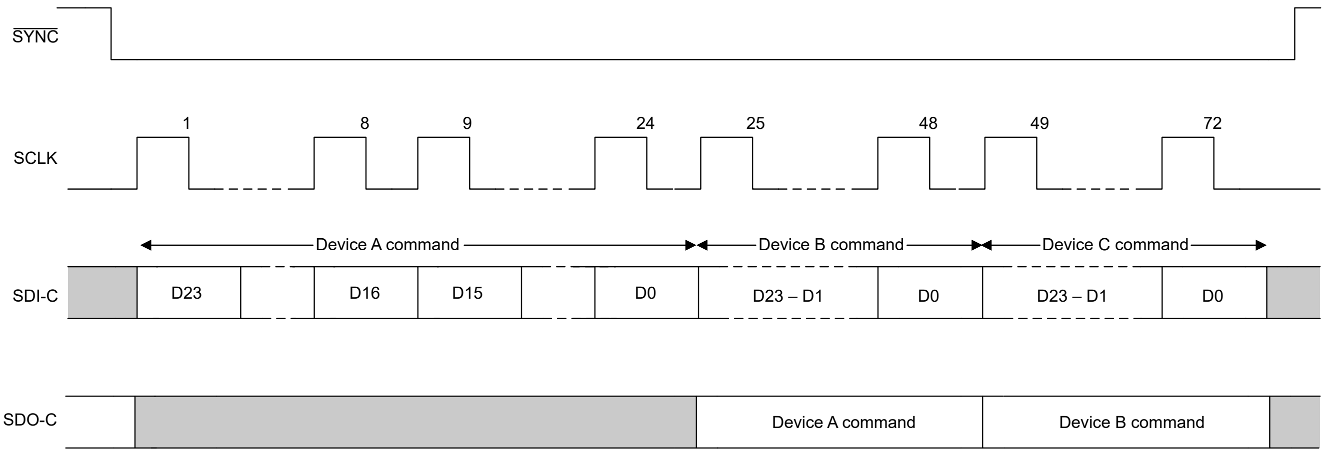


图 7-17. SPI Daisy-Chain Write Cycle

7.5.2 I^2C Programming Mode

The DACx300x devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0); see also 图 5-1. The I^2C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through the open drain I/O pins, SDA and SCL.

The I^2C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I^2C bus is typically a microcontroller or digital signal processor (DSP). The DACx300x family operates as a target on the I^2C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, the DACx300x family operates as a target receiver. A controller writes to the DACx300x, a target receiver. However, if a controller requires the DACx300x internal register data, the DACx300x operate as a target transmitter. In this case, the controller reads from the DACx300x. According to I^2C terminology, read and write refer to the controller.

The DACx300x family supports the following data transfer modes:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode plus (1.0 Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current would be 3 mA; similar to the case of standard and fast modes. The DACx300x family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I^2C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. 图 7-18 depicts a not-acknowledge, when the SDA line is left high during the high period of the ninth clock cycle.

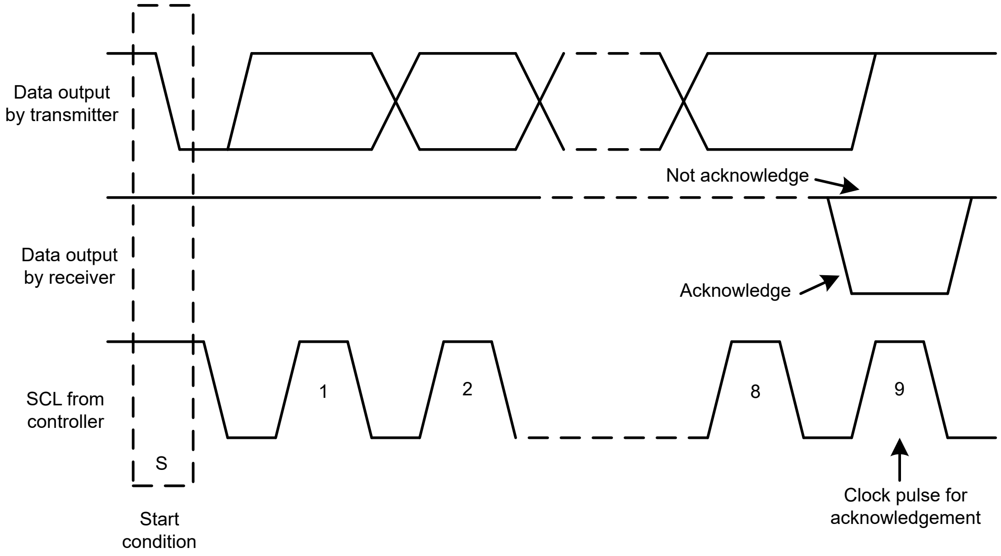


图 7-18. Acknowledge and Not Acknowledge on the I^2C Bus

7.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. 图 7-19 shows that the start condition is when a high-to-low transition occurs on the SDA line while SCL is high. All I^2C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit ($R/\overline{W}$) on the SDA line. During all transmissions, the controller makes sure that data are valid. 图 7-20 shows that a valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle (see also 图 7-18). When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit ($R/\overline{W}$ bit 0) or receive ($R/\overline{W}$ bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. 图 7-19 shows that to signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high. This action releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.

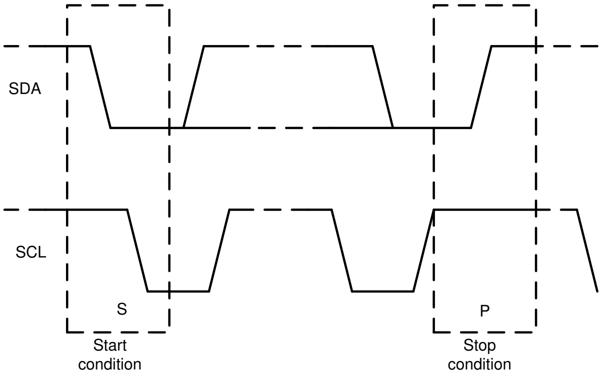


图 7-19. Start and Stop Conditions

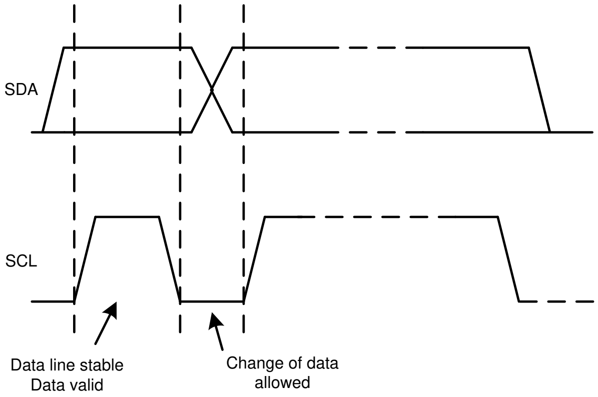


图 7-20. Bit Transfer on the I^2C Bus

7.5.2.2 I^{2}C Update Sequence

表 7-14 shows that for a single update, the DACx300x require a start condition, a valid I^{2}C address byte, a command byte, and two data bytes.

表 7-14. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte 节 7.5.2.2.1				Command byte 节 7.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

图 7-21 shows that after each byte is received, the DACx300x family acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I^{2}C address byte selects the DACx300x.

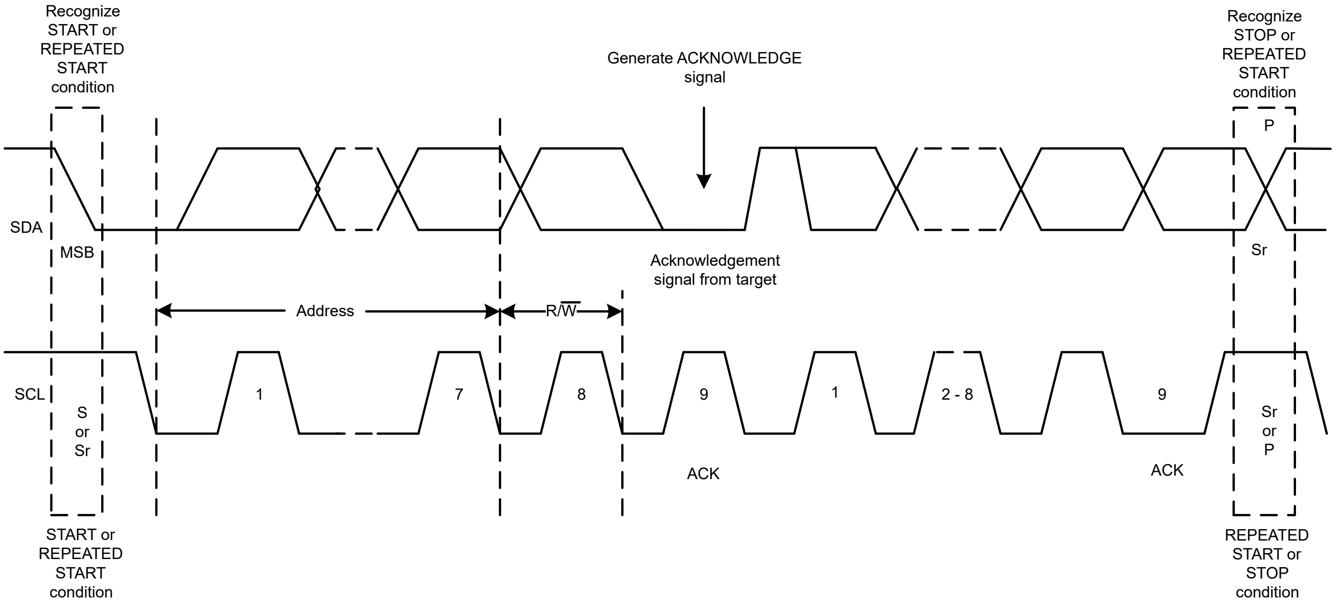


图 7-21. I^{2}C Bus Protocol

The command byte sets the operating mode of the selected DACx300x device. For a data update to occur when the operating mode is selected by this byte, the DACx300x device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The DACx300x device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the DACx300x device releases the I^{2}C bus and awaits a new start condition.

7.5.2.2.1 Address Byte

表 7-15 depicts the address byte, the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to 表 7-16.

表 7-15. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/$\overline{W}$
General address	1	0	0	1	See *Target Address* column in 表 7-16			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

表 7-16. Address Format

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The DACx300x supports broadcast addressing, which is used for synchronously updating or powering down multiple DACx300x devices. When the broadcast address is used, the DACx300x responds regardless of the address pin state. Broadcast is supported only in write mode.

7.5.2.2.2 Command Byte

表 7-21 lists the command byte in the ADDRESS column.

7.5.2.3 I^{2}C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the R/$\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the R/$\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

表 7-17. Read Sequence

S	MSB	…	R/$\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/$\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	Address byte 节 7.5.2.2.1				Command byte 节 7.5.2.2				Sr	Address byte 节 7.5.2.2.1				MSDB				LSDB			
From controller				Target	From controller			Target	From controller				Target	From target			Controller	From Target			Controller

7.5.3 General-Purpose Input/Output (GPIO) Modes

Together with I^{2}C and SPI, the DACx300x also support a GPIO that can be configured in the NVM for multiple functions. This pin allows for updating the DAC output channels and reading status bits without using the programming interface, thus enabling *processor-less* operation. In the GPIO-CONFIG register, write 1 to the GPI-EN bit to set the GPIO pin as an input, or write 1 to the GPO-EN bit to set the pin as output. There are global and channel-specific functions mapped to the GPIO pin. For channel-specific functions, select the channels using the GPI-CH-SEL field in the GPIO-CONFIG register. 表 7-18 lists the functional options available for the GPIO as input and 表 7-19 lists the options for the GPIO as output. Some of the GP input operations are edge-triggered after the device boots up. After the power supply ramps up, the device registers the GPI level and executes the associated command. This feature allows the user to configure the initial output state at power-on. By default, the GPIO pin is not mapped to any operation. When the GPIO pin is mapped to a specific input function, the corresponding software bit functionality is disabled to avoid a race condition. When used as a $\overline{\text{RESET}}$ input, the GPIO pin must transmit an active-low pulse for triggering a device reset. All other constraints of the functions are applied to the GPIO-based trigger.

备注

Pull the GPIO pin high or low when not used. When the GPIO pin is used as $\overline{\text{RESET}}$, the configuration must be programmed into the NVM. Otherwise, the setting is cleared after the device resets.

表 7-18. General-Purpose Input Function Map

REGISTER	BIT FIELD	VALUE	CHANNELS	GPIO EDGE / LEVEL	FUNCTION
GPIO-CONFIG	GPI-CONFIG	0000	All	Falling edge	Trigger DEEP-SLEEP mode.
				Rising edge	Bring the device out of deep-sleep.
		0010	All	Falling edge	Trigger FAULT-DUMP
				Rising edge	No effect
		0011	As per GPI-CH-SEL	Falling edge	IOUT power-down
				Rising edge	IOUT power-up
		0100	As per GPI-CH-SEL	Falling edge	VOUT power-down. Pulldown resistor as per the VOUT-PDN-X setting
				Rising edge	VOUT power-up
		0101	All	Falling edge	Trigger PROTECT function
				Rising edge	No effect
		0111	All	Falling edge	Trigger CLR function
				Rising edge	No effect
		1000	As per GPI-CH-SEL, both the SYNC-CONFIG-X and the GPI-CH-SEL must be configured for every channel.	Falling edge	Trigger LDAC function
				Rising edge	No effect
		1001	As per GPI-CH-SEL	Falling edge	Stop function generation
				Rising edge	Start function generation
		1010	As per GPI-CH-SEL	Falling edge	Trigger margin-low
				Rising edge	Trigger margin-high
		1011	All	Low pulse	Trigger device RESET. The RESET configuration must be programmed into the NVM.
				Rising edge	No effect
		1100	All	Falling edge	Allows NVM programming
				Rising edge	Blocks NVM programming
		1101	All	Falling edge	Allows register map update
				Rising edge	Blocks register map write except a write to the DEV-UNLOCK field through I^{2}C or SPI and to the RESET field through I^{2}C
		Others	N/A	N/A	Not applicable

表 7-19. General-Purpose Output (STATUS) Function Map

REGISTER	BIT FIELD	VALUE	FUNCTION
GPIO-CONFIG	GPO-CONFIG	0001	NVM-BUSY
		0100	DAC-1-BUSY
		0111	DAC-0-BUSY
		1000	WIN-CMP-1
		1011	WIN-CMP-0
		Others	Not applicable

7.6 Register Map

表 7-20. Register Map

<table>
<tr><th rowspan="2">REGISTER[(1) (2)]</th><th colspan="8">MOST SIGNIFICANT DATA BYTE (MSDB)</th><th colspan="8">LEAST SIGNIFICANT DATA BYTE (LSDB)</th></tr>
<tr><th>BIT15</th><th>BIT14</th><th>BIT13</th><th>BIT12</th><th>BIT11</th><th>BIT10</th><th>BIT9</th><th>BIT8</th><th>BIT7</th><th>BIT6</th><th>BIT5</th><th>BIT4</th><th>BIT3</th><th>BIT2</th><th>BIT1</th><th>BIT0</th></tr>
<tr><td>NOP</td><td colspan="16">NOP</td></tr>
<tr><td>DAC-X-MARGIN-HIGH</td><td colspan="12">DAC-X-MARGIN-HIGH</td><td colspan="4">X</td></tr>
<tr><td>DAC-X-MARGIN-LOW</td><td colspan="12">DAC-X-MARGIN-LOW</td><td colspan="4">X</td></tr>
<tr><td>DAC-X-VOUT-CMP-CONFIG</td><td colspan="3">X</td><td colspan="3">VOUT-X-GAIN</td><td colspan="5">X</td><td>CMP-X-OD-EN</td><td>CMP-X-OUT-EN</td><td>CMP-X-HIZ-IN-DIS</td><td>CMP-X-INV-EN</td><td>CMP-X-EN</td></tr>
<tr><td>DAC-X-IOUT-MISC-CONFIG</td><td colspan="3">X</td><td colspan="4">IOUT-X-RANGE</td><td colspan="9">X</td></tr>
<tr><td>DAC-X-CMP-MODE-CONFIG</td><td colspan="4">X</td><td colspan="2">CMP-X-MODE</td><td colspan="10">X</td></tr>
<tr><td>DAC-X-FUNC-CONFIG</td><td>CLR-SEL-X</td><td>SYNC-CONFIG-X</td><td>BRD-CONFIG-X</td><td colspan="13">FUNC-GEN-CONFIG-BLOCK-X</td></tr>
<tr><td>DAC-X-DATA</td><td colspan="12">DAC-X-DATA</td><td colspan="4">X</td></tr>
<tr><td>COMMON-CONFIG</td><td>WIN-LATCH-EN</td><td>DEV-LOCK</td><td>EE-READ-ADDR</td><td>EN-INT-REF</td><td colspan="2">VOUT-PDN-0</td><td>IOUT-PDN-0</td><td colspan="6">X</td><td colspan="2">VOUT-PDN-1</td><td>IOUT-PDN-1</td></tr>
<tr><td>COMMON-TRIGGER</td><td colspan="4">DEV-UNLOCK</td><td colspan="4">RESET</td><td>LDAC</td><td>CLR</td><td>X</td><td>FAULT-DUMP</td><td>PROTECT</td><td>READ-ONE-TRIG</td><td>NVM-PROG</td><td>NVM-RELOAD</td></tr>
<tr><td>COMMON-DAC-TRIG</td><td>RST-CMP-FLAG-1</td><td>TRIG-MAR-LO-1</td><td>TRIG-MAR-HI-1</td><td>START-FUNC-1</td><td colspan="8">X</td><td>RST-CMP-FLAG-0</td><td>TRIG-MAR-LO-0</td><td>TRIG-MAR-HI-0</td><td>START-FUNC-0</td></tr>
<tr><td>GENERAL-STATUS</td><td>NVM-CRC-FAIL-INT</td><td>NVM-CRC-FAIL-USER</td><td>X</td><td>DAC-BUSY-0</td><td colspan="2">X</td><td>DAC-BUSY-1</td><td>NVM-BUSY</td><td colspan="8">DEVICE-ID</td></tr>
<tr><td>CMP-STATUS</td><td colspan="7">X</td><td>PROTECT-FLAG</td><td>WIN-CMP-0</td><td colspan="2">X</td><td>WIN-CMP-1</td><td>CMP-FLAG-0</td><td colspan="2">X</td><td>CMP-FLAG-1</td></tr>
<tr><td>GPIO-CONFIG</td><td>GF-EN</td><td>DEEP-SLEEP-EN</td><td>GPO-EN</td><td colspan="4">GPO-CONFIG</td><td colspan="4">GPI-CH-SEL</td><td colspan="4">GPI-CONFIG</td><td>GPI-EN</td></tr>
<tr><td>DEVICE-MODE-CONFIG</td><td colspan="2">RESERVED</td><td>DIS-MODE-IN</td><td colspan="3">RESERVED</td><td colspan="2">PROTECT-CONFIG</td><td colspan="3">RESERVED</td><td colspan="5">X</td></tr>
<tr><td>INTERFACE-CONFIG</td><td colspan="3">X</td><td>TIMEOUT-EN</td><td colspan="3">X</td><td>EN-PMBUS</td><td colspan="5">X</td><td>FAST-SDO-EN</td><td>X</td><td>SDO-EN</td></tr>
<tr><td>SRAM-CONFIG</td><td colspan="8">X</td><td colspan="8">SRAM-ADDR</td></tr>
<tr><td>SRAM-DATA</td><td colspan="16">SRAM-DATA</td></tr>
<tr><td>BRDCAST-DATA</td><td colspan="12">BRDCAST-DATA</td><td colspan="4">X</td></tr>
<tr><td>PMBUS-PAGE</td><td colspan="8">PMBUS-PAGE</td><td colspan="8">Not applicable</td></tr>
<tr><td>PMBUS-OP-CMD</td><td colspan="8">PMBUS-OPERATION-CMD-X</td><td colspan="8">Not applicable</td></tr>
<tr><td>PMBUS-CML</td><td colspan="6">X</td><td>CML</td><td>X</td><td colspan="8">Not applicable</td></tr>
<tr><td>PMBUS-VERSION</td><td colspan="8">PMBUS-VERSON</td><td colspan="8">Not applicable</td></tr>
</table>

(1) The highlighted gray cells indicate the register bits or fields that are stored in the NVM.
(2) X = Don't care.

表 7-21. Register Names

I²C/SPI ADDRESS	PMBUS PAGE ADDR	PMBUS REGISTER ADDR	REGISTER NAME	SECTION
00h	FFh	D0h	NOP	节 7.6.1
01h	00h	25h	DAC-1-MARGIN-HIGH	节 7.6.2
02h	00h	26h	DAC-1-MARGIN-LOW	节 7.6.3
03h	FFh	D1h	DAC-1-VOUT-CMP-CONFIG	节 7.6.4
04h	FFh	D2h	DAC-1-IOUT-MISC-CONFIG	节 7.6.5
05h	FFh	D3h	DAC-1-CMP-MODE-CONFIG	节 7.6.6
06h	FFh	D4h	DAC-1-FUNC-CONFIG	节 7.6.7
13h	03h	25h	DAC-0-MARGIN-HIGH	节 7.6.1
14h	03h	26h	DAC-0-MARGIN-LOW	节 7.6.2
15h	FFh	DDh	DAC-0-VOUT-CMP-CONFIG	节 7.6.3
16h	FFh	DEh	DAC-0-IOUT-MISC-CONFIG	节 7.6.4
17h	FFh	DFh	DAC-0-CMP-MODE-CONFIG	节 7.6.5
18h	FFh	E0h	DAC-0-FUNC-CONFIG	节 7.6.6
19h	00h	21h	DAC-1-DATA	节 7.6.8
1Ch	03h	21h	DAC-0-DATA	节 7.6.8
1Fh	FFh	E3h	COMMON-CONFIG	节 7.6.9
20h	FFh	E4h	COMMON-TRIGGER	节 7.6.10
21h	FFh	E5h	COMMON-DAC-TRIG	节 7.6.11
22h	FFh	E6h	GENERAL-STATUS	节 7.6.12
23h	FFh	E7h	CMP-STATUS	节 7.6.13
24h	FFh	E8h	GPIO-CONFIG	节 7.6.14
25h	FFh	E9h	DEVICE-MODE-CONFIG	节 7.6.15
26h	FFh	EAh	INTERFACE-CONFIG	节 7.6.16
2Bh	FFh	EFh	SRAM-CONFIG	节 7.6.17
2Ch	FFh	F0h	SRAM-DATA	节 7.6.18
50h	FFh	F1h	BRDCAST-DATA	节 7.6.19
NA	All pages	00h	PMBUS-PAGE	节 7.6.20
NA	00h	01h	PMBIS-OP-CMD-0	节 7.6.21
NA	01h	01h	PMBUS-OP-CMD-1	节 7.6.21
NA	02h	01h	PMBUS-OP-CMD-2	节 7.6.21
NA	03h	01h	PMBUS-OP-CMD-3	节 7.6.21
NA	All pages	78h	PMBUS-CML	节 7.6.22
NA	All pages	98h	PMBUS-VERSION	节 7.6.23

表 7-22. Access Type Codes

Access Type	Code	Description
X	X	Don't care
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 NOP Register (address = 00h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D0h

图 7-22. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R-0h															

表 7-23. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R	0000h	No operation

7.6.2 DAC-X-MARGIN-HIGH Register (address = 13h, 01h) [reset = 0000h]

PMBus page address = 03h, 00h, PMBus register address = 25h

图 7-23. DAC-X-MARGIN-HIGH Register (X = 0, 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC6300x: DAC-X-MARGIN-HIGH[11:0] DAC5300x: DAC-X-MARGIN-HIGH[9:0]												X			
R/W̅-0h												X-0h			

表 7-24. DAC-X-MARGIN-HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC6300x: DAC-X-MARGIN-HIGH[11:0] DAC5300x: DAC-X-MARGIN-HIGH[9:0]	R/W̅	000h	Margin-high code for DAC output Data are in straight-binary format. MSB left aligned. Use the following bit alignment: DAC63001: {DAC-X-MARGIN-HIGH[11:0]} DAC63002: {DAC-X-MARGIN-HIGH[11:0]} DAC53001: {DAC-X-MARGIN-HIGH[9:0], X, X} DAC53002: {DAC-X-MARGIN-HIGH[9:0], X, X} X = Don't care bits.
3-0	X	X	0	Don't care

7.6.3 DAC-X-MARGIN-LOW Register (address = 14h, 02h) [reset = 0000h]

PMBus page address = 03h, 00h, PMBus register address = 26h

图 7-24. DAC-X-MARGIN-LOW Register (X = 0, 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC6300x: DAC-X-MARGIN-LOW[11:0] DAC5300x: DAC-X-MARGIN-LOW[9:0]												X			
R/W̅-0h												X-0h			

表 7-25. DAC-X-MARGIN-LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC6300x: DAC-X-MARGIN-LOW[11:0] DAC5300x: DAC-X-MARGIN-LOW[9:0]	R/W̅	000h	Margin-low code for DAC output Data are in straight-binary format. MSB left aligned. Use the following bit alignment: DAC63001: {DAC-X-MARGIN-HIGH[11:0]} DAC63002: {DAC-X-MARGIN-HIGH[11:0]} DAC53001: {DAC-X-MARGIN-HIGH[9:0], X, X} DAC53002: {DAC-X-MARGIN-HIGH[9:0], X, X} X = Don't care bits.
3-0	X	X	0	Don't care

7.6.4 DAC-X-VOUT-CMP-CONFIG Register (address = 15h, 03h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = DDh, D1h

图 7-25. DAC-X-VOUT-CMP-CONFIG Register (X = 0, 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			VOUT-GAIN-X			X					CMP-X-OD-EN	CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN
X-0h			R/W̅-0h			X-0h					R/W̅-0h	R/W̅-0h	R/W̅-0h	R/W̅-0h	R/W̅-0h

表 7-26. DAC-X-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-10	VOUT-GAIN-X	R/W̅	0h	000: Gain = 1x, external reference on VREF pin 001: Gain = 1x, VDD as reference 010: Gain = 1.5x, internal reference 011: Gain = 2x, internal reference 100: Gain = 3x, internal reference 101: Gain = 4x, internal reference Others: Invalid
9-5	X	X	0h	Don't care
4	CMP-X-OD-EN	R/W̅	0	0: Set OUTx pin as push-pull 1: Set OUTx pin as open-drain in comparator mode (CMP-X-EN = 1 and CMP-X-OUT-EN = 1)
3	CMP-X-OUT-EN	R/W̅	0	0: Generate comparator output but consume internally 1: Bring comparator output to the respective OUTx pin
2	CMP-X-HIZ-IN-DIS	R/W̅	0	0: FBx input has high-impedance. Input voltage range is limited. 1: FBx input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-X-INV-EN	R/W̅	0	0: Don't invert the comparator output 1: Invert the comparator output
0	CMP-X-EN	R/W̅	0	0: Disable comparator mode 1: Enable comparator mode. Current-output must be in power-down. Voltage-output mode must be enabled.

7.6.5 DAC-X-IOUT-MISC-CONFIG Register (address = 16h, 04h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = DEh, D2h

图 7-26. DAC-X-IOUT-MISC-CONFIG Register (X = 0, 1)

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">X</td><td colspan="4">IOUT-RANGE-X</td><td colspan="9">X</td></tr>
<tr><td colspan="3">X-0h</td><td colspan="4">R/W̅-0h</td><td colspan="9">X-0h</td></tr>
</table>

表 7-27. DAC-X-IOUT-MISC-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-9	IOUT-RANGE-X	R/W̅	0000	0000: 0 μA to 25 μA 0001: 0 μA to 50 μA 0010: 0 μA to 125 μA 0011: 0 μA to 250 μA 0100: 0 μA to –24 μA 0101: 0 μA to –48 μA 0110: 0 μA to –120 μA 0111: 0 μA to –240 μA 1000: –25 μA to +25 μA 1001: –50 μA to +50 μA 1010: –125 μA to +125 μA 1011: –250 μA to +250 μA Others: Invalid
8-0	X	X	000h	Don't care

7.6.6 DAC-X-CMP-MODE-CONFIG Register (address = 17h, 05h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = DFh, D3h

图 7-27. DAC-X-CMP-MODE-CONFIG Register (X = 0, 1)

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">X</td><td colspan="2">CMP-X-MODE</td><td colspan="10">X</td></tr>
<tr><td colspan="4">X-0h</td><td colspan="2">R/W̅-0h</td><td colspan="10">X-0h</td></tr>
</table>

表 7-28. DAC-X-CMP-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	00h	Don't care
11-10	CMP-X-MODE	R/W̅	00	00: No hysteresis or window function 01: Hysteresis provided using DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers 10: Window comparator mode with DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers setting window bounds 11: Invalid
9-0	X	X	000h	Don't care

7.6.7 DAC-X-FUNC-CONFIG Register (address = 18h, 06h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E0h, D4h

图 7-28. DAC-X-FUNC-CONFIG Register (X = 0, 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR-SEL-X	SYNC-CONFIG-X	BRD-CONFIG-X	FUNC-GEN-CONFIG-BLOCK												
R/$\overline{\text{W}}$-0h	R/$\overline{\text{W}}$-0h	R/$\overline{\text{W}}$-0h	R/$\overline{\text{W}}$-0h												

表 7-29. DAC-X-FUNC-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CLR-SEL-X	R/$\overline{\text{W}}$	0	0: Clear DAC-X to zero-scale 1: Clear DAC-X to mid-scale
14	SYNC-CONFIG-X	R/$\overline{\text{W}}$	0	0: DAC-X output updates immediately after a write command 1: DAC-X output updates with $\overline{\text{LDAC}}$ pin falling-edge or when the LDAC bit in the COMMON-TRIGGER register is set to 1
13	BRD-CONFIG-X	R/$\overline{\text{W}}$	0	0: Don't update DAC-X with broadcast command 1: Update DAC-X with broadcast command

表 7-30. Linear-Slew Mode: FUNC-GEN-CONFIG-BLOCK Field Descriptions

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-X	R/$\overline{\text{W}}$	0	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-X	R/$\overline{\text{W}}$	0	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-X	R/$\overline{\text{W}}$	0	0: Enable linear slew
6-4	CODE-STEP-X	R/$\overline{\text{W}}$	0	CODE-STEP for linear slew mode: 000: 1-LSB 001: 2-LSB 010: 3-LSB 011: 4-LSB 100: 6-LSB 101: 8-LSB 110: 16-LSB 111: 32-LSB
3-0	SLEW-RATE-X	R/$\overline{\text{W}}$	0	SLEW-RATE for linear slew mode: 0000: No slew for margin-high and margin-low. Invalid for waveform generation. 0001: 4 µs/step 0010: 8 µs/step 0011: 12 µs/step 0100: 18 µs/step 0101: 27.04 µs/step 0110: 40.48 µs/step 0111: 60.72 µs/step 1000: 91.12 µs/step 1001: 136.72 µs/step 1010: 239.2 µs/step 1011: 418.64 µs/step 1100: 732.56 µs/step 1101: 1282 µs/step 1110: 2563.96 µs/step 1111: 5127.92 µs/step

表 7-31. Logarithmic-Slew Mode: FUNC-GEN-CONFIG-BLOCK Field Descriptions

Bit	Field	Type	Reset	Description
12-11	PHASE-SEL-X	R/$\overline{W}$	0	00: 0° 01: 120° 10: 240° 11: 90°
10-8	FUNC-CONFIG-X	R/$\overline{W}$	0	000: Triangular wave 001: Sawtooth wave 010: Inverse sawtooth wave 100: Sine wave 111: Disable function generation Others: Invalid
7	LOG-SLEW-EN-X	R/$\overline{W}$	0	1: Enable logarithmic slew. In logarithmic slew mode, the DAC output moves from the DAC-X-MARGIN-LOW code to the DAC-X-MARGIN-HIGH code, or vice versa, in 3.125% steps. When slewing in the positive direction, the next step is (1 + 0.03125) times the current step. When slewing in the negative direction, the next step is (1 – 0.03125) times the current step. When DAC-X-MARGIN-LOW is 0, the slew starts from code 1. The time interval for each step is defined by RISE-SLEW-X and FALL-SLEW-X.
6-4	RISE-SLEW-X	R/$\overline{W}$	0	SLEW-RATE for logarithmic slew mode (DAC-X-MARGIN-LOW to DAC-X-MARGIN-HIGH): 000: 4 µs/step 001: 12 µs/step 010: 27.04 µs/step 011: 60.72 µs/step 100: 136.72 µs/step 101: 418.64 µs/step 110: 1282 µs/step 111: 5127.92 µs/step
3-1	FALL-SLEW-X	R/$\overline{W}$	0	SLEW-RATE for logarithmic slew mode (DAC-X-MARGIN-HIGH to DAC-X-MARGIN-LOW): 000: 4 µs/step 001: 12 µs/step 010: 27.04 µs/step 011: 60.72 µs/step 100: 136.72 µs/step 101: 418.64 µs/step 110: 1282 µs/step 111: 5127.92 µs/step
0	X	X	0	Don't care

7.6.8 DAC-X-DATA Register (address = 1Ch, 19h) [reset = 0000h]

PMBus page address = 03h, 00h, PMBus register address = 21h

图 7-29. DAC-X-DATA Register (X = 0, 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC6300x: DAC-X-DATA[11:0] DAC5300x: DAC-X-DATA[9:0]												X			
R/W-0h												X-0h			

表 7-32. DAC-X-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC6300x: DAC-X-DATA[11:0] DAC5300x: DAC-X-DATA[9:0]	R/W	000h	Data for DAC output Data are in straight-binary format. MSB left-aligned. MSB left-aligned. Use the following bit-alignment: DAC63001: {DAC-X-MARGIN-HIGH[11:0]} DAC63002: {DAC-X-MARGIN-HIGH[11:0]} DAC53001: {DAC-X-MARGIN-HIGH[9:0], X, X} DAC53002: {DAC-X-MARGIN-HIGH[9:0], X, X} X = Don't care bits.
3-0	X	X	0h	Don't care

7.6.9 COMMON-CONFIG Register (address = 1Fh) [reset = 0FFFh]

PMBus page address = FFh, PMBus register address = E3h

图 7-30. COMMON-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIN-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	VOUT-PDN-0		IOUT-PDN-0	Don't care						VOUT-PDN-1		IOUT-PDN-1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-11b		R/W-1b	X-11h						R/W-11b		R/W-1b

表 7-33. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	WIN-LATCH-EN	R/W	0	0: Non-latching window-comparator output 1: Latching window-comparator output
14	DEV-LOCK	R/W	0	0: Device not locked 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	EE-READ-ADDR	R/W	0	0: Fault-dump read enable at address 0x00 1: Fault-dump read enable at address 0x01
12	EN-INT-REF	R/W	0	0: Disable internal reference 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10, 2-1	VOUT-PDN-X	R/W	11	00: Power-up VOUT-X 01: Power-down VOUT-X with 10 kΩ to AGND 10: Power-down VOUT-X with 100 kΩ to AGND 11: Power-down VOUT-X with Hi-Z to AGND
9, 0	IOUT-PDN-X	R/W	1	0: Power-up IOUT-X 1: Power-down IOUT-X
8-3	X	X	11h	Don't care

7.6.10 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E4h

图 7-31. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				LDAC	CLR	X	FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD
R/W̄-0h				R/W̄-0h				R/W̄-0h	R/W̄-0h	X-0h	R/W̄-0h	R/W̄-0h	R/W̄-0h	R/W̄-0h	R/W̄-0h

表 7-34. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W̄	0000	0101: Device unlocking password Others: Don't care
11-8	RESET	W̄	0000	1010: POR reset triggered. This bit self-resets. Others: Don't care
7	LDAC	R/W̄	0	0: LDAC operation not triggered 1: LDAC operation triggered if the respective SYNC-CONFIG-X bit in the DAC-X-FUNC-CONFIG register is 1. This bit self-resets.
6	CLR	R/W̄	0	0: DAC registers and outputs unaffected 1: DAC registers and outputs set to zero-code or mid-code based on the respective CLR-SEL-X bit in the DAC-X-FUNC-CONFIG register. This bit self-resets.
5	X	X	0	Don't care
4	FAULT-DUMP	R/W̄	0	0: Fault-dump is not triggered 1: Triggers fault-dump sequence. This bit self-resets.
3	PROTECT	R/W̄	0	0: PROTECT function not triggered 1: Trigger PROTECT function. This bit is self-resetting.
2	READ-ONE-TRIG	R/W̄	0	0: Fault-dump read not triggered 1: Read one row of NVM for fault-dump. This bit self-resets.
1	NVM-PROG	R/W̄	0	0: NVM write not triggered 1: NVM write triggered. This bit self-resets.
0	NVM-RELOAD	R/W̄	0	0: NVM reload not triggered 1: Reload data from NVM to register map. This bit self-resets.

7.6.11 COMMON-DAC-TRIG Register (address = 21h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E5h

图 7-32. COMMON-DAC-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	Don't care								RESET-CMP-FLAG-0	TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0
W̄-0h	W̄-0h	W̄-0h	R/W̄-0h	X-0h								W̄-0h	W̄-0h	W̄-0h	R/W̄-0h

表 7-35. COMMON-DAC-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15, 3	RESET-CMP-FLAG-X	W̄	0	0: Latching-comparator output unaffected 1: Reset latching-comparator and window-comparator output. This bit self-resets.
14, 2	TRIG-MAR-LO-X	W̄	0	0: Don't care 1: Trigger margin-low command. This bit self-resets.
13, 1	TRIG-MAR-HI-X	W̄	0	0: Don't care 1: Trigger margin-high command. This bit self-resets.
12, 0	START-FUNC-X	R/W̄	0	0: Stop function generation 1: Start function generation as per FUNC-GEN-CONFIG-X in the DAC-X-FUNC-CONFIG register.
11-4	X	X	0h	Don't care

7.6.12 GENERAL-STATUS Register (address = 22h) [reset = 00h, DEVICE-ID, VERSION-ID]

PMBus page address = FFh, PMBus register address = E6h

图 7-33. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-0-BUSY	X		DAC-1-BUSY	X	DEVICE-ID						VERSION-ID	
R-0h	R-0h	R-0h	R-0h	X-0h		R-0h	X-0h	R						R-0h	

表 7-36. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this temporary error condition.
13	X	R	0	Don't care
12	DAC-0-BUSY	R	0	0: DAC-0 channel can accept commands 1: DAC-0 channel does not accept commands
11-10	X	X	0	Don't care
9	DAC-1-BUSY	R	0	0: DAC-1 channel can accept commands 1: DAC-1 channel does not accept commands
8	X	R	0	Don't care
7-2	DEVICE-ID	R	DAC63002: 08h DAC63001: 09h DAC53002: 0Ah DAC53001: 0Bh	Device identifier
1-0	VERSION-ID	R	00	Version identifier

7.6.13 CMP-STATUS Register (address = 23h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E7h

图 7-34. CMP-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X							PROTECT-FLAG	WIN-CMP-0	X		WIN-CMP-1	CMP-FLAG-0	X		CMP-FLAG-1
X-0h							R-0h	R-0h	X-0h		R-0h	R-0h	X-0h		R-0h

表 7-37. CMP-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9, 6-5, 2-1	X	X	0	Don't care
8	PROTECT-FLAG	R	0	0: PROTECT operation not triggered. 1: PROTECT function is completed or in progress. This bit resets to 0 when read.
7, 4	WIN-CMP-X	R	0	Window comparator output from respective channels. The output is latched or unlatched based on the WINDOW-LATCH-EN setting in the COMMON-CONFIG register.
3, 0	CMP-FLAG-X	R	0	Synchronized comparator output from respective channels.

7.6.14 GPIO-CONFIG Register (address = 24h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E8h

图 7-35. GPIO-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GF-EN	X	GPO-EN	GPO-CONFIG				GPI-CH-SEL				GPI-CONFIG				GPI-EN
R/$\overline{\text{W}}$-0h	X-0h	R/$\overline{\text{W}}$-0h	R/$\overline{\text{W}}$-0h				R/$\overline{\text{W}}$-0h				R/$\overline{\text{W}}$-0h				R/$\overline{\text{W}}$-0h

表 7-38. GPIO-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GF-EN	R/$\overline{\text{W}}$	0	0: Glitch filter disabled for GP input. This setting provides faster response. 1: Glitch filter enabled for GPI. This setting introduces additional propagation delay but provides robustness.
14	X	X	0	Don't care.
13	GPO-EN	R/$\overline{\text{W}}$	0	0: Disable output mode for GPIO pin. 1: Enable output mode for GPIO pin.
12-9	GPO-CONFIG	R/$\overline{\text{W}}$	0000	$\overline{\text{STATUS}}$ function setting. The GPIO pin is mapped to the following register bits as output: 0001: NVM-BUSY 0100: DAC-1-BUSY 0111: DAC-0-BUSY 1000: WIN-CMP-1 1011:WIN-CMP-0 Others: NA
8-5	GPI-CH-SEL	R/$\overline{\text{W}}$	0000	Two bits correspond to two DAC channels. 0b is *disabled* and 1b is *enabled*. GPI-CH-SEL[0]: Channel 1 GPI-CH-SEL[3]: Channel 0 Example: when GPI-CH-SEL is 1001, both channel-0 and channel-1 are enabled.

表 7-38. GPIO-CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-1	GPI-CONFIG	R/$\overline{\text{W}}$	0000	GPIO pin input configuration. Global settings act on the entire device. Channel-specific settings are dependent on the channel selection by the GPI-CH-SEL bits: 0000: $\overline{\text{DEEP-SLEEP}}$ (global). GPIO falling edge triggers deep-sleep mode, GPIO rising edge brings the device out of deep-sleep. 0010: $\overline{\text{FAULT-DUMP}}$ (global). GPIO falling edge triggers fault dump, GPIO = 1 has no effect. 0011: IOUT power up-down (channel-specific). GPIO falling edge triggers power down, GPIO rising edge triggers power up. 0100: VOUT power up-down (channel-specific). The output load is as per the VOUT-PDN-X setting. GPIO falling edge triggers power down, GPIO rising edge triggers power up. 0101: $\overline{\text{PROTECT}}$ input (global). GPIO falling edge asserts $\overline{\text{PROTECT}}$ function, GPIO = 1 has no effect. 0111: $\overline{\text{CLR}}$ input (global). GPIO = 0 asserts $\overline{\text{CLR}}$ function, GPIO = 1 has no effect. 1000: $\overline{\text{LDAC}}$ input (channel-specific). GPIO falling edge asserts $\overline{\text{LDAC}}$ function, GPIO = 1 has no effect. Both the SYNC-CONFIG-X and the GPI-CH-SEL must be configured for every channel. 1001: Start and stop function generation (channel-specific). GPIO falling edge stops function generation. GPIO rising edge starts function generation. 1010: Trigger margin high-low (channel-specific). GPIO falling edge triggers margin low. GPIO rising edge triggers margin high. 1011: $\overline{\text{RESET}}$ input (global). The falling edge of the GPIO pin asserts the $\overline{\text{RESET}}$ function. The $\overline{\text{RESET}}$ input must be a pulse. The GPIO rising edge brings the device out of reset. The $\overline{\text{RESET}}$ configuration must be programmed into the NVM. Otherwise the setting is cleared after the device reset. 1100: NVM write protection (global). GPIO falling edge allows NVM programming. GPIO rising edge blocks NVM programming. 1101: Register-map lock (global). GPIO falling edge allows update to the register map. GPIO rising edge blocks any register map update except a write to the DEV-UNLOCK field through I^2C or SPI and to the RESET field through I^2C. Others: Invalid
0	GPI-EN	R/$\overline{\text{W}}$	0	0: Disable input mode for GPIO pin. 1: Enable input mode for GPIO pin.

7.6.15 DEVICE-MODE-CONFIG Register (address = 25h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E9h

图 7-36. DEVICE-MODE-CONFIG Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>DIS-MODE-IN</td><td colspan="3">RESERVED</td><td colspan="2">PROTECT-CONFIG</td><td colspan="3">RESERVED</td><td colspan="5">X</td></tr>
<tr><td colspan="2">R/$\overline{W}$-0h</td><td>R/$\overline{W}$-0h</td><td colspan="3">R/$\overline{W}$-0h</td><td colspan="2">R/$\overline{W}$-0h</td><td colspan="3">R/$\overline{W}$-0h</td><td colspan="5">X-0h</td></tr>
</table>

表 7-39. DEVICE-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/$\overline{W}$	00	Always write 0b00
13	DIS-MODE-IN	R/$\overline{W}$	0	Write 1 to this bit for low-power consumption.
12-10	RESERVED	R/$\overline{W}$	0	Always write 0b000
9-8	PROTECT-CONFIG	R/$\overline{W}$	00	00: Switch to Hi-Z power-down (no slew) 01: Switch to DAC code stored in NVM (no slew) and then switch to Hi-Z power-down 10: Slew to margin-low code and then switch to Hi-Z power-down 11: Slew to margin-high code and then switch to Hi-Z power-down
7-5	RESERVED	R/$\overline{W}$	0	Always write 0b000
4-0	X	R/$\overline{W}$	00h	Don't care

7.6.16 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

图 7-37. INTERFACE-CONFIG Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">X</td><td>TIMEOUT-EN</td><td colspan="3">X</td><td>EN-PMBUS</td><td colspan="5">X</td><td>FSDO-EN</td><td>X</td><td>SDO-EN</td></tr>
<tr><td colspan="3">X-0h</td><td>R/$\overline{W}$-0h</td><td colspan="3">X-0h</td><td>R/$\overline{W}$-0h</td><td colspan="5">X-0h</td><td>R/$\overline{W}$-0h</td><td>X-0h</td><td>R/$\overline{W}$-0h</td></tr>
</table>

表 7-40. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12	TIMEOUT-EN	R/$\overline{W}$	0	0: I^2C timeout disabled 1: I^2C timeout enabled
11-9	X	X	0h	Don't care
8	EN-PMBUS	R/$\overline{W}$	0	0: PMBus disabled 1: Enable PMBus
7-3	X	X	00h	Don't care
2	FSDO-EN	R/$\overline{W}$	0	0: Fast SDO disabled 1: Fast SDO enabled
1	X	X	0	Don't care
0	SDO-EN	R/$\overline{W}$	0	0: SDO disabled 1: SDO enabled on GPIO pin

7.6.17 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

PMBus page address = FFh, PMBus register address = EFh

图 7-38. SRAM-CONFIG Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">X</td><td colspan="8">SRAM-ADDR</td></tr>
<tr><td colspan="8">X-0h</td><td colspan="8">R/$\overline{W}$-0h</td></tr>
</table>

表 7-41. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	0h	Don't care
7-0	SRAM-ADDR	R/$\overline{W}$	0h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a write to the SRAM.

7.6.18 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

PMBus page address = FFh, PMBus register address = F0h

图 7-39. SRAM-DATA Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">SRAM-DATA</td></tr>
<tr><td colspan="16">R/$\overline{W}$-0h</td></tr>
</table>

表 7-42. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-ADDR	R/$\overline{W}$	0h	16-bit SRAM data. This data is written to or read from the address configured in the SRAM-CONFIG register.

7.6.19 BRDCAST-DATA Register (address = 50h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = F1h

图 7-40. BRDCAST-DATA Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="12">DAC6300x: BRDCAST-DATA[11:0]
DAC5300x: BRDCAST-DATA[9:0]</td><td colspan="4">X</td></tr>
<tr><td colspan="12">R/$\overline{W}$-0h</td><td colspan="4">X-0h</td></tr>
</table>

表 7-43. BRDCAST-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DAC6300x: BRDCAST-DATA[11:0] DAC5300x: BRDCAST-DATA[9:0]	R/$\overline{W}$	000h	Broadcast code for all DAC channels Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: DAC63001: {DAC-X-MARGIN-HIGH[11:0]} DAC63002: {DAC-X-MARGIN-HIGH[11:0]} DAC53001: {DAC-X-MARGIN-HIGH[9:0], X, X} DAC53002: {DAC-X-MARGIN-HIGH[9:0], X, X} X = Don't care bits. The BRD-CONFIG-X bit in the DAC-X-FUNC-CONFIG register must be enabled for the respective channels.
3-0	X	X	0h	Don't care.

7.6.20 PMBUS-PAGE Register [reset = 0300h]

PMBus page address = X, PMBus register address = 00h

图 7-41. PMBUS-PAGE Register

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">PMBUS-PAGE</td><td colspan="8">X</td></tr>
<tr><td colspan="8">R/$\overline{W}$-03h</td><td colspan="8">X-00h</td></tr>
</table>

表 7-44. PMBUS_OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PMBUS-PAGE	R/$\overline{W}$	03h	8-bit PMBus page address as specified in 表 7-21.
7-0	X	X	00h	Not applicable

7.6.21 PMBUS-OP-CMD-X Register [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 01h

图 7-42. PMBUS-OP-CMD-X Register (X = 0, 1, 2, 3)

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">PMBUS-OPERATION-CMD-X</td><td colspan="8">X</td></tr>
<tr><td colspan="8">R/$\overline{W}$-00h</td><td colspan="8">X-00h</td></tr>
</table>

表 7-45. PMBUS-OP-CMD-X Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PMBUS-OPERATION-CMD-X	R/$\overline{W}$	00h	PMBus operation commands: 00h: Turn off 80h: Turn on A4h: Margin high, DAC output margins high to DAC-X-MARGIN-HIGH code 94h: Margin low, DAC output margins low to DAC-X-MARGIN-LOW code
7-0	X	X	00h	Not applicable

7.6.22 PMBUS-CML Register [reset = 0000h]

PMBus page address = X, PMBus register address = 78h

图 7-43. PMBUS-CML Register

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="6">X</td><td>CML</td><td>X</td><td colspan="8">N/A</td></tr>
<tr><td colspan="6">X-00h</td><td>R/$\overline{W}$-0h</td><td>X-0h</td><td colspan="8">X-00h</td></tr>
</table>

表 7-46. PMBUS-CML Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	X	X	00h	Don't care
9	CML	R/$\overline{W}$	0h	0: No communication fault 1: PMBus communication fault for write with incorrect number of clocks, read before write command, invalid command address, and invalid or unsupported data value; reset this bit by writing 1.
8	X	X	0h	Don't care
7-0	X	X	00h	Not applicable

7.6.23 PMBUS-VERSION Register [reset = 2200h]

PMBus page address = X, PMBus register address =98h

图 7-44. PMBUS-VERSION Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-VERSION								X							
R-22h								X-00h							

表 7-47. PMBUS-VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	PMBUS-VERSION	R	22h	PMBus version
7-0	X	X	00h	Not applicable

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’ s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DACx300x are single-channel and dual-channel buffered, force-sense output, voltage-output and current-output smart DACs that include an NVM and internal reference, and available in a tiny 3-mm × 3-mm package.

- In voltage-output mode, short the OUTx and FBx pins for each channel. In current-output mode, leave the FBx pins unconnected. The FBx pins function as inputs in comparator mode.
- The external reference must not exceed VDD, either during transient or steady-state conditions. For the best Hi-Z output performance, use a pullup resistor on the VREF pin to VDD.
- In case VDD remains floating during the off condition, place a 100-kΩ resistor to AGND for proper detection of the VDD off condition for voltage margining.
- All the digital outputs are open drain; use external pullup resistors on these pins.
- The interface protocol is detected at power-on, and the device locks to the protocol as long as VDD is on.
- When allocating nonoverlapping I^2C addresses on a system I^2C bus, consider the broadcast address as well. I^2C timeout can be enabled for robustness.
- SPI mode is 3-wire by default. Configure the GPIO pin as SDO in the NVM for SPI readback capability. The SPI clock speed in readback mode is slower than in write mode.
- Power-down mode sets the DAC outputs to Hi-Z by default. Change the configuration appropriately for different power-down settings. The DAC channels can also power-up with a programmed DAC code in NVM.

8.2 Typical Application

A power-supply margining and scaling circuit is used to trim, scale, or test the output of a power converter. This example circuit is used to test a system by margining the power supplies for adaptive voltage scaling or to program a desired value at the output. Adjustable power supplies, such as low-dropout regulators (LDOs) and DC/DC converters, provide a feedback or adjust the input that is used to set the desired output. A precision voltage-output DAC is the best choice for controlling the power-supply output linearly. 图 8-1 shows a control circuit for a switch-mode power supply (SMPS) using the DACx300x. Typical applications of power-supply margining are communications equipment, enterprise servers, test and measurement, and general-purpose power-supply modules.

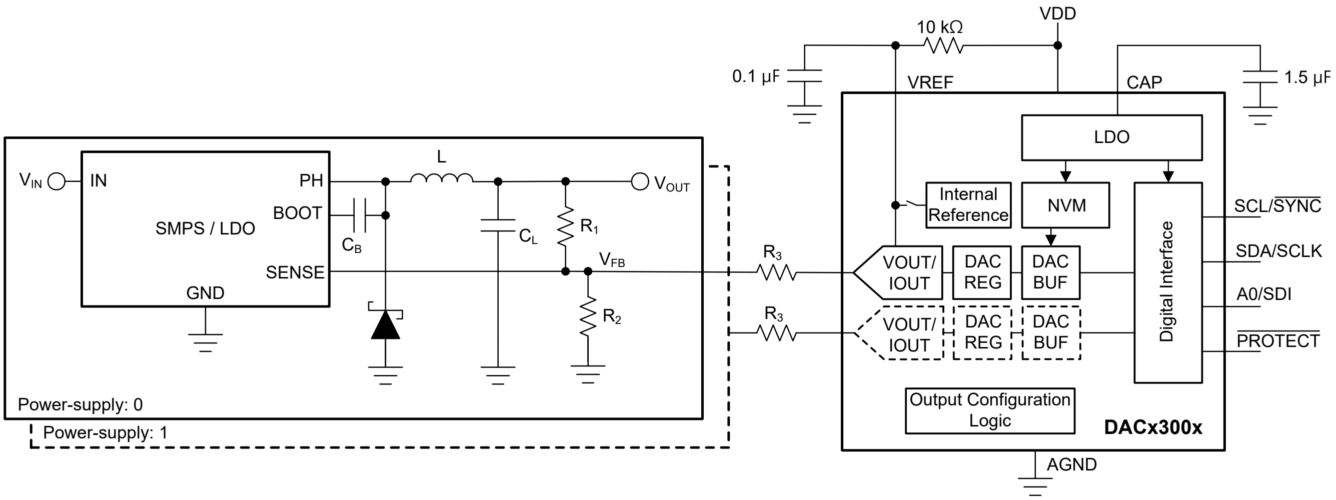


图 8-1. Voltage Margining and Scaling

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Power-supply nominal output	3.3 V
Reference voltage of the converter (V_{FB})	0.6 V
Margin	±10% (that is, 2.97 V to 3.63 V)
DAC output range	1.8 V
Nominal current through R_1 and R_2	100 µA

8.2.2 Detailed Design Procedure

The DACx300x features a Hi-Z power-down mode that is set by default at power-up, unless the device is programmed otherwise using the NVM. When the DAC output is at Hi-Z, the current through R_3 is zero and the SMPS is set at the nominal output voltage of 3.3 V. To have the same nominal condition when the DAC powers up, bring up the device at the same output as V_{FB} (that is 0.6 V). This configuration makes sure there is no current through R_3 even at power-up. Calculate R_1 as (V_{OUT} – V_{FB}) / 100 µA = 27 kΩ.

To achieve ±10% margin-high and margin-low conditions, the DAC must sink or source additional current through R_1. Calculate the current from the DAC (I_{MARGIN}) using 方程式 10 as 12 µA.

$$I_{MARGIN} = \left(\frac{V_{OUT} \times (1 + MARGIN) - V_{FB}}{R_1} \right) - I_{NOMINAL} \tag{10}$$

where

- I_{MARGIN} is the margin current sourced or sinked from the DAC.
- MARGIN is the percentage margin value divided by 100.
- $I_{NOMINAL}$ is the nominal current through R_1 and R_2.
- V_{OUT} is the output voltage of the respective DAC channel.
- V_{FB} is the reference voltage at the SENSE node of the power converter.
- R_1 is the resistance between the output and SENSE pin of the power converter.

To calculate the value of R_3, first decide the DAC output range, and make sure to avoid the codes near zero-scale and full-scale for safe operation in the linear region. A DAC output of 20 mV is a safe consideration as the minimum output, and (1.8 V – 0.6 V – 20 mV = 1.18 V) as the maximum output. When the DAC output is at 20 mV, the power supply goes to margin high, and when the DAC output is at 1.18 V, the power supply goes to margin low. Calculate the value of R_3 using 方程式 11 as 48.3 kΩ. Choose a standard resistor value and adjust the DAC outputs. Choosing R_3 = 47 kΩ makes the DAC margin high code as 1.164 V and the DAC margin low code as 36 mV.

$$R_3 = \frac{|V_{DAC} - V_{FB}|}{I_{MARGIN}} \tag{11}$$

When the DACx300x are set to current-output mode, series resistor R_3 is not required. Set the DAC output at the current-output range of –25 µA to +25 µA, and set the DAC code accordingly to achieve a margin current of ±12 µA.

The DACx300x have a slew-rate feature that is used to toggle between margin high, margin low, and nominal outputs with a defined slew rate; see also 节 7.6.7.

备注

The DAC-X-MARGIN-HIGH register value in DACx300x results in the *margin-low* value at the power supply output. Similarly, the DAC-X-MARGIN-LOW register value in DACx300x results in the *margin-high* value at the power-supply output.

The pseudocode for getting started with a power-supply control application is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Write DAC code for nominal output (repeat for all DAC channels)
//For a 1.8-V output range, the 10-bit hex code for 0.6 V is 0x155. With 16-bit left alignment,
this becomes 0x5540
WRITE DAC_0_DATA(0x1C), 0x55, 0x40
//Power-up voltage output on both the channels, enables internal reference
WRITE COMMON-CONFIG(0x1F), 0x12, 0x01
//Set channel 0 gain setting to 1.5x internal reference (1.8 V)
WRITE DAC-0-VOUT-CMP-CONFIG(0x15), 0x08, 0x00
//Set channel 1 gain setting to 1.5x internal reference (1.8 V)
WRITE DAC-1-VOUT-CMP-CONFIG(0x3), 0x08, 0x00
//Configure GPI for Margin-High, Low trigger for all channels
WRITE GPIO-CONFIG(0x24), 0x01, 0x35
//Set slew rate and code step (repeat for all channels)
//CODE_STEP: 2 LSB, SLEW_RATE: 60.72 µs/step
WRITE DAC-0-FUNC-CONFIG(0x18), 0x00, 0x17
//Write DAC margin high code (repeat for all channels)
//For a 1.8-V output range, the 10-bit hex code for 1.164 V is 0x296. With 16-bit left alignment,
this becomes 0xA540
WRITE DAC-0-MARGIN-HIGH(0x13), 0xA5, 0x40
//Write DAC margin low code (repeat for all channels)
//For a 1.8-V output range, the 10-bit hex code for 36 mV is 0x14. With 16-bit left alignment, this
becomes 0x0500
WRITE DAC-0-MARGIN-LOW(0x14), 0x05, 0x00
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

8.2.3 Application Curves

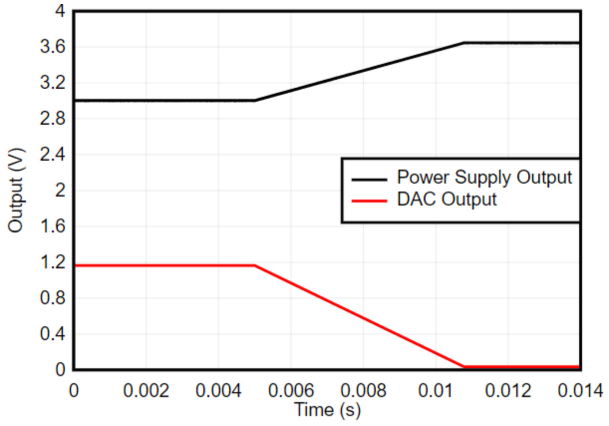


图 8-2. Power-Supply Margin High

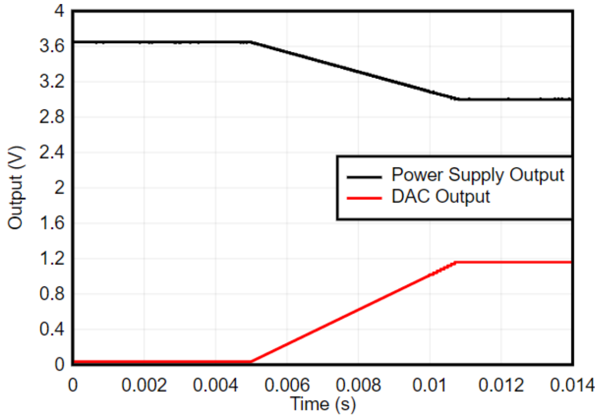


图 8-3. Power-Supply Margin Low

9 Power Supply Recommendations

The DACx300x family of devices does not require specific power-supply sequencing. These devices require a single power supply, V_{DD}. However, make sure the external voltage reference is applied after VDD. Use a 0.1-μF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately 1.5 μF for the CAP pin.

10 Layout

10.1 Layout Guidelines

The DACx300x pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

10.2 Layout Example

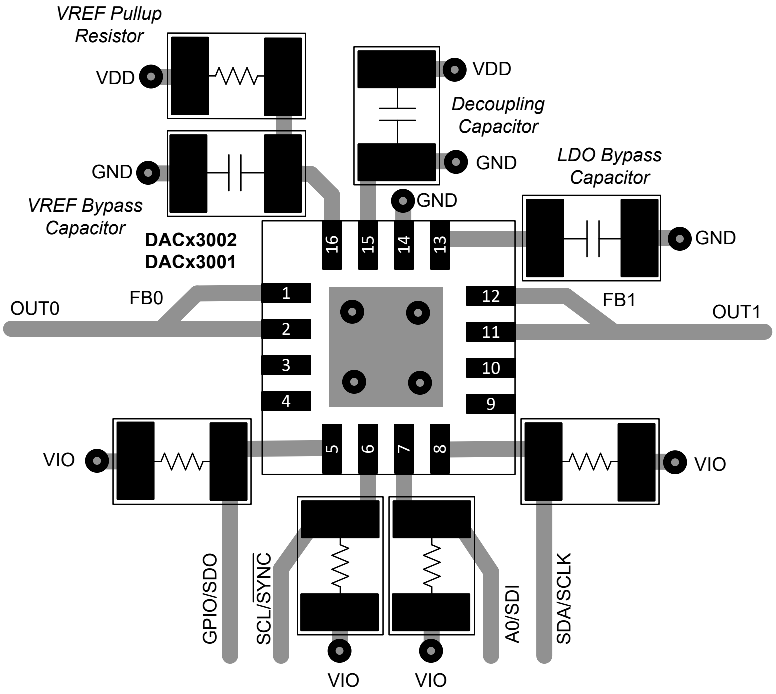


图 10-1. Layout Example

Note: The ground and power planes have been omitted for clarity. Connect the thermal pad to ground.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

PMBus™ is a trademark of SMIF, Inc..
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC53001RTER	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53001
DAC53001RTER.A	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53001
DAC53002RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53002
DAC53002RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53002
DAC63001RTER	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63001
DAC63001RTER.A	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63001
DAC63002RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63002
DAC63002RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D63002

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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GENERIC PACKAGE VIEW

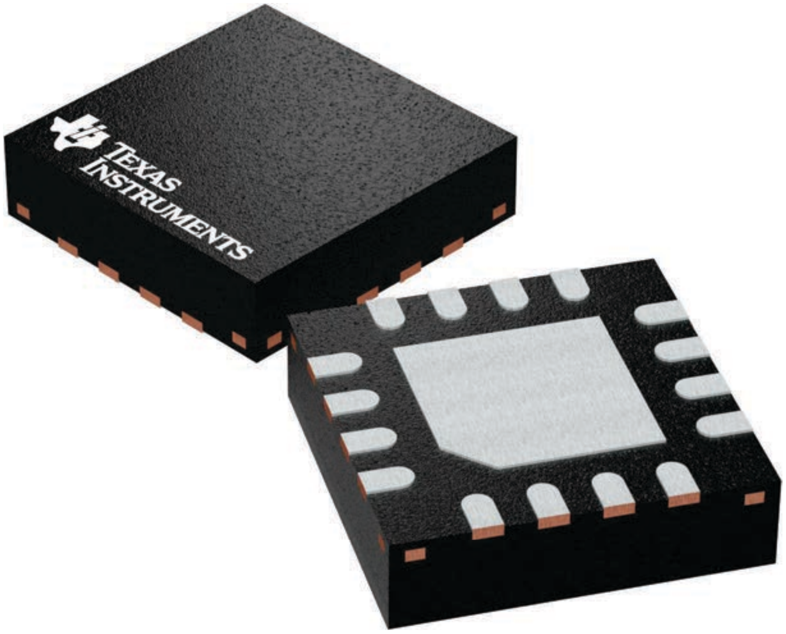
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

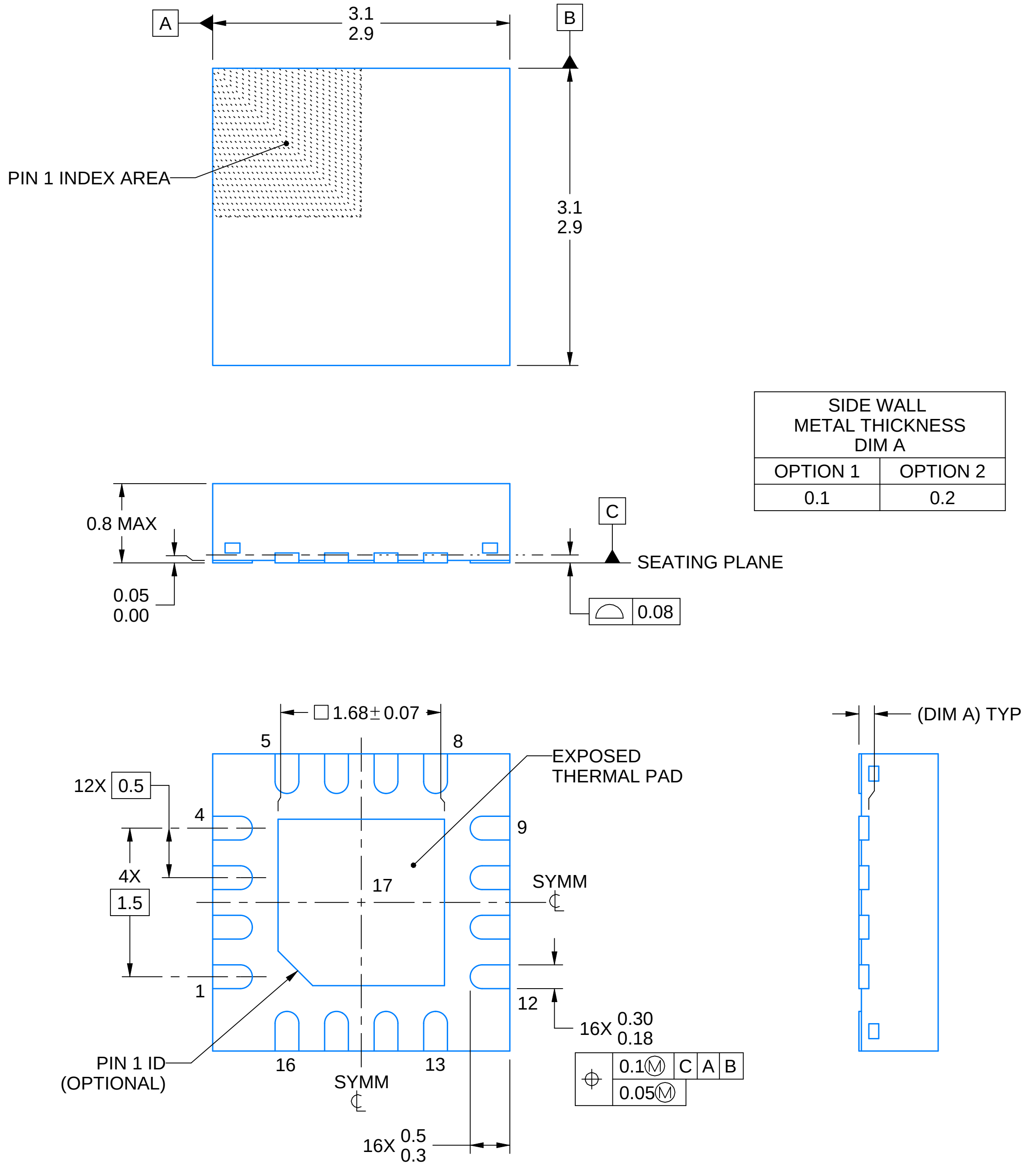


PACKAGE OUTLINE

RTE0016C

WQFN - 0.8 mm max height

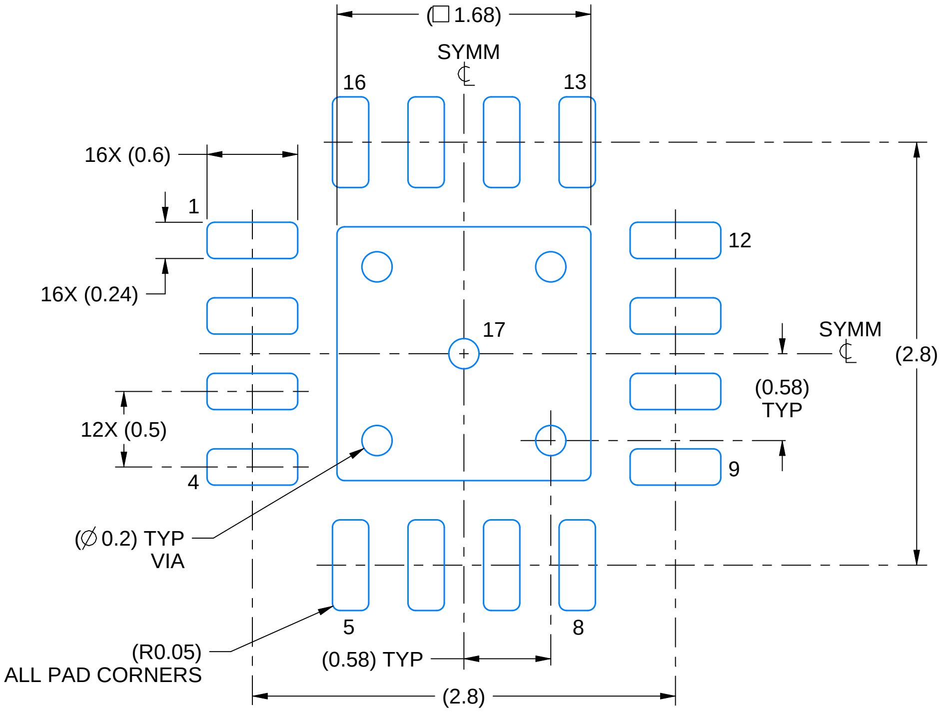
PLASTIC QUAD FLATPACK - NO LEAD



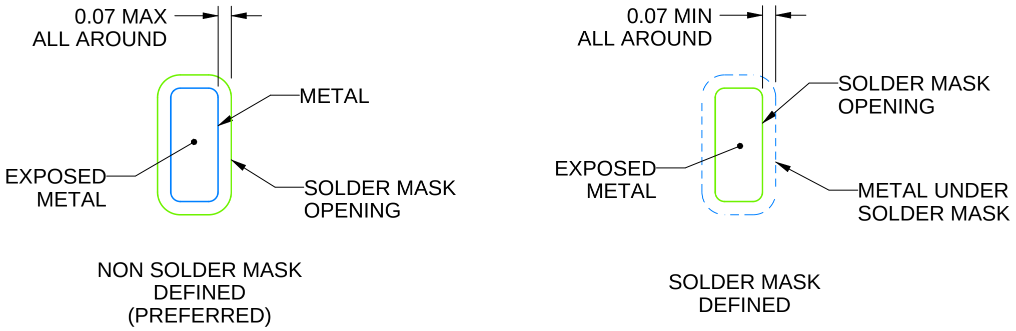
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

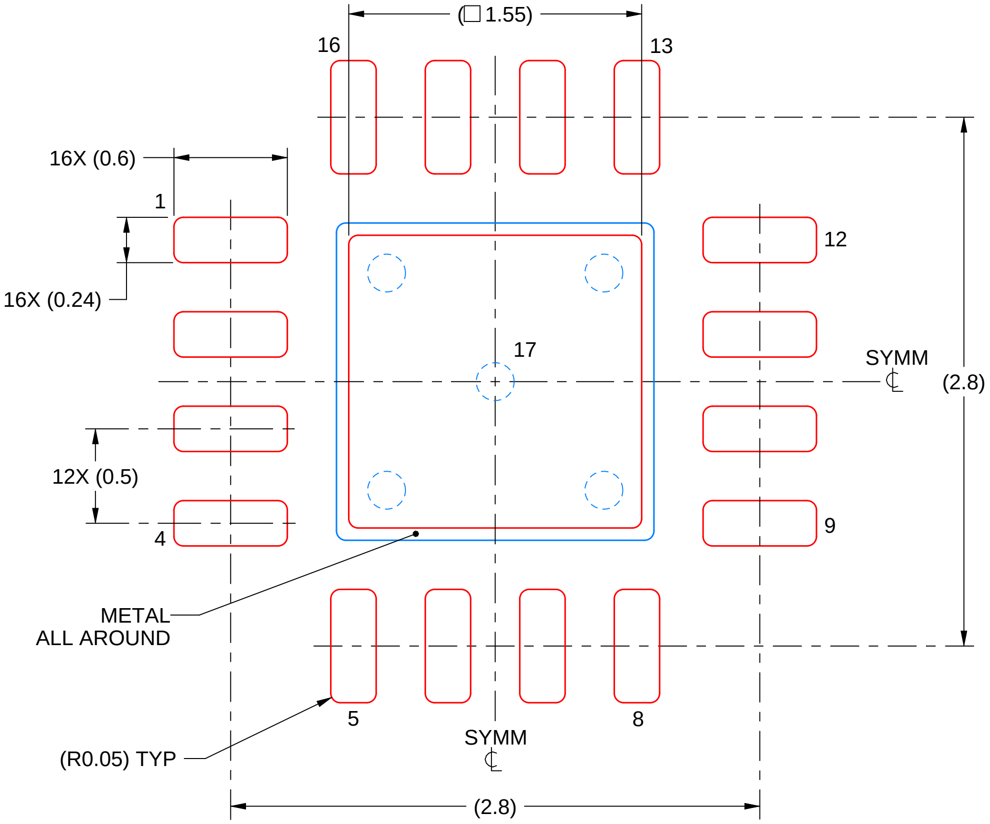


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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