



# DAC60096 具有转换触发器的 96 通道、12 位、低功耗、 串行输入、高电压输出 DAC

## 1 特性

- 高通道数
  - 96 通道数模转换器 (DAC)
  - 指定单调性为 12 位
- 较宽的未缓冲输出电压范围:  $\pm 10.5\text{V}$
- DAC 输出同时更新
- 清零功能
- 集成参考缓冲器: 2.5V 输入
- 专用 A-B 触发引脚
  - 可利用切换模式生成方波
- SPI™- 兼容串行接口
  - 4 线模式, 3V 至 5.5V 工作电压
- 低功耗: 440mW 典型值 (工作时)
- 工作温度范围:  $-40^{\circ}\text{C}$  至  $+85^{\circ}\text{C}$
- 196 焊球、15mm × 15mm NFBGA, 1mm 间距

## 2 应用

- 光电开关
- 光衰减器
- 自动测试设备 (ATE)
- 仪表

## 3 说明

DAC60096 是一款低功耗、快速稳定、96 通道、12 位数模转换器 (DAC)。该器件可提供  $\pm 10.5\text{V}$  的未缓冲双极性电压输出范围。DAC60096 拥有高通道数、低功耗运行和良好线性度等特性, 因此是需要大量精确模拟输出的系统的理想解决方案。

通过一个高速、四线制且兼容行业标准微处理器和微控制器的串行接口可以与该器件进行通信。

DAC60096 经过设置可同时清零或更新所有 DAC。此外, 通用外部转换触发器使得每个 DAC 通道均可作为具有独立幅值控制的方波发生器来运行。

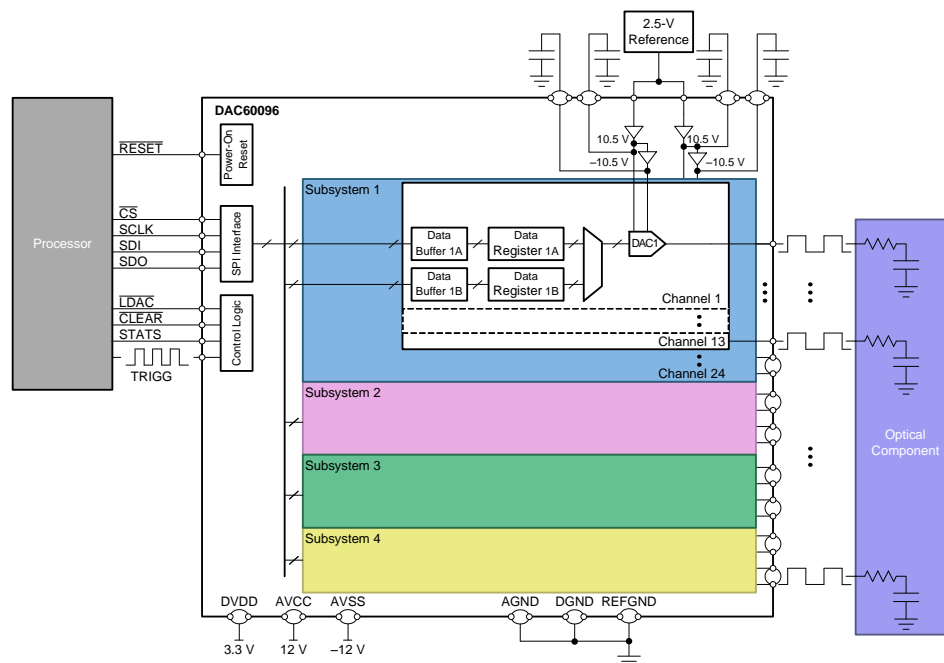
DAC60096 的额定工作温度范围为  $-40^{\circ}\text{C}$  至  $+85^{\circ}\text{C}$ , 并且采用 196 焊球、15mm × 15mm、1mm 间距的球栅阵列 (BGA) 封装。

### 器件信息<sup>(1)</sup>

| 部件号      | 封装    | 封装尺寸 (标称值)      |
|----------|-------|-----------------|
| DAC60096 | NFBGA | 15.0mm x 15.0mm |

(1) 要了解所有可用封装, 请参见数据表末尾的封装选项附录。

### 典型应用



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## 4 修订历史记录

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|   |                   |   |
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| • | 已从“产品预览”更改为“量产数据” | 1 |
|---|-------------------|---|

## 5 Pin Configuration and Functions

**ZEB Package  
196-Ball NFBGA  
Top View**

|    | A           | B           | C           | D           | E           | F           | G          | H           | J           | K           | L           | M           | N           | P           |
|----|-------------|-------------|-------------|-------------|-------------|-------------|------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 14 | DAC14<br>G4 | AVSS<br>G4  | VREFL<br>G4 | VREFH<br>G4 | AVCC<br>G4  | DNC         | REF2       | REF<br>GND2 | DNC         | AVCC<br>G5  | VREFH<br>G5 | VREFL<br>G5 | AVSS<br>G5  | DAC13<br>G5 |
| 13 | DAC15<br>G4 | DAC17<br>G4 | DAC20<br>G4 | DAC21<br>G4 | DAC22<br>G4 | DAC24<br>G4 | DAC2<br>G3 | DAC3<br>G5  | DAC5<br>G5  | DAC6<br>G5  | DAC7<br>G5  | DAC8<br>G5  | DAC10<br>G5 | DAC12<br>G5 |
| 12 | DAC16<br>G4 | DAC18<br>G4 | DAC19<br>G4 | DAC23<br>G4 | DAC4<br>G3  | DAC3<br>G3  | DAC1<br>G3 | DAC4<br>G5  | DAC24<br>G6 | DAC23<br>G6 | DAC21<br>G6 | DAC9<br>G5  | DAC19<br>G6 | DAC11<br>G5 |
| 11 | DAC10<br>G3 | DAC8<br>G3  | DAC6<br>G3  | DAC5<br>G3  | DAC24<br>G2 | DNC         | DNC        | DNC         | DNC         | DAC1<br>G7  | DAC22<br>G6 | DAC20<br>G6 | DAC18<br>G6 | DAC17<br>G6 |
| 10 | DAC11<br>G3 | DAC9<br>G3  | DAC7<br>G3  | AGND        | AGND        | AGND        | AGND       | AGND        | AGND        | AGND        | AGND        | DAC5<br>G7  | DAC7<br>G7  | DAC16<br>G6 |
| 9  | DAC12<br>G3 | AVSS<br>G3  | VREFL<br>G3 | VREFH<br>G3 | AVCC<br>G3  | AVSS<br>S2  | DGND       | DGND        | AVSS<br>S3  | AVCC<br>G6  | VREFH<br>G6 | VREFL<br>G6 | AVSS<br>G6  | DAC15<br>G6 |
| 8  | DAC13<br>G3 | AVSS<br>G3  | VREFL<br>G3 | VREFH<br>G3 | AVCC<br>G3  | AVCC<br>S2  | DVDD       | DVDD        | AVCC<br>S3  | AVCC<br>G6  | VREFH<br>G6 | VREFL<br>G6 | AVSS<br>G6  | DAC14<br>G6 |
| 7  | DAC14<br>G2 | AVSS<br>G2  | VREFL<br>G2 | VREFH<br>G2 | AVCC<br>G2  | AVCC<br>S1  | DVDD       | DVDD        | AVCC<br>S4  | AVCC<br>G7  | VREFH<br>G7 | VREFL<br>G7 | AVSS<br>G7  | DAC13<br>G7 |
| 6  | DAC15<br>G2 | AVSS<br>G2  | VREFL<br>G2 | VREFH<br>G2 | AVCC<br>G2  | AVSS<br>S1  | DGND       | DGND        | AVSS<br>S4  | AVCC<br>G7  | VREFH<br>G7 | VREFL<br>G7 | AVSS<br>G7  | DAC12<br>G7 |
| 5  | DAC16<br>G2 | DAC17<br>G2 | DAC20<br>G2 | DAC21<br>G2 | DAC22<br>G2 | AGND        | AGND       | CLEAR       | AGND        | DAC3<br>G7  | DAC4<br>G7  | DAC6<br>G7  | DAC9<br>G7  | DAC11<br>G7 |
| 4  | DAC10<br>G1 | DAC7<br>G1  | DAC19<br>G2 | DAC23<br>G2 | DAC1<br>G1  | RESET       | CS         | SCLK        | LDAC        | DAC2<br>G7  | DAC25<br>G8 | DAC21<br>G8 | DAC8<br>G7  | DAC10<br>G7 |
| 3  | DAC11<br>G1 | DAC8<br>G1  | DAC18<br>G2 | DAC3<br>G1  | DAC2<br>G1  | STATS       | SDO        | SDI         | TRIGG       | DAC26<br>G8 | DAC24<br>G8 | DAC19<br>G8 | DAC17<br>G8 | DAC16<br>G8 |
| 2  | DAC12<br>G1 | DAC9<br>G1  | DAC6<br>G1  | DAC5<br>G1  | DAC4<br>G1  | AGND        | AGND       | AGND        | AGND        | DAC23<br>G8 | DAC22<br>G8 | DAC20<br>G8 | DAC18<br>G8 | DAC15<br>G8 |
| 1  | DAC13<br>G1 | AVSS<br>G1  | VREFL<br>G1 | VREFH<br>G1 | AVCC<br>G1  | AGND        | REF1       | REF<br>GND1 | AGND        | AVCC<br>G8  | VREFH<br>G8 | VREFL<br>G8 | AVSS<br>G8  | DAC14<br>G8 |

DAC Output  
Subsystem 1

DAC Output  
Subsystem 2

DAC Output  
Subsystem 3

DAC Output  
Subsystem 4

Digital I/O

Reference  
Inputs (2.5 V)

Reference  
Compensation

Do Not Connect

AVCC

AVSS

DVDD

Ground

### Pin Functions

| PIN                       |  | TYPE | DESCRIPTION  |
|---------------------------|--|------|--|
| NAME                      | NO.  |      |  |
| AGND                      | D10, E10,<br>F1, F2, F5, F10,<br>G2, G5, G10, H2, H10,<br>J1, J2, J5, J10,<br>K10, L10 | GND  | Analog ground.   |
| AVCC                      | E1, E6, E7, E8, E9, E14,<br>F7, F8, J7, J8,<br>K1, K6, K7, K8, K9, K14                 | PWR  | Positive analog supply voltage. (11.2 V to 12.6 V). A 100-nF bypass capacitor for each AVCC_n (n = G1, G2, G3, G4, G5, G6, G7, G8, S1, S2, S3 or S4) is required; place as close as possible to the pins.  |
| AVSS                      | B1, B6, B7, B8, B9, B14,<br>F6, F9, J6, J9,<br>N1, N6, N7, N8, N9, N14                 | PWR  | Negative analog supply voltage. (-12.6V to -11.2V). A 100-nF bypass capacitor for each AVSS_n (n = G1, G2, G3, G4, G5, G6, G7, G8, S1, S2, S3 or S4) is required; place as close as possible to the pins.  |
| $\overline{\text{CLEAR}}$ | H5   | I    | Asynchronous clear control input, active low. When $\overline{\text{CLEAR}}$ is low, all DACs are loaded with code 000h. When $\overline{\text{CLEAR}}$ is high, all DACs return to normal operation   |
| $\overline{\text{CS}}$    | G4   | I    | Serial data enable, active low. This input is the frame synchronization signal for the serial data.  |
| DAC[1-13]_G1              | A1, A2, A3, A4,<br>B2, B3, B4, C2, D2, D3,<br>E2, E3, E4                               | O    | Subsystem 1 Regular DAC outputs: DAC group 1 and DAC group 2. Each DAC subsystem can be controlled independently through the serial interface.   |
| DAC[14-26]_G2             | A5, A6, A7, B5,<br>C3, C4, C5,<br>D4, D5, E5, E11                                      | O    |  |
| DAC[1-13]_G3              | A8, A9, A10, A11,<br>B10, B11, C10, C11,<br>D11, E12, F12, G12, G13                    | O    | Subsystem 2 Regular DAC outputs: DAC group 3 and DAC group 4. Each DAC subsystem can be controlled independently through the serial interface.   |
| DAC[14-24]_G4             | A12, A13, A14,<br>B12, B13, C12, C13,<br>D12, D13, E13, F13                            | O    |  |
| DAC[3-13]_G5              | H12, H13, J13, K13, L13,<br>M12, M13, N13,<br>P12, P13, P14                            | O    | Subsystem 3 Regular DAC outputs: DAC group 5 and DAC group 6. Each DAC subsystem can be controlled independently through the serial interface.   |
| DAC[14-26]_G6             | J12, K12<br>L11, L12, M11, N11, N12,<br>P8, P9, P10, P11                               | O    |  |
| DAC[1-13]_G7              | K4, K5, K11, L5,<br>M5, M10, N4, N5, N10,<br>P4, P5, P6, P7                            | O    | Subsystem 4 Regular DAC outputs: DAC group 7 and DAC group 8. Each DAC subsystem can be controlled independently through the serial interface.   |
| DAC[14-26]_G8             | K2, K3, L2, L3, L4,<br>M2, M3, M4, N2, N3,<br>P1, P2, P3                               | O    |  |
| DGND                      | G6, G9, H6, H9   | GND  | Digital ground. Ground reference point for all digital circuitry on the device.  |
| DNC                       | F11, F14, G11<br>H11, J11, J14   | —    | Reserved for factory use. For proper operation, do not connect.  |
| DVDD                      | G7, G8, H7, H8   | PWR  | Digital supply voltage. (3 V to 5.5 V). A 100-nF bypass capacitor is required; place as close as possible to the pins.   |
| $\overline{\text{LDAC}}$  | J4   | I    | Synchronous DAC load control input, active low. When $\overline{\text{LDAC}}$ is low, the DAC outputs are updated immediately after a register write. If left high during DAC register updates, bringing $\overline{\text{LDAC}}$ low causes all DAC outputs to update simultaneously. |
| $\overline{\text{RESET}}$ | F4   | I    | Reset input, active low. Logic low on this pin causes the device to perform a hardware reset.  |
| REFGND1                   | H1   | GND  | Reference ground. Ground reference point for REF1. REFGND1 should be star connected at the system GND source and not connected to the GND plane for best performance.  |
| REFGND2                   | H14  | GND  | Reference ground. Ground reference point for REF2. REFGND2 should be star connected at the system GND source and not connected to the GND plane for best performance.  |
| SCLK                      | H4   | I    | Serial interface clock.  |
| SDI                       | H3   | I    | Serial interface data input. Data are clocked into the input shift register on each rising edge of SCLK.   |
| SDO                       | G3   | O    | Serial interface data output. The SDO pin is in high impedance when $\overline{\text{CS}}$ is high. Data can be clocked out of the input shift register on either rising or falling edges of SCLK as specified by PHAINV in the CON register.  |
| STATS                     | F3   | O    | DAC output status indicator. Identifies which of the two DAC data registers is active.   |
| REF1                      | G1   | I    | Input voltage reference pin 1 (2.5 V). A 100-nF bypass capacitor between this pin and REFGND1 is required.   |
| REF2                      | G14  | I    | Input voltage reference pin 2 (2.5 V). A 100-nF bypass capacitor between this pin and REFGND2 is required.   |

### Pin Functions (continued)

| PIN   |  | TYPE | DESCRIPTION   |
|-------|--|------|---|
| NAME  | NO.  |      |   |
| TRIGG | J3   | I    | Trigger input signal. Enables all DAC outputs to toggle between the two DAC data registers associated with each DAC. This functionality enables the device to operate as a square-wave generator. The DAC registers are prepared for toggle mode operation on a TRIGG rising edge and the outputs are toggled on each following TRIGG falling edge. |
| VREFH | D1, D6, D7, D8, D9, D14, L1, L6, L7, L8, L9, L14 | O    | Compensation capacitor connection for the internal 10.5 V reference voltage. A 100-nF bypass capacitor for each VREFH_n (n = G1, G2, G3, G4, G5, G6, G7 or G8) is required; place as close as possible to the pins.   |
| VREFL | C1, C6, C7, C8, C9, C14, M1, M6, M7, M8, M9, M14 | O    | Compensation capacitor connection for the internal -10.5 V reference voltage. A 100-nF bypass capacitor for each VREFL_n (n = G1, G2, G3, G4, G5, G6, G7 or G8) is required; place as close as possible to the pins.  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                |  | MIN                    | MAX                    | UNIT |
|----------------|--|------------------------|------------------------|------|
| Supply voltage | AV <sub>CC</sub> to DGND   | −0.3                   | 13                     | V    |
|                | AV <sub>SS</sub> to DGND   | −13                    | 0.3                    |      |
|                | DV <sub>DD</sub> to DGND   | −0.3                   | 6                      |      |
|                | AV <sub>CC</sub> to AV <sub>SS</sub>   | −0.3                   | 26                     |      |
|                | DGND to AGND   | −0.3                   | 0.3                    |      |
|                | DGND to REFGND[1,2]  | −0.3                   | 0.3                    |      |
| Pin voltage    | REF1 to REFGND1  | −0.3                   | 6                      | V    |
|                | REF2 to REFGND2  | −0.3                   | 6                      |      |
|                | DAC to DGND  | AV <sub>SS</sub> − 0.3 | AV <sub>CC</sub> + 0.3 |      |
|                | CLEAR, $\overline{\text{CS}}$ , LDAC, $\overline{\text{RESET}}$ , SCLK, SDI, SDO, TRIGG, STATS to DGND | −0.3                   | DV <sub>DD</sub> + 0.3 |      |
|                | VREFH to DGND  | −0.3                   | AV <sub>CC</sub> + 0.3 |      |
|                | VREFL to DGND  | AV <sub>SS</sub> − 0.3 | 0.3                    |      |
|                | VREFH to adjacent VREFL  | −0.3                   | 26                     |      |
| Temperature    | Operating, T <sub>A</sub>  | −40                    | 85                     | °C   |
|                | Junction, T <sub>J</sub>   | −40                    | 150                    |      |
|                | Storage, T <sub>stg</sub>  | −40                    | 150                    |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|  |  | VALUE | UNIT |
|--|--|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|  | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|   | MIN   | NOM | MAX              | UNIT |
|---|-------|-----|------------------|------|
| <b>POWER SUPPLY</b>                           |       |     |                  |      |
| AV <sub>CC</sub>                              | 11.2  | 12  | 12.6             | V    |
| AV <sub>SS</sub>                              | −12.6 | −12 | −11.2            | V    |
| DV <sub>DD</sub>                              | 3     | 3.3 | 5.5              | V    |
| AV <sub>CC</sub> to AV <sub>SS</sub>          | 22.4  | 24  | 25.2             | V    |
| <b>DIGITAL INPUTS</b>                         |       |     |                  |      |
| Digital input voltage                         | 0     |     | DV <sub>DD</sub> | V    |
| <b>REFERENCE INPUT</b>                        |       |     |                  |      |
| Reference input voltage, V <sub>REF</sub>     | 2.475 | 2.5 | 2.525            | V    |
| <b>TEMPERATURE</b>                            |       |     |                  |      |
| Operating ambient temperature, T <sub>A</sub> | −40   |     | 85               | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | DAC60096    | UNIT |
|-------------------------------|--|-------------|------|
|                               |  | ZEB (NFBGA) |      |
|                               |  | 196 BALLS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 21.4        | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 7.5         | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 5.1         | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.4         | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 5.0         | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A         | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics: DAC DC

at AV<sub>CC</sub> = 11.2 V to 12.6 V, AV<sub>SS</sub> = –12.6 V to –11.2 V, DV<sub>DD</sub> = 3 V to 5.5 V, AGND = DGND = REFGND[1,2] = 0 V, REF1 = REF2 = 2.5 V (specifications exclude any reference contributions), no load on DACs, and T<sub>A</sub> = –40°C to +85°C (unless otherwise noted)

| PARAMETER                     | TEST CONDITIONS   | MIN                        | TYP   | MAX   | UNIT   |
|-------------------------------|---|----------------------------|-------|-------|--------|
| <b>STATIC PERFORMANCE</b>     |   |                            |       |       |        |
| Resolution                    |   | 12                         |       |       | Bits   |
| INL                           | Relative accuracy   |                            | ±0.15 | ±1    | LSB    |
| DNL                           | Differential nonlinearity   | Specified 12-bit monotonic | ±0.1  | ±0.9  | LSB    |
| Gain error                    | T <sub>A</sub> = 25°C   |                            | ±0.05 | ±0.15 | %FSR   |
| Zero-code error               | T <sub>A</sub> = 25°C, code 000h  |                            | ±2    | ±7    | mV     |
| Gain error drift              |   |                            | ±1    |       | ppm/°C |
| Zero-code error drift         |   |                            | ±1    |       | ppm/°C |
| <b>OUTPUT CHARACTERISTICS</b> |   |                            |       |       |        |
| Output voltage                |   | –10.5                      |       | 10.5  | V      |
| Output impedance              |   |                            | 41    |       | kΩ     |
| DC crosstalk                  | Measured channel at code 000h, all others transition from code 7FFh to 02Bh   |                            | 0.5   |       | LSB    |
| Settling time                 | DAC output transition:<br>code 800h to 7FFh to within 1 LSB,<br>6x load:<br>R <sub>(SERIES)</sub> = 17 kΩ, C <sub>LOAD</sub> = 300 pF |                            | 160   |       | μs     |
|                               | DAC output transition:<br>code 800h to 7FFh to within 1 LSB,<br>1x load:<br>R <sub>(SERIES)</sub> = 100 kΩ, C <sub>LOAD</sub> = 50 pF |                            | 65    |       |        |
| Output noise                  | T <sub>A</sub> = 25°C, 1 kHz, code 000h   |                            | 60    |       | nV/√Hz |

**DAC60096**

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**6.6 Electrical Characteristics: Square-Wave Output**

at  $AV_{CC} = 11.2\text{ V}$  to  $12.6\text{ V}$ ,  $AV_{SS} = -12.6\text{ V}$  to  $-11.2\text{ V}$ ,  $DV_{DD} = 3\text{ V}$  to  $5.5\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT          |
|---|--|-----|-----|-----|---------------|
| <b>DAC OUTPUTS – 6x LOAD: <math>R_{(SERIES)} = 17\text{ k}\Omega</math>, <math>C_{LOAD} = 300\text{ pF}</math></b>                |  |     |     |     |               |
| Frequency   | For amplitude $\geq 9.1\text{ V}_{RMS}$ , amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h  |     | 3   |     | kHz           |
| Amplitude   | Frequency = 3 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h                         | 9.1 |     |     | $V_{RMS}$     |
|   | Frequency = 5 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h                         | 8   |     |     | $V_{RMS}$     |
| Amplitude step precision  | Frequency = 3 kHz, amplitude $\geq 1\text{ V}_{RMS}$   |     |     | 6   | $mV_{RMS}$    |
| Amplitude temperature drift   | Frequency = 3 kHz, amplitude = $\pm 5\text{ V}_{PP}$ , codes 3CFh to C31h                            |     |     | 5   | $mV_{RMS}$    |
|   | Frequency = 3 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h                         |     |     | 15  | $mV_{RMS}$    |
| Offset voltage  | Frequency = 3 kHz, amplitude = $\pm 5\text{ V}_{PP}$ , codes 3CFh to C31h                            | -10 |     | 10  | mV            |
|   | Frequency = 3 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h                         | -10 |     | 10  | mV            |
| Rise and fall time  | Frequency = 3 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , 10% to 90%, codes 7FFh to 801h             |     | 40  |     | $\mu\text{s}$ |
| <b>DAC OUTPUTS – 1x LOAD: <math>R_{(SERIES)} = 100\text{ k}\Omega</math>, <math>C_{LOAD} = 50\text{ pF}</math> <sup>(1)</sup></b> |  |     |     |     |               |
| Frequency   | For amplitude $\geq 9.1\text{ V}_{RMS}$ , amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh and 801h |     | 5   |     | kHz           |
| Amplitude   | Frequency = 3 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h                         | 10  |     |     | $V_{RMS}$     |
|   | Frequency = 5 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h                         | 9.5 |     |     | $V_{RMS}$     |
| Amplitude step precision  | Frequency = 3 kHz, amplitude $\geq 1\text{ V}_{RMS}$   |     |     | 7   | $mV_{RMS}$    |
| Amplitude temperature drift   | Frequency = 3 kHz, amplitude = $\pm 5\text{ V}_{PP}$ , codes 3CFh to C31h                            |     |     | 5   | $mV_{RMS}$    |
|   | Frequency = 3 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h                         |     |     | 15  | $mV_{RMS}$    |
| Offset voltage  | Frequency = 3 kHz, amplitude = $\pm 5\text{ V}_{PP}$ , codes 3CFh to C31h                            | -10 |     | 10  | mV            |
|   | Frequency = 3 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , codes 7FFh to 801h                         | -10 |     | 10  | mV            |
| Rise and fall time  | Frequency = 3 kHz, amplitude = $\pm 10.5\text{ V}_{PP}$ , 10% to 90%, codes 7FFh to 801h             |     | 10  |     | $\mu\text{s}$ |

(1) Specified by design and characterization. Not tested during production.



## 6.7 Electrical Characteristics: General

at  $AV_{CC} = 11.2\text{ V to }12.6\text{ V}$ ,  $AV_{SS} = -12.6\text{ V to }-11.2\text{ V}$ ,  $DV_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                         |                                 | TEST CONDITIONS   | MIN                    | TYP   | MAX   | UNIT |
|-----------------------------------|---------------------------------|---|------------------------|-------|-------|------|
| EXTERNAL REFERENCE INPUTS         |                                 |   |                        |       |       |      |
| V <sub>REF</sub>                  | Input voltage range             | REF1 and REF2 input pins  | 2.475                  | 2.5   | 2.525 | V    |
|                                   | Reference input current         | Per input pin   |                        | 1     |       | μA   |
| DIGITAL LOGIC                     |                                 |   |                        |       |       |      |
| V <sub>IH</sub>                   | High-level input voltage        |   | 0.7 × DV <sub>DD</sub> |       |       | V    |
| V <sub>IL</sub>                   | Low-level input voltage         |   | 0.3 × DV <sub>DD</sub> |       |       | V    |
| V <sub>OH</sub>                   | High-level output voltage       | I <sub>LOAD</sub> = 1 mA, SDO2x = 01  | DV <sub>DD</sub> - 0.2 |       |       | V    |
| V <sub>OL</sub>                   | Low-level output voltage        | I <sub>LOAD</sub> = −1 mA, SDO2x = 01   | 0.4                    |       |       | V    |
|                                   | Input capacitance               |   | 20                     |       |       | pF   |
| POWER REQUIREMENTS <sup>(1)</sup> |                                 |   |                        |       |       |      |
| I <sub>(AVCC)</sub>               | AV <sub>CC</sub> supply current | 6x load:<br>R <sub>(SERIES)</sub> = 17 kΩ, C <sub>LOAD</sub> = 300 pF<br>frequency = 3 kHz<br>48 DAC outputs, codes 7FFh and 801h<br>48 DAC outputs, codes 117h and EE9h                | 18.1                   | 25    |       | mA   |
| I <sub>(AVSS)</sub>               | AV <sub>SS</sub> supply current |   | −25                    | −18.1 |       | mA   |
| I <sub>(DVDD)</sub>               | DV <sub>DD</sub> supply current |   | 2                      | 10    |       | mA   |
|                                   | Power consumption               |   | 440                    |       |       | mW   |
| I <sub>(AVCC)</sub>               | AV <sub>CC</sub> supply current | 1x load:<br>R <sub>(SERIES)</sub> = 100 kΩ, C <sub>LOAD</sub> = 50 pF<br>frequency = 3 kHz<br>48 DAC outputs, codes 7FFh and 801h<br>48 DAC outputs, codes 117h and EE9h <sup>(2)</sup> | 17                     | 22    |       | mA   |
| I <sub>(AVSS)</sub>               | AV <sub>SS</sub> supply current |   | −22                    | −17   |       | mA   |
| I <sub>(DVDD)</sub>               | DV <sub>DD</sub> supply current |   | 2                      | 10    |       | mA   |
|                                   | Power consumption               |   | 415                    |       |       | mW   |
| I <sub>(AVCC)</sub>               | AV <sub>CC</sub> supply current | 6x load:<br>R <sub>(SERIES)</sub> = 17 kΩ, C <sub>LOAD</sub> = 300 pF<br>frequency = 3 kHz<br>All DAC outputs, codes 02Bh and FD5h  | 25                     | 30    |       | mA   |
| I <sub>(AVSS)</sub>               | AV <sub>SS</sub> supply current |   | −30                    | −25   |       | mA   |
| I <sub>(DVDD)</sub>               | DV <sub>DD</sub> supply current |   | 2                      | 10    |       | mA   |
|                                   | Power consumption               |   | 650                    | 760   |       | mW   |

- (1) Power requirements tested unloaded during production. Load current contribution to power consumption specified by design and characterization.
- (2) Specified by design and characterization. Not tested during production.

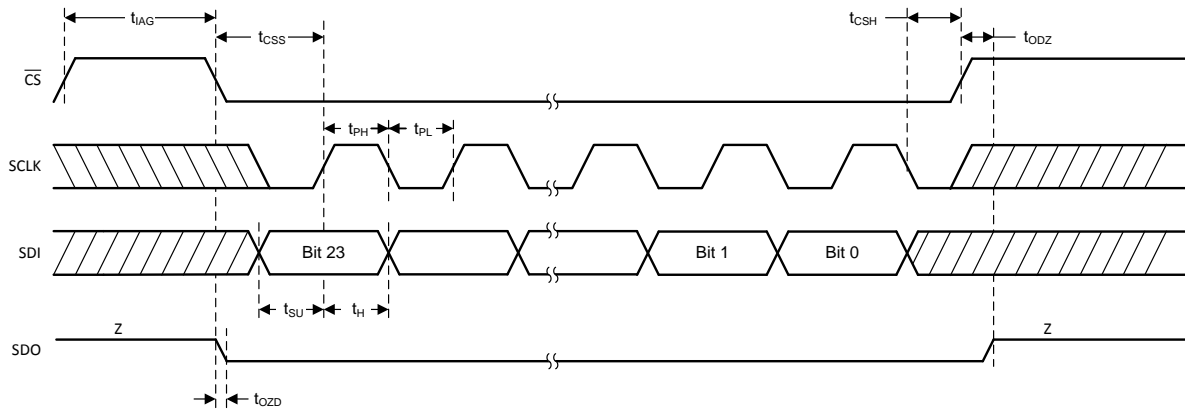
## 6.8 Timing Requirements<sup>(1)(2)</sup>

at  $V_{CC} = 11.2\text{ V}$  to  $12.6\text{ V}$ ,  $V_{SS} = -12.6\text{ V}$  to  $-11.2\text{ V}$ ,  $DV_{DD} = 3\text{ V}$  to  $5.5\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted)

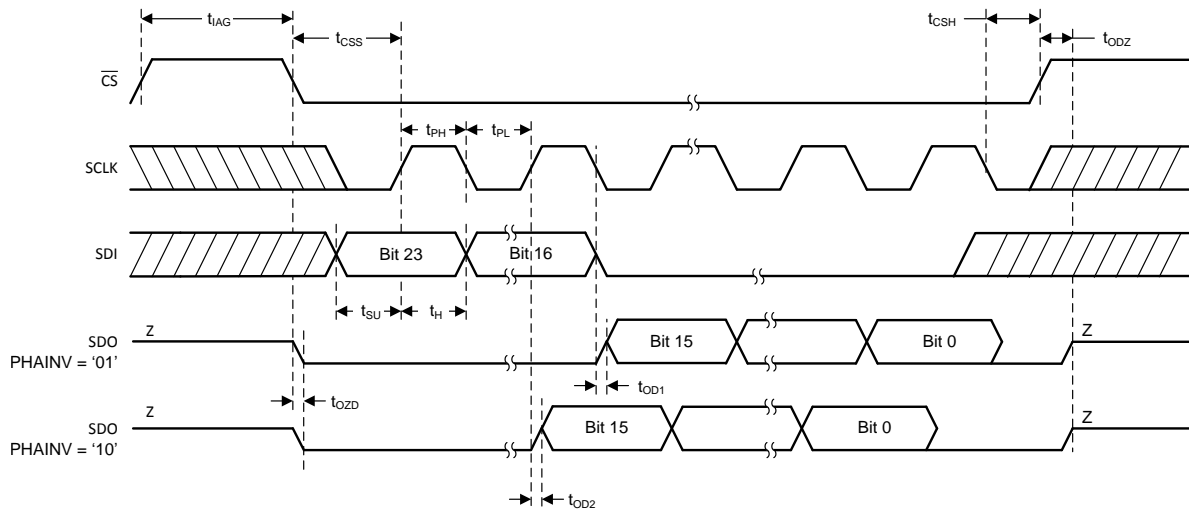
|   |                                |   | MIN | NOM | MAX | UNIT          |
|---|--------------------------------|---|-----|-----|-----|---------------|
| <b>SERIAL INTERFACE – DEFAULT MODE: SDO2X = 01, PHAINV = 01</b> |                                |   |     |     |     |               |
| $f_{SCLK}$  | SCLK frequency                 | Write operation                               |     |     | 32  | MHz           |
|   |                                | Read operation                                |     |     | 18  | MHz           |
| $t_{PH}$  | SCLK pulse width high          | Write operation                               | 14  |     |     | ns            |
|   |                                | Read operation                                | 26  |     |     | ns            |
| $t_{PL}$  | SCLK pulse width low           | Write operation                               | 14  |     |     | ns            |
|   |                                | Read operation                                | 26  |     |     | ns            |
| $t_{SU}$  | SDI setup                      |   | 5   |     |     | ns            |
| $t_H$   | SDI hold                       |   | 10  |     |     | ns            |
| $t_{CSS}$   | $\overline{CS}$ setup          |   | 10  |     |     | ns            |
| $t_{CSH}$   | $\overline{CS}$ hold           |   | 20  |     |     | ns            |
| $t_{IAG}$   | Inter-access gap               |   | 70  |     |     | ns            |
| $t_{ODZ}$   | SDO driven to tri-state        | Read operation                                | 0   |     | 20  | ns            |
| $t_{OZD}$   | SDO tri-state to driven        | Read operation                                | 0   |     | 20  | ns            |
| $t_{OD1}$   | SDO output delay               | Read operation                                | 0   |     | 20  | ns            |
| <b>SERIAL INTERFACE – FAST MODE: SDO2X = 10, PHAINV = 10</b>    |                                |   |     |     |     |               |
| $f_{SCLK}$  | SCLK frequency                 | Write operation                               |     |     | 32  | MHz           |
|   |                                | Read operation                                |     |     | 32  | MHz           |
| $t_{PH}$  | SCLK pulse width high          | Write operation                               | 14  |     |     | ns            |
|   |                                | Read operation                                | 14  |     |     | ns            |
| $t_{PL}$  | SCLK pulse width low           | Write operation                               | 14  |     |     | ns            |
|   |                                | Read operation                                | 14  |     |     | ns            |
| $t_{SU}$  | SDI setup                      |   | 5   |     |     | ns            |
| $t_H$   | SDI hold                       |   | 10  |     |     | ns            |
| $t_{CSS}$   | $\overline{CS}$ setup          |   | 10  |     |     | ns            |
| $t_{CSH}$   | $\overline{CS}$ hold           |   | 20  |     |     | ns            |
| $t_{IAG}$   | Inter-access gap               |   | 70  |     |     | ns            |
| $t_{ODZ}$   | SDO driven to tri-state        | Read operation                                | 0   |     | 20  | ns            |
| $t_{OZD}$   | SDO tri-state to driven        | Read operation                                | 0   |     | 20  | ns            |
| $t_{OD2}$   | SDO output delay               | Read operation                                | 0   |     | 20  | ns            |
| <b>DIGITAL LOGIC</b>  |                                |   |     |     |     |               |
| $t_{RESETDLY}$  | Reset delay                    | Delay from power-on-reset to normal operation | 100 | 250 |     | $\mu\text{s}$ |
|   |                                | Delay from hardware reset to normal operation | 10  | 50  |     | $\mu\text{s}$ |
|   |                                | Delay from software reset to normal operation | 10  | 50  |     | $\mu\text{s}$ |
| $t_{RESETWD}$   | $\overline{RESET}$ pulse width |   | 500 |     |     | ns            |
| $t_{LDACS}$   | $\overline{LDAC}$ setup        |   | 0   |     |     | ns            |
| $t_{LDACH}$   | $\overline{LDAC}$ hold         |   | 0   |     |     | ns            |
| $t_{TRIGH}$   | TRIGG pulse width high         |   | 30  |     |     | ns            |
| $t_{TRIGL}$   | TRIGG pulse width low          |   | 30  |     |     | ns            |
| $t_{STADLY}$  | STATS output delay             |   |     |     | 25  | ns            |

(1) Specified by design and characterization. Not tested during production.

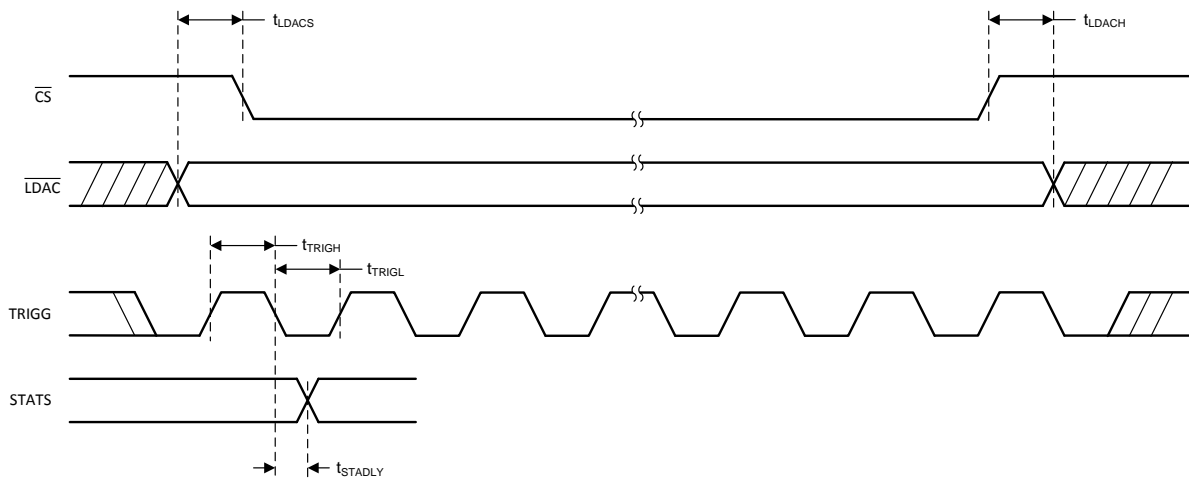
(2) SDO loaded with 10-pF load capacitance for SDO timing specifications.



**Figure 1. Serial Interface Write Timing Diagram**



**Figure 2. Serial Interface Read Timing Diagram**



**Figure 3. Digital Logic Timing Diagram**

## 6.9 Typical Characteristics: DC Mode

at  $AV_{CC} = 12\text{ V}$ ,  $AV_{SS} = -12\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

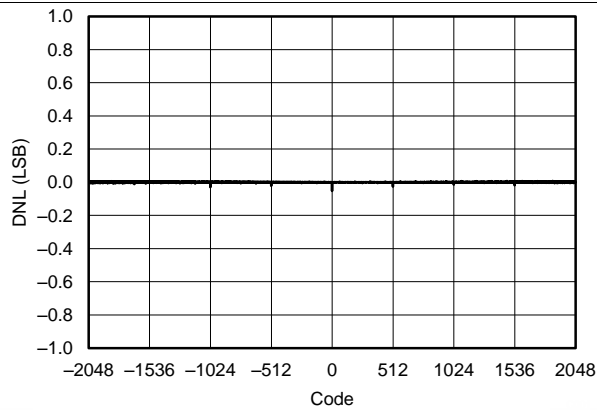


Figure 4. Differential Linearity Error (DNL)

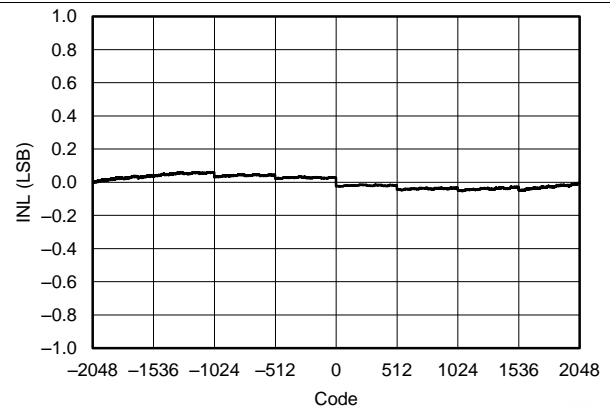


Figure 5. Integral Linearity Error (INL)

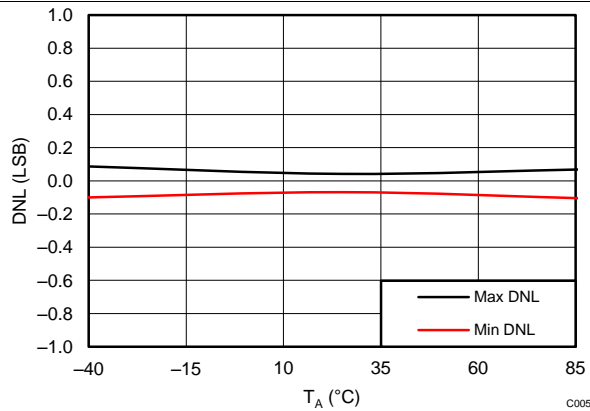


Figure 6. DNL vs Temperature

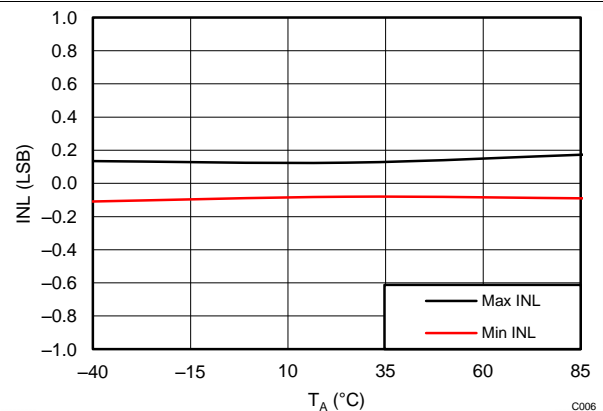


Figure 7. INL vs Temperature

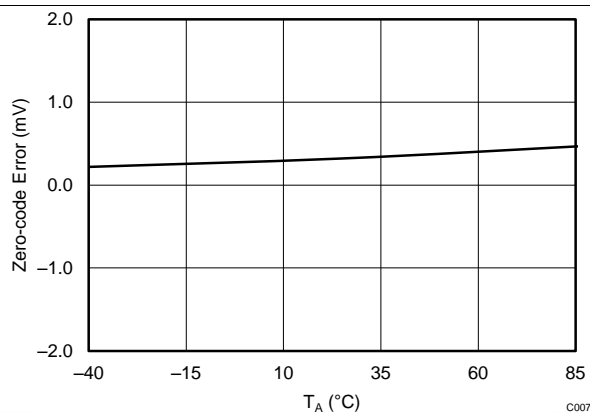


Figure 8. Zero-Code Error vs Temperature

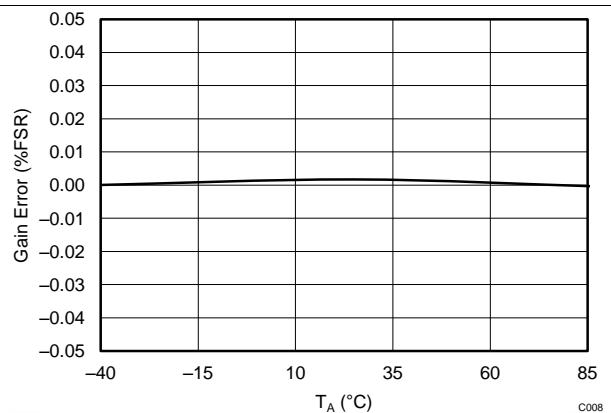
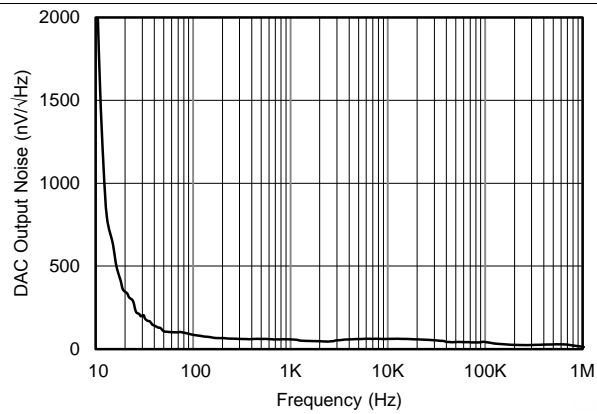


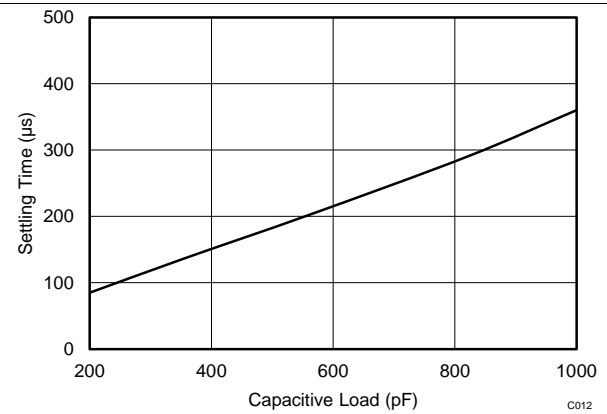
Figure 9. Gain Error vs Temperature

## Typical Characteristics: DC Mode (continued)

at  $AV_{CC} = 12\text{ V}$ ,  $AV_{SS} = -12\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



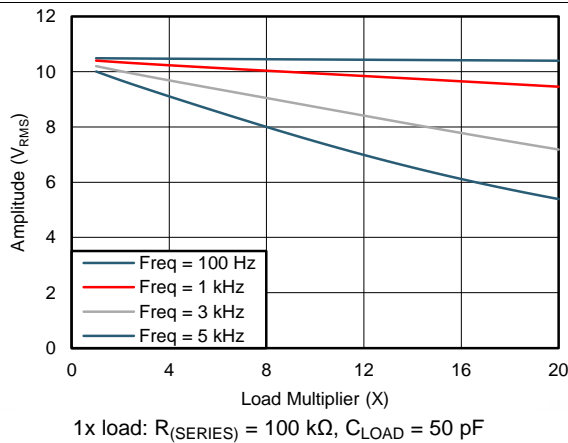
**Figure 10. DAC Output Noise vs Frequency**



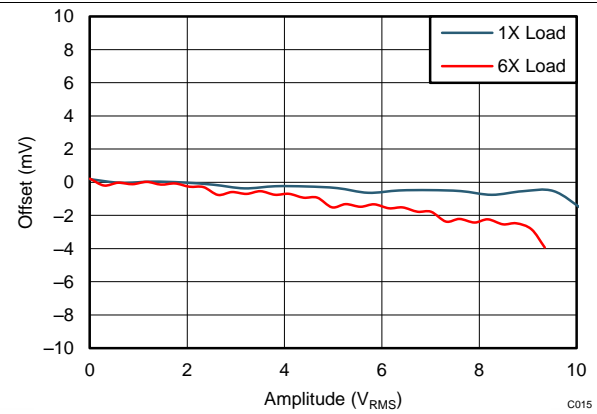
**Figure 11. Settling Time Amplitude vs Capacitive Load**

## 6.10 Typical Characteristics: Toggle Mode

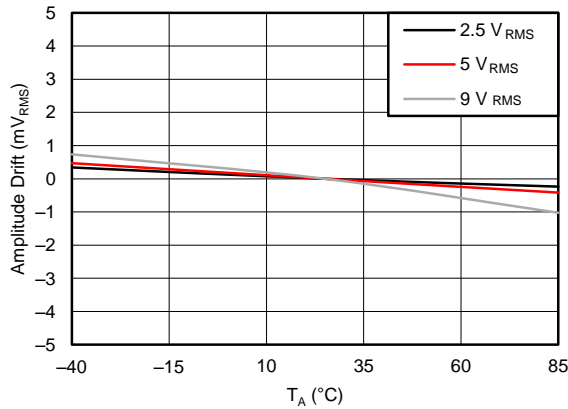
at  $AV_{CC} = 12\text{ V}$ ,  $AV_{SS} = -12\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



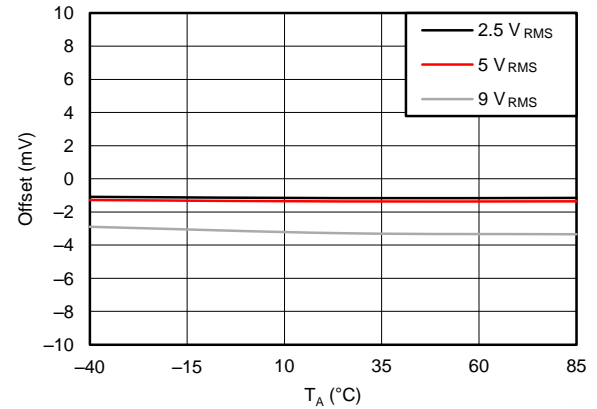
**Figure 12. Maximum Amplitude vs Capacitive Load**



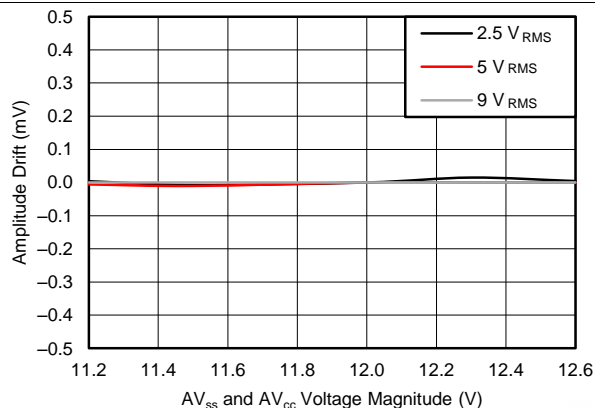
**Figure 13. Offset vs Amplitude**



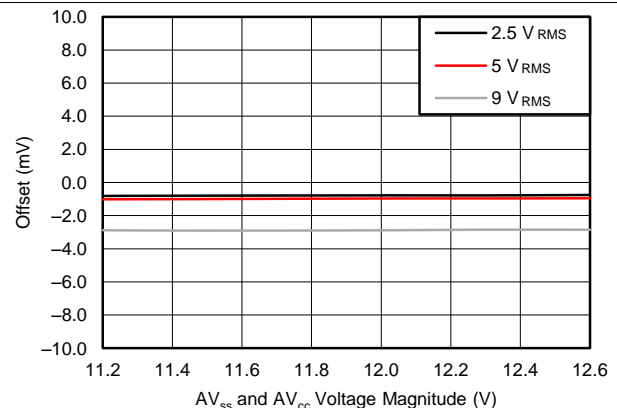
**Figure 14. Amplitude Drift vs Temperature**



**Figure 15. Offset vs Temperature**



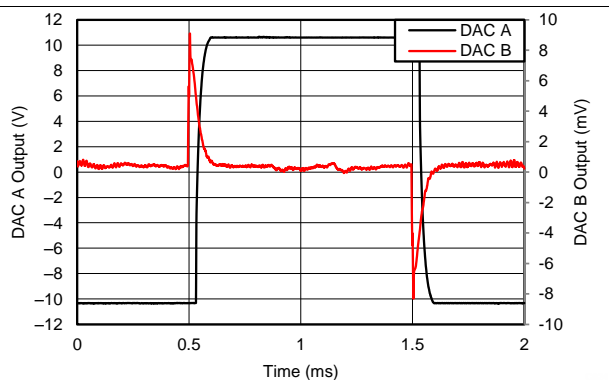
**Figure 16. Amplitude Drift vs Supply Voltage**



**Figure 17. Offset vs Supply Voltage**

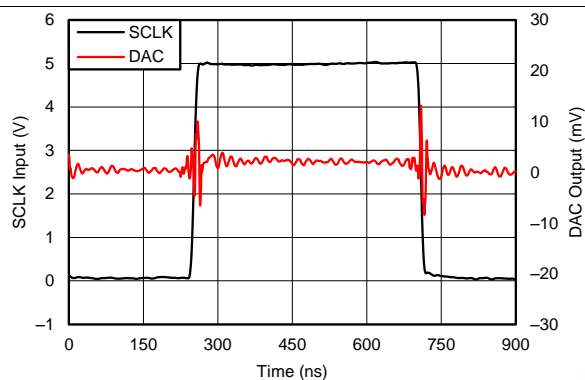
## 6.11 Typical Characteristics, General

at  $AV_{CC} = 12\text{ V}$ ,  $AV_{SS} = -12\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



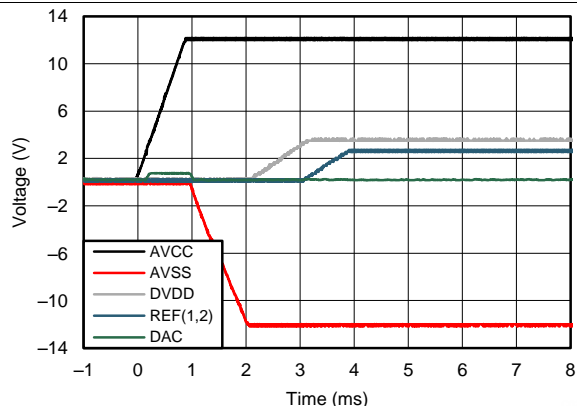
DAC A: square-wave output, freq = 1 kHz, full-scale amplitude  
DAC B: zero-code inputs

**Figure 18. DAC to DAC Crosstalk**

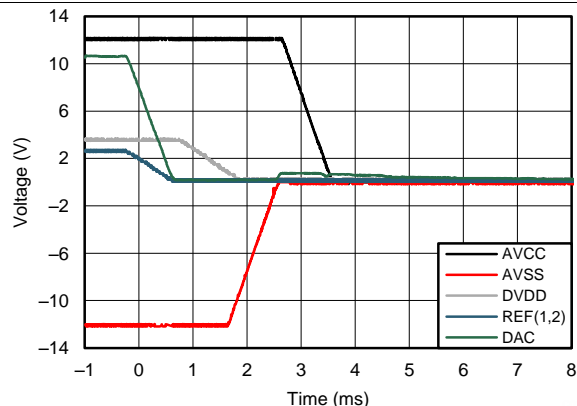


All DACs with zero-code inputs  
SCLK frequency = 1 MHz

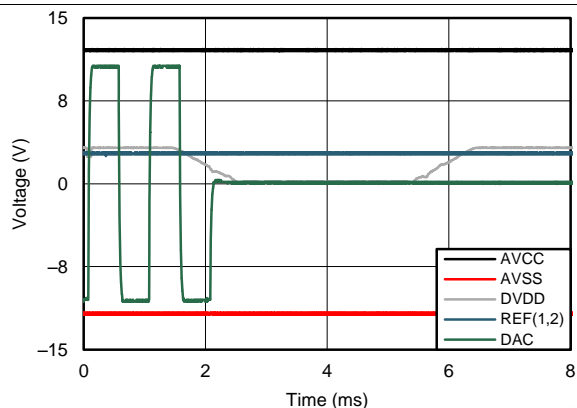
**Figure 19. SPI to DAC Crosstalk**



**Figure 20. Recommended Power-Up Sequence**

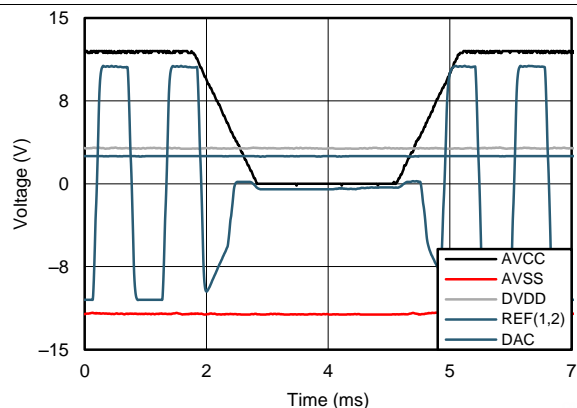


**Figure 21. Recommended Power-Down Sequence**



6x load:  $R_{\text{SERIES}} = 17\text{ k}\Omega$ ,  $C_{\text{LOAD}} = 300\text{ pF}$   
Square-wave output: freq = 1 kHz, full-scale amplitude

**Figure 22.  $DV_{DD}$  Collapse and Recover**

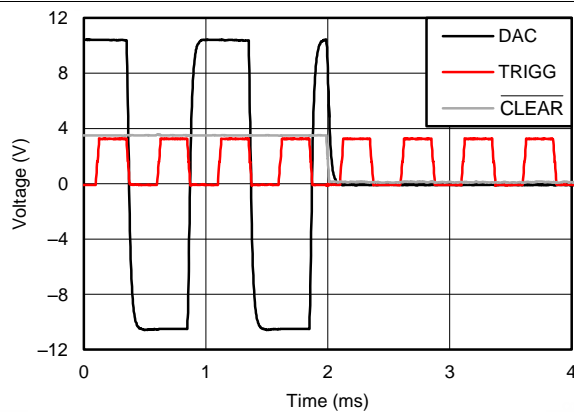
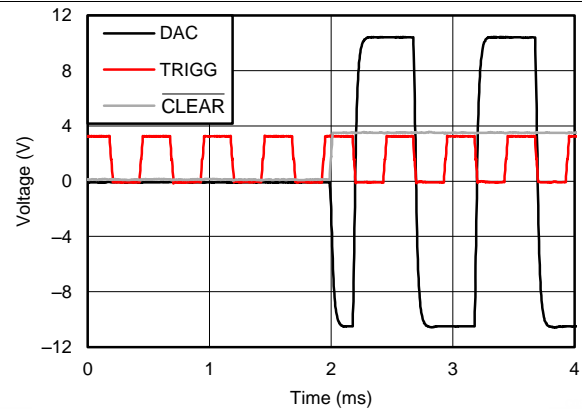
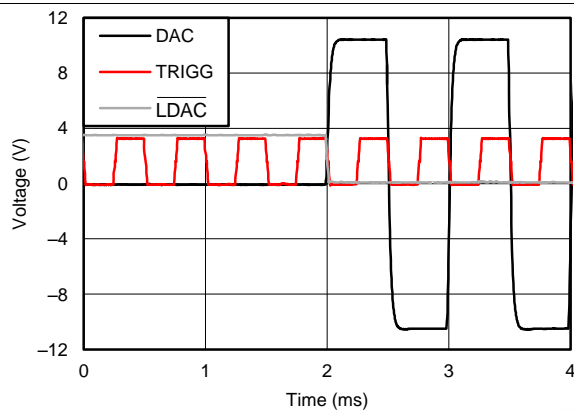
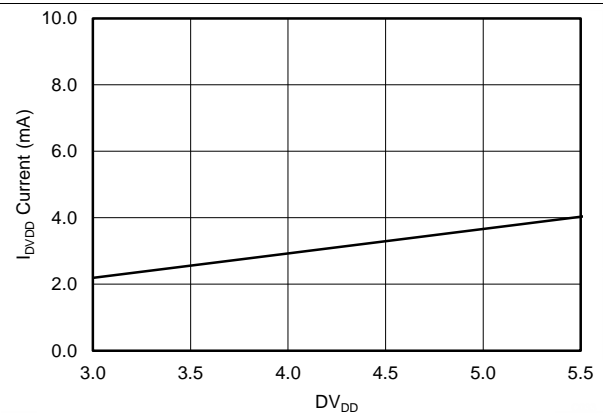
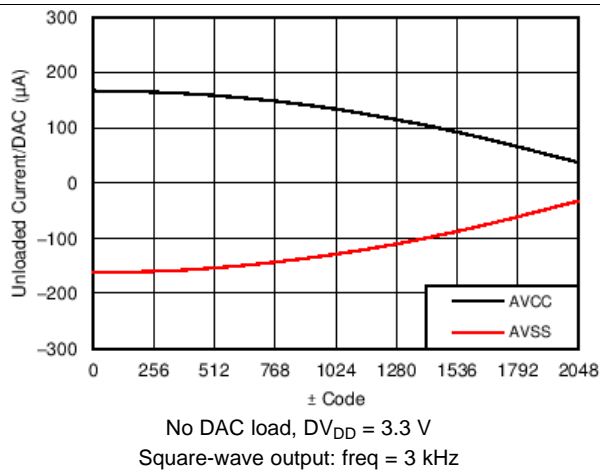
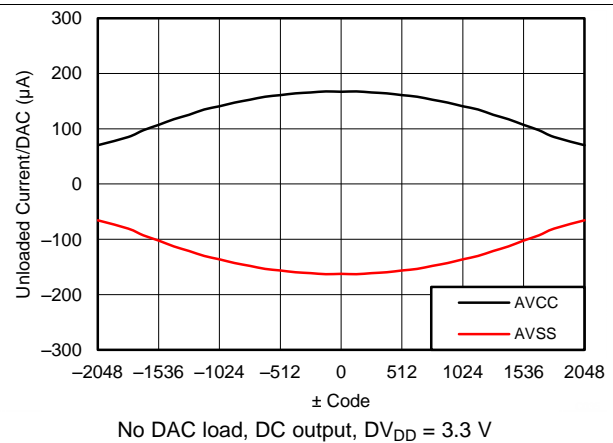


6x load:  $R_{\text{SERIES}} = 17\text{ k}\Omega$ ,  $C_{\text{LOAD}} = 300\text{ pF}$   
Square-wave output: freq = 1 kHz, full-scale amplitude

**Figure 23.  $AV_{CC}$  Collapse and Recover**

## Typical Characteristics, General (continued)

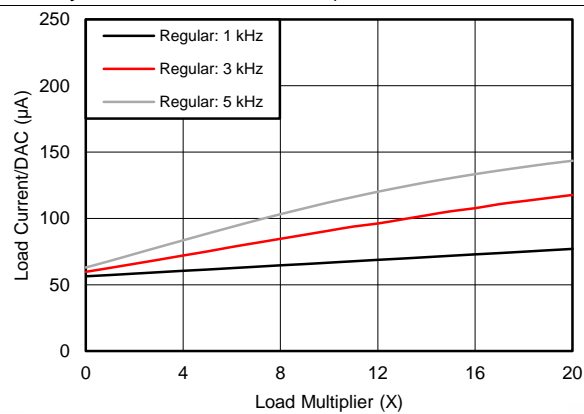
at  $AV_{CC} = 12\text{ V}$ ,  $AV_{SS} = -12\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)


**Figure 24. Normal to Clear State Transition**

**Figure 25. Clear State to Normal Transition**

**Figure 26. LDAC DAC Transition**

**Figure 27.  $DV_{DD}$  Current Consumption**

**Figure 28. Unloaded  $AV_{CC}/AV_{SS}$  Current Consumption**

**Figure 29. Unloaded  $AV_{CC}/AV_{SS}$  Current Consumption**



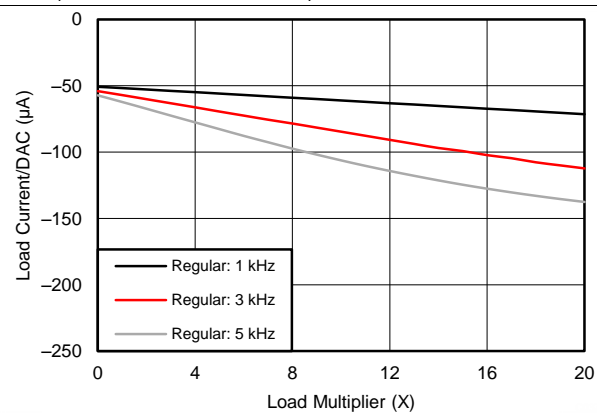
## Typical Characteristics, General (continued)

at  $AV_{CC} = 12\text{ V}$ ,  $AV_{SS} = -12\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $AGND = DGND = REFGND[1,2] = 0\text{ V}$ ,  $REF1 = REF2 = 2.5\text{ V}$  (specifications exclude any reference contributions), no load on DACs, and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



1x load:  $R_{(SERIES)} = 100\text{ k}\Omega$ ,  $C_{LOAD} = 50\text{ pF}$ ,  $DV_{DD} = 3.3\text{ V}$   
Square-wave output, full-scale amplitude

**Figure 30.  $AV_{CC}$  Load Current Consumption**



1x load:  $R_{(SERIES)} = 100\text{ k}\Omega$ ,  $C_{LOAD} = 50\text{ pF}$ ,  $DV_{DD} = 3.3\text{ V}$   
Square-wave output, full-scale amplitude

**Figure 31.  $AV_{SS}$  Load Current Consumption**

## 7 Detailed Description

### 7.1 Overview

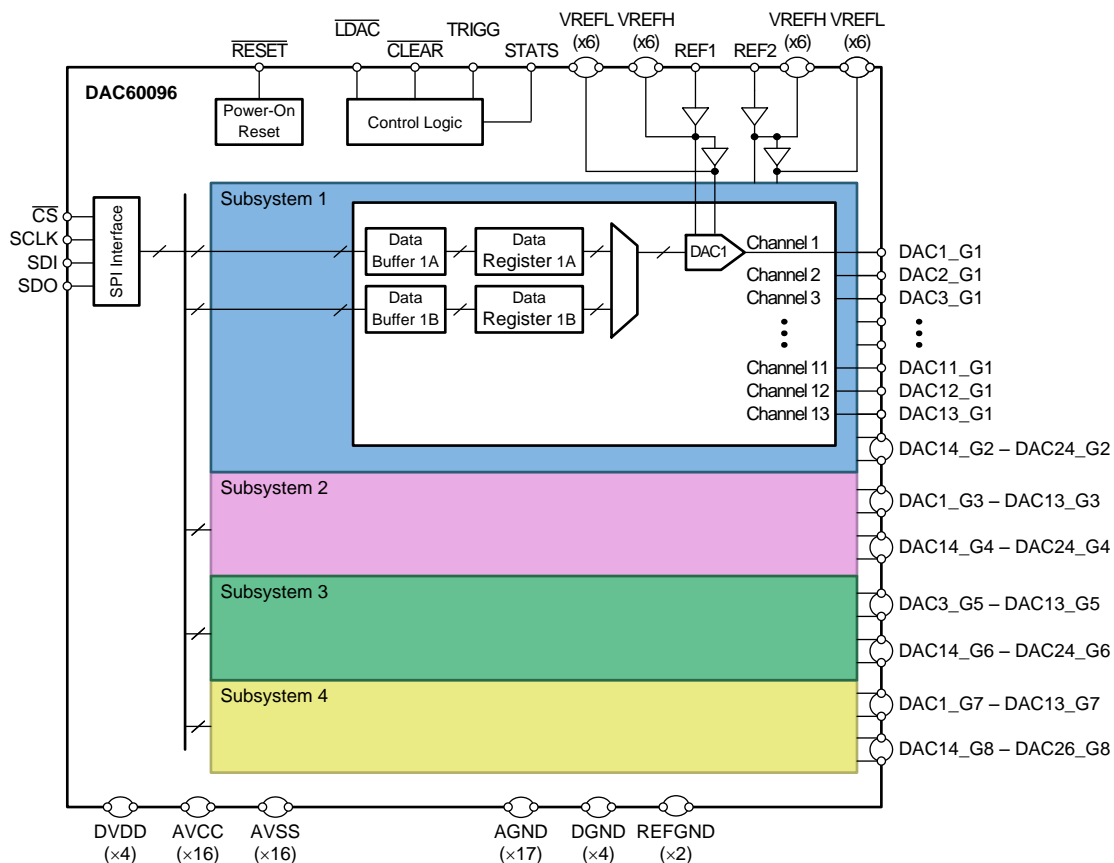
The DAC60096 is a low-power, 96-channel, 12-bit, digital-to-analog converter (DAC). The device provides  $\pm 10.5\text{-V}$  unbuffered bipolar voltage outputs while maintaining extremely low-power operation and good linearity. The device integrates dedicated reference buffers that enable operation from an external 2.5-V reference source.

The DAC60096 can be set up to clear or update all DACs simultaneously. In addition a versatile external conversion trigger allows each DAC to operate as an amplitude-independent square-wave generator. The device incorporates a reset circuit that ensures all DAC outputs power up and remain at zero scale prior to device configuration.

The DAC60096 features simplify the design of systems requiring a high number of precise analog control signals such as those found in optical communications switches and attenuators.

The DAC60096 is designed as four DAC subsystems. Each DAC subsystem is configured independently through a high speed 4-wire serial interface compatible with industry standard microprocessors and microcontrollers. The DAC60096 is characterized for operation over the temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , and is available in a 196-ball, 15-mm  $\times$  15-mm, 1-mm pitch BGA package.

### 7.2 Functional Block Diagram

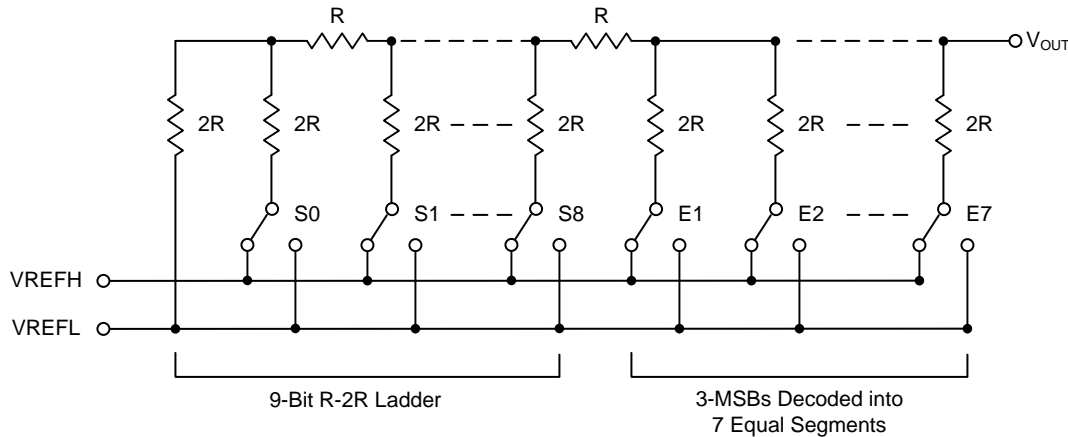


## 7.3 Feature Description

### 7.3.1 Digital-to-Analog Converters (DACs)

The DAC60096 is a 96-channel, 12-bit digital-to-analog converter (DAC) with integrated reference buffers. Each DAC output consists of an R-2R ladder configuration as shown in [Figure 32](#).

The DAC60096 includes reference buffers that enable bipolar DAC output voltages of  $\pm 10.5$  V from a 2.5-V reference source. The outputs of the reference buffers drive the R-2R ladders.



**Figure 32. R-2R Ladder Configuration**

#### 7.3.1.1 DAC Transfer Function

The DAC60096 integrates dedicated reference buffers that enable operation from an external 2.5-V reference source. The reference buffers generate the voltages, VREFH and VREFL, required to drive the DAC R-2R ladders.

$$V_{REFH} = V_{REF} \times \frac{10.5}{2.5} \quad (1)$$

$$V_{REFL} = -1 \times V_{REFH} \quad (2)$$

where  $V_{REF}$  is the reference input voltage at pins REF1 and REF2.

Input data are written to the individual DAC data registers in 12-bit two's complement format. After power-on or a reset event, all DAC registers are set to zero scale. The DAC transfer function is given by [Equation 3](#).

$$V_{OUT} = \frac{Code}{4096} \times (V_{REFH} - V_{REFL}) \quad (3)$$

where *Code* is the signed decimal equivalent of the binary code loaded to the DAC register and ranges from -2048 to 2047 (See [Table 1](#)).

**Table 1. DAC Data Format**

| DIGITAL CODE   | SIGNED DECIMAL VALUE | DAC OUTPUT VOLTAGE (V) |
|----------------|----------------------|------------------------|
| 0111 1111 1111 | +2047                | 10.49487               |
| 0111 1111 1110 | +2046                | 10.48975               |
| 0000 0000 0001 | +1                   | 0.005127               |
| 0000 0000 0000 | 0                    | 0                      |
| 1111 1111 1111 | -1                   | -0.005127              |
| 1000 0000 0001 | -2047                | -10.49487              |
| 1000 0000 0000 | -2048                | -10.5                  |

### 7.3.1.2 DAC Register Structure

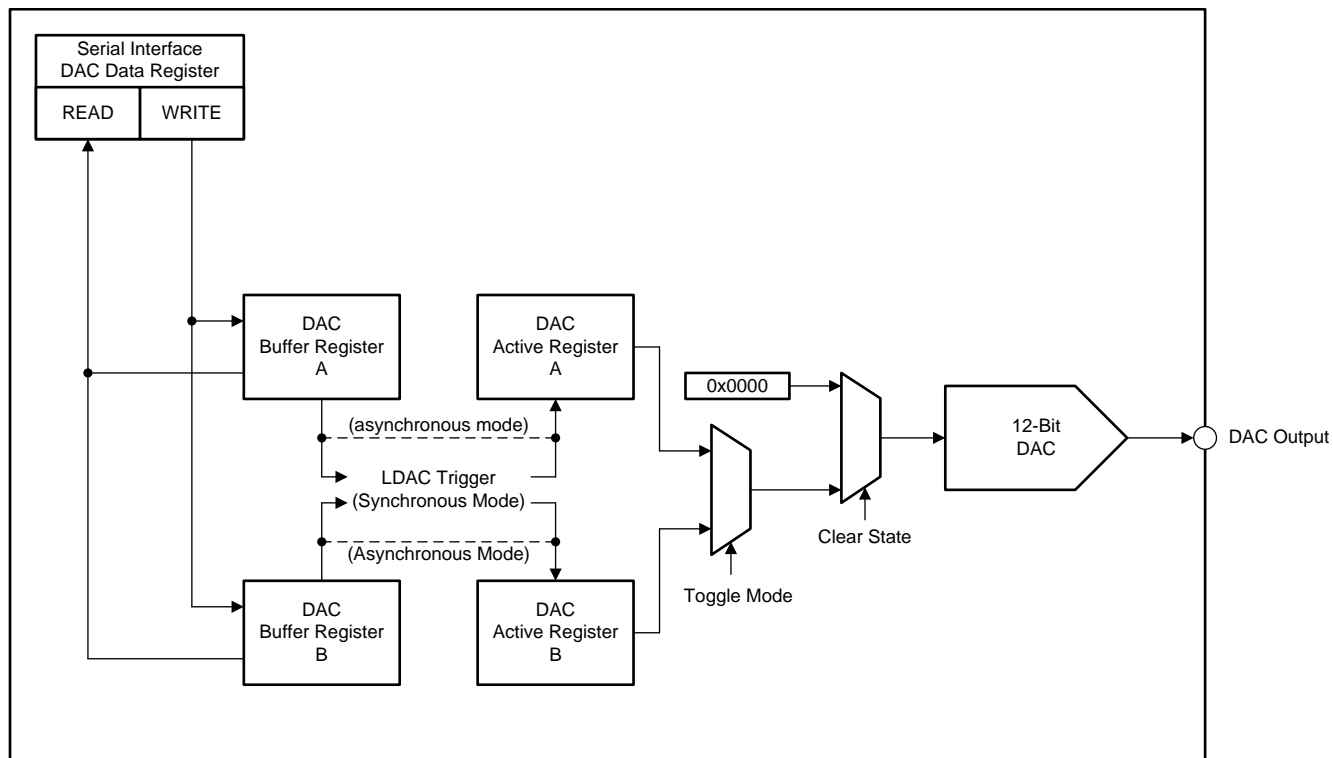
Each DAC in the device incorporates two data registers: Register A and Register B. These two data registers and the TRIGG pin enable toggle mode operation. Alternatively, if the TRIGG pin is left fixed the device is in DC mode operation and only one of the data registers is used to control the DAC output (Register A by default).

Data written to the DAC data registers is initially stored in the DAC buffer registers. Transfer of data from the DAC buffer registers to the active DAC registers can be set to happen immediately (asynchronous mode) or initiated by an LDAC trigger (synchronous mode). After data are transferred to the DAC active registers, the DAC outputs are updated. When the host reads from a DAC data register, the value held in the DAC buffer register is returned (not the value held in the DAC active register).

The DAC update mode is determined by the status of the  $\overline{\text{LDAC}}$  input pin. If the  $\overline{\text{LDAC}}$  pin is held low the device is in asynchronous mode. In asynchronous mode, a write to a DAC data register results in an immediate update of the DAC active register and the corresponding output. If  $\overline{\text{LDAC}}$  is held high, the device is in synchronous mode. In synchronous mode, writing to a DAC data register does not automatically update the DAC output. Instead, the update occurs only after an LDAC trigger occurs. An LDAC trigger is generated either through a high-to-low transition on the LDAC pin in which case all 96 DACs update at the same time or by the self-clearing LDAC bit in each of the four subsystems CON registers (address 0x4, bit 15) which enables synchronization of all the DACs in the selected subsystem.

After the DAC outputs have been configured, a clear event enables the DACs to be loaded with zero-code while retaining the previously programmed values, thus allowing the possibility to return to the voltage being output before the clear event was issued. Note that the DAC data registers can be updated while the device is in clear state allowing the DACs to output new values upon return to normal operation. When the device exits the clear state the DAC outputs are immediately loaded with the data in the DAC active registers.

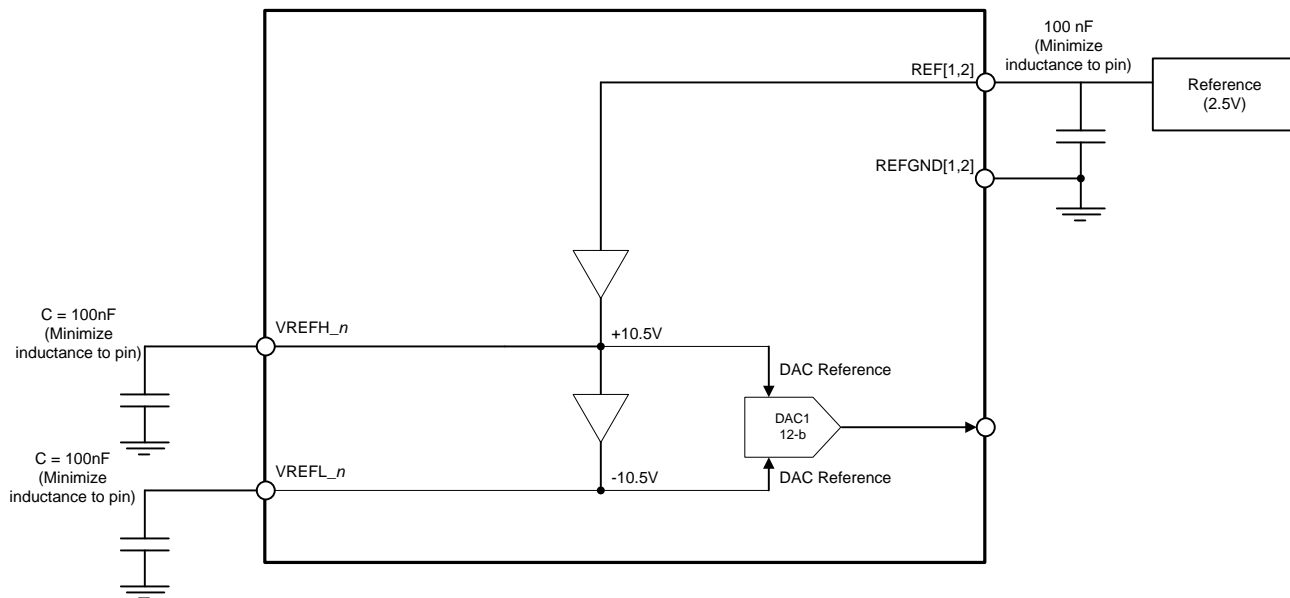
The device is set into clear state through the  $\overline{\text{CLEAR}}$  pin. Setting the  $\overline{\text{CLEAR}}$  pin low forces all 96 DACs into clear state. Setting the  $\overline{\text{CLEAR}}$  pin back high returns all DACs to normal operation. Alternatively, the CLRDAC bits in each of the four subsystems CON registers (Address 0x4, bits [5:4]) can be used to enter or exit clear state at a subsystem level.



**Figure 33. DAC60096 DAC Block Diagram**

### 7.3.2 Reference Specifications

The DAC60096 integrates dedicated reference buffers that enable operation from an external 2.5-V reference source. The reference buffers generate the  $\pm 10.5$ -V levels used to drive the DACs in the device. A 100-nF bypass capacitor should be placed between the REF[1,2] input pins and REFGND[1,2]. Additionally a compensation 100-nF bypass capacitor for each VREFH\_n and VREFL\_n pin (n = G1, G2, G3, G4, G5, G6, G7 or G8) is required and should be placed as close as possible to the pins.



**Figure 34. Reference Operation**

## **7.4 Device Functional Modes**

### **7.4.1 Toggle Mode**

Each DAC in the device incorporates two DAC registers: Register A and Register B. The TRIGG pin is used to switch the DAC outputs back and forth between the contents of the two DAC specific registers. The DAC registers are prepared for trigger mode operation on a TRIGG rising edge and the outputs are toggled on each following high-to-low transition. This feature enables the generation of 96 amplitude independent square-waves.

The device incorporates an auto-populate feature that simplifies register configuration in toggle mode. Auto-populate is enabled by the APB bits in the CON register (address 0x4, bits [1:0]). When auto-populate is enabled, a Register A update automatically loads Register B with the negative value of the data written to A. Although the Register B data can be modified by a direct register write, this update does not auto-populate the Register A contents.

The STATS output pin is used to identify the active register. A logic-low is output for Register A and logic-high for register B. The STATS pin is in high impedance mode by default and must be enabled by the SDRV bits in the CON register for subsystem 1 (address 0x4, bits [9:8]). The SDRV bits in the other three subsystems should be set to high impedance mode (default mode). The toggling rate of the STATS terminal is determined by the SDIV register (address 0x9). The SDIV register should only be updated after a device reset and before configuring the DAC outputs. The STATS output pin toggles on every  $2^{\text{SDIV}}$  trigger pulse ( $\text{SDIV} = 0, 1, \dots, 6$ ).

### **7.4.2 DC Mode**

A fixed TRIGG pin puts the device in DC mode operation. In DC mode only one of the two DAC data registers is used to control the DAC output. If no TRIGG rising edge is detected by the device after power-up, Register A is by default the active register.

## 7.5 Programming

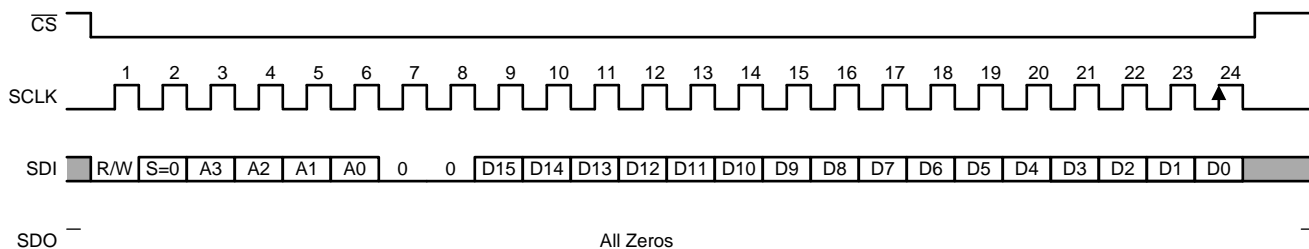
The DAC60096 is controlled through a flexible four-wire serial interface that is compatible with SPI type interfaces used on many microcontrollers and DSP controllers. The interface provides read/write access to all registers of the DAC60096.

For simplification of the register structure, communication to the device is done at a subsystem level through the PTR global pointer register (address 0x6). Subsystem addressing is done through SID[1:0], where subsystem 1 is the default setting. Access to all other registers in the device will affect only the subsystem selected by SID. The DAC pointer setting, DPTR[4:0], also in the PTR register allows access to the data registers (BUFA and BUFB) for any of the DACs in the chosen subsystem.

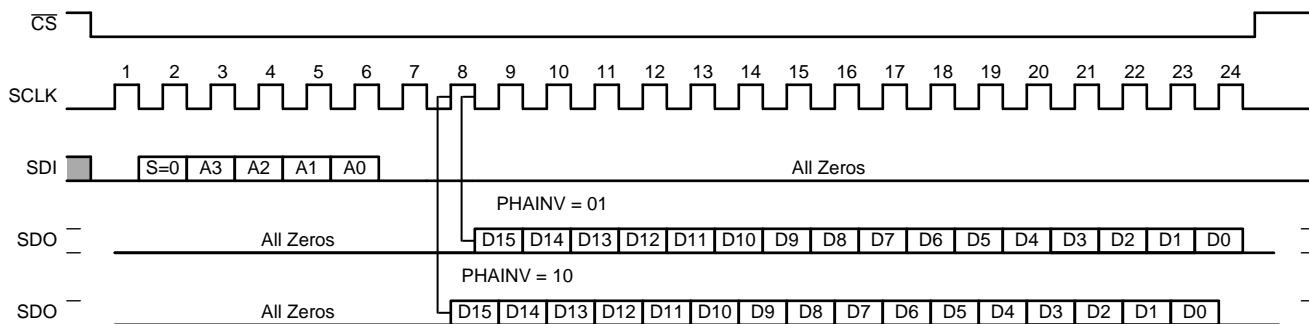
Each serial interface access cycle is exactly 24 bits long. A frame is initiated by asserting the  $\overline{CS}$  pin low. The frame ends when the  $\overline{CS}$  pin is deasserted high. The frame's first byte input to SDI is the instruction cycle which identifies the request as a read or write, streaming or single, and the 4-bit address to be accessed. The following bits in the frame form the data cycle. For all writes, data are clocked on the rising edge of SCLK. On read access, data are clocked out on the SDO pin on either the falling edge or rising edge of SCLK according to the PHAINV setting in each of the four subsystems CON registers (address 0x4, bits [7:6]).

**Table 2. Serial Interface Cycle**

| Bit   | Field    | Description  |
|-------|----------|--|
| 23    | R/W      | Identifies the communication as a read or write command to the addressed register.<br>R/W = 0 sets a write operation. R/W = 1 sets a read operation.   |
| 22    | S        | Identifies the communication as a streaming operation.<br>S = 0 is used for single command instructions. Bit = 1 is used for streaming operation.  |
| 21:18 | A[3:0]   | Register address.<br>Specifies the register to be accessed during the read or write operation.   |
| 17:16 | Reserved | Reserved. Set to zeros for proper operation.   |
| 15:0  | D[15:0]  | Data cycle bits.<br>If a write command, the data cycle bits are the values to be written to the register with address A[3:0]<br>If a read command, the data cycle bits are <i>don't care</i> values. |



**Figure 35. Serial Interface Write Bus Cycle**



**Figure 36. Serial Interface Read Bus Cycle**

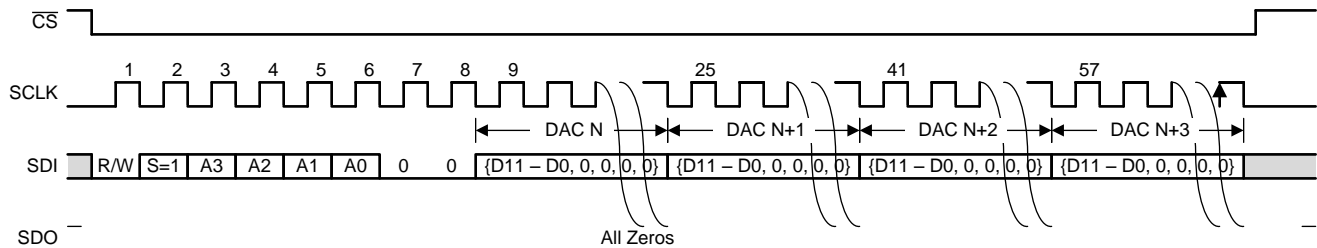
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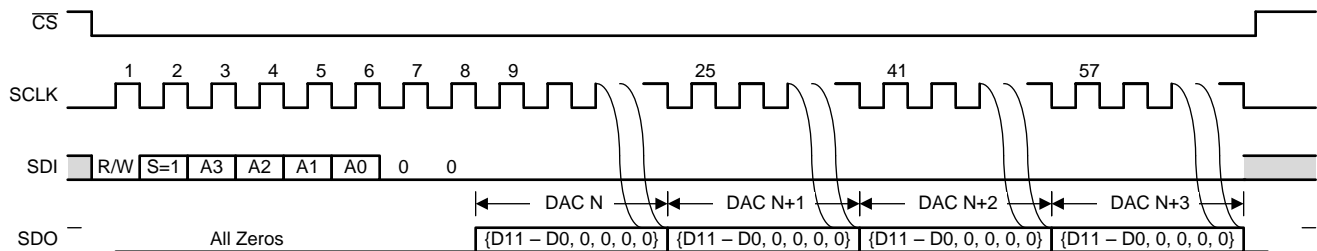
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In order to simplify write or read operations to multiple DACs in a subsystem, streaming mode is supported. In streaming mode, multiple bytes of data can be written to or read from the DAC60096 without specifically providing instructions for each byte and is implemented by continually holding the  $\overline{\text{CS}}$  pin active and continuing to shift new data in or old data out of the device.

The DAC60096 starts reading or writing data to the DAC data register selected by the PTR register and automatically increments the DAC pointer (DPTR) as long as the  $\overline{\text{CS}}$  pin is asserted. If the last DAC in the chosen subsystem has been reached and the  $\overline{\text{CS}}$  pin is still asserted, the data register for this DAC will be overwritten with the new data.



**Figure 37. Serial Interface Streaming Write Cycle**



**Figure 38. Serial Interface Streaming Read Cycle**

### 7.5.1 Frame Error Checking

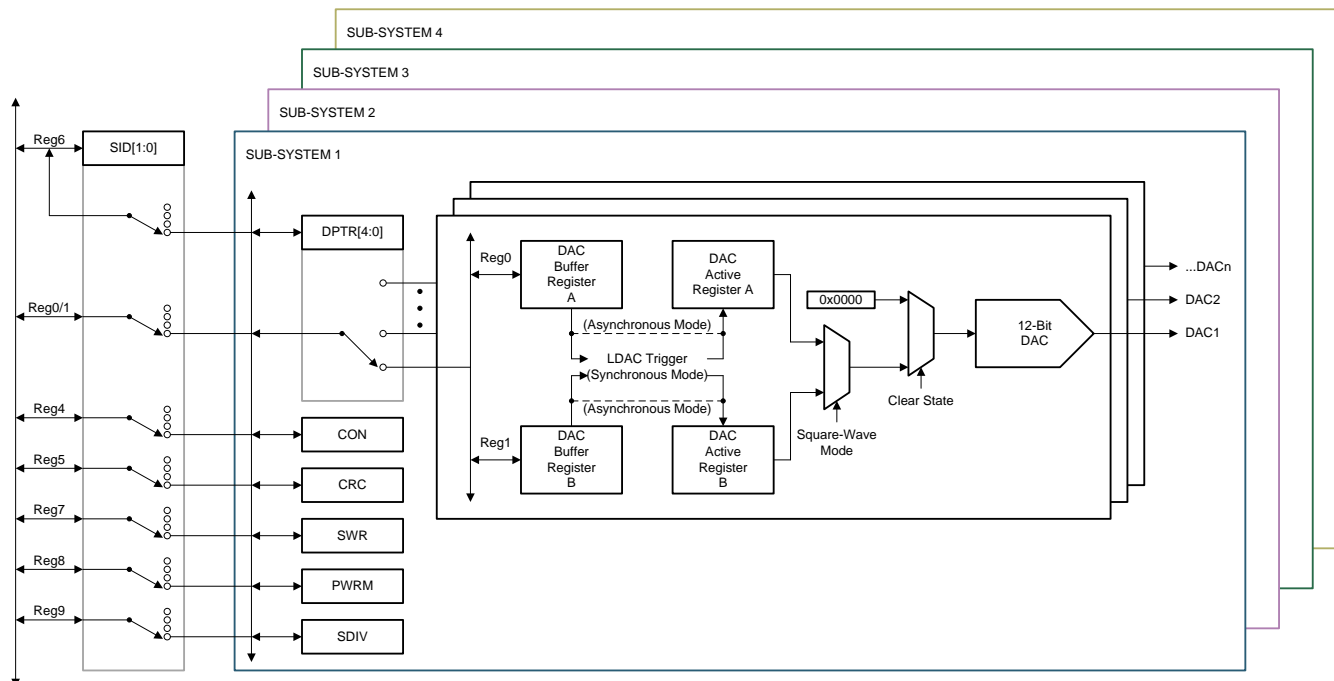
If the DAC60096 is used in a noisy environment, error checking can be used to check the integrity of the serial interface data communication between the device and the host processor. The frame error checking scheme is based on the CRC-CCITT-16 polynomial  $x^{16} + x^{12} + x^5 + 1$  (that is, 0x1021). The CRC register (address 0x5) stores the CRC computation for each single-command or streaming serial interface data write. Reading the CRC register resets its contents to 0xFFFF.

Only valid data cycles are included in the CRC computation. For single-command instructions CRC is calculated and updated only after 16 data bits are received. If a data cycle is longer than 16 bits, the additional bits are not included into the CRC calculation. For streaming commands CRC is calculated and updated on the multiple 16-bit data cycles received. If the number of data bits received is not a multiple of 16, the modulo 16 bits are discarded from the CRC calculation.



## 7.6 Register Maps

Communication to the DAC60096 is done at a subsystem level. Subsystem addressing is done through the global pointer register, SID[1:0]. Each subsystem has 16 registers. Access to the data registers of any of the DACs in the chosen subsystem is done through a DAC pointer, DPTR[4:0].



**Figure 39. Register Configuration**

**Table 3. Register Map**

| REGISTER | TYPE | RESET | ADDRESS   |    |    |    | REGISTER SETUP |     |     |     |       |      |    |        |    |        |    |      |      |     |    |    |
|----------|------|-------|-----------|----|----|----|----------------|-----|-----|-----|-------|------|----|--------|----|--------|----|------|------|-----|----|----|
|          |      |       | A3        | A2 | A1 | A0 | D15            | D14 | D13 | D12 | D11   | D10  | D9 | D8     | D7 | D6     | D5 | D4   | D3   | D2  | D1 | D0 |
| BUFA     | R/W  | 0000  | 0         | 0  | 0  | 0  | BUFA           |     |     |     |       |      |    |        |    |        |    |      | 0    | 0   | 0  | 0  |
| BUFB     | R/W  | 0000  | 0         | 0  | 0  | 1  | BUFB           |     |     |     |       |      |    |        |    |        |    |      | 0    | 0   | 0  | 0  |
| RESERVED | --   | 0000  | 0         | 0  | 1  | 0  | 0              | 0   | 0   | 0   | 0     | 0    | 0  | 0      | 0  | 0      | 0  | 0    | 0    | 0   | 0  |    |
| RESERVED | --   | 0000  | 0         | 0  | 1  | 1  | 0              | 0   | 0   | 0   | 0     | 0    | 0  | 0      | 0  | 0      | 0  | 0    | 0    | 0   | 0  |    |
| CON      | R/W  | 0555  | 0         | 1  | 0  | 0  | LDAC           | 0   | 0   | 0   | SDO2x | SDRV |    | PHAINV |    | CLRDAC |    | 0    | 1    | APB |    |    |
| CRC      | R    | FFFF  | 0         | 1  | 0  | 1  | CRC            |     |     |     |       |      |    |        |    |        |    |      |      |     |    |    |
| PTR      | R    | 0000  | 0         | 1  | 1  | 0  | 0              | 0   | SID |     | 0     | 0    | 0  | 0      | 0  | 0      | 0  | DPTR |      |     |    |    |
| SWR      | R/W  | 0000  | 0         | 1  | 1  | 1  | SWR            |     |     |     |       |      |    |        |    |        |    |      |      |     |    |    |
| PWRM     | R/W  | CAFE  | 1         | 0  | 0  | 0  | PWRM           |     |     |     |       |      |    |        |    |        |    |      |      |     |    |    |
| SDIV     | R/W  | 0000  | 1         | 0  | 0  | 1  | 0              | 0   | 0   | 0   | 0     | 0    | 0  | 0      | 0  | 0      | 0  | 0    | SDIV |     |    |    |
| RESERVED | --   | 0000  | 0xA – 0xF |    |    |    | -----          |     |     |     |       |      |    |        |    |        |    |      |      |     |    |    |

**DAC60096**

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**7.6.1 8.5.1 BUFA Register (address = 0x0) [reset = 0x0000]**
**Figure 40. BUFA Register**

|      |    |    |    |          |    |   |   |
|------|----|----|----|----------|----|---|---|
| 15   | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| BUFA |    |    |    |          |    |   |   |
| R/W  |    |    |    |          |    |   |   |
| 7    | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| BUFA |    |    |    | RESERVED |    |   |   |
| R/W  |    |    |    | R/W      |    |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 4. BUFA Register**

| Bit  | Field    | Type | Reset | Description   |
|------|----------|------|-------|---|
| 15:4 | BUFA     | R/W  | 0000  | Double-buffer MSB aligned 12-bit data for DAC register A. The specific DAC accessed by this register must be first set by the subsystem address (SID) and DAC pointer (DPTR). |
| 3:0  | Reserved | R/W  | 0000  | Not used  |

**7.6.2 BUFB Register (address = 0x1) [reset = 0x0000]**
**Figure 41. BUFB Register**

|      |    |    |    |          |    |   |   |
|------|----|----|----|----------|----|---|---|
| 15   | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| BUFB |    |    |    |          |    |   |   |
| R/W  |    |    |    |          |    |   |   |
| 7    | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| BUFB |    |    |    | Reserved |    |   |   |
| R/W  |    |    |    | R/W      |    |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 5. BUFB Register**

| Bit  | Field    | Type | Reset | Description   |
|------|----------|------|-------|---|
| 15:4 | BUFB     | R/W  | 0000  | Double-buffer MSB aligned 12-bit data for DAC register B. The specific DAC accessed by this register must be first set by the subsystem address (SID) and DAC pointer (DPTR). |
| 3:0  | Reserved | R/W  | 0000  | Not used  |

### 7.6.3 CON Register (address = 0x4) [reset = 0x0555]

**Figure 42. CON Register**

|             |          |             |    |            |    |           |   |
|-------------|----------|-------------|----|------------|----|-----------|---|
| 15          | 14       | 13          | 12 | 11         | 10 | 9         | 8 |
| LDAC        | Reserved |             |    | SDO2x[1:0] |    | SDRV[1:0] |   |
| R/W         | R/W      |             |    | R/W        |    | R/W       |   |
| 7           | 6        | 5           | 4  | 3          | 2  | 1         | 0 |
| PHAINV[1:0] |          | CLRDAC[1:0] |    | Reserved   |    | APB[1:0]  |   |
| R/W         |          | R/W         |    | R/W        |    | R/W       |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 6. CON Register**

| Bit   | Field       | Type | Reset | Description  |
|-------|-------------|------|-------|--|
| 15    | LDAC        | R/W  | 0     | Setting this bit to 1 issues an LDAC trigger at $\overline{CS}$ rising edge. Self-clearing bit.  |
| 14:12 | Reserved    | R/W  | 000   | Not used.  |
| 11:10 | SDO2x[1:0]  | R/W  | 01    | SDO 1x/2x drive strength:<br>01: 1x (default)<br>10: 2x<br>Writing 00 or 11 has no effect  |
| 9:8   | SDRV[1:0]   | R/W  | 01    | SDRV control STATS pin drive type:<br>01: Hi-Z. STATS pin is disabled (default)<br>10: CMOS Push-pull output. Should only be enabled for subsystem 1.<br>Writing 00 or 11 has no effect  |
| 7:6   | PHAINV[1:0] | R/W  | 01    | PHAINV controls SDO output edge:<br>01: SCLK NegEdge (default)<br>10: SCLK PosEdge<br>Writing 00 or 11 has no effect   |
| 5:4   | CLRDAC[1:0] | R/W  | 01    | Clear DAC state control:<br>01: Normal operating state (default)<br>10: Clear DAC state<br>Writing 00 or 11 has no effect  |
| 3:2   | Reserved    | R/W  | 01    | Reserved for factory use   |
| 1:0   | APB[1:0]    | R/W  | 01    | Auto populate B:<br>01: Auto-populates BUFB with the negative value of BUFA after each BUFA register write. Writing to BUFB has no auto-populate effect (default)<br>10: Disable auto populate B feature<br>Writing 00 or 11 has no effect |

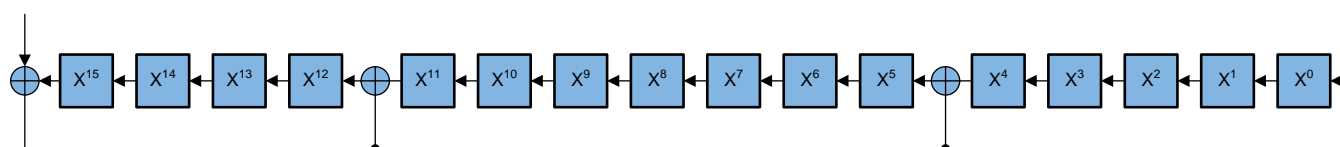
**7.6.4 CRC Register (address = 0x5) [reset = 0xFFFF]**
**Figure 43. CRC Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CRC[15:0] |    |    |    |    |    |   |   |
| R         |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CRC[15:0] |    |    |    |    |    |   |   |
| R         |    |    |    |    |    |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7. CRC Register**

| Bit  | Field     | Type | Reset | Description  |
|------|-----------|------|-------|--|
| 15:0 | CRC[15:0] | R    | FFFF  | Stores the CRC computation data for each SPI data write. CRC includes stream writes. The address byte is not included in the CRC computation.<br>Reading Reg CRC resets current CRC value to 0xFFFF. CRC is calculated when $\overline{CS}$ is enabled and the data cycle contains a multiple of 16 bits. The redundant data are not written into the register.<br>CRC-CCITT polynomial is used $x^{16} + x^{12} + x^5 + 1$ , or in hex: 0x1021 with default 0xFFFF. |


**Figure 44. CRC CCITT 16**

### 7.6.5 PTR Register (address = 0x6) [reset = 0x0000]

**Figure 45. PTR Register**

|          |    |          |           |          |    |   |   |
|----------|----|----------|-----------|----------|----|---|---|
| 15       | 14 | 13       | 12        | 11       | 10 | 9 | 8 |
| Reserved |    | SID[1:0] |           | Reserved |    |   |   |
| R/W      |    | R/W      |           | R/W      |    |   |   |
| 7        | 6  | 5        | 4         | 3        | 2  | 1 | 0 |
| Reserved |    |          | DPTR[4:0] |          |    |   |   |
| R/W      |    |          | R/W       |          |    |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 8. PTR Register**

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 15:14 | Reserved  | R/W  | 00    | Reserved for factory use   |
| 13:12 | SID[1:0]  | R/W  | 00    | Subsystem address:<br>00: Subsystem 1<br>01: Subsystem 2<br>10: Subsystem 3<br>11: Subsystem 4 |
| 11:8  | Reserved  | R/W  | 0000  | Not used   |
| 7:5   | Reserved  | R/W  | 000   | Reserved for factory use   |
| 4:0   | DPTR[4:0] | R/W  | 0000  | DAC pointer  |

### 7.6.6 SWR Register (address = 0x7) [reset = 0x0000]

**Figure 46. SWR Register**

|     |    |    |    |    |    |   |   |
|-----|----|----|----|----|----|---|---|
| 15  | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SWR |    |    |    |    |    |   |   |
| R/W |    |    |    |    |    |   |   |
| 7   | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| SWR |    |    |    |    |    |   |   |
| R/W |    |    |    |    |    |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9. SWR Register**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 15:0 | SWR   | R/W  | 0000  | Writing 0xA5A5 to this register generates a software reset on the $\overline{CS}$ rising edge of the command for a subsystem. The software reset is similar to a hardware reset, which resets all registers and logic states.<br>Reading this register gives the hardware version of the subsystem. |

### 7.6.7 PWRM Register (address = 0x6) [reset = 0xCAFE]

**Figure 47. PWRM Register**

|      |    |    |    |    |    |   |   |
|------|----|----|----|----|----|---|---|
| 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PWRM |    |    |    |    |    |   |   |
| R/W  |    |    |    |    |    |   |   |
| 7    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| PWRM |    |    |    |    |    |   |   |
| R/W  |    |    |    |    |    |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 10. PWRM Register**

| Bit  | Field | Type | Reset | Description  |
|------|-------|------|-------|--|
| 15:0 | PWRM  | R/W  | 0000  | <p>DV<sub>DD</sub> Power Monitor:</p> <p>After device power up, the PWRM register is 0xCAFE. Any register write to PWRM sets PWRM to 0xABBA. PWRM is reset to 0xCAFE after a DVDD collapse initiated POR event. Reading PWRM with value 0xCAFE indicates power failure or uninitialized value.</p> <p>The system controller can monitor PWRM to check for active power status. The device toggles the PWRM value after every PWRM register read. If the current read value is 0xABBA, the next read value will be 0xBAAB, and vice versa.</p> <p>The PWRM register only monitors DV<sub>DD</sub> power failure. AV<sub>CC</sub> is monitored by the analog reset circuit. When there is a power failure on AV<sub>CC</sub> all the DACs in the device go into clear state.</p> |

### 7.6.8 SDIV Register (address = 0x9) [reset = 0x0000]

**Figure 48. SDIV Register**

|          |    |    |    |    |      |   |   |
|----------|----|----|----|----|------|---|---|
| 15       | 14 | 13 | 12 | 11 | 10   | 9 | 8 |
| Reserved |    |    |    |    |      |   |   |
| R/W      |    |    |    |    |      |   |   |
| 7        | 6  | 5  | 4  | 3  | 2    | 1 | 0 |
| Reserved |    |    |    |    | SDIV |   |   |
| R/W      |    |    |    |    | R/W  |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 11. SDIV Register**

| Bit  | Field    | Type | Reset | Description  |
|------|----------|------|-------|--|
| 15:3 | Reserved | R/W  | 0000  | Not Used   |
| 2:0  | SDIV     | R/W  | 000   | <p>Status signal toggle rate:</p> <p>STATS pin toggling rate is controlled by SDIV register. SDIV is valid between 0 and 6. The STATS pin toggles on every 2<sup>SDIV</sup> trigger pulse.</p> <p>The SDIV setting should only be updated after a device reset and before configuring the DAC outputs.</p> |

## 8 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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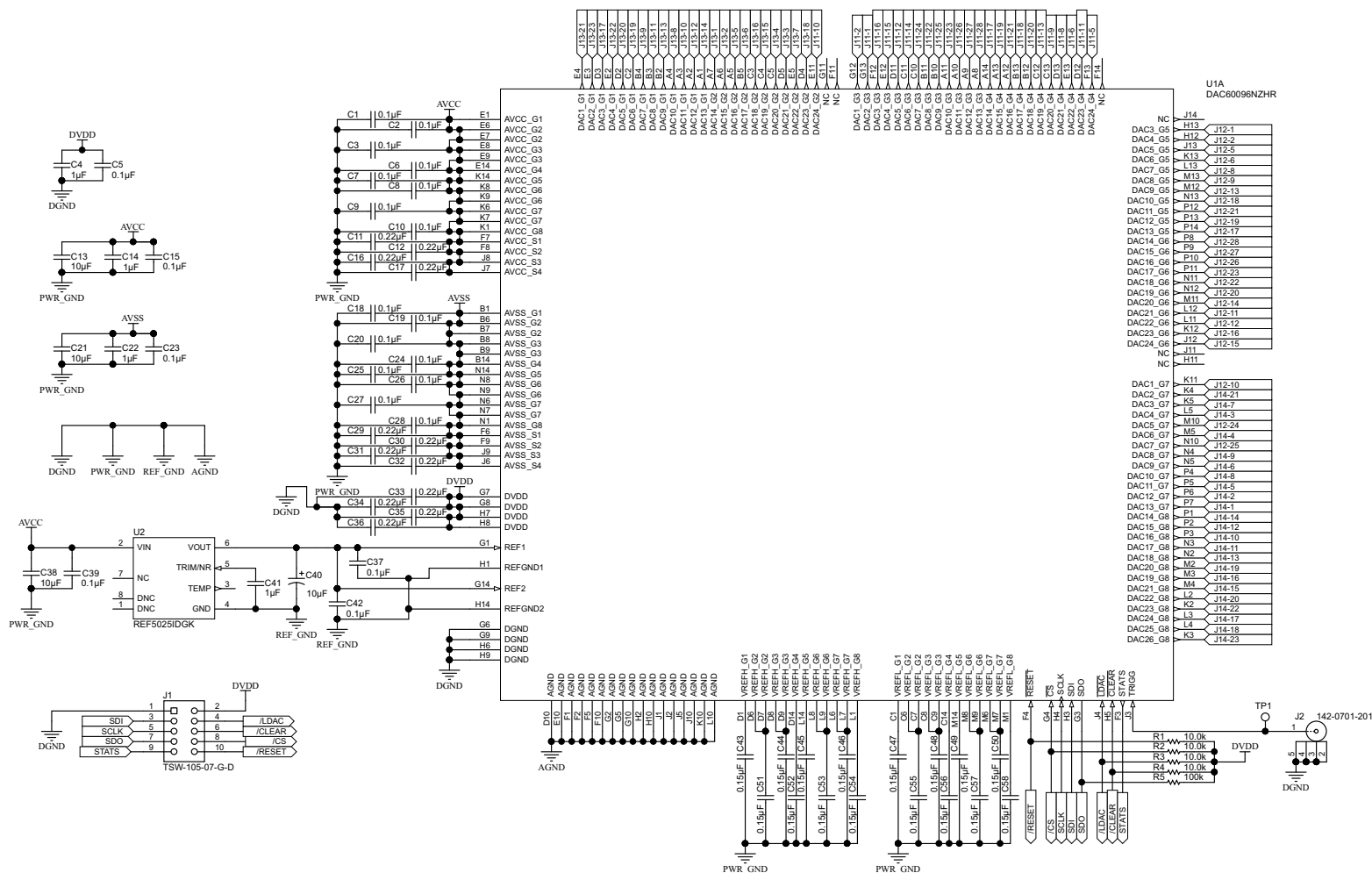
### 8.1 Application Information

The DAC60096 is a low-power, 96-channel, 12-bit, digital-to-analog converter (DAC). The device provides unbuffered bipolar voltage outputs up to  $\pm 10.5$  V.

This device is suitable for many applications involving multichannel bipolar DACs. Such applications include multichannel variable optical attenuators, MEMS mirror control, and ATE level drivers.

## 8.2 Typical Application

An example schematic incorporating the DAC60096 device is shown in [Figure 49](#).



**Figure 49. Example Schematic**



## 8.2.1 Design Requirements

Figure 49 uses the parameters shown in Table 12.

Table 12. Design Parameters

| PARAMETER        | VALUE |
|------------------|-------|
| AV <sub>CC</sub> | 12 V  |
| DV <sub>DD</sub> | 5 V   |
| AV <sub>SS</sub> | –12 V |
| REF1             | 2.5 V |
| REF2             | 2.5 V |

## 8.2.2 Detailed Design Procedure

The following sections display components and applications that may facilitate the design process.

### 8.2.2.1 Power-Supply Bypassing

For accurate, high-resolution performance, all power supply pins should be bypassed to ground with low ESR ceramic bypass capacitors. For additional noise filtering, use a 10-μF capacitor in parallel with a 0.1-μF capacitor.

### 8.2.2.2 Reference Input

The internal reference buffers of the DAC60096 device require an external 2.5-V reference voltage source, which can be driven externally through a precision voltage source or generated from a high precision voltage IC. One such integrated circuit is the REF5025, which is a low-noise, low-drift, high precision voltage reference. The basic connections are listed in Figure 50. A supply bypass capacitor ranging between 1 μF to 10 μF is recommended. A 1-μF to 50-μF output capacitor must be connected from V<sub>OUT</sub> to GND. The ESR value of the output capacitor must be less than or equal to 1.5 Ω to ensure output stability. To help minimize noise, an additional 1-μF capacitor is connected from TRIM/NR to GND.

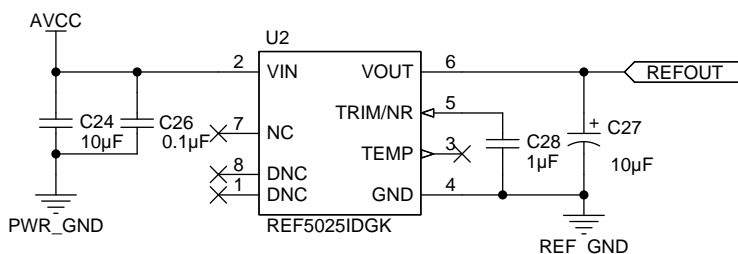


Figure 50. External Reference

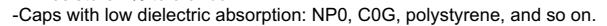
### 8.2.2.3 TRIGG/Signal Conditioning

The TRIGG input signal provides the square waveform required for the DAC60096 device to operate as a square-wave generator. The DAC registers are prepared for square wave operation on a TRIGG rising edge and the outputs toggle on the falling edge. The [Timing Requirements<sup>\(1\)\(2\)</sup>](#) table specifies the timing parameters required for proper operation.

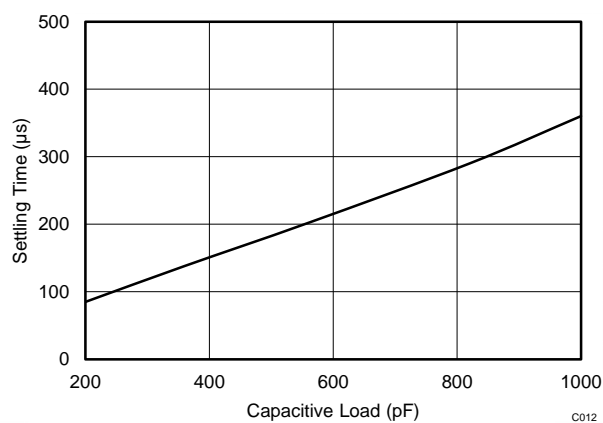
The TRIGG input signal can be supplied from a waveform generator or voltage-to-frequency converter. An example device with schematic is provided in Figure 51. The device highlighted is the LM231, a precision voltage-to-frequency converter with wide range of full-scale frequency (1 Hz to 100 kHz). In Figure 51 the device is configured to display 0.05% linearity over an output frequency range of 10 Hz to 4 kHz with an input range of 25 mV to 12.5 V. For more information, refer to the *Typical Applications* section of the LM231 datasheet (SNOSBI2).

(1) Specified by design and characterization. Not tested during production.

(2) SDO loaded with 10-pF load capacitance for SDO timing specifications.



### 8.2.3 Application Curves



**Figure 53. DAC Settling Time vs Capacitive Load**

## 9 Power Supply Recommendations

It is highly recommended that  $AV_{CC}$  is supplied prior to  $AV_{SS}$ .  $DV_{DD}$  sequencing is not critical. The recommended sequence is  $AV_{CC}$  followed by  $AV_{SS}$  with  $DV_{DD}$  and the REF[1,2] inputs applied last.

**Table 13. Input-Voltage Recommendations**

|                                  |                         |                          | MIN   | TYP | MAX   | UNIT |
|----------------------------------|-------------------------|--------------------------|-------|-----|-------|------|
| Supply voltage                   | $AV_{CC}$               |                          | 11.2  | 12  | 12.6  | V    |
|                                  | $AV_{SS}$               |                          | –12.6 | –12 | –11.2 | V    |
|                                  | $DV_{DD}$               |                          | 3     | 3.3 | 5.5   | V    |
|                                  | $AV_{CC}$ to $AV_{SS}$  |                          | 22.4  | 24  | 25.2  | V    |
| <b>EXTERNAL REFERENCE INPUTS</b> |                         |                          |       |     |       |      |
| $V_{REF}$                        | Reference input voltage | REF1 and REF2 input pins | 2.475 | 2.5 | 2.525 | V    |

### 9.1 Device Reset Options

#### 9.1.1 Power-on-Reset (POR)

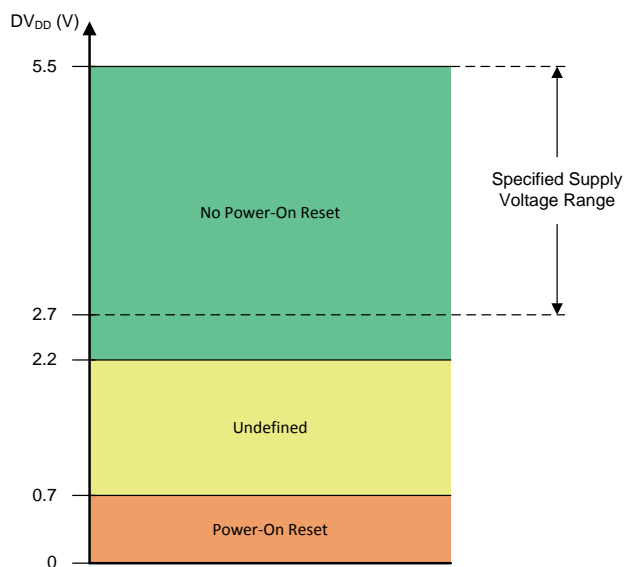
The DAC60096 includes a power-on reset function. After the  $DV_{DD}$  supply has been established a POR event is issued. The POR causes all registers to initialize to their default values and communication with the device is valid only after a 250  $\mu$ s power-on-reset delay. The default value for all DACs is zero-code.

A power failure on  $DV_{DD}$  also results in a power-on-reset event. The PWRM register (address 0x8) can be used to monitor a  $DV_{DD}$  power failure. After power-up the PWRM register is set to 0xCAFE. Any register write to the PWRM register changes its contents to 0xABBA. If a PWRM register read returns 0xCAFE either the PWRM register has not been initialized or a  $DV_{DD}$  power failure has occurred.

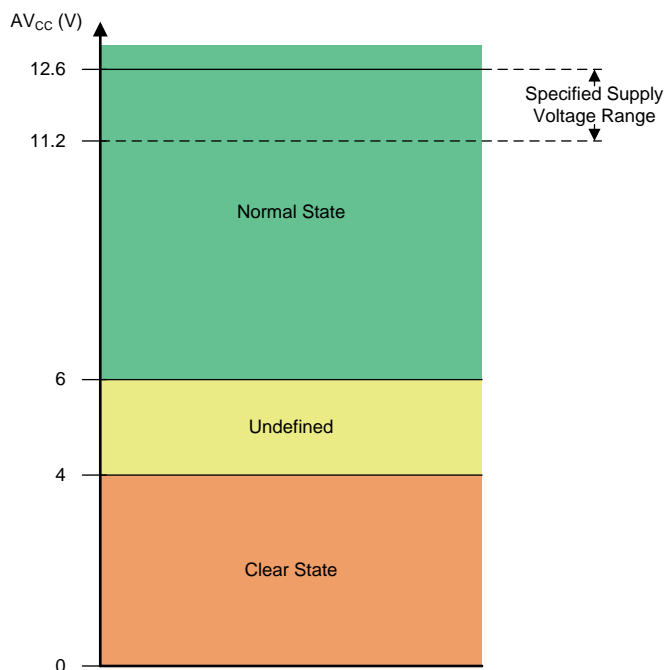
The device also includes an  $AV_{CC}$  power failure detection circuit. In contrast to a  $DV_{DD}$  power failure, a collapse in  $AV_{CC}$  does not result in a reset event. An  $AV_{CC}$  power failure forces all DACs to go into clear state but does not reset the DAC data register values which enables the device to return to normal operation once  $AV_{CC}$  recovers. Even though the DACs are loaded with zero-code during an  $AV_{CC}$  power failure, it is important to note that this does not necessarily indicate the DAC outputs will be at 0 V due to  $AV_{CC}$  being outside of its supply voltage range.

As long as  $DV_{DD}$  and  $AV_{CC}$  remain above their specified high threshold a power failure event will not occur. In order to ensure a  $DV_{DD}$  or  $AV_{CC}$  collapse is registered as such by the device, these supplies must be below their corresponding low threshold for at least 1 ms. When the supplies drop below their high threshold but remain over the lower one (shown as the undefined region of [Figure 54](#) and [Figure 55](#)), the device may or may not reset ( $DV_{DD}$ ) or go into clear state ( $AV_{CC}$ ) under all specified temperature and power-supply conditions.

## Device Reset Options (continued)



**Figure 54. Threshold Levels for DV<sub>DD</sub> POR Circuit**



**Figure 55. Threshold Levels for AV<sub>CC</sub> Clear Circuit**

### 9.1.2 Hardware Reset

A device hardware reset event is initiated by a minimum 500 ns logic low on the  $\overline{\text{RESET}}$  pin. A hardware reset causes all registers to initialize to their default values and communication with the device is valid only after a 50  $\mu\text{s}$  reset delay. The default value for all DACs is zero-code.

### 9.1.3 Software Reset

A subsystem software reset event is initiated by writing 0xA5A5 to the SWR register (address 0x7) for that particular subsystem. The software reset command is triggered on the  $\overline{\text{CS}}$  rising edge of the instruction. As with the hardware reset, a software reset causes all registers to initialize to their default values and communication with the device is valid only after a 50  $\mu\text{s}$ . Note, however, that the reset only applies to the subsystem being addressed during the command. In order to reset the entire device as a hardware reset does, a software reset command should be issued to each of the four subsystems in the device.

## 10 Layout

### 10.1 Layout Guidelines

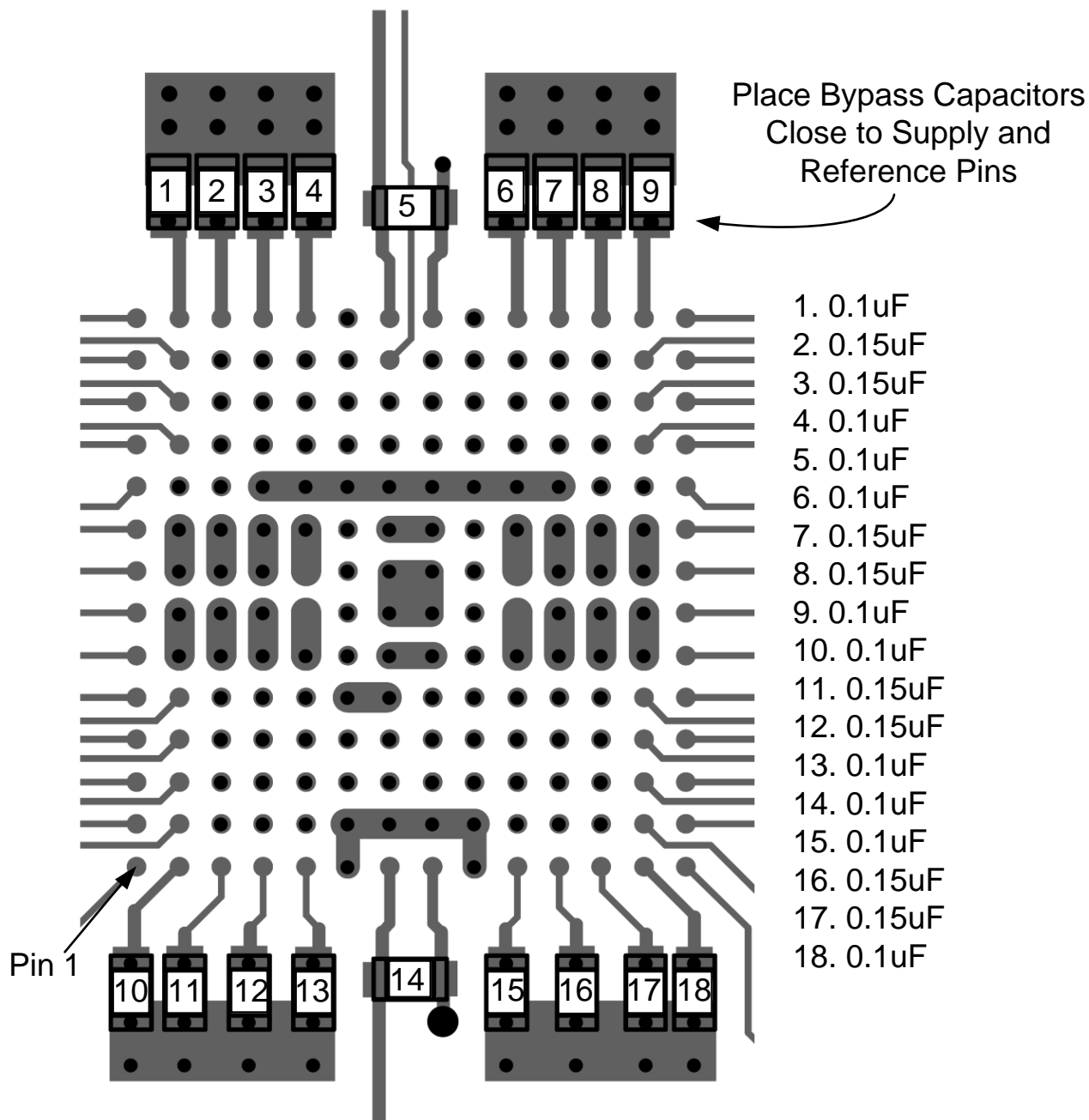
- Bypass all power-supply pins to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1- $\mu$ F to 0.22- $\mu$ F ceramic with a X7R or NP0 dielectric.
- Place power supplies and VREFH/L bypass capacitors close to pins to minimize inductance and optimize performance. Inner supply and reference pads can connect to the bypass arrangement on the bottom layer of the PCB through vias to minimize trace length. This is illustrated in [Figure 56](#) and [Figure 59](#).
- Include a 100-nF bypass capacitor for both internal reference inputs between this pin and their respective ground pins.
- Use a high-quality ceramic type NP0 or X7R for optimal performance across temperature, and low dissipation factor.
- Make sure that the digital and analog sections have proper placement with respect to the digital pins and analog pins of the DAC60096 device. The separation of analog and digital blocks allow for better design and practice because it reduces coupling into neighboring blocks, and minimizes the interaction between analog and digital return currents.

### 10.2 Layout Examples

#### 10.2.1 Optimal Layout Example

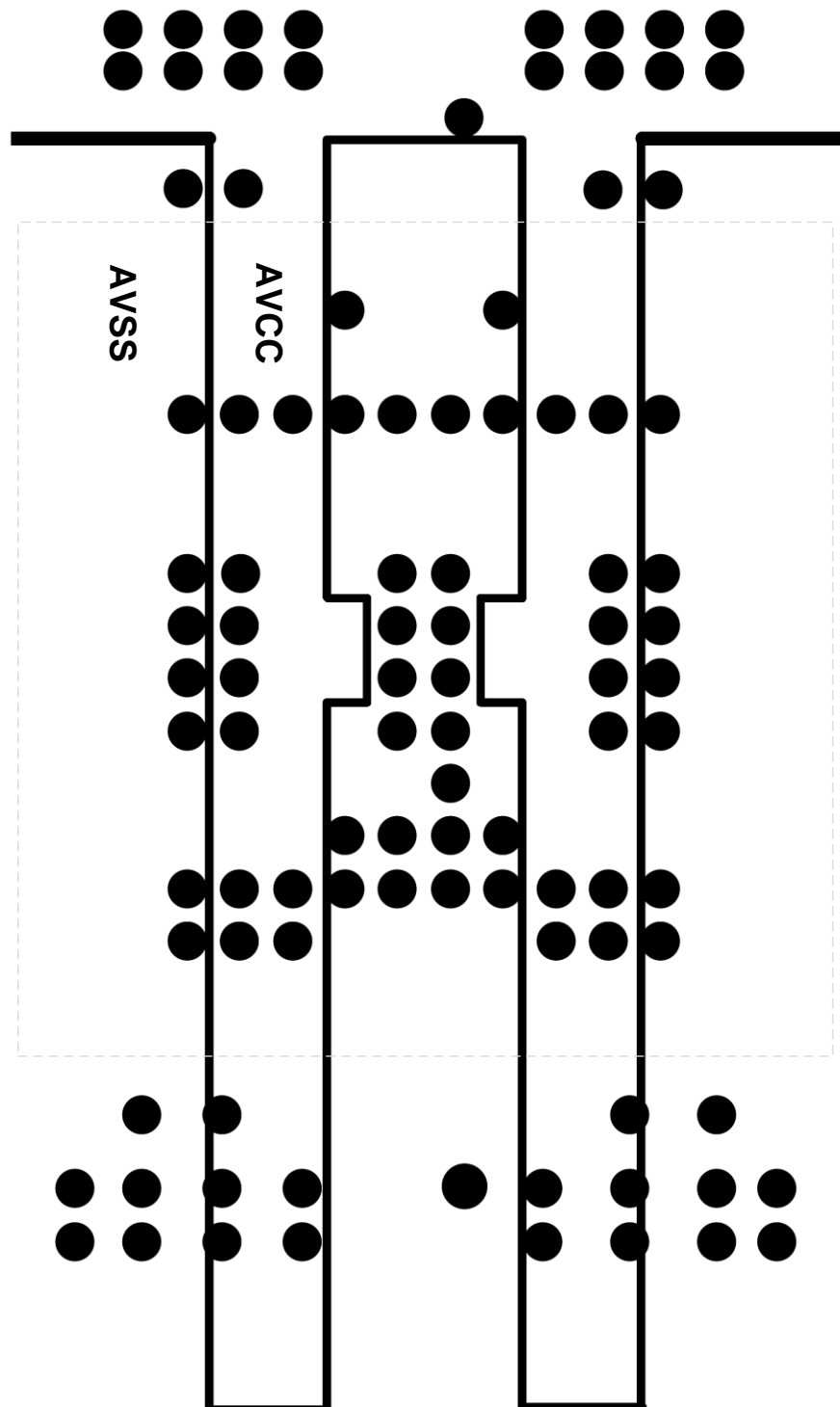
Optimal layout requires the addition of blind vias. This layout reduces trace length and brings the bypass capacitor arrangements closer to the device pads. [Figure 56](#) to [Figure 59](#) show the board layouts.

## Layout Examples (continued)



**Figure 56. DAC60096 Example Board Layout – Top Layer PCB**

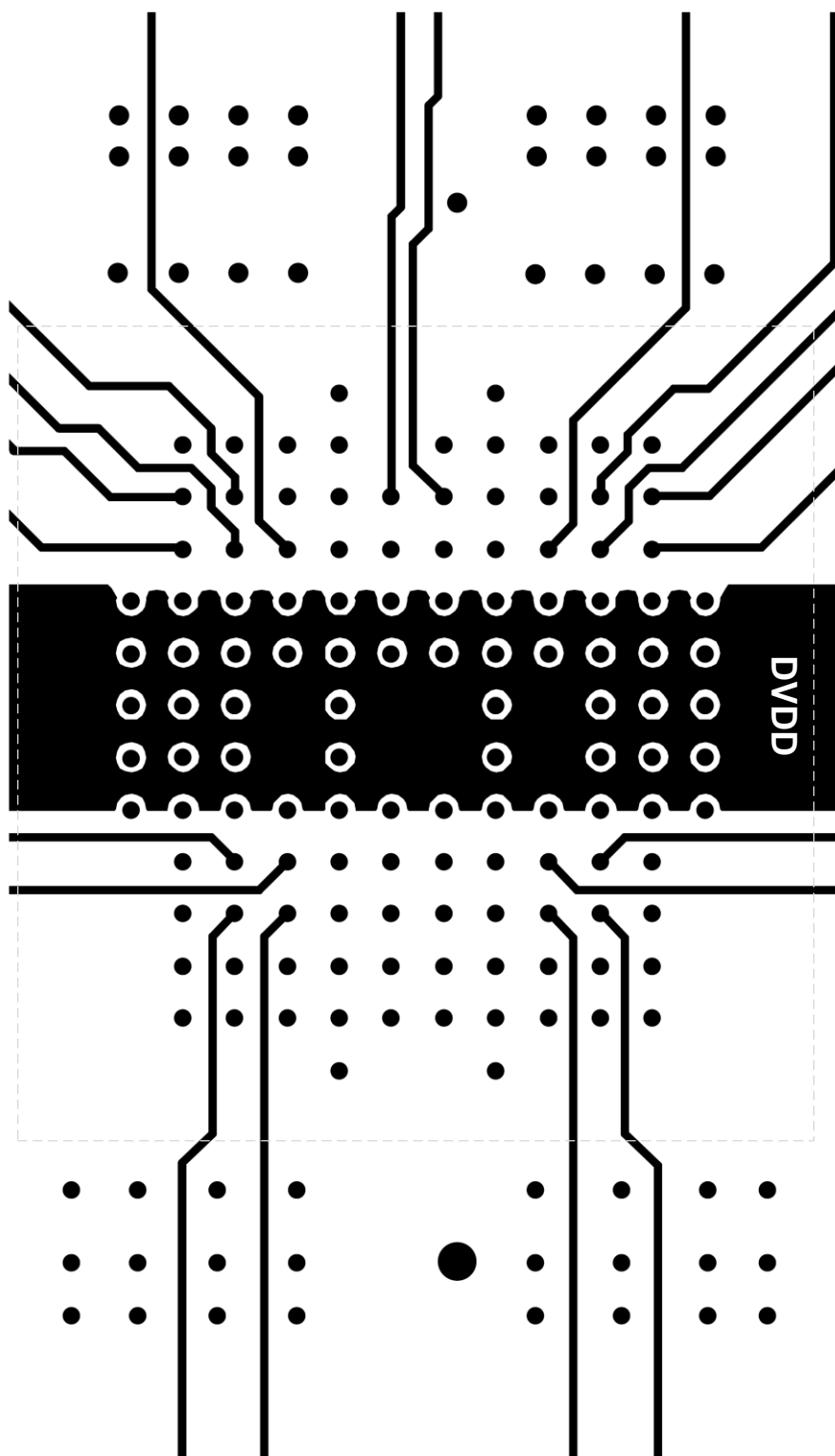
**Layout Examples (continued)**



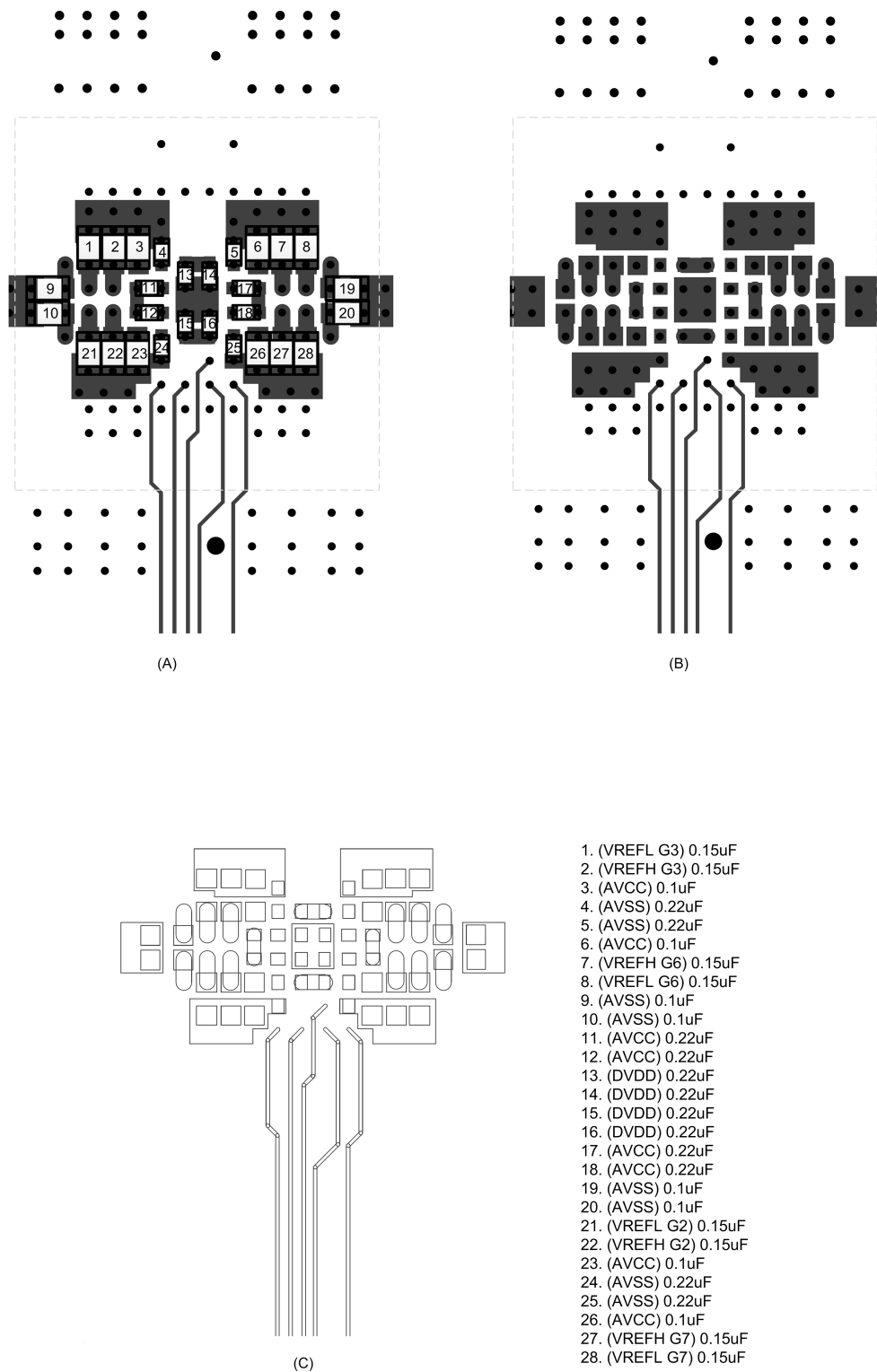
**Figure 57. DAC60096 Example Board Layout – Internal AVCC and AVSS Plane**



## Layout Examples (continued)



**Figure 58. DAC60096 Example Board Layout – DVDD Internal Plane With Select DAC Outputs**

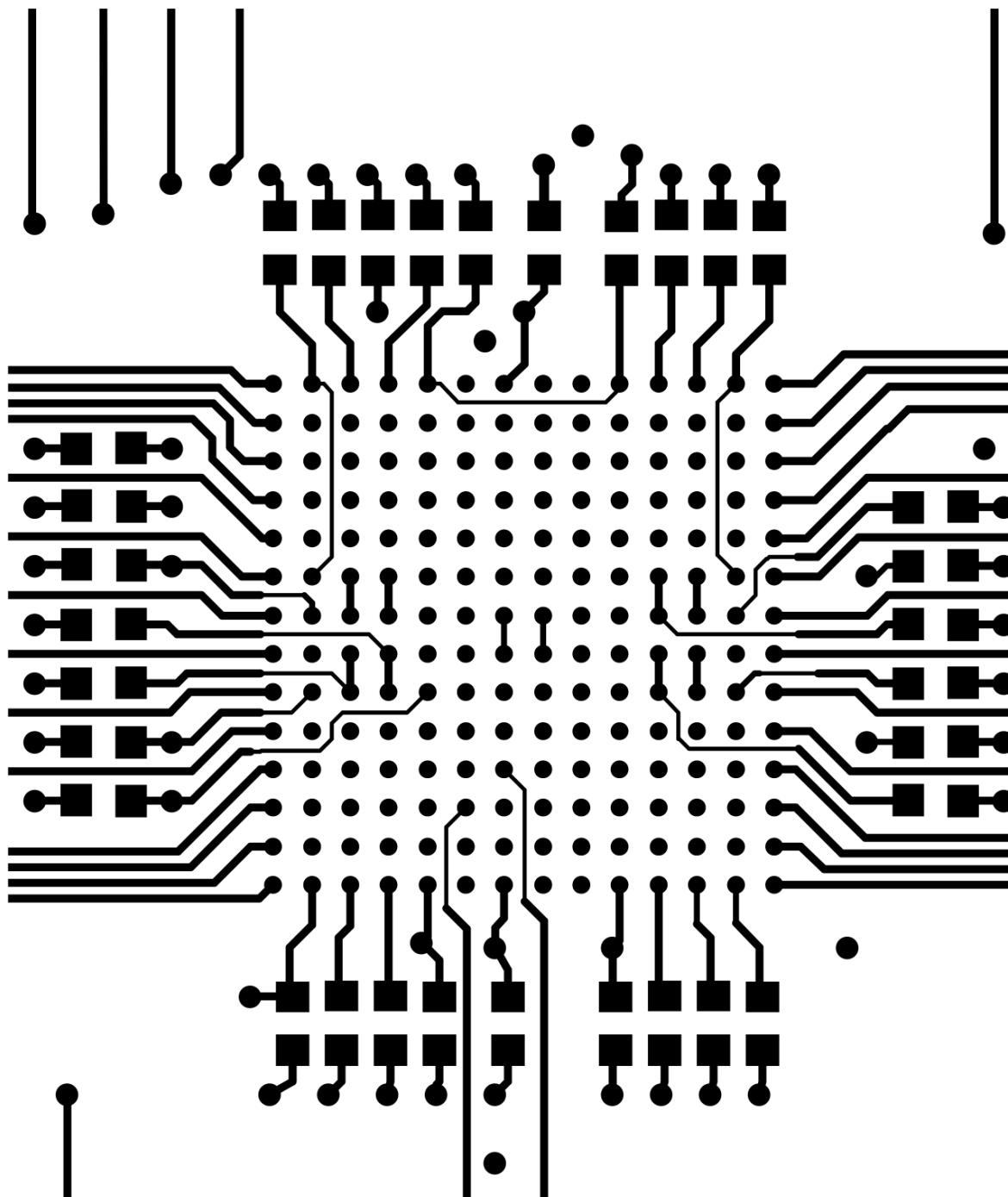
**Layout Examples (continued)**


**Figure 59. DAC60096 Example Board Layout – Bottom Layer PCB.**  
**(A): Bypass Capacitor Arrangement; (B) Polygon Pours; (C) PAD With Pours**

## Layout Examples (continued)

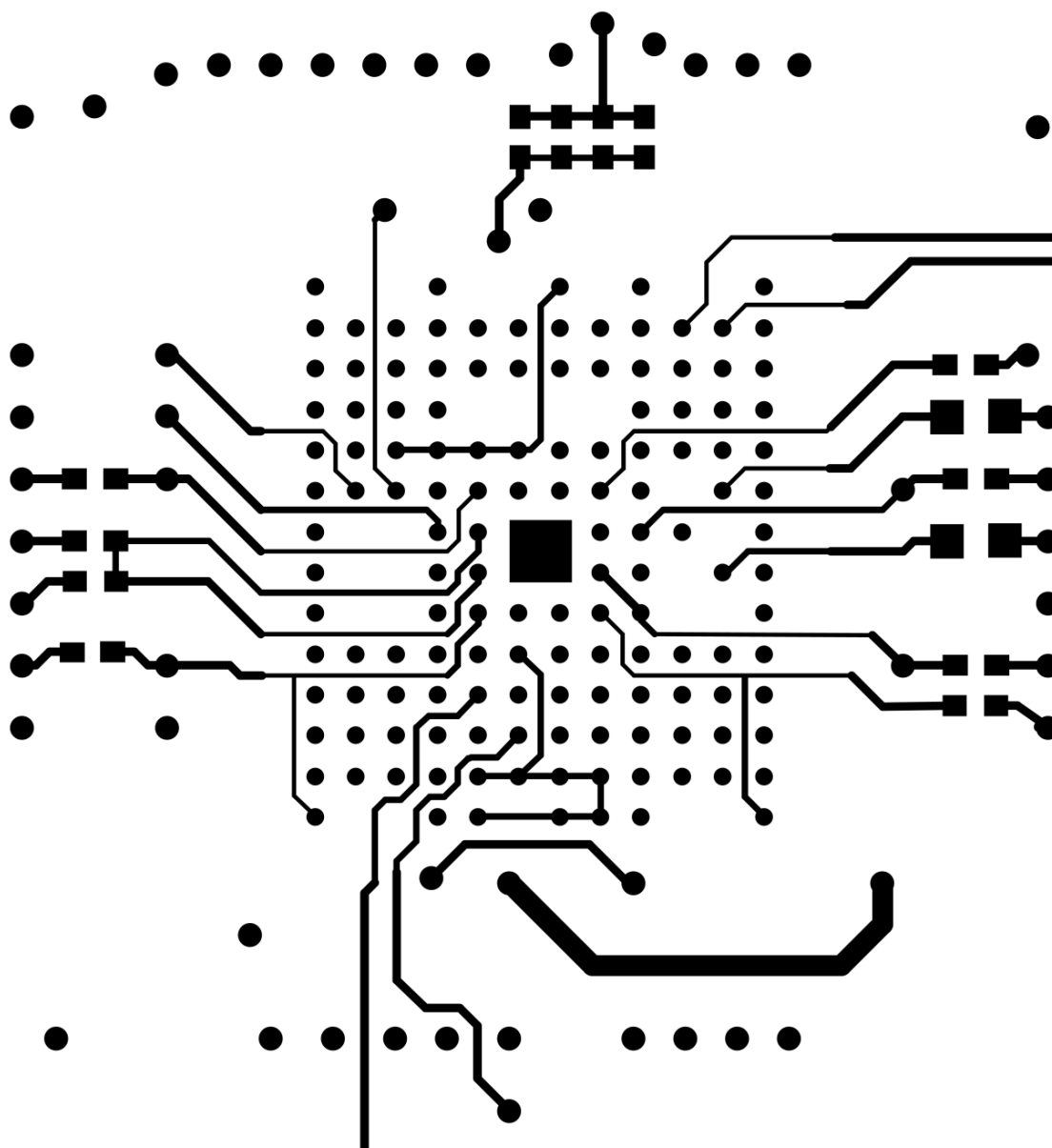
### 10.2.2 Standard Layout Example

Only through-hole vias are included in this layout. Bypass capacitors are placed as close to their respective device pads. Bottom bypass brought out from device. This layout can lead to increased trace length, which will increase the series inductance of the net making it more susceptible to noise and voltage spikes. [Figure 60](#) to [Figure 61](#) show the board layouts.



**Figure 60. DAC60096 Example Board Layout – Top Layer**

**Layout Examples (continued)**



**Figure 61. DAC60096 Example Board Layout – Bottom Layer**

## 11 器件和文档支持

### 11.1 文档支持

#### 11.1.1 相关文档

《LM231 数据表》， [SNOSBI2](#)

### 11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧导航栏。

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-------------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DAC60096IZEB</a> | Active        | Production           | NFBGA (ZEB)   196 | 126   JEDEC TRAY (10+1) | Yes         | SNAGCU                               | Level-3-260C-168 HR               | -40 to 85    | DAC60096            |
| DAC60096IZEB.B               | Active        | Production           | NFBGA (ZEB)   196 | 126   JEDEC TRAY (10+1) | -           | Call TI                              | Call TI                           | -40 to 85    |                     |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

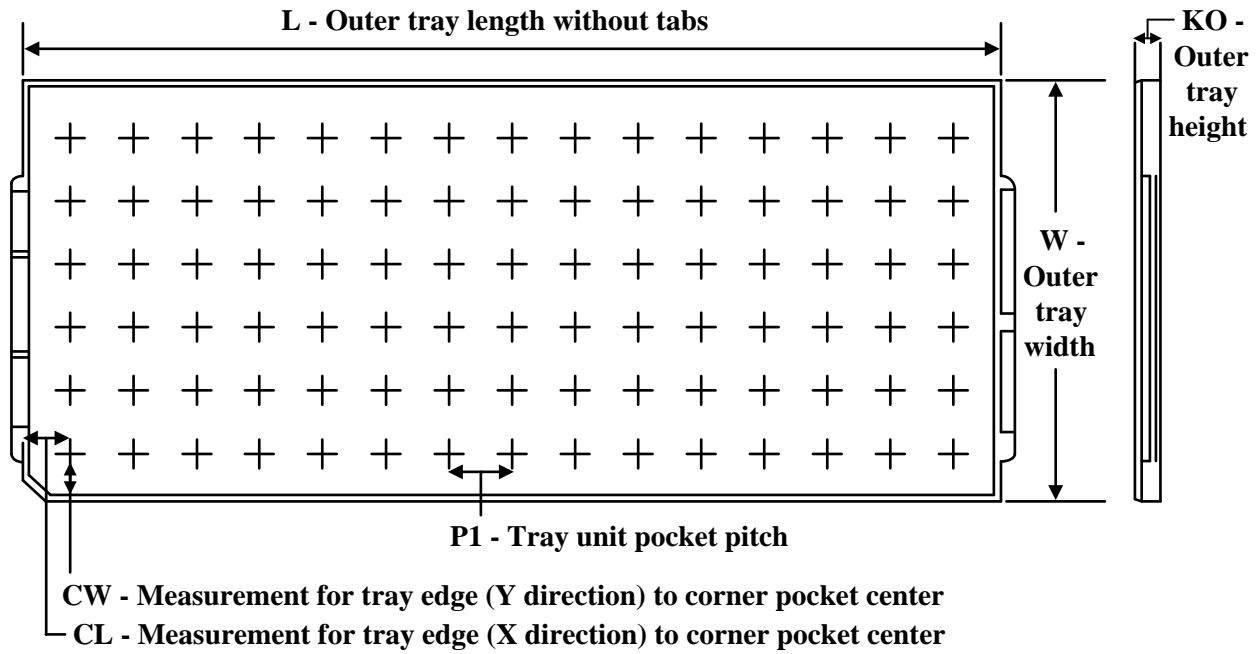
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TRAY

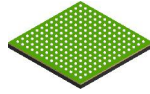


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| DAC60096IZEB | ZEB          | NFBGA        | 196  | 126 | 7 X 18            | 150                  | 315    | 135.9  | 7620    | 17.2    | 11.3    | 16.35   |

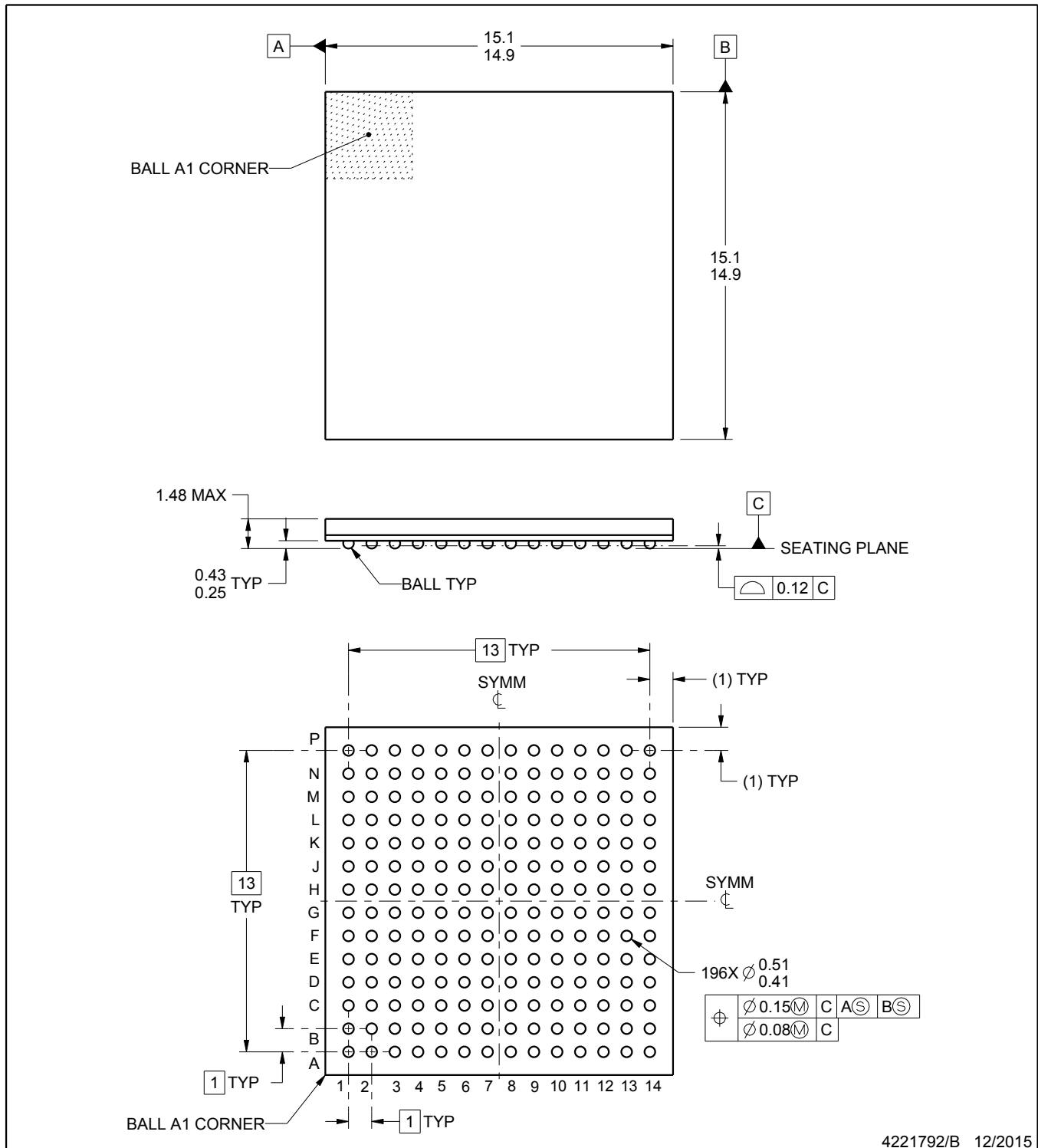
**ZEB0196A**



## PACKAGE OUTLINE

**NFBGA - 1.48 mm max height**

PLASTIC BALL GRID ARRAY



4221792/B 12/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

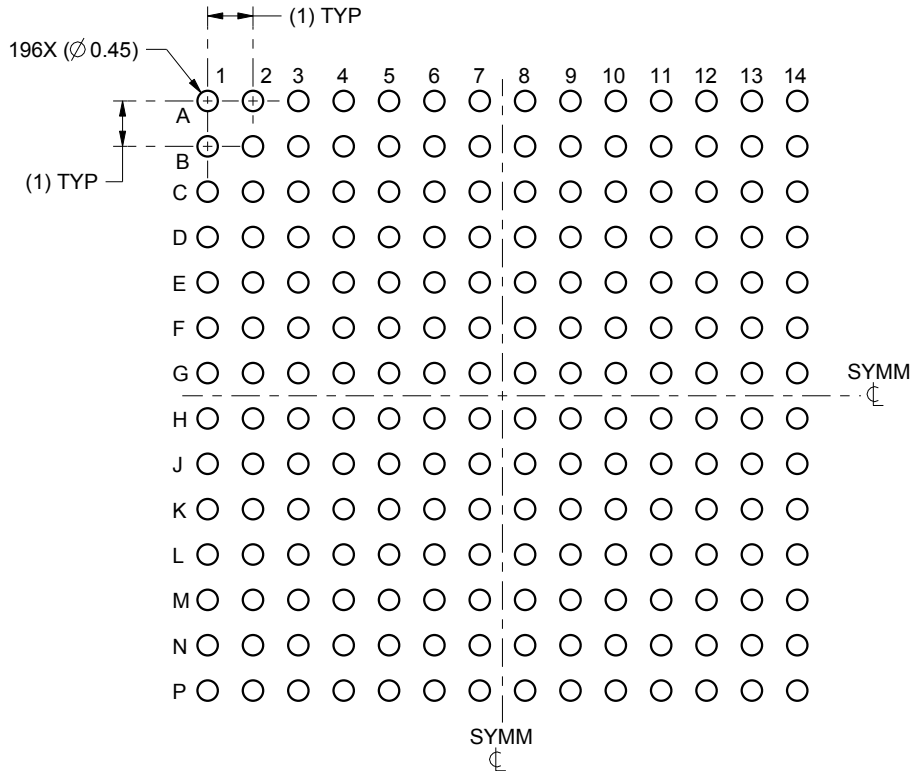


# EXAMPLE BOARD LAYOUT

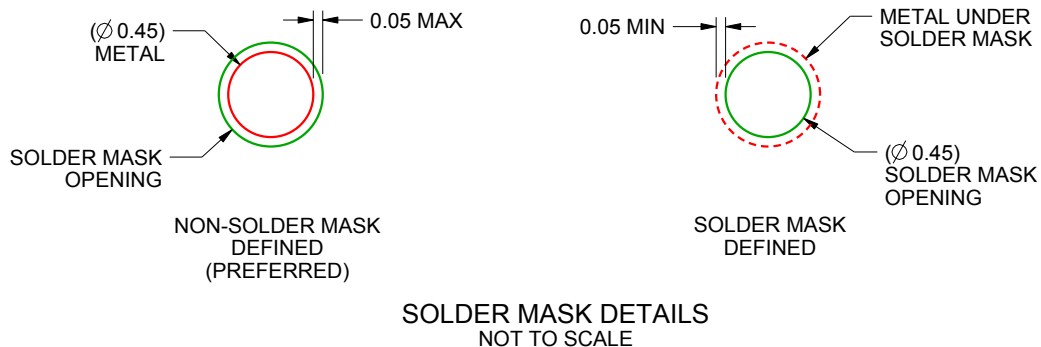
**ZEB0196A**

**NFBGA - 1.48 mm max height**

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:6X



4221792/B 12/2015

NOTES: (continued)

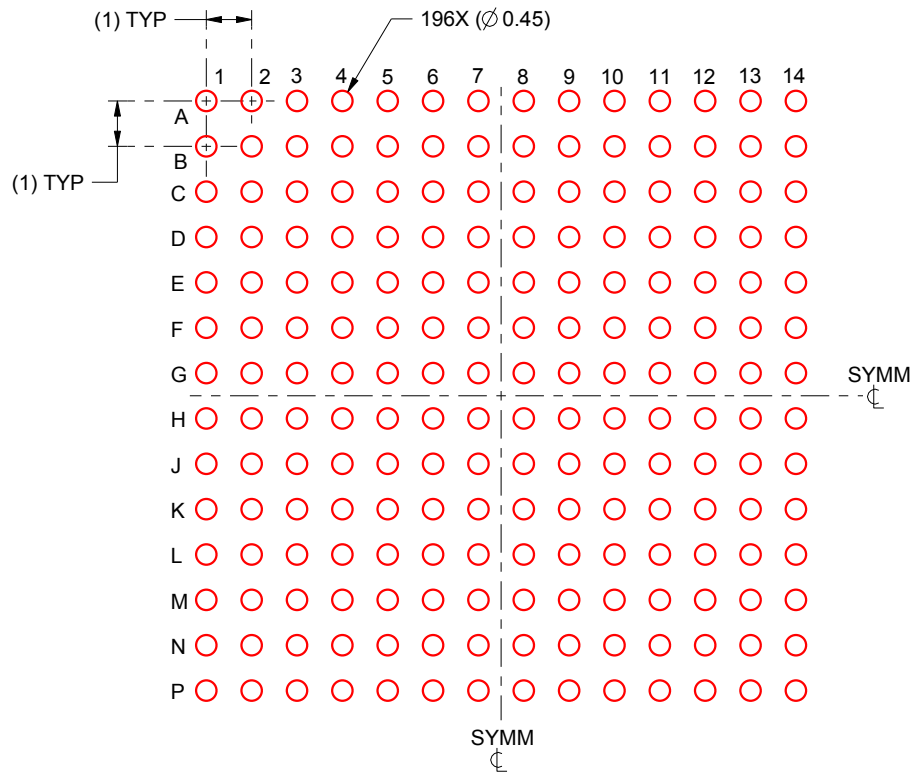
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

# EXAMPLE STENCIL DESIGN

ZEB0196A

NFBGA - 1.48 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:6X

4221792/B 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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