

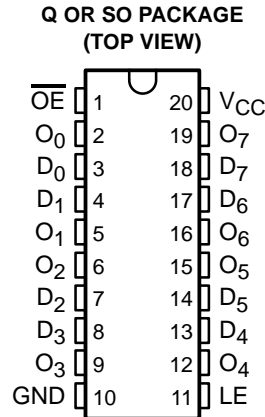
CY74FCT2373T

8-BIT LATCH

WITH 3-STATE OUTPUTS

SCCS039B – SEPTEMBER 1994 – REVISED OCTOBER 2001

- Function and Pinout Compatible With the Fastest Bipolar Logic
- 25-Ω Output Series Resistors Reduce Transmission-Line Reflection Noise
- Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- 3-State Outputs
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- 12-mA Output Sink Current
15-mA Output Source Current



description

The CY74FCT2373T is an 8-bit, high-speed CMOS, TTL-compatible buffered latch with 3-state outputs that is ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25-Ω termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2373T can replace the CY74FCT373T to reduce noise in an existing design.

When the latch-enable (LE) input is high, the flip-flops appear transparent to the data. Data that meets the required setup times are latched when LE transitions from high to low. Data appears on the bus when the output-enable (\overline{OE}) input is low. When \overline{OE} is high, the bus output is in the high-impedance state. In this mode, data can be entered into the latches.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

| TA | PACKAGE† | | SPEED (ns) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-----------|---------------|------------|-----------------------|------------------|
| –40°C to 85°C | QSOP – Q | Tape and reel | 4.7 | CY74FCT2373CTQCT | FCT2373C |
| | SOIC – SO | Tube | 4.7 | CY74FCT2373CTSOC | FCT2373C |
| | | Tape and reel | 4.7 | CY74FCT2373CTSOCT | |
| | QSOP – Q | Tape and reel | 5.2 | CY74FCT2373ATQCT | FCT2373A |
| | QSOP – Q | Tape and reel | 8 | CY74FCT2373TQCT | FCT2373 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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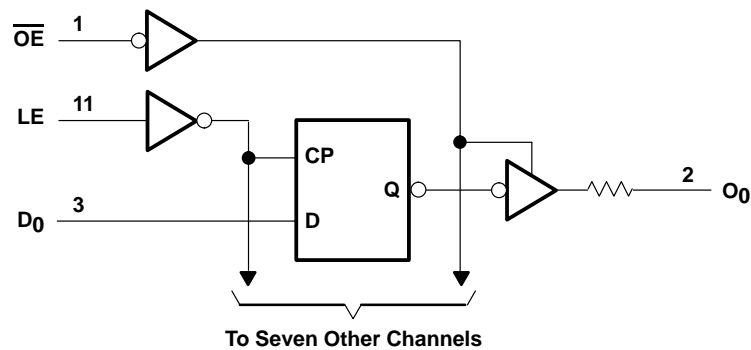
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FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-----------------|----|---|--------|
| \overline{OE} | LE | D | O |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance
state, Q_0 = Previous state of flip flops
(Q_0-1)

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|----------------|
| Supply voltage range to ground potential | −0.5 V to 7 V |
| DC input voltage range | −0.5 V to 7 V |
| DC output voltage range | −0.5 V to 7 V |
| DC output current (maximum sink current/pin) | 120 mA |
| Package thermal impedance, θ_{JA} (see Note 1): Q package | 68°C/W |
| SO package | 58°C/W |
| Ambient temperature range with power applied, T_A | −65°C to 135°C |
| Storage temperature range, T_{stg} | −65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

| | MIN | NOM | MAX | UNIT |
|--------------------------------------|------|-----|------|------|
| V_{CC} Supply voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.8 | V |
| I_{OH} High-level output current | | | −15 | mA |
| I_{OL} Low-level output current | | | 12 | mA |
| T_A Operating free-air temperature | −40 | | 85 | °C |

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------|---|--|--|------|------|--------|
| V _{IK} | V _{CC} = 4.75 V, | I _{IN} = −18 mA | | −0.7 | −1.2 | V |
| V _{OH} | V _{CC} = 4.75 V, | I _{OH} = −15 mA | 2.4 | 3.3 | | V |
| V _{OL} | V _{CC} = 4.75 V, | I _{OL} = 12 mA | | 0.3 | 0.55 | V |
| R _{OUT} | V _{CC} = 4.75 V, | I _{OL} = 12 mA | 20 | 28 | 40 | Ω |
| V _{hys} | All inputs | | | 0.2 | | V |
| I _I | V _{CC} = 5.25 V, | V _{IN} = V _{CC} | | | 5 | μA |
| I _{IH} | V _{CC} = 5.25 V, | V _{IN} = 2.7 V | | | ±1 | μA |
| I _{IL} | V _{CC} = 5.25 V, | V _{IN} = 0.5 V | | | ±1 | μA |
| I _{OZH} | V _{CC} = 5.25 V, | V _{OUT} = 2.7 V | | | 10 | μA |
| I _{OZL} | V _{CC} = 5.25 V, | V _{OUT} = 0.5 V | | | −10 | μA |
| I _{OS} ‡ | V _{CC} = 5.25 V, | V _{OUT} = 0 V | −60 | −120 | −225 | mA |
| I _{off} | V _{CC} = 0 V, | V _{OUT} = 4.5 V | | | ±1 | μA |
| I _{CC} | V _{CC} = 5.25 V, | V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} − 0.2 V | | 0.1 | 0.2 | mA |
| ΔI _{CC} | V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open | | | 0.5 | 2 | mA |
| I _{CCD} ¶ | V _{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, OE = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V | | | 0.06 | 0.12 | mA/MHz |
| I _C # | V _{CC} = 5.25 V, Outputs open, OE = GND, LE = V _{CC} | One input switching at f ₁ = 10 MHz at 50% duty cycle | V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V | 0.7 | 1.4 | mA |
| | | | V _{IN} = 3.4 V or GND | 1 | 2.4 | |
| | | Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle | V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V | 1.3 | 2.6 | |
| | | | V _{IN} = 3.4 V or GND | 3.3 | 10.6 | |
| C _i | | | | 6 | 10 | pF |
| C _o | | | | 8 | 12 | pF |

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4\text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD}(f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | | CY74FCT2373T | | CY74FCT2373AT | | CY74FCT2373CT | | UNIT |
|-----------------|-------------------------|-------------|--------------|-----|---------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | | 6 | | 5 | | 5 | | ns |
| t _{su} | Setup time, D to LE | High to low | 2 | | 2 | | 2 | | ns |
| t _h | Hold time, D to LE | High to low | 1.5 | | 1.5 | | 1.5 | | ns |

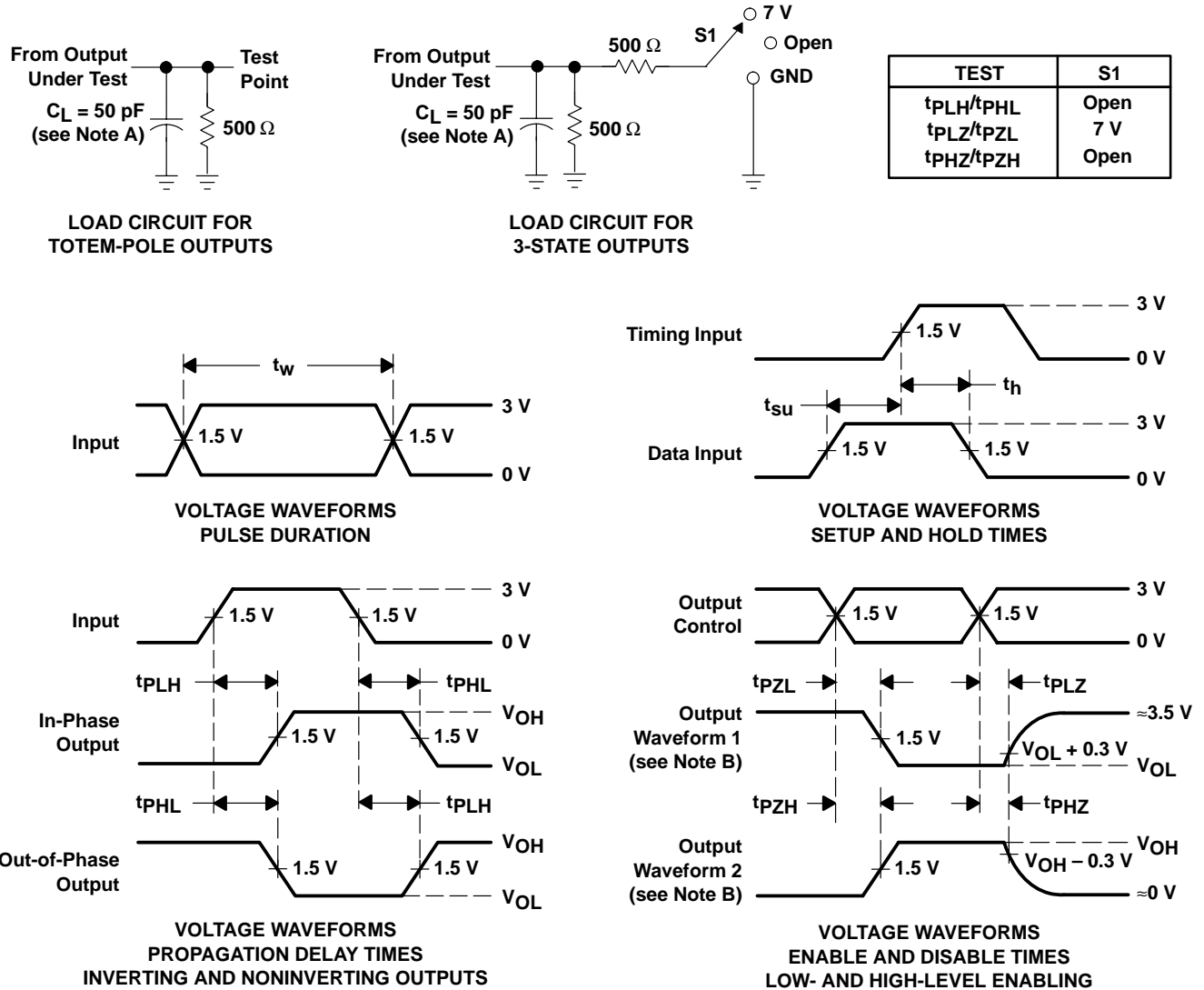
switching characteristics over operating free-air temperature range (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY74FCT2373T | | CY74FCT2373AT | | CY74FCT2373CT | | UNIT |
|------------------|-----------------|----------------|--------------|-----|---------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | D | O | 1.5 | 8 | 1.5 | 5.2 | 1.5 | 4.7 | ns |
| t _{PHL} | | | 1.5 | 8 | 1.5 | 5.2 | 1.5 | 4.7 | |
| t _{PLH} | LE | O | 2 | 13 | 2 | 8.5 | 2 | 5.5 | ns |
| t _{PHL} | | | 2 | 13 | 2 | 8.5 | 2 | 5.5 | |
| t _{PZH} | \overline{OE} | O | 1.5 | 11 | 1.5 | 6.5 | 1.5 | 5.5 | ns |
| t _{PZL} | | | 1.5 | 11 | 1.5 | 6.5 | 1.5 | 5.5 | |
| t _{PHZ} | \overline{OE} | O | 1.5 | 7 | 1.5 | 5.5 | 1.5 | 5 | ns |
| t _{PLZ} | | | 1.5 | 7 | 1.5 | 5.5 | 1.5 | 5 | |



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CY74FCT2373CTSOC | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2373C |
| CY74FCT2373CTSOC.B | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2373C |
| CY74FCT2573ATQCT | Active | Production | SSOP (DBQ) 20 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2573A |
| CY74FCT2573ATQCT.B | Active | Production | SSOP (DBQ) 20 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2573A |
| CY74FCT2573CTQCT | Active | Production | SSOP (DBQ) 20 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2573C |
| CY74FCT2573CTQCT.B | Active | Production | SSOP (DBQ) 20 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2573C |
| CY74FCT2573CTSOC | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2573C |
| CY74FCT2573CTSOC.B | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2573C |
| CY74FCT2573CTSOCT | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2573C |
| CY74FCT2573CTSOCT.B | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2573C |
| CY74FCT2573TSOC | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2573 |
| CY74FCT2573TSOC.B | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2573 |
| CY74FCT2573TSOCT | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2573 |
| CY74FCT2573TSOCT.B | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2573 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CY74FCT2573ATQCT | SSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT2573CTQCT | SSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT2573CTSOCT | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CY74FCT2573TSOCT | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CY74FCT2573ATQCT | SSOP | DBQ | 20 | 2500 | 353.0 | 353.0 | 32.0 |
| CY74FCT2573CTQCT | SSOP | DBQ | 20 | 2500 | 353.0 | 353.0 | 32.0 |
| CY74FCT2573CTSOCT | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| CY74FCT2573TSOCT | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |

TUBE

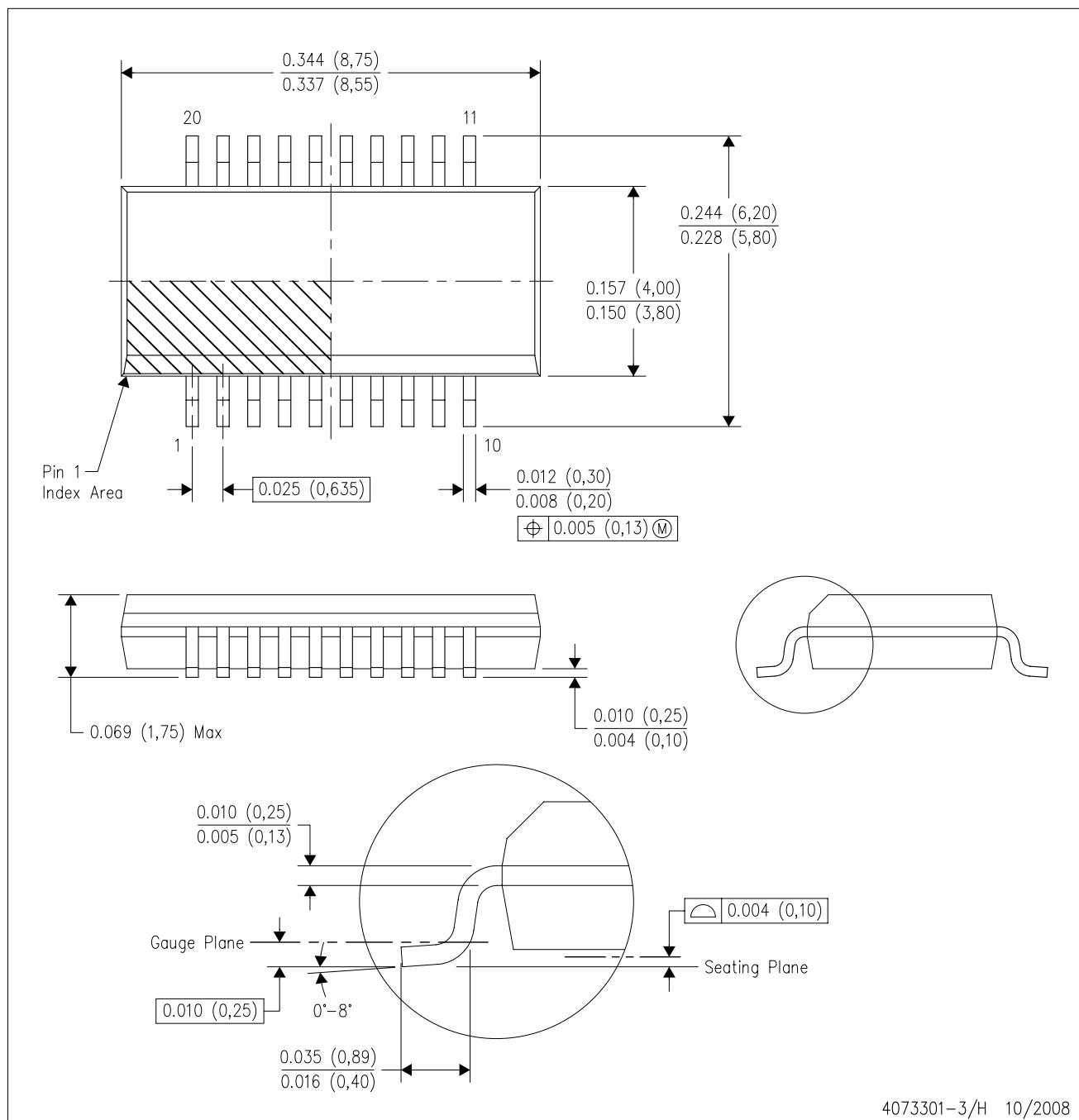


*All dimensions are nominal

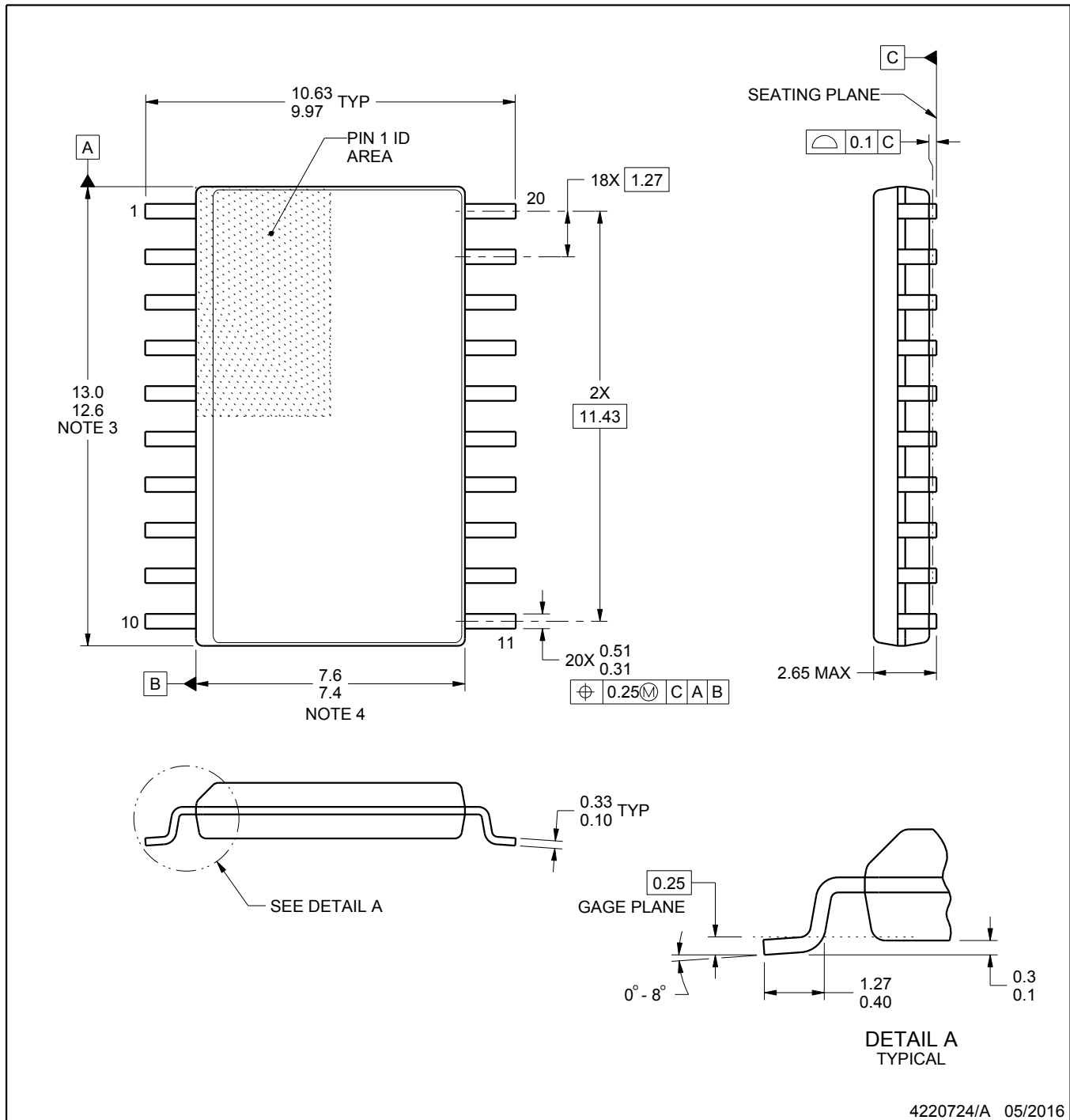
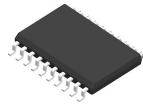
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CY74FCT2373CTSOC | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CY74FCT2373CTSOC.B | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CY74FCT2573CTSOC | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CY74FCT2573CTSOC.B | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CY74FCT2573TSOC | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CY74FCT2573TSOC.B | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO-137 variation AD.



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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