

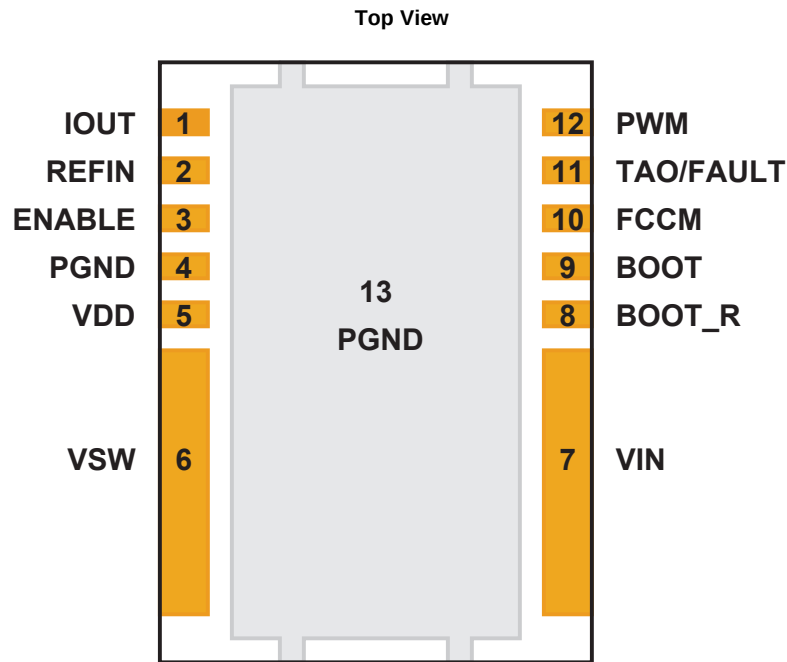
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4 修订历史记录

日期	修订版本	注释
2 月 2016	*	最初发布。

5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NUMBER	NAME	
1	IOUT	Output of current sensing amplifier. $V(IOUT) - V(REFIN)$ is proportional to the phase current.
2	REFIN	External reference voltage input for current sensing amplifier.
3	ENABLE	Enables device operation. If ENABLE = logic HIGH, turns on device. If ENABLE = logic LOW, the device is turned off and both MOSFET gates are actively pulled low. An internal 100 k Ω pulldown resistor will pull the ENABLE pin LOW if left floating.
4	P _{GND}	Power ground, connected directly to pin 13.
5	V _{DD}	Supply voltage to gate driver and internal circuitry.
6	V _{SW}	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.
7	V _{IN}	Input voltage pin. Connect input capacitors close to this pin.
8	BOOT_R	Return path for HS gate driver, connected to V _{SW} internally.
9	BOOT	Bootstrap capacitor connection. Connect a minimum of 0.1 μ F 16 V X7R ceramic capacitor from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
10	FCCM	This pin enables the diode emulation function. When this pin is held LOW, diode emulation mode is enabled for sync FET. When FCCM is HIGH, the device is operated in forced continuous conduction mode. An internal 5 μ A current source will pull the FCCM pin to 3.3 V if left floating.
11	TAO/ FAULT	Temperature Analog Output. Reports a voltage proportional to the die temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown occurs. TAO should be bypassed to P _{GND} with a 1 nF 16 V X7R ceramic capacitor.
12	PWM	Pulse width modulated tri-state input from external controller. Logic LOW sets control FET gate low and sync FET gate high. Logic HIGH sets control FET gate high and sync FET gate low. Open or High Z sets both MOSFET gates low if greater than the tri-state shutdown hold-off time (t_{3HT}).
13	P _{GND}	Power ground.

6 Specifications

6.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
V_{IN} to P_{GND}	–0.3	20	V
V_{IN} to V_{SW}	–0.3	20	V
V_{IN} to V_{SW} (10 ns)		23	V
V_{SW} to P_{GND}	–0.3	20	V
V_{SW} to P_{GND} (10 ns)	–7	23	V
V_{DD} to P_{GND}	–0.3	7	V
ENABLE, PWM, FCCM, TAO, IOUT, REFIN to P_{GND} ⁽²⁾	–0.3	$V_{DD} + 0.3\text{ V}$	V
BOOT to BOOT_R ⁽²⁾	–0.3	$V_{DD} + 0.3\text{ V}$	V
P_D Power dissipation		12	W
T_J Operating junction	–55	150	$^\circ\text{C}$
T_{stg} Storage temperature	–55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Should not exceed 7 V.

6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM) Charged device model (CDM)	± 2000 ± 500
		V

6.3 Recommended Operating Conditions

 $T_A = 25^\circ$ (unless otherwise noted)

	MIN	MAX	UNIT
V_{DD} Gate drive voltage	4.5	5.5	V
V_{IN} Input supply voltage ⁽¹⁾		16	V
V_{OUT} Output voltage		5.5	V
I_{OUT} Continuous output current	$V_{IN} = 12\text{ V}$, $V_{DD} = 5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $f_{SW} = 500\text{ kHz}$, $L_{OUT} = 0.225\text{ }\mu\text{H}$ ⁽²⁾		60
I_{OUT-PK} Peak output current ⁽³⁾			90
f_{SW} Switching frequency	$C_{BST} = 0.1\text{ }\mu\text{F}$ (min)	1250	kHz
On time duty cycle	$f_{SW} = 1\text{ MHz}$	85%	
Minimum PWM on time	40		ns
Operating temperature	–40	125	$^\circ\text{C}$

- (1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
- (2) Measurement made with six 10 μF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
- (3) System conditions as defined in Note 1. Peak Output Current is applied for $t_p = 50\text{ }\mu\text{s}$.

6.4 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

THERMAL METRIC	MIN	TYP	MAX	UNIT
$R_{\theta JC(top)}$ Junction-to-case (top of package) thermal resistance ⁽¹⁾			5	$^\circ\text{C/W}$
$R_{\theta JB}$ Junction-to-board thermal resistance ⁽²⁾			1.5	

- (1) $R_{\theta JC(top)}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2-oz (0.071 mm thick) Cu pad on a 1.5 inches x 1.5 inches, 0.06-inch (1.52-mm) thick FR4 board.
- (2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

8 器件和文档支持

8.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.2 商标

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8.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.4 Glossary

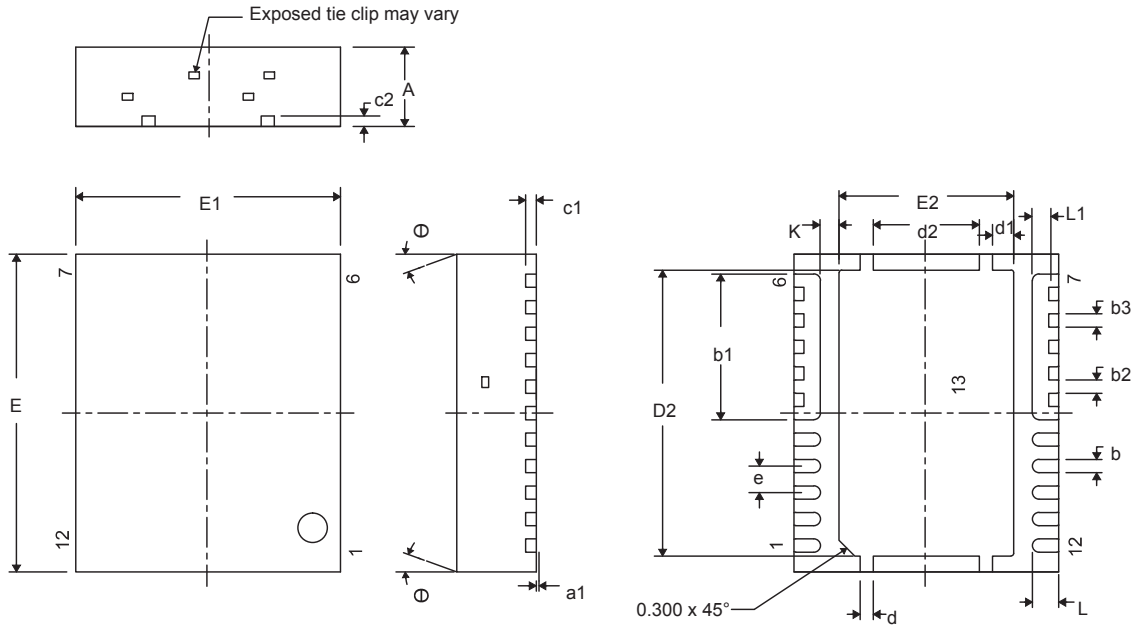
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

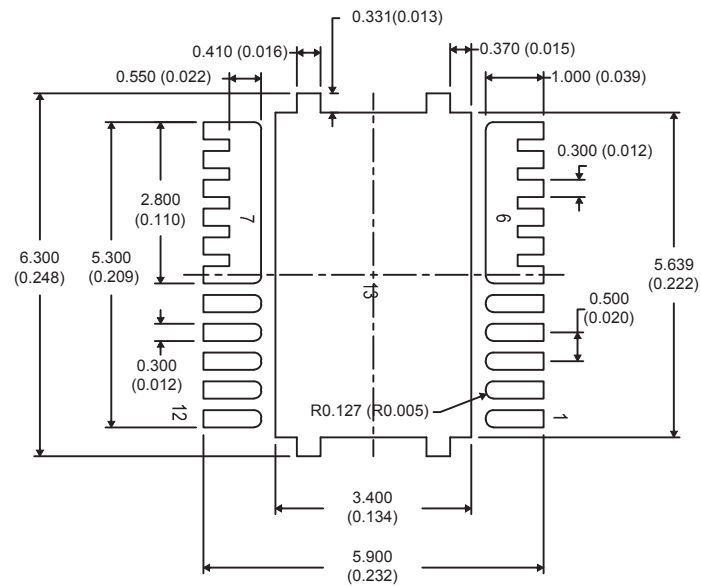
以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

9.1 机械制图



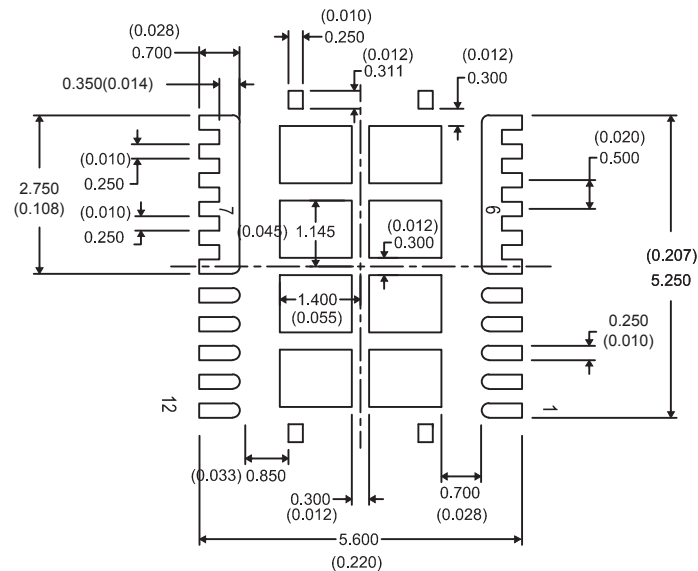
DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.950	1.000	1.050	0.037	0.039	0.041
a1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.320	0.008	0.010	0.013
b1	2.750 典型值			0.108 典型值		
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3	0.250 典型值			0.010 典型值		
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.200	0.250	0.300	0.008	0.010	0.012
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e	0.500 典型值			0.020 典型值		
K	0.350 典型值			0.014 典型值		
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

9.2 建议印刷电路板 (PCB) 焊盘图案



1. 尺寸单位为 mm（英寸）。

9.3 建议模板开口



1. 尺寸单位为 mm（英寸）。
2. 模板厚度为 100μm。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD95472Q5MC	Active	Production	VSON-CLIP (DMC) 12	2500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95472MC
CSD95472Q5MC.A	Active	Production	VSON-CLIP (DMC) 12	2500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95472MC
CSD95472Q5MC.B	Active	Production	VSON-CLIP (DMC) 12	2500 LARGE T&R	-	Call TI	Call TI	-55 to 150	
CSD95472Q5MCT	Active	Production	VSON-CLIP (DMC) 12	250 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95472MC
CSD95472Q5MCT.A	Active	Production	VSON-CLIP (DMC) 12	250 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95472MC
CSD95472Q5MCT.B	Active	Production	VSON-CLIP (DMC) 12	250 SMALL T&R	-	Call TI	Call TI	-55 to 150	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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