CSD87350Q5D 同步降压 NexFET™电源块

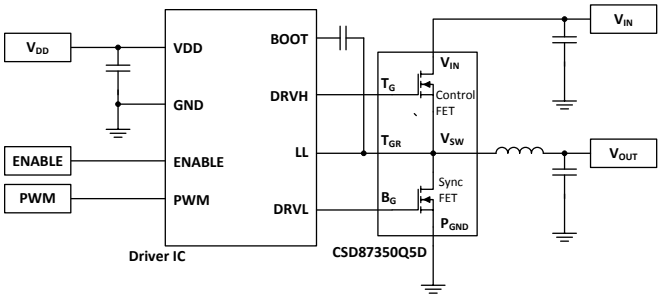
1 特性

- 半桥电源块
- 25A 电流下系统效率达 90%
- 工作电流高达 40A
- 高频工作（高达 1.5MHz）
- 高密度 SON 5mm × 6mm 封装
- 针对 5V 栅极驱动进行了优化
- 开关损耗较低
- 超低电感封装
- 符合 RoHS 标准
- 无卤素
- 无铅引脚镀层

2 应用范围

- 同步降压转换器
  - 高频 应用
  - 高电流、低占空比 应用
- 多相位同步降压转换器
- 负载点直流 - 直流转换器
- IMVP、VRM 和 VRD 应用

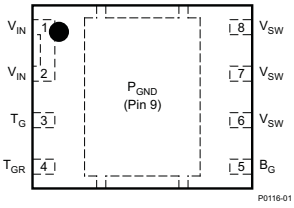
典型电路



3 说明

CSD87350Q5D NexFET™电源块是面向同步降压 应用 的优化设计方案，能够以 5mm × 6mm 的小巧外形提供高电流、高效率以及高频率性能。该产品针对 5V 栅极驱动 应用进行了优化，可提供一套灵活的解决方案，在与来自外部控制器或驱动器的任一 5V 栅极驱动配套使用时，均可提供高密度电源。

俯视图

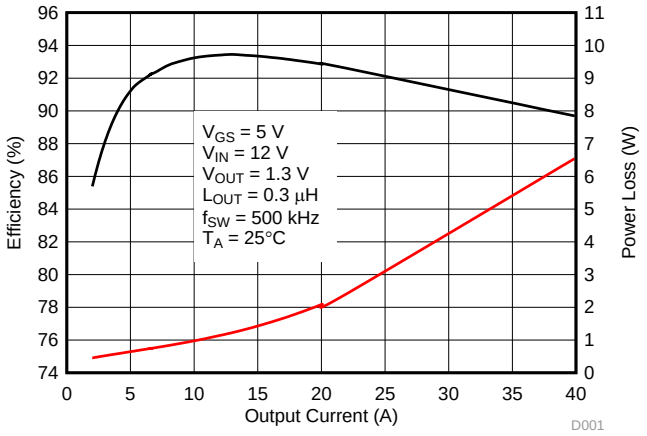


器件信息(1)

器件	包装介质	数量	封装	运输
CSD87350Q5D	13 英寸卷带	2500	小外形尺寸无引线 (SON) 5mm × 6mm 塑料封装	卷带封装

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型电源块效率与功率损耗



目录

4 修订历史记录

Changes from Revision D (September 2014) to Revision E — **Page**

- Added note for I_{DM} in the *Absolute Maximum Ratings* table ... 3
- 已添加 *接收文档更新通知*部分和*社区资源*部分（位于*器件和文档支持*部分 ... 17

Changes from Revision C (October 2011) to Revision D — **Page**

- 已添加*处理额定值表*、*应用和实施*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和订购信息*部分。 ... 1

Changes from Revision B (September 2011) to Revision C — **Page**

- 将“DIM a”以毫米为单位的最大值由 1.55 更改为 1.5，将以英寸为单位的最大值由 0.061 更改为 0.059 ... 18

Changes from Revision A (August 2011) to Revision B — **Page**

- Replaced $R_{DS(on)}$ with $Z_{DS(on)}$ ... 4
- Added Equivalent System Performance section ... 10
- Added the Comparison of $R_{DS(on)}$ vs $Z_{DS(on)}$ table ... 12
- Added Electrical Performance bullet ... 15

Changes from Original (March 2011) to Revision A — **Page**

- Changed Power Dissipation, P_D in the Absolute Maximum Ratings table From; 13 W to 12 W ... 3

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Voltage	V_{IN} to P_{GND}	–0.8	30	V
		T_G to T_{GR}	–8	10	V
		B_G to P_{GND}	–8	10	V
I_{DM}	Pulsed current rating(2)			120	A
P_D	Power dissipation			12	W
E_{AS}	Avalanche energy	Sync FET, I_D = 105 A, L = 0.1 mH		551	mJ
		Control FET, I_D = 60 A, L = 0.1 mH		180	
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse duration ≤ 50 µs. Duty cycle ≤ 0.01%.

5.2 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

		MIN	MAX	UNIT
V_{GS}	Gate drive voltage	4.5	8	V
V_{IN}	Input supply voltage		27	V
f_{SW}	Switching frequency C_{BST} = 0.1 µF (min)	200	1500	kHz
	Operating current		40	A
T_J	Operating temperature		125	°C

5.3 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu)(1)(2)			102	°C/W
	Junction-to-ambient thermal resistance (max Cu)(1)(2)			50	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)(2)			20	°C/W
	Junction-to-case thermal resistance (P_{GND} pin)(2)			2	°C/W

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2) Cu.
(2) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

5.4 Power Block Performance

T_A = 25° (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power loss(1)	V_{IN} = 12 V V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 µH, T_J = 25°C		3		W
I_{QVIN}	V_{IN} quiescent current	T_G to T_{GR} = 0 V ,B_G to P_{GND} = 0 V		10		µA

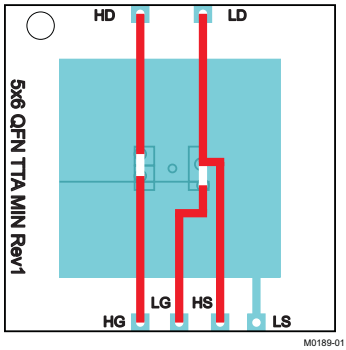
(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high-current 5-V driver IC.

5.5 Electrical Characteristics

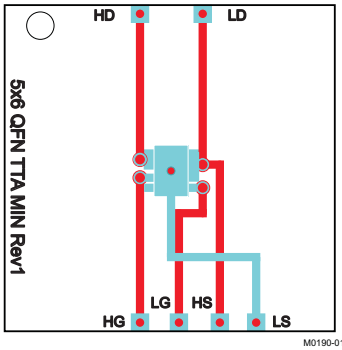
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8			100			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1		2.1	0.75		1.4	V
$Z_{DS(on)}$ (1)	Effective AC on-impedance	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 20 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 µH		5			1.2		mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 20 A		97			157		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		1360	1770		2950	3835	pF
C_{OSS}	Output capacitance			565	735		1300	1690	pF
C_{RSS}	Reverse transfer capacitance			19	25		50	65	pF
R_G	Series gate resistance			1.3	3		0.8	2	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 20 A		8.4	10.9		20	26	nC
Q_{gd}	Gate charge gate-to-drain			1.6			3.6		nC
Q_{gs}	Gate charge gate-to-source			2.6			4.3		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.6			2.3		nC
Q_{OSS}	Output charge	V_{DS} = 17 V, V_{GS} = 0 V		9.7			28		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 20 A, R_G = 2 Ω		7			8		ns
t_r	Rise time			17			10		ns
$t_{d(off)}$	Turnoff delay time			13			33		ns
t_f	Fall time			2.3			4.7		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	I_{DS} = 20 A, V_{GS} = 0 V		0.85	1		0.77	1	V
Q_{rr}	Reverse recovery charge	V_{dd} = 17 V, I_F = 20 A, di/dt = 300 A/µs		12.5			32		nC
t_{rr}	Reverse recovery time			22			28		ns

(1) Equivalent based on application testing. See *Equivalent System Performance* section for details.



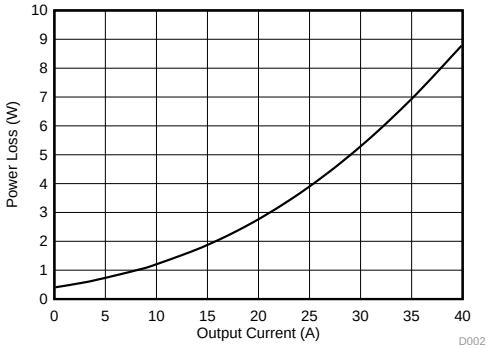
Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 102°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

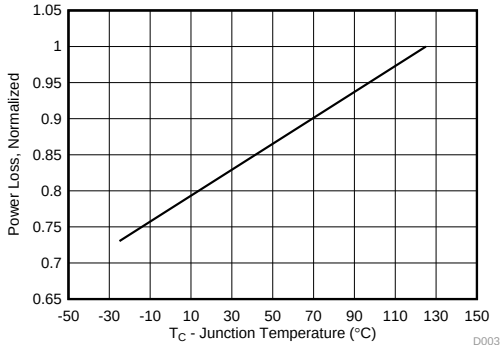
5.6 Typical Power Block Device Characteristics

T_J = 125°C, unless stated otherwise. The typical power block system characteristic curves Figure 3, Figure 4, and Figure 5 are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See *Application and Implementation* for detailed explanation.



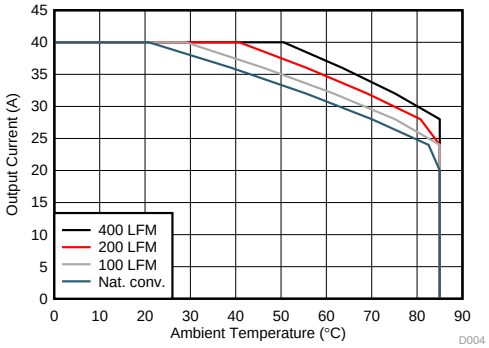
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.3 µH

Figure 1. Power Loss vs Output Current



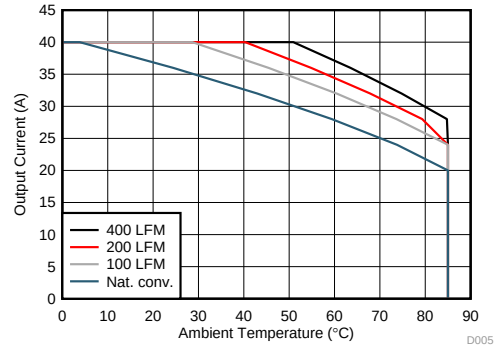
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.3 µH

Figure 2. Normalized Power Loss vs Temperature



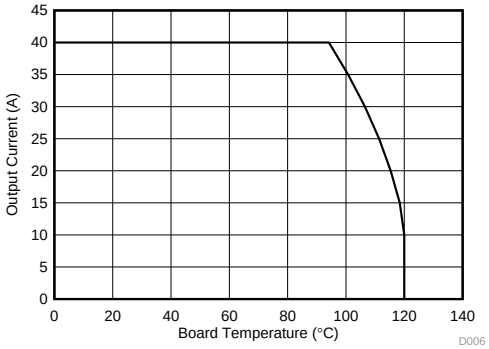
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.3 µH

Figure 3. Safe Operating Area (SOA) – PCB Vertical Mount



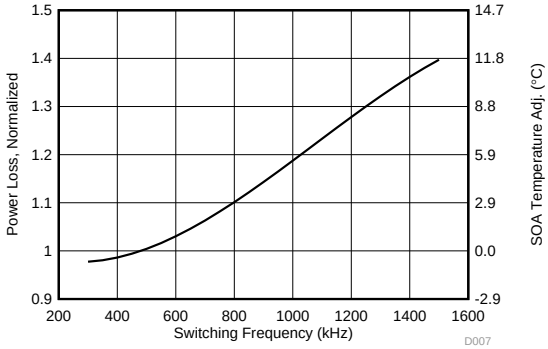
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.3 µH

Figure 4. Safe Operating Area (SOA) – PCB Horizontal Mount



V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.3 µH

Figure 5. Typical Safe Operating Area (SOA)

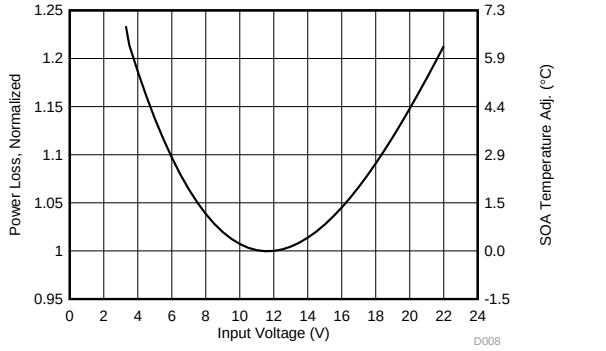


V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
L_{OUT} = 0.3 µH I_{OUT} = 40 A

Figure 6. Normalized Power Loss vs Switching Frequency

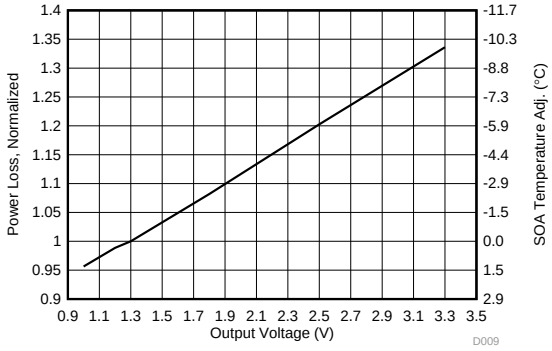
Typical Power Block Device Characteristics (continued)

T_J = 125°C, unless stated otherwise. The typical power block system characteristic curves Figure 3, Figure 4, and Figure 5 are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See *Application and Implementation* for detailed explanation.



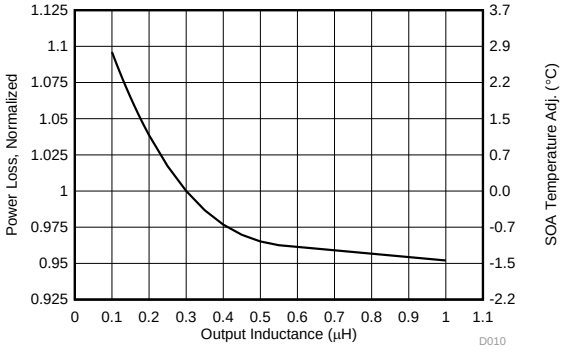
V_{IN} = 12 V V_{OUT} = 1.3 V L_{OUT} = 0.3 µH
f_{SW} = 500 kHz I_{OUT} = 40 A

Figure 7. Normalized Power Loss vs Input Voltage



V_{IN} = 12 V V_{GS} = 5 V f_{SW} = 500 kHz
L_{OUT} = 0.3 µH I_{OUT} = 40 A

Figure 8. Normalized Power Loss vs Output Voltage



V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz I_{OUT} = 40 A

Figure 9. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

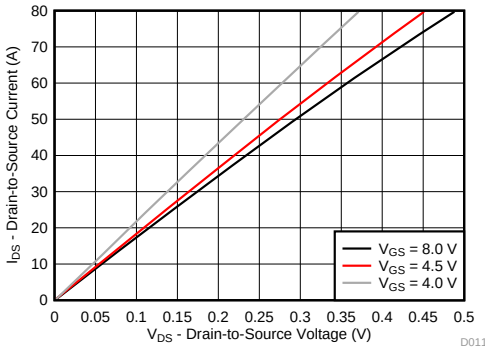


Figure 10. Control MOSFET Saturation

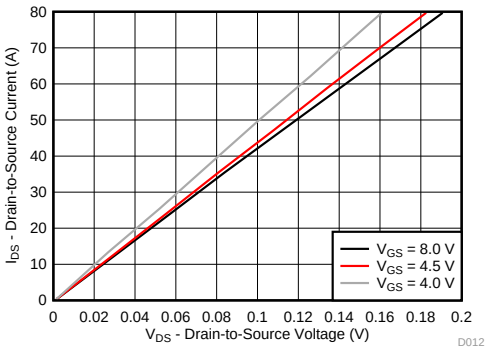


Figure 11. Sync MOSFET Saturation

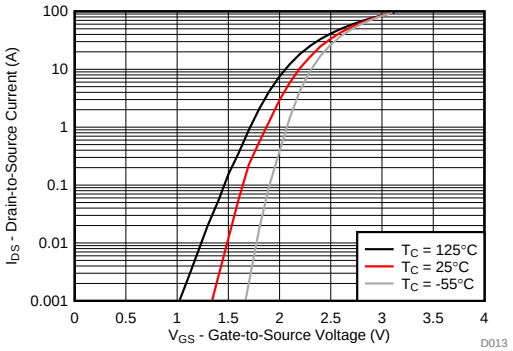


Figure 12. Control MOSFET Transfer

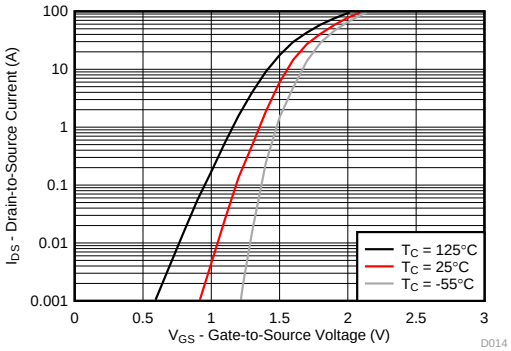


Figure 13. Sync MOSFET Transfer

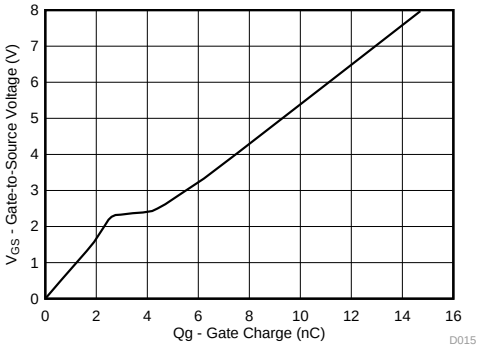


Figure 14. Control MOSFET Gate Charge

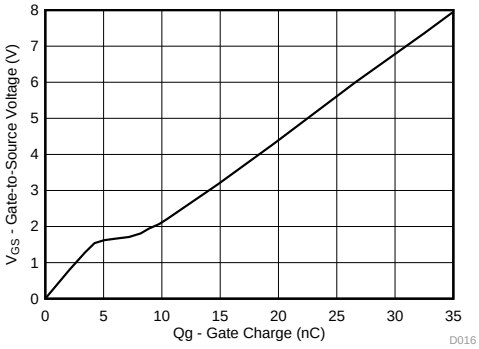
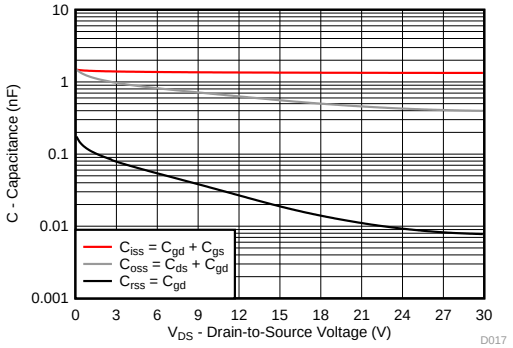


Figure 15. Sync MOSFET Gate Charge

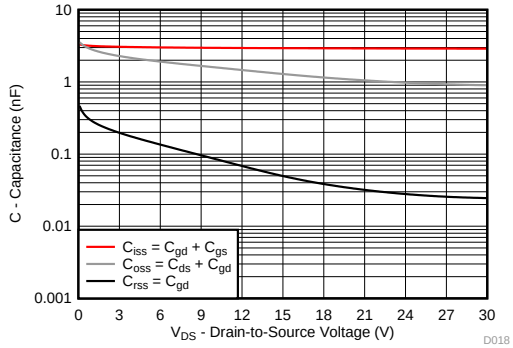
Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.



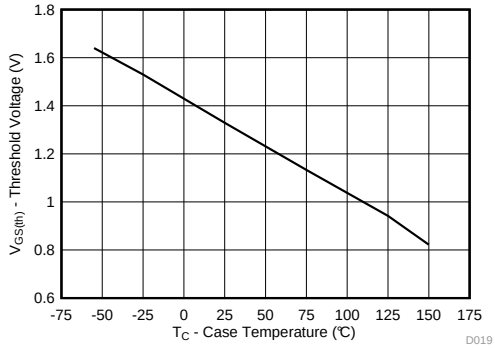
f = 1 MHz V_{GS} = 0

Figure 16. Control MOSFET Capacitance



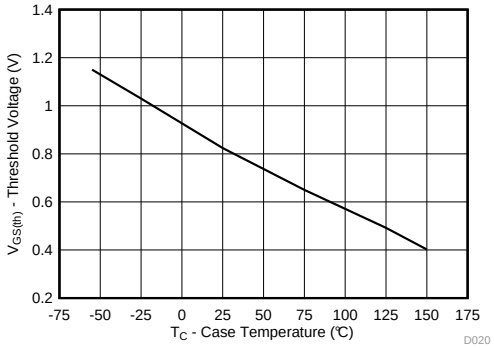
f = 1 MHz V_{GS} = 0

Figure 17. Sync MOSFET Capacitance



I_D = 250 µA

Figure 18. Control MOSFET $V_{GS(th)}$



I_D = 250 µA

Figure 19. Sync MOSFET $V_{GS(th)}$

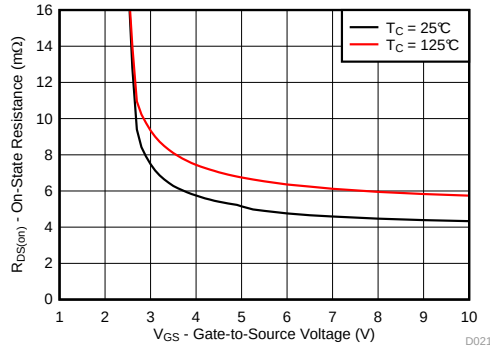


Figure 20. Control MOSFET $R_{DS(on)}$ vs V_{GS}

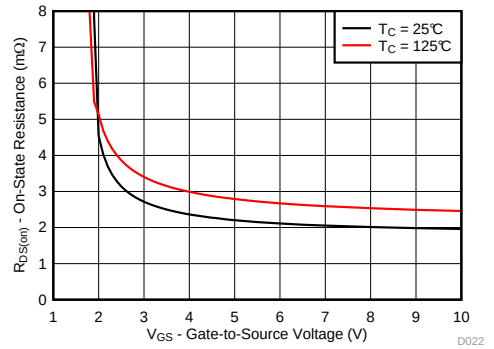


Figure 21. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

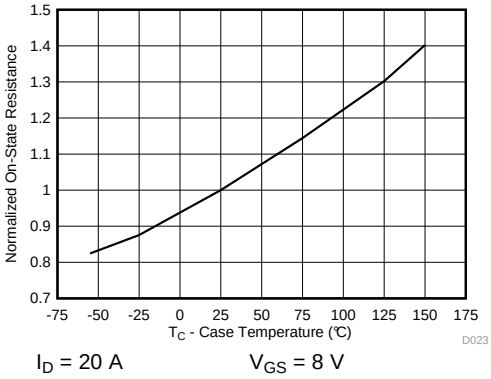


Figure 22. Control MOSFET Normalized $R_{DS(on)}$

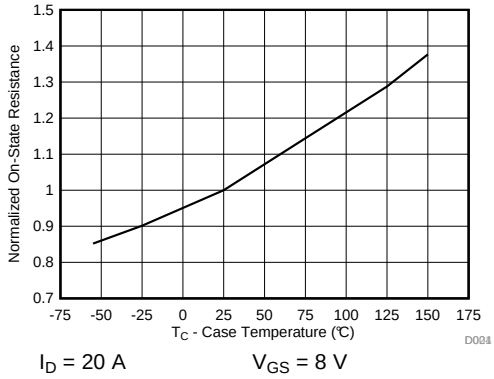


Figure 23. Sync MOSFET Normalized $R_{DS(on)}$

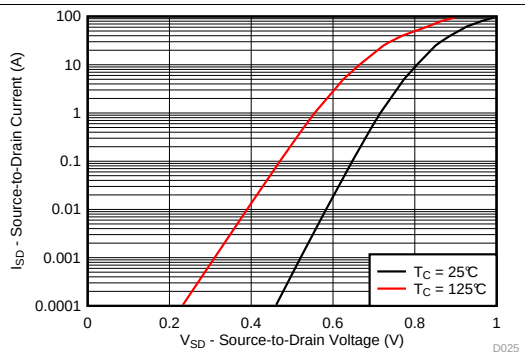


Figure 24. Control MOSFET Body Diode

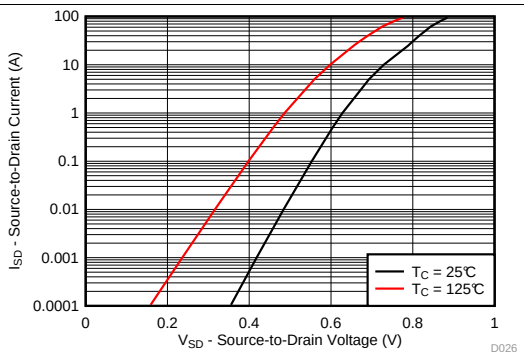


Figure 25. Sync MOSFET Body Diode

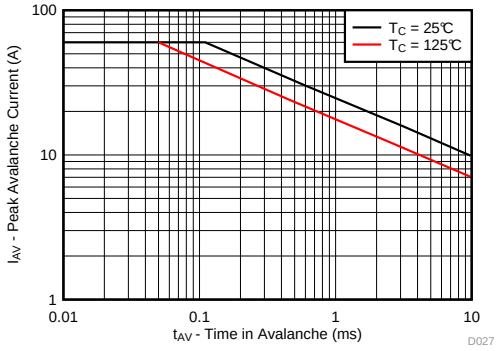


Figure 26. Control MOSFET Unclamped Inductive Switching

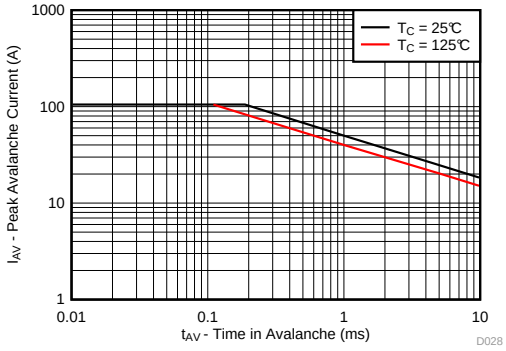


Figure 27. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87350Q5D NexFET power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area (SOA), and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.1 Equivalent System Performance

Many of today's high-performance computing systems require low-power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's synchronous buck topology. In particular, there has been an emphasis in improving the performance of the critical power semiconductor in the power stage of this application (see Figure 28). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

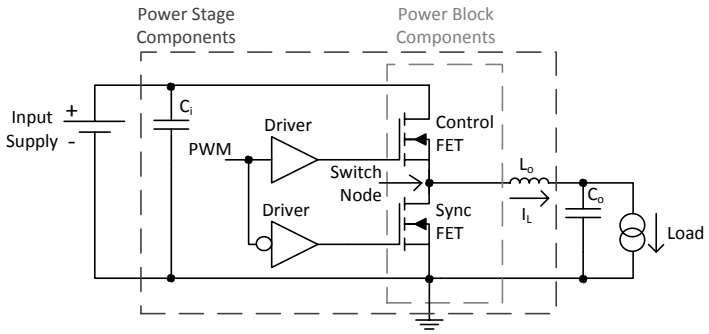


Figure 28. Equivalent System Schematic

The CSD87350Q5D is part of TI's power block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD}, Q_{GS}, and Q_{RR}. Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the control FET and sync FET connections (see Figure 29). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in *Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters* (SLPA009).

Application Information (continued)

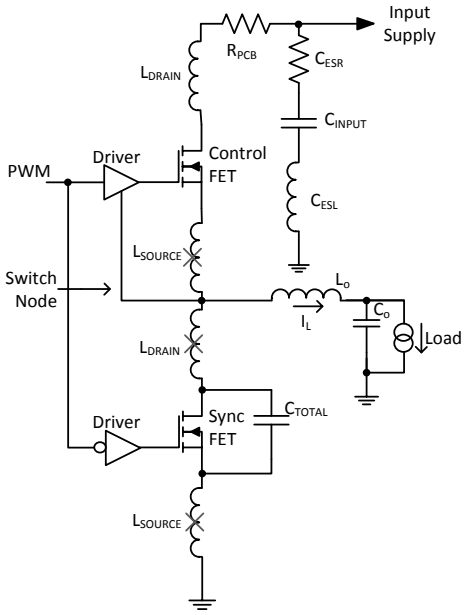


Figure 29. Elimination of Parasitic Inductances

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. Figure 30 and Figure 31 compare the efficiency and power loss performance of the CSD87350Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD87350Q5D clearly highlights the importance of considering the Effective AC On-Impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's power block technology.

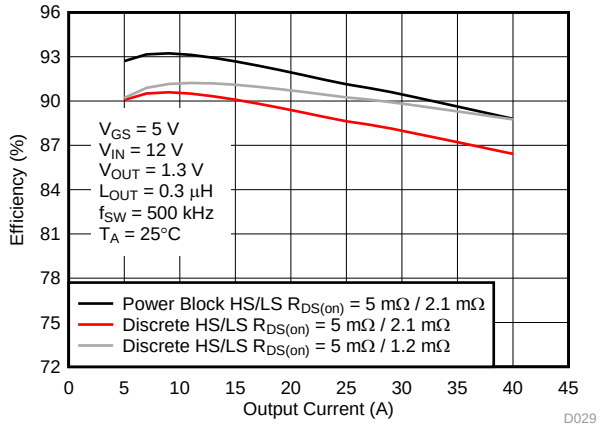


Figure 30. Efficiency

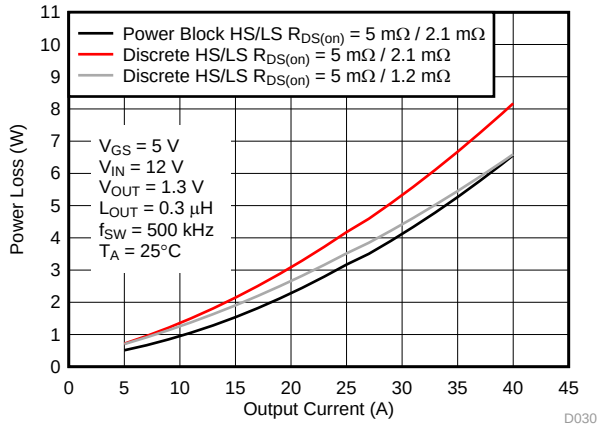


Figure 31. Power Loss

Application Information (continued)

Table 1 compares the traditional DC measured $R_{DS(ON)}$ of CSD87350Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's power block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD87350Q5D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid- to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

Table 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$

PARAMETER	HS		LS		UNIT
	TYP	MAX	TYP	MAX	
Effective AC on-impedance $Z_{DS(ON)}$ (V_{GS} = 5 V)	5	–	1.2	–	mΩ
DC measured $R_{DS(ON)}$ (V_{GS} = 4.5 V)	5	6.8	2.1	2.8	

6.1.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87350Q5D as a function of load current. This curve is measured by configuring and running the CSD87350Q5D as it would be in the final application (see Figure 32).The measured power loss is the CSD87350Q5D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{power loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.3 Safe Operating Area (SOA) Curves

The SOA curves in the CSD87350Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 5 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

6.1.4 Normalized Curves

The normalized curves in the CSD87350Q5D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

6.2 Typical Application

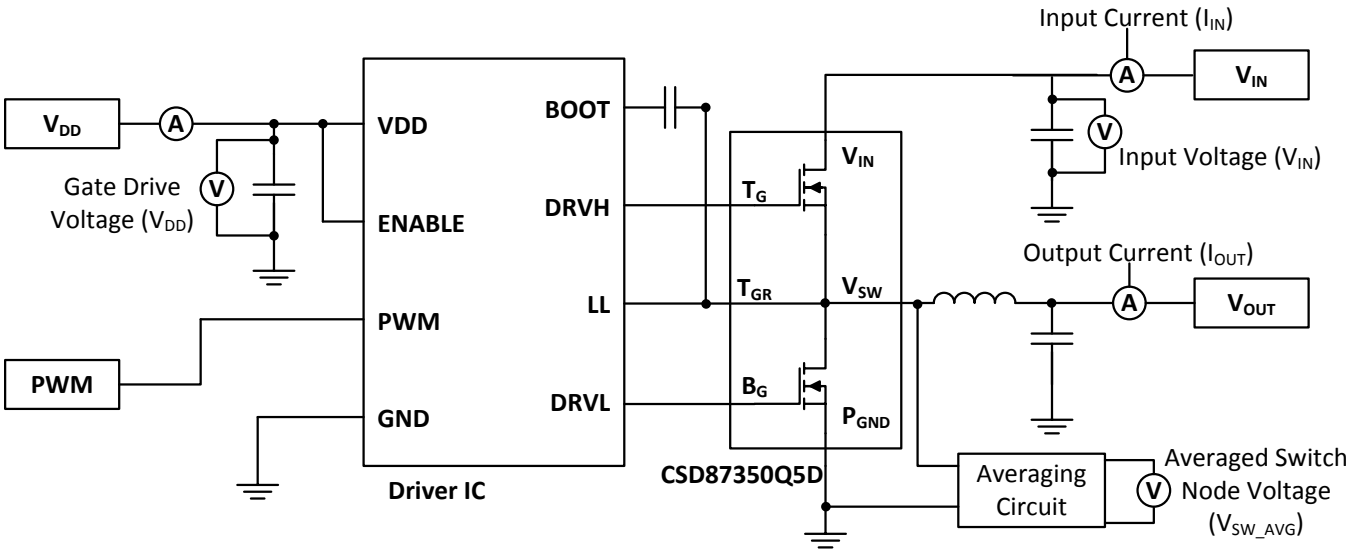


Figure 32.

6.2.1 Design Example: Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Operating Conditions*). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.2.2 Operating Conditions

- Output current = 25 A
- Input voltage = 7 V
- Output voltage = 1 V
- Switching frequency = 800 kHz
- Inductor = 0.2 µH

6.2.2.1 Calculating Power Loss

- Power Loss at 25 A = 3.5 W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.07 (Figure 7)
- Normalized Power Loss for output voltage ≈ 0.95 (Figure 8)
- Normalized Power Loss for switching frequency ≈ 1.11 (Figure 6)
- Normalized Power Loss for output inductor ≈ 1.07 (Figure 9)
- **Final calculated Power Loss = 3.5 W × 1.07 × 0.95 × 1.11 × 1.07 ≈ 4.23 W**

6.2.2.2 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 2°C (Figure 7)
- SOA adjustment for output voltage ≈ –1.3°C (Figure 8)
- SOA adjustment for switching frequency ≈ 2.8°C (Figure 6)
- SOA adjustment for output inductor ≈ 1.6°C (Figure 9)
- **Final calculated SOA adjustment = 2 + (-1.3) + 2.8 + 1.6 ≈ 5.1°C**

In the previous design example, the estimated power loss of the CSD87350Q5D would increase to 4.23 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 5.1°C. Figure 33 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.

Typical Application (continued)

2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 5.1°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

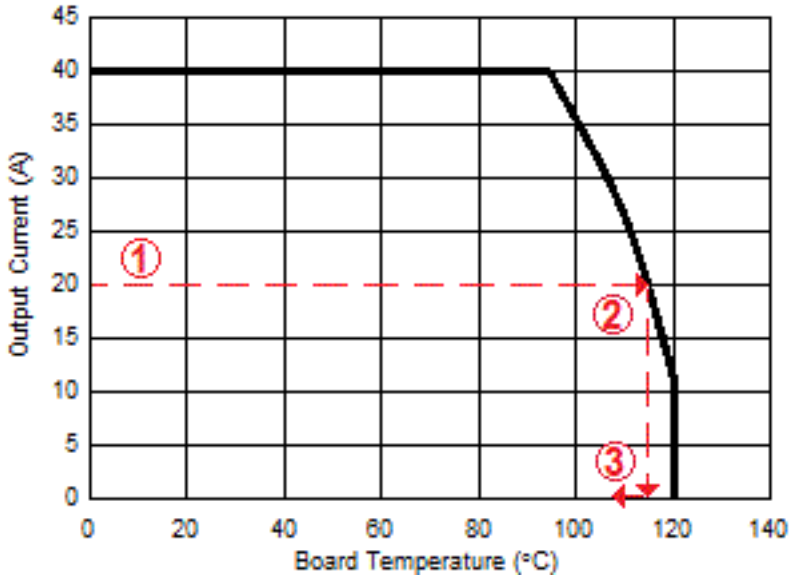


Figure 33. Power Block SOA

7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. The following sections provide a brief description on how to address each parameter.

7.1.1 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10kV/µs. Take special care with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 34). The example in Figure 34 uses 6 × 10-µF ceramic capacitors (TDK Part C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
- The driver IC should be placed relatively close to the power block gate pins. T_G and B_G should connect to the outputs of the driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.
- In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Refer to *Snubber Circuits: Theory , Design and Application* (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the Vsw node and PGND see Figure 34. (1)

7.1.2 Thermal Considerations

The power block has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 34 uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.2 Layout Example

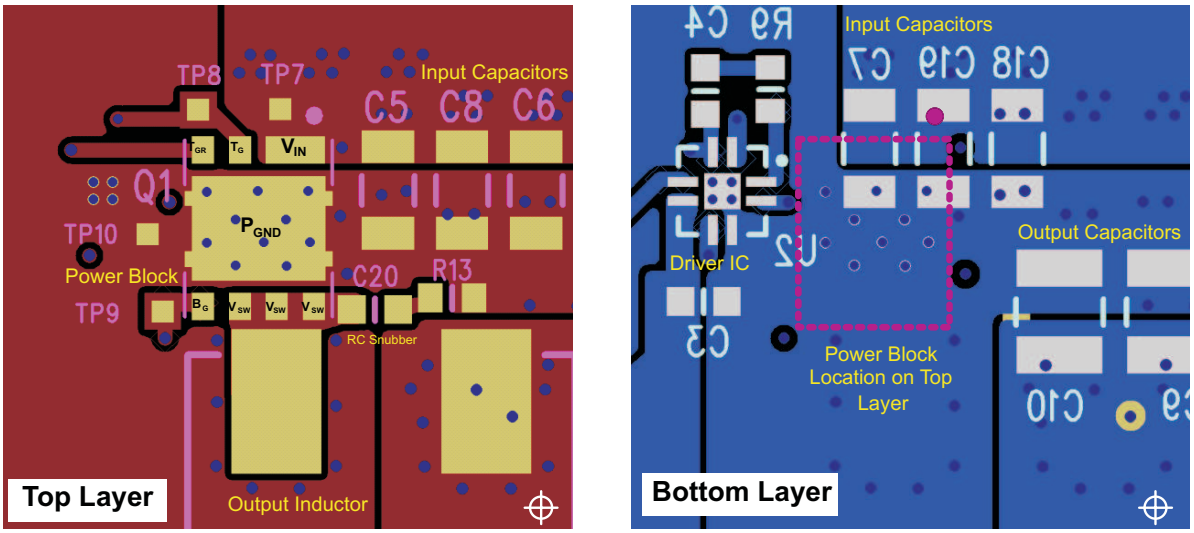


Figure 34. Recommended PCB Layout (Top View)

中）

8 器件和文档支持

8.1 文档支持

8.1.1 相关文档

相关文档请参见以下部分：

- *通过 PCB 布局技术来降低振铃*
- *针对同步降压转换器的功率损耗计算（包含共源电感注意事项）*
- *《缓冲电路：理论，设计和应用》*

8.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

8.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.4 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.6 Glossary

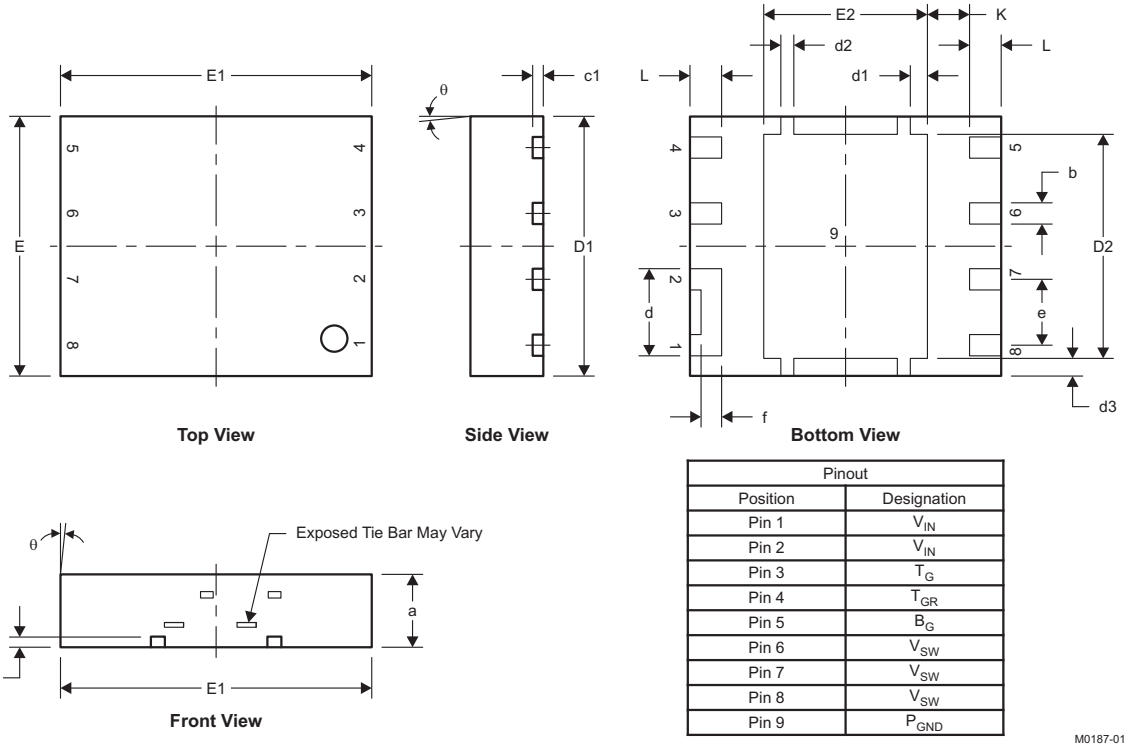
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

9.1 Q5D 封装尺寸

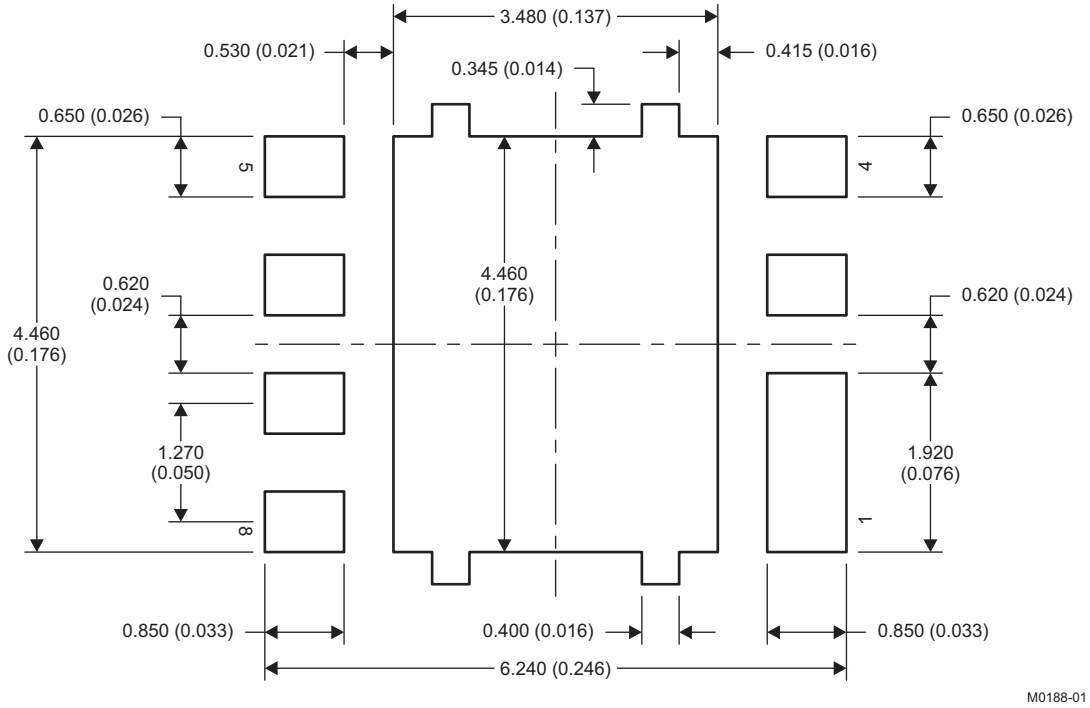


Pinout	
Position	Designation
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

M0187-01

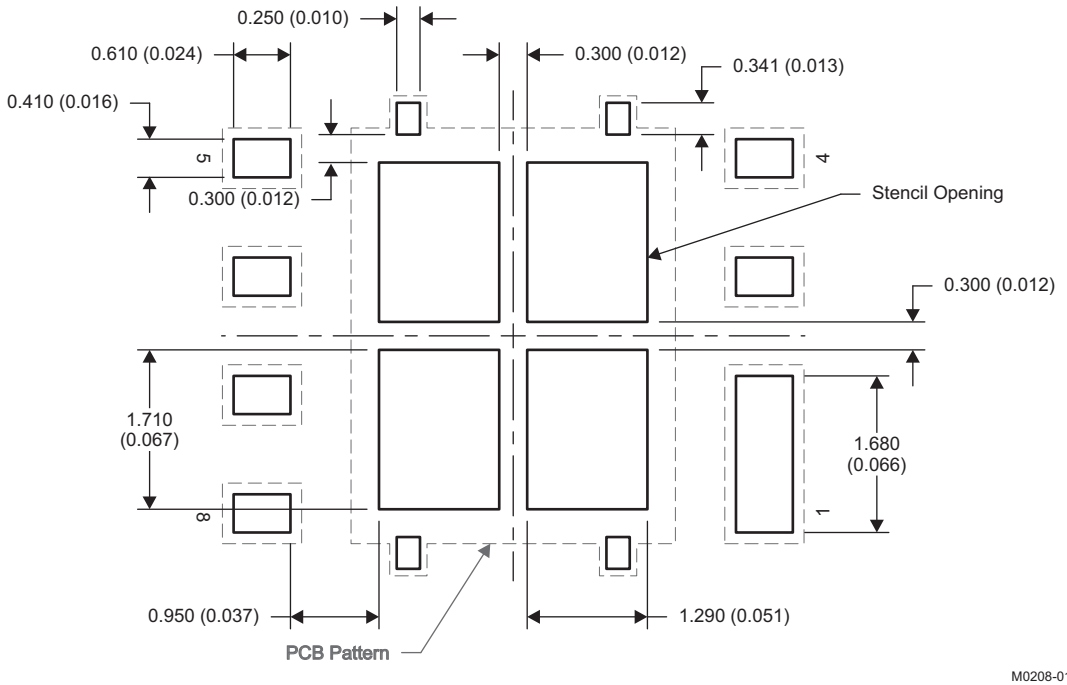
DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
a	1.40	1.5	0.055	0.059
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 典型值		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—
K	0.812		0.032	

9.2 焊盘布局建议



NOTE: 尺寸单位为 mm（英寸）。

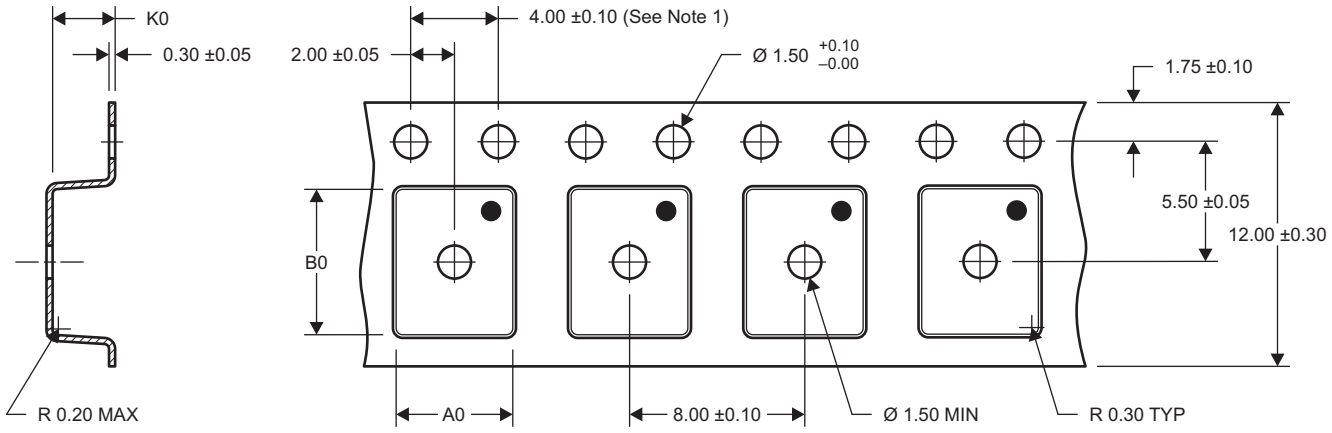
9.3 模板建议



NOTE: 尺寸单位为 mm（英寸）。

有关针对 PCB 设计的建议电路布局布线，请参见*《通过 PCB 布局布线技巧来减少振铃》*（文献编号：SLPA005）。

9.4 Q5D 卷带信息



NOTES: 1. 10 链轮孔距累积容差为 ±0.2

2. 每 100mm 长度的翘曲不能超过 1mm，250mm 长度的非累积量 (Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm)。

3. 材料：黑色抗静电聚苯乙烯。

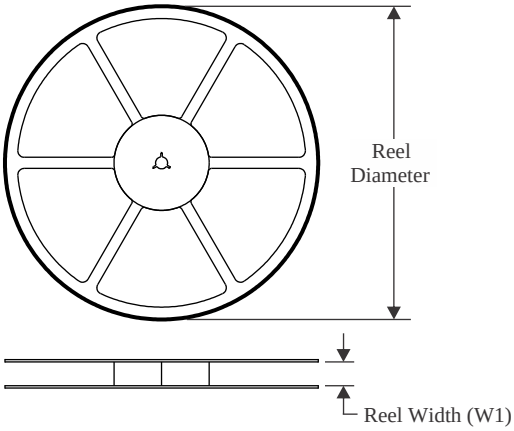
4. 全部尺寸单位为 mm，除非另外注明。

5. 厚度：0.3 ± 0.05mm。

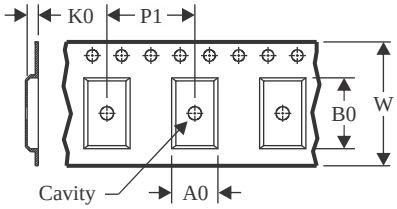
6. MSL1 260°C（红外 (IR) 和传导）PbF 回流焊兼容

TAPE AND REEL INFORMATION

REEL DIMENSIONS

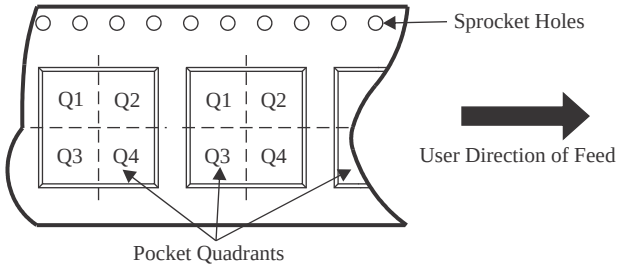


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

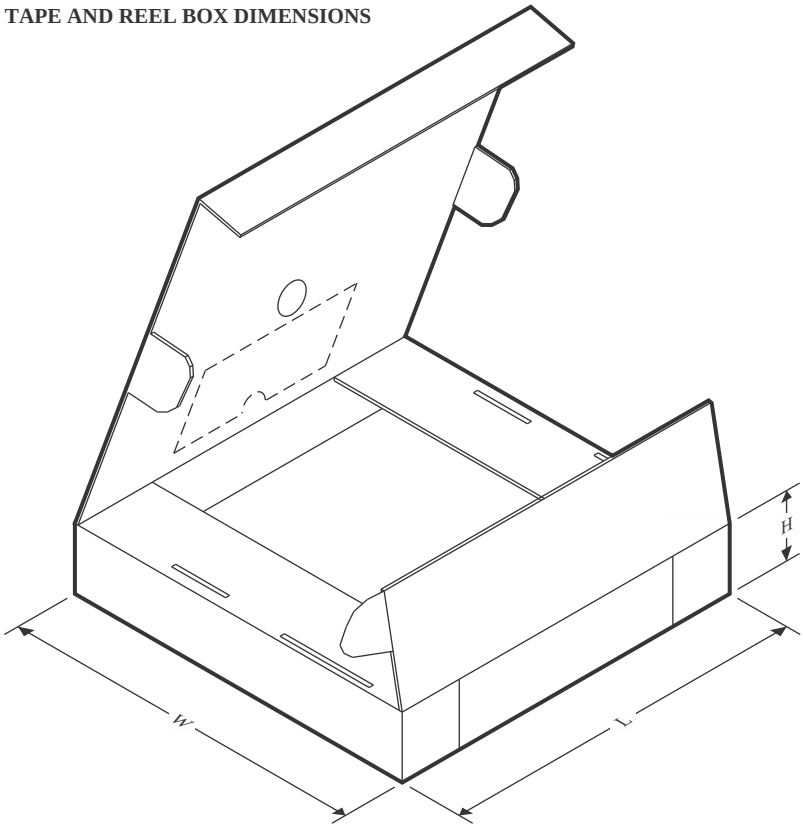
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87350Q5D	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2
CSD87350Q5DG4	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87350Q5D	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0
CSD87350Q5DG4	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265