CSD87334Q3D 同步降压 NexFET™ 电源块

1 特性

- 半桥电源块
- 针对高占空比进行了优化
- 输入电压高达 24V
- 12A 电流时系统效率达 96.1%
- 12A 电流时，P_{Loss} 为 1.6W
- 工作电流高达 20A
- 高频工作（高达 1.5MHz）
- 高密度 3.3mm × 3.3mm 小外形尺寸无引线 (SON) 封装
- 针对 5V 栅极驱动进行了优化
- 开关损耗较低
- 超低电感封装
- 符合 RoHS 环保标准
- 无卤素
- 无铅引脚镀层

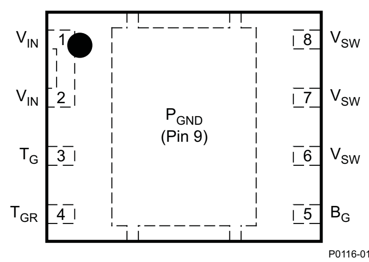
2 应用范围

- 同步降压转换器
  - 高频 应用
  - 高占空比 应用
- 同步升压转换器
- 负载点 (POL) 直流 - 直流转换器

3 说明

CSD87334Q3D NexFET™电源块是面向同步降压和升压 应用 的优化设计方案，能够以 3.3mm × 3.3mm 的小巧外形提供高电流、高效率以及高频率性能。该产品针对 5V 栅极驱动 应用进行了优化，在与外部控制器或驱动器配合使用时， 可在高占空比应用中 提供灵活的解决方案

俯视图

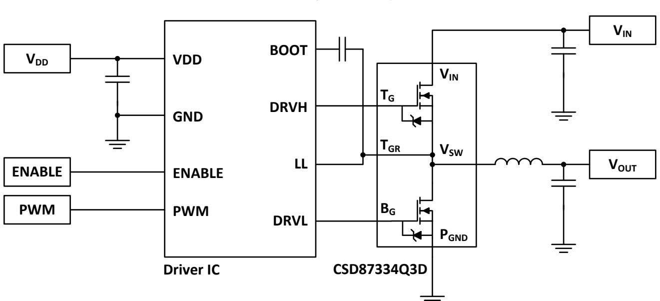


器件信息(1)

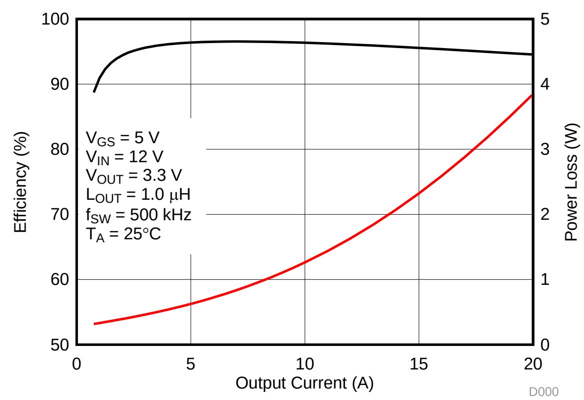
器件	数量	包装介质	封装	运输
CSD87334Q3D	2500	13 英寸卷带	SON 3.30mm × 3.30mm 塑料封装	卷带封装
CSD87334Q3DT	250	7 英寸卷带		

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

典型电路



典型电源块效率与功率损耗



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4 修订历史记录

Changes from Original (August 2015) to Revision A — **Page**

- Changed T_G to T_{GR} minimum voltage, from –8 V : to –0.3 V in *Absolute Maximum Ratings* table ... 3
- Changed B_G to P_{GND} minimum voltage, from –8 V : to –0.3 V in *Absolute Maximum Ratings* table ... 3
- Changed I_{GSS} test condition for V_{GS}, from +10 / –8 V : to 10 V in *Electrical Characteristics* table ... 4
- 已添加 *“接收文档更新通知”*部分和*“社区资源”*部分添加到了*“器件和文档支持”*部分 ... 14

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (see [1])

			MIN	MAX	UNIT
	Voltage	V_{IN} to P_{GND}		30	V
		V_{SW} to P_{GND}		30	
		V_{SW} to P_{GND} (10 ns)		32	
		T_G to T_{GR}	–0.3	10	
		B_G to P_{GND}	–0.3	10	
I_{DM}	Pulsed current rating			60	A
P_D	Power dissipation			6	W
E_{AS}	Avalanche energy	Sync FET, I_D = 31 A, L = 0.1 mH		48	mJ
		Control FET, I_D = 31 A, L = 0.1 mH		48	
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{GS}	Gate drive voltage		3.3	8	V
V_{IN}	Input supply voltage			24	V
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)		1500	kHz
	Operating current			20	A
T_J	Operating temperature			125	°C

5.3 Power Block Performance

T_A = 25°C (unless otherwise noted) (see [1])

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power loss[1]	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 12 A, f_{SW} = 500 kHz, L_{OUT} = 1 µH, T_J = 25°C		1.6		W
I_{QVIN}	V_{IN} quiescent current	T_G to T_{GR} = 0 V B_G to P_{GND} = 0 V			10	µA

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5-V driver IC.

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

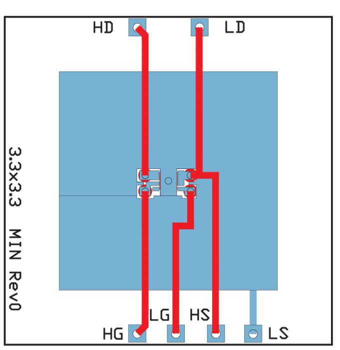
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu)[1]			130	°C/W
	Junction-to-ambient thermal resistance (max Cu)[1][2]			75	
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)[1]			21	°C/W
	Junction-to-case thermal resistance (P_{GND} pin)[1]			2.1	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2) Cu.

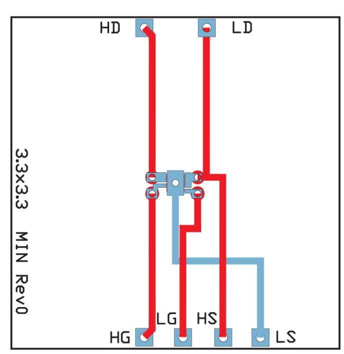
5.5 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	30			30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			100			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.75	0.90	1.20	0.75	0.90	1.20	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 3.5 V, I_{DS} = 12 A		6.3	8.3		6.3	8.3	mΩ
		V_{GS} = 4.5 V, I_{DS} = 12 A		5.6	7.0		5.6	7.0	
		V_{GS} = 8 V, I_{DS} = 12 A		4.9	6.0		4.9	6.0	
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 12 A		62			62		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, *f* = 1 MHz		971	1260		971	1260	pF
C_{OSS}	Output capacitance			453	589		453	589	pF
C_{RSS}	Reverse transfer capacitance			16	21		16	21	pF
R_G	Series gate resistance			1.0	2.0		1.0	2.0	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 12 A		6.4	8.3		6.4	8.3	nC
Q_{gd}	Gate charge gate-to-drain			1.0			1.0		nC
Q_{gs}	Gate charge gate-to-source			1.9			1.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.9			0.9		nC
Q_{OSS}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		10.5			10.5		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 12 A, R_G = 2 Ω		4			4		ns
t_r	Rise time			7			7		ns
$t_{d(off)}$	Turnoff delay time			11			11		ns
t_f	Fall time			17			17		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	I_{DS} = 12 A, V_{GS} = 0 V		0.8	1.0		0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS} = 15 V, I_F = 12 A, di/dt = 300 A/μs		23			23		nC
t_{rr}	Reverse recovery Time			18			18		ns



Max $R_{\theta JA}$ = 75°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 130°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.6 Typical Power Block Device Characteristics

The typical power block system characteristic curves (Figure 1 through Figure 9) are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See *Application and Implementation* for detailed explanation. Conditions for Figure 1 through Figure 5 are given by the following; V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 3.3 V, f_{SW} = 500 kHz, L_{OUT} = 1 µH. T_A = 125°C, unless stated otherwise.

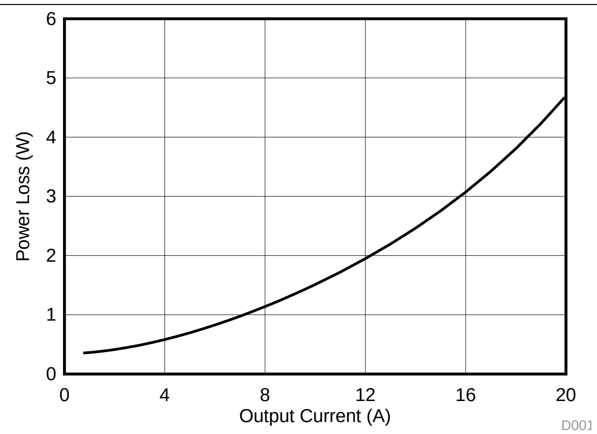


Figure 1. Power Loss vs Output Current

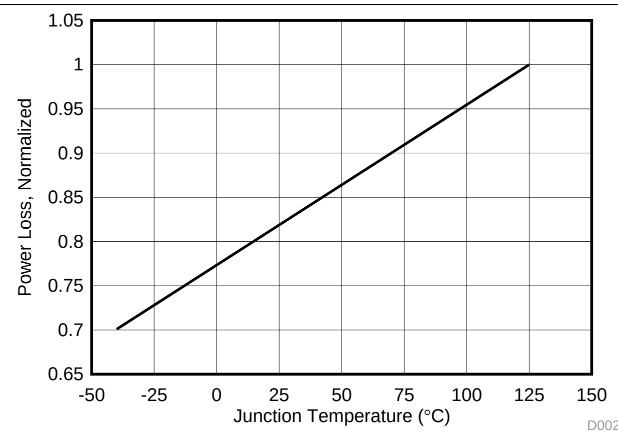


Figure 2. Power Loss vs Temperature

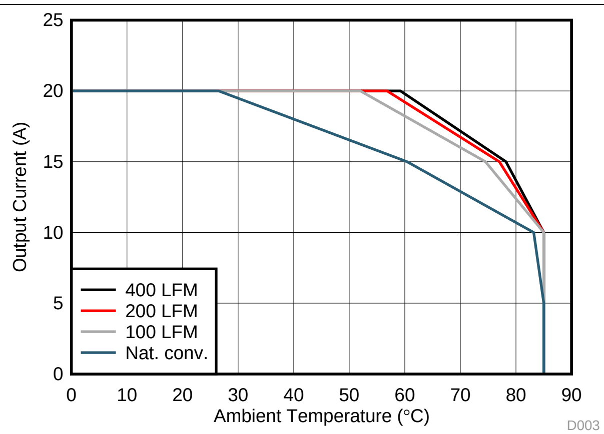


Figure 3. Safe Operating Area – PCB Horizontal Mount

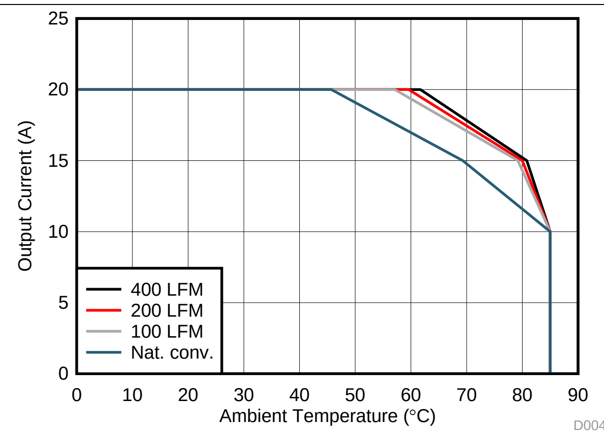


Figure 4. Safe Operating Area – PCB Vertical Mount

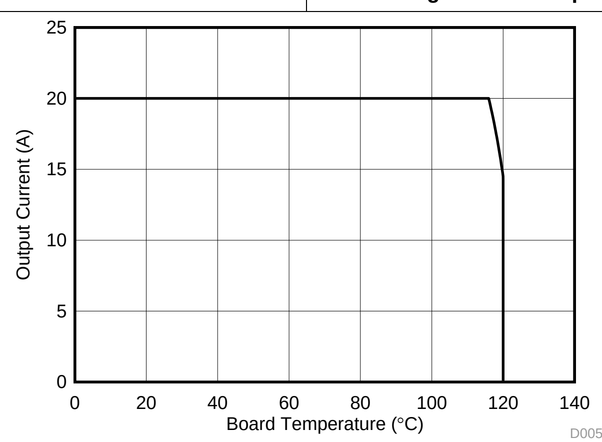


Figure 5. Typical Safe Operating Area

Typical Power Block Device Characteristics (continued)

The typical power block system characteristic curves (Figure 1 through Figure 9) are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See *Application and Implementation* for detailed explanation. Conditions for Figure 1 through Figure 5 are given by the following; V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 3.3 V, f_{SW} = 500 kHz, L_{OUT} = 1 µH. T_A = 125°C, unless stated otherwise.

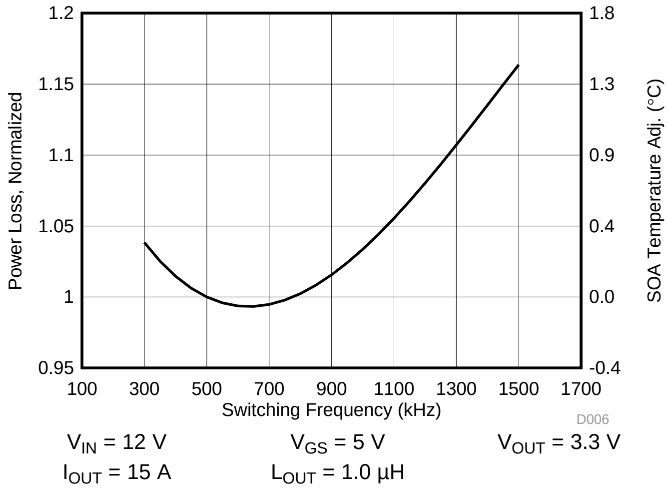


Figure 6. Normalized Power Loss vs Switching Frequency

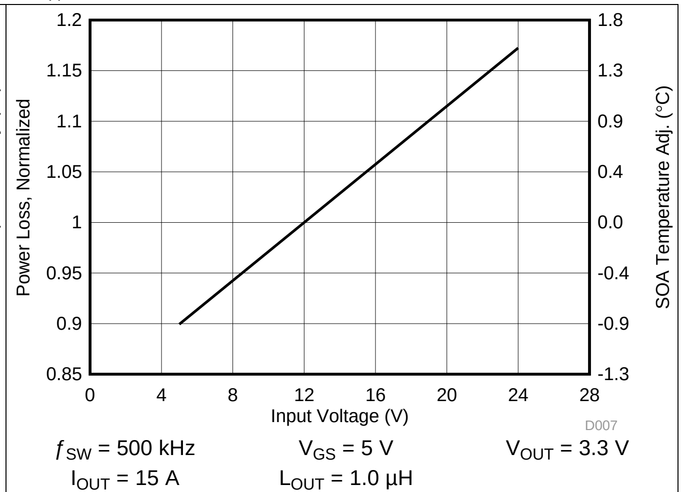


Figure 7. Normalized Power Loss vs Input Voltage

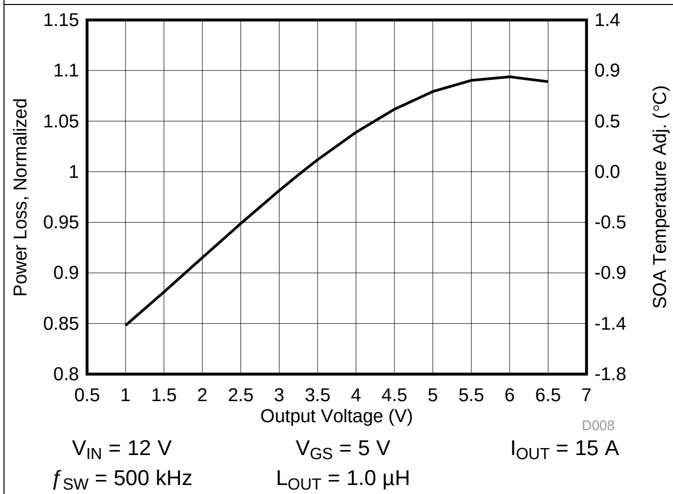


Figure 8. Normalized Power Loss vs Output Voltage

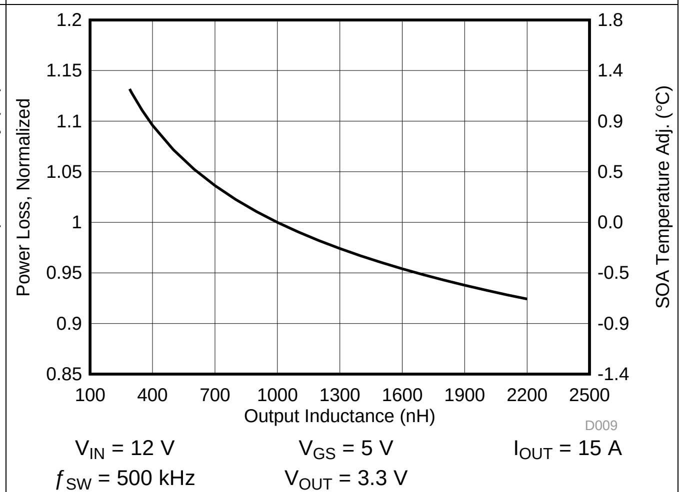


Figure 9. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

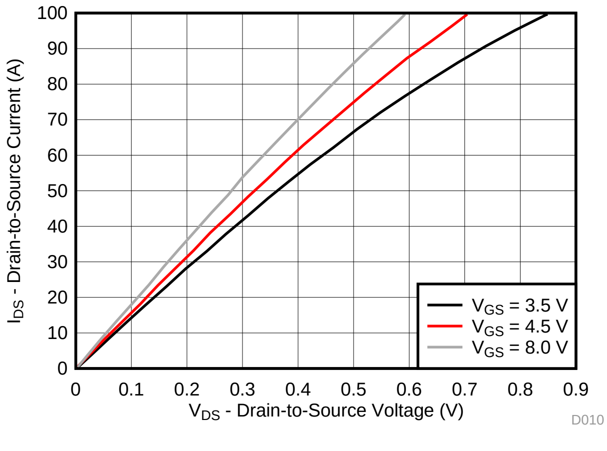


Figure 10. MOSFET Saturation Characteristics

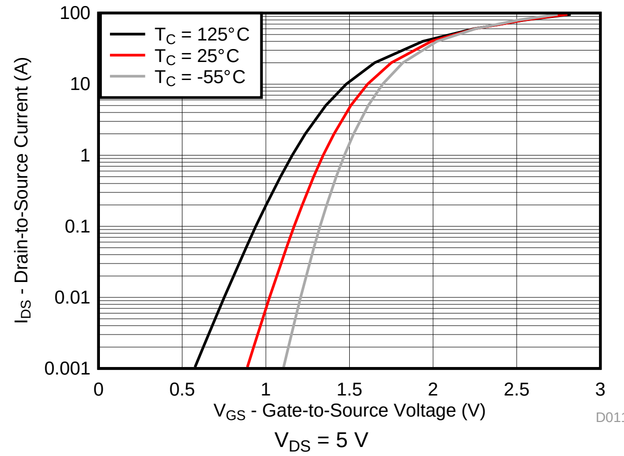


Figure 11. MOSFET Transfer Characteristics

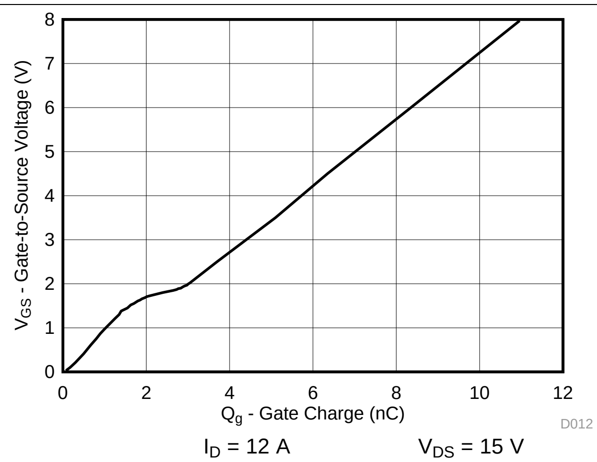


Figure 12. MOSFET Gate Charge

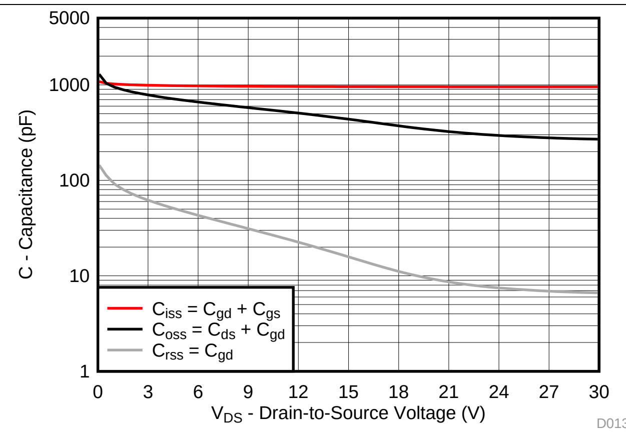


Figure 13. MOSFET Capacitance

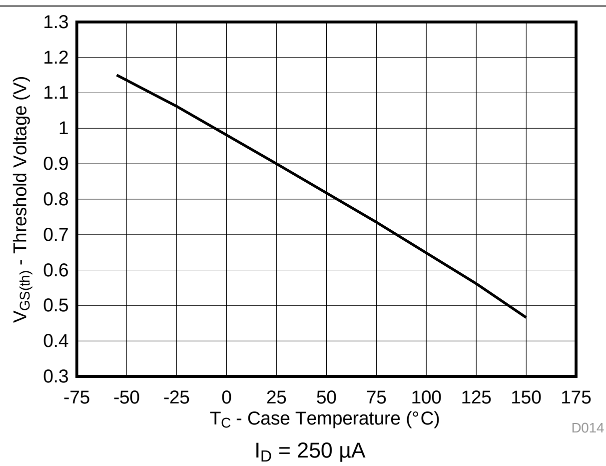


Figure 14. MOSFET $V_{GS(th)}$

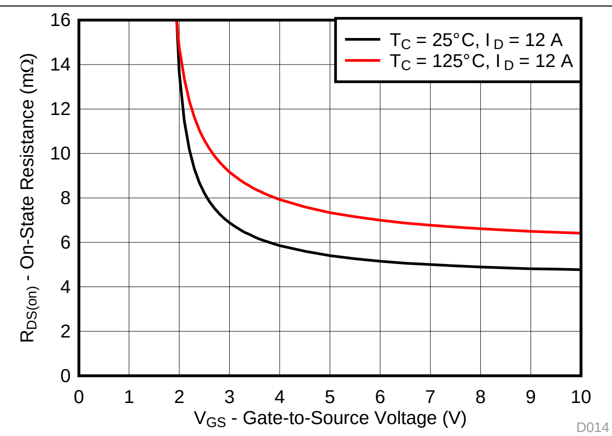


Figure 15. MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

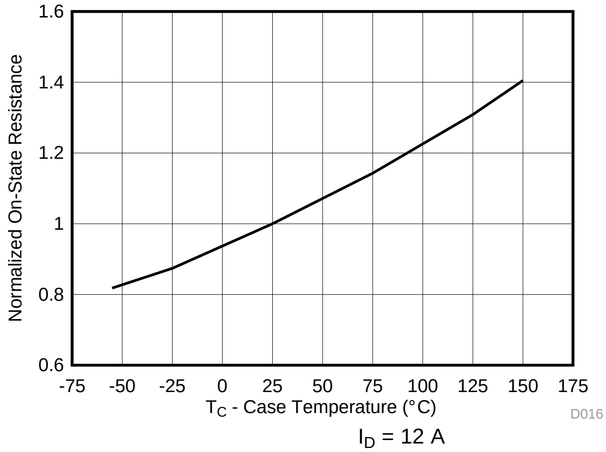


Figure 16. MOSFET Normalized $R_{DS(on)}$

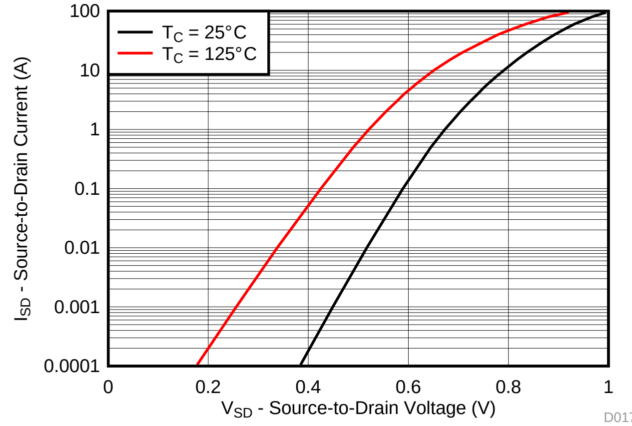


Figure 17. MOSFET Body Diode

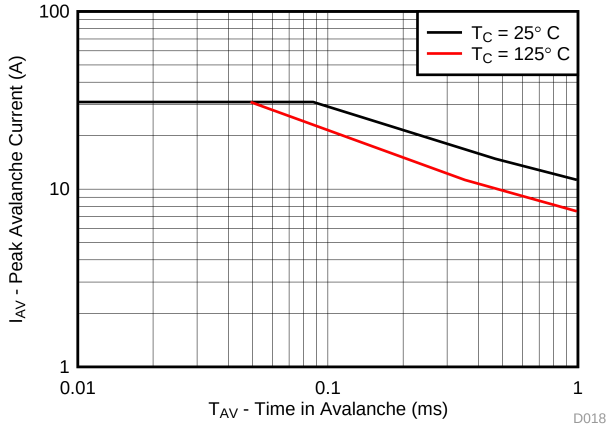


Figure 18. MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87334Q3D NexFET power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.2 Typical Application

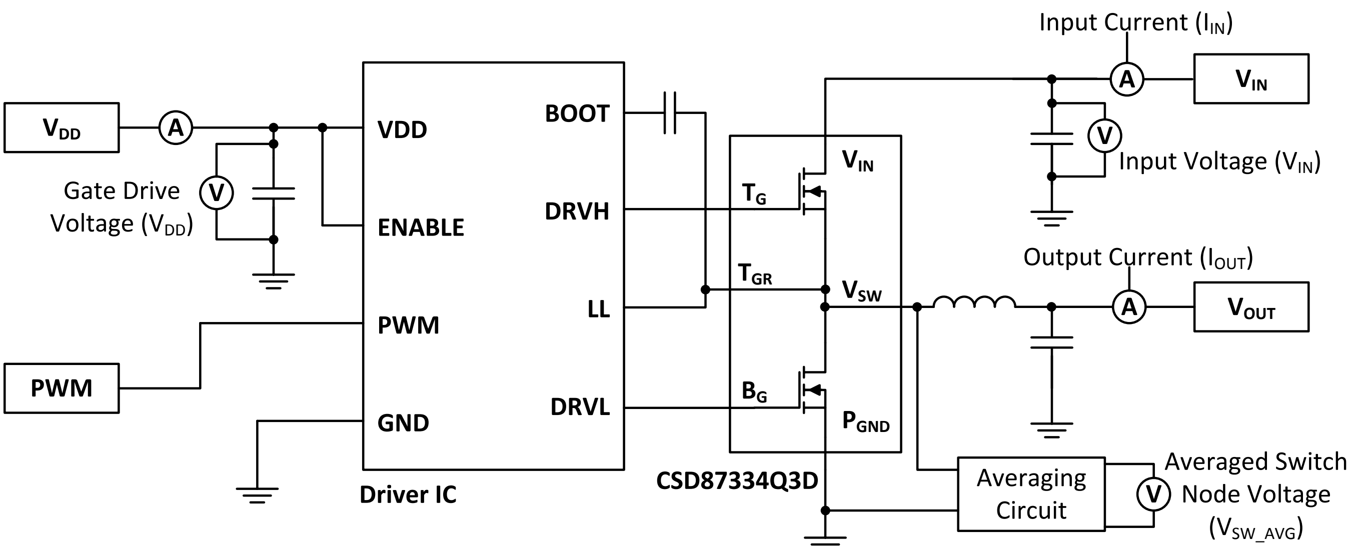


Figure 19. Typical Circuit Application

6.3 System Example

6.3.1 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87334Q3D as a function of load current. This curve is measured by configuring and running the CSD87334Q3D as it would be in the final application (see Figure 19). The measured power loss is the CSD87334Q3D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\text{Power loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

System Example (continued)

6.3.2 Safe Operating Area (SOA) Curves

The SOA curves in the CSD87334Q3D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 5 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the SOA. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

6.3.3 Normalized Curves

The normalized curves in the CSD87334Q3D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss, and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

6.3.4 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example* section). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

6.3.4.1 Design Example

Operating conditions:

- Output current = 15 A
- Input voltage = 16 V
- Output voltage = 5 V
- Switching frequency = 1000 kHz
- Inductor = 0.6 µH

6.3.4.2 Calculating Power Loss

- Power loss at 15 A = 2.8 W (Figure 1)
- Normalized power loss for input voltage ≈ 1.05 (Figure 7)
- Normalized power loss for output voltage ≈ 1.08 (Figure 8)
- Normalized power loss for switching frequency ≈ 1.03 (Figure 6)
- Normalized power loss for output inductor ≈ 1.05 (Figure 9)
- **Final calculated power loss = 2.8 W × 1.05 × 1.08 × 1.03 × 1.05 ≈ 3.4 W**

6.3.4.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 0.5°C (Figure 7)
- SOA adjustment for output voltage ≈ 0.7°C (Figure 8)
- SOA adjustment for switching frequency ≈ 0.3°C (Figure 6)
- SOA adjustment for output inductor ≈ 0.5°C (Figure 9)
- **Final calculated SOA adjustment = 0.5 + 0.7 + 0.3 + 0.5 ≈ 2°C**

In the design example, the estimated power loss of the CSD87334Q3D would increase to 3.4 W. In addition, the maximum allowable board or ambient temperature, or both, would have to decrease by 2°C. Figure 20 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board or ambient temperature.
3. Adjust the SOA board or ambient temperature by subtracting the temperature adjustment value.

System Example (continued)

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 2°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board or ambient temperature.

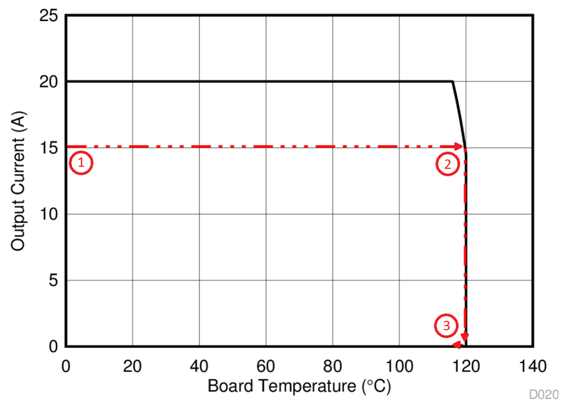


Figure 20. Power Block SOA

7 Layout

7.1 Layout Guidelines

7.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1.2 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's V_{IN} and P_{GND} pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the V_{IN} and P_{GND} pins (see Figure 21). The example in Figure 21 uses six 10-µF ceramic capacitors (TDK C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
- The driver IC should be placed relatively close to the power block gate pins. T_G and B_G should connect to the outputs of the driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, and so forth). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block V_{SW} pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.[1] In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R, and from 330 pf to 2200 pF for the C. Please refer to *Snubber Circuits: Theory, Design and Application* (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the V_{SW} node and P_{GND} (see Figure 21). [1]

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.2 Layout Example

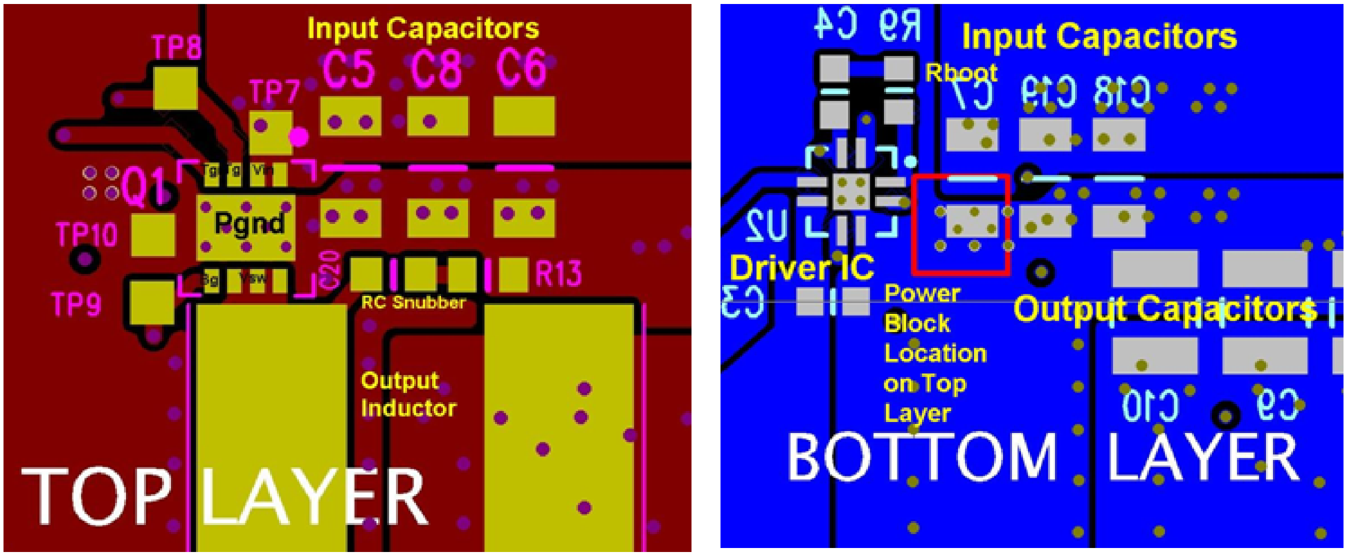


Figure 21. Recommended PCB Layout (Top Down)

7.3 Thermal Considerations

The power block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 21 uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the PCB design rules and manufacturing capabilities of the end user.

8 器件和文档支持

8.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

8.2 社区资源

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8.3 商标

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8.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.5 Glossary

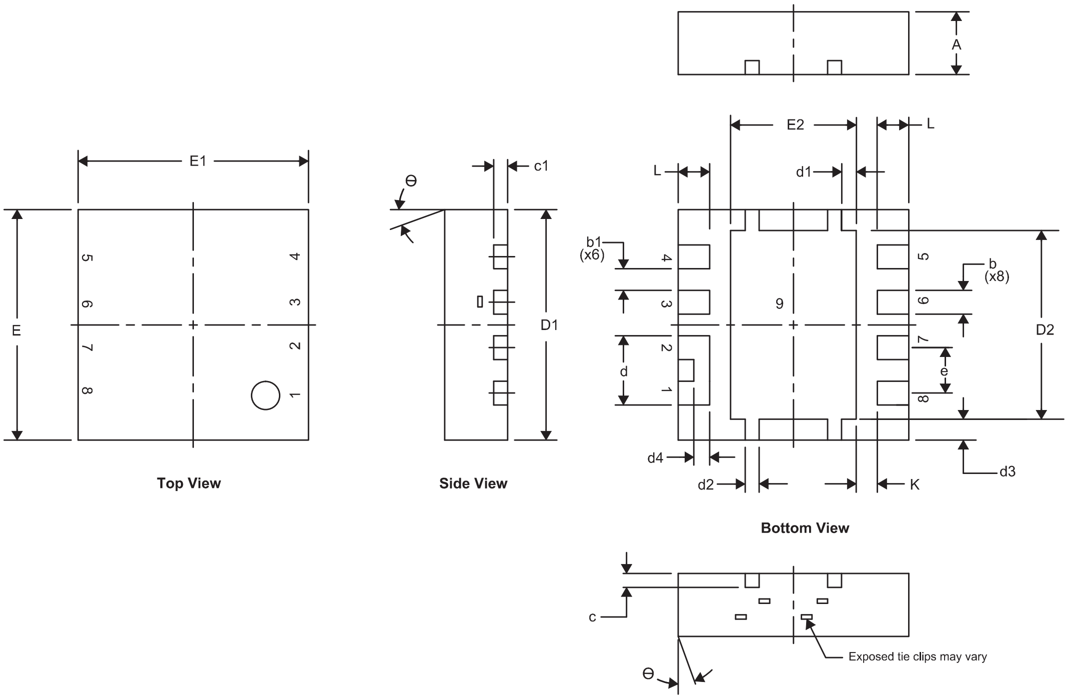
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

9.1 Q3D 封装尺寸

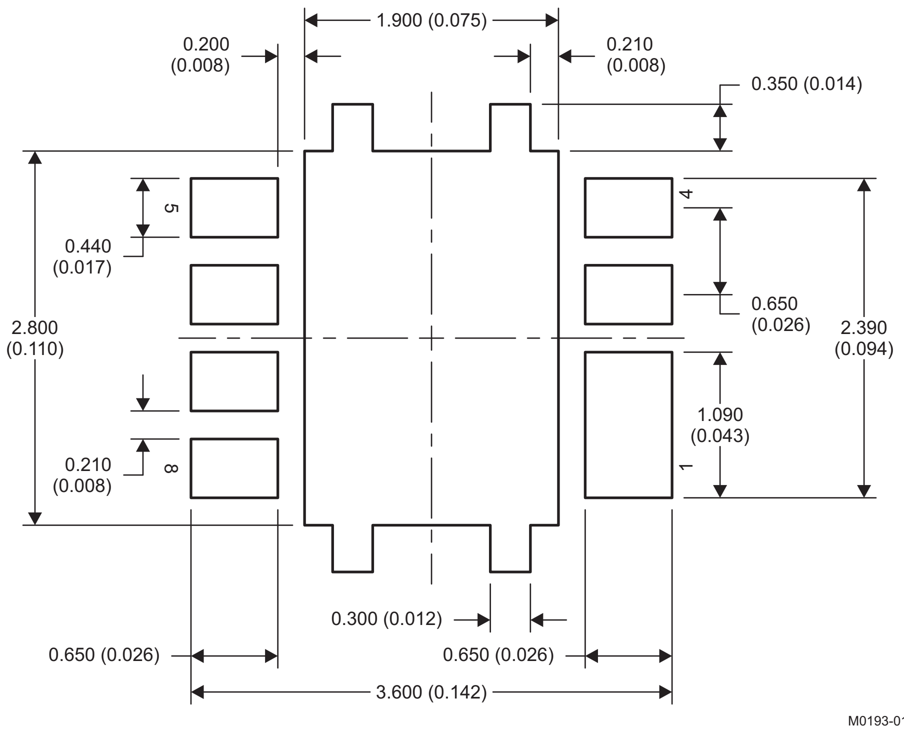


DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.850		1.050	0.033		0.041
b	0.280		0.400	0.011		0.016
b1		0.310			0.012	
c	0.150		0.250	0.006		0.010
c1	0.150		0.250	0.006		0.010
d	0.940		1.040	0.037		0.041
d1	0.160		0.260	0.006		0.010
d2	0.150		0.250	0.006		0.010
d3	0.250		0.350	0.010		0.014
d4	0.175		0.275	0.007		0.011
D1	3.200		3.400	0.126		0.134
D2	2.650		2.750	0.104		0.108
E	3.200		3.400	0.126		0.134
E1	3.200		3.400	0.126		0.134
E2	1.750		1.850	0.069		0.073
e		0.650 典型值			0.026 典型值	
L	0.400		0.500	0.016		0.020
θ	0.000		—	—		—
K		0.300 典型值			0.012 典型值	

表 **1.** 引脚布局配置

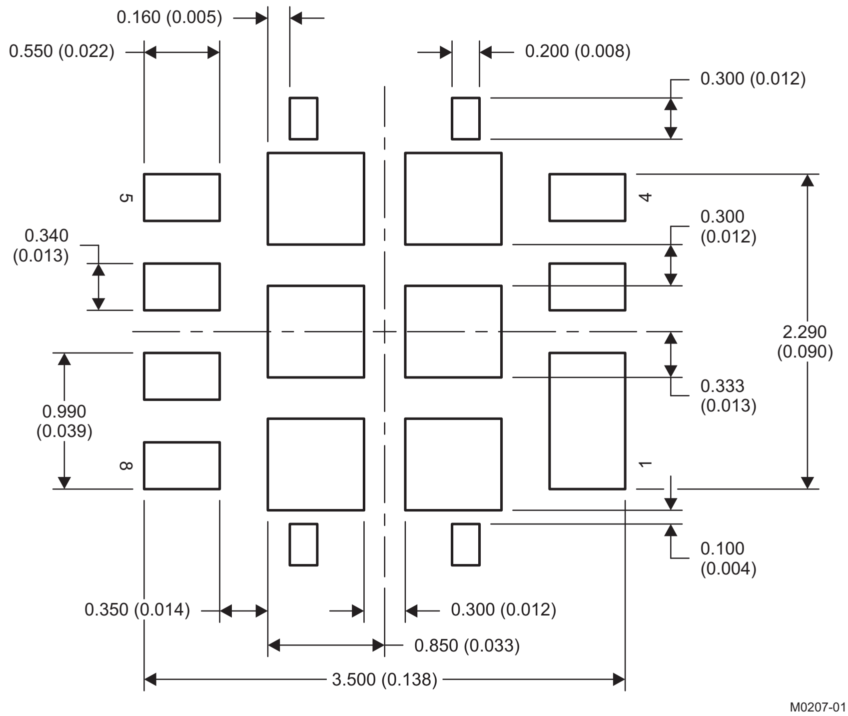
位置	名称
引脚 1	V_{IN}
引脚 2	V_{IN}
引脚 3	T_G
引脚 4	T_{GR}
引脚 5	B_G
引脚 6	V_{SW}
引脚 7	V_{SW}
引脚 8	V_{SW}
引脚 9	P_{GND}

9.2 焊盘布局建议



NOTE: 尺寸单位为 mm（英寸）。

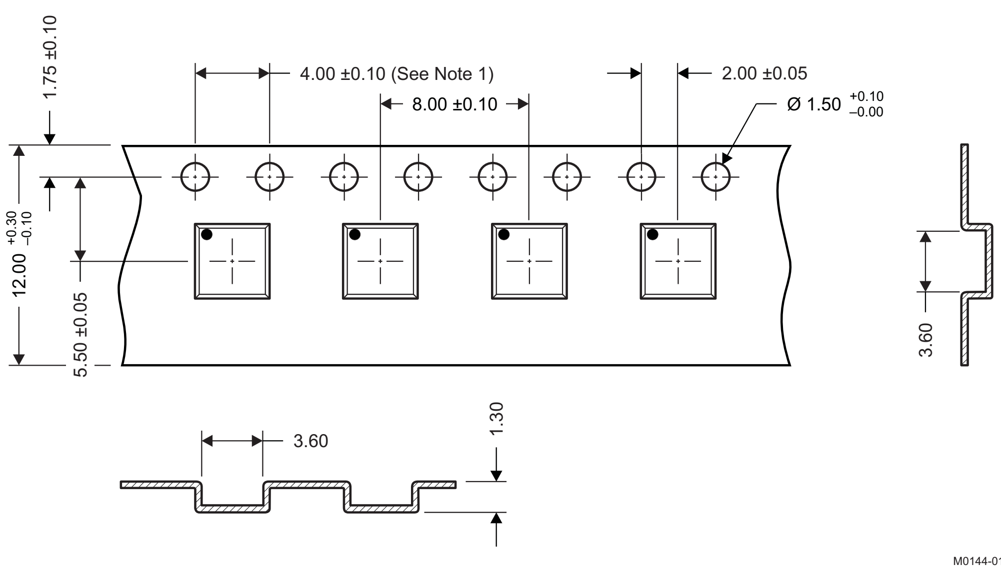
9.3 模板建议



NOTE: 尺寸单位为 mm（英寸）。

有关针对 PCB 设计的建议电路布局布线，请参见*《通过 PCB 布局布线技巧来减少振铃》*（文献编号：SLPA005）。

9.4 Q3D 卷带信息



NOTES: 1. 10 链齿孔距累积容差 ±0.2。

2. 每 100mm 长度的外倾角不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 全部尺寸单位为 mm，除非另外注明。
5. 厚度：0.3 ± 0.05mm。
6. 符合 MSL1 260°C（红外和对流）PbF 回流焊要求。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD87334Q3D	Active	Production	VSON-CLIP (DPB) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3D.B	Active	Production	VSON-CLIP (DPB) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3DG4	Active	Production	VSON-CLIP (DPB) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3DG4.B	Active	Production	VSON-CLIP (DPB) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3DT	Active	Production	VSON-CLIP (DPB) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	87334D
CSD87334Q3DT.B	Active	Production	VSON-CLIP (DPB) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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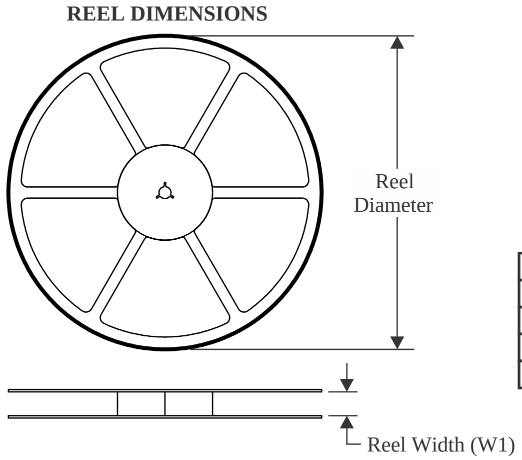
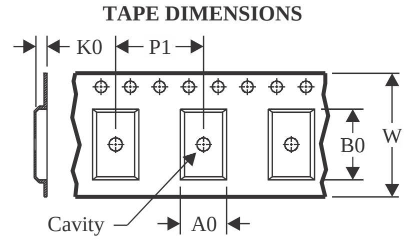
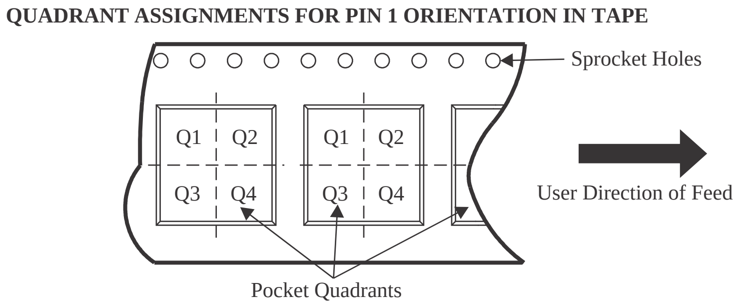
TAPE AND REEL INFORMATION





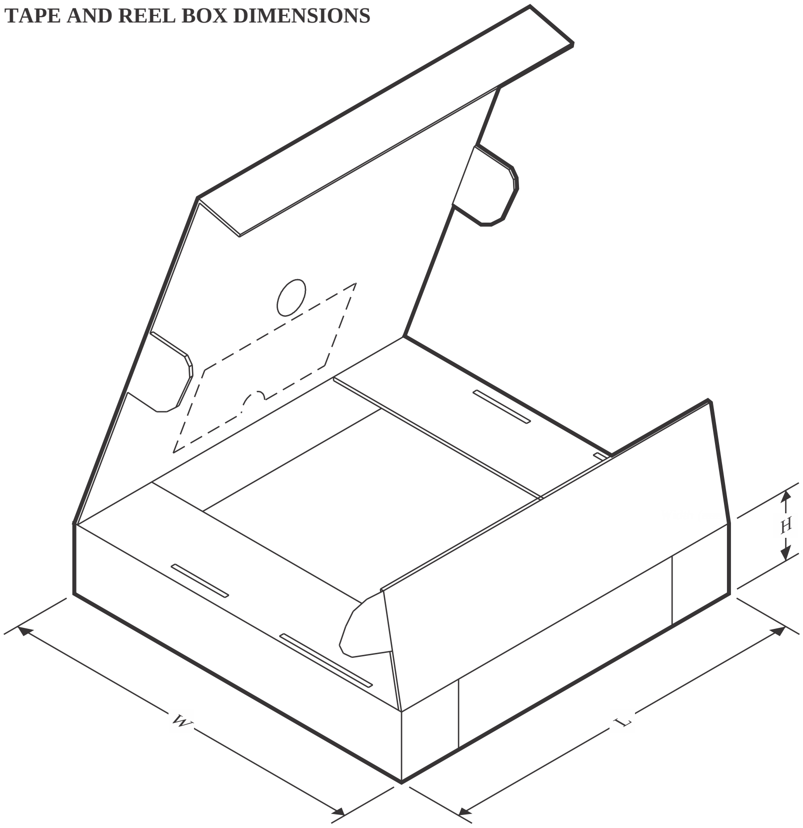
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

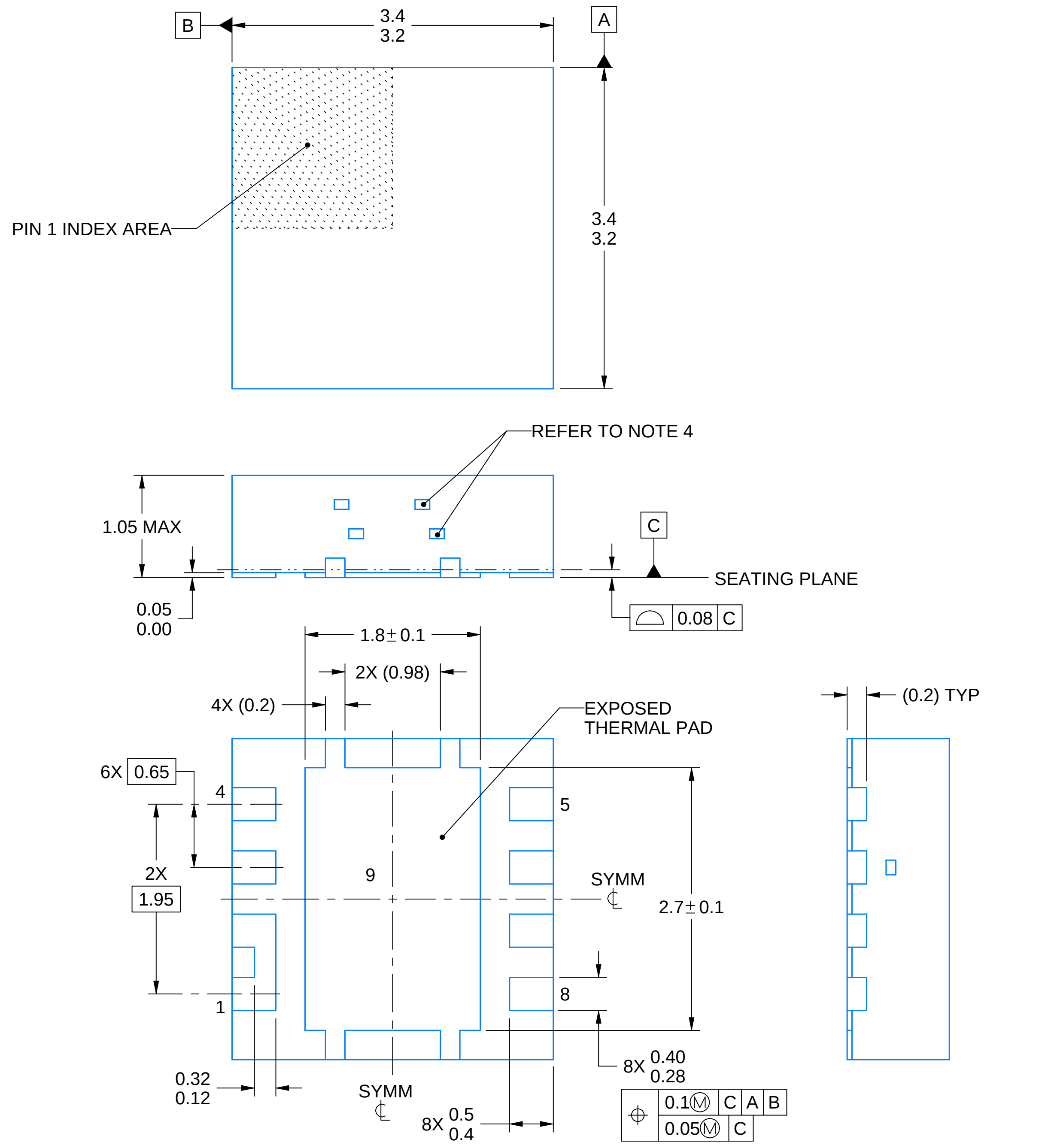
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87334Q3D	VSON-CLIP	DPB	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87334Q3DG4	VSON-CLIP	DPB	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87334Q3DT	VSON-CLIP	DPB	8	250	180.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87334Q3D	VSON-CLIP	DPB	8	2500	346.0	346.0	33.0
CSD87334Q3DG4	VSON-CLIP	DPB	8	2500	346.0	346.0	33.0
CSD87334Q3DT	VSON-CLIP	DPB	8	250	182.0	182.0	20.0



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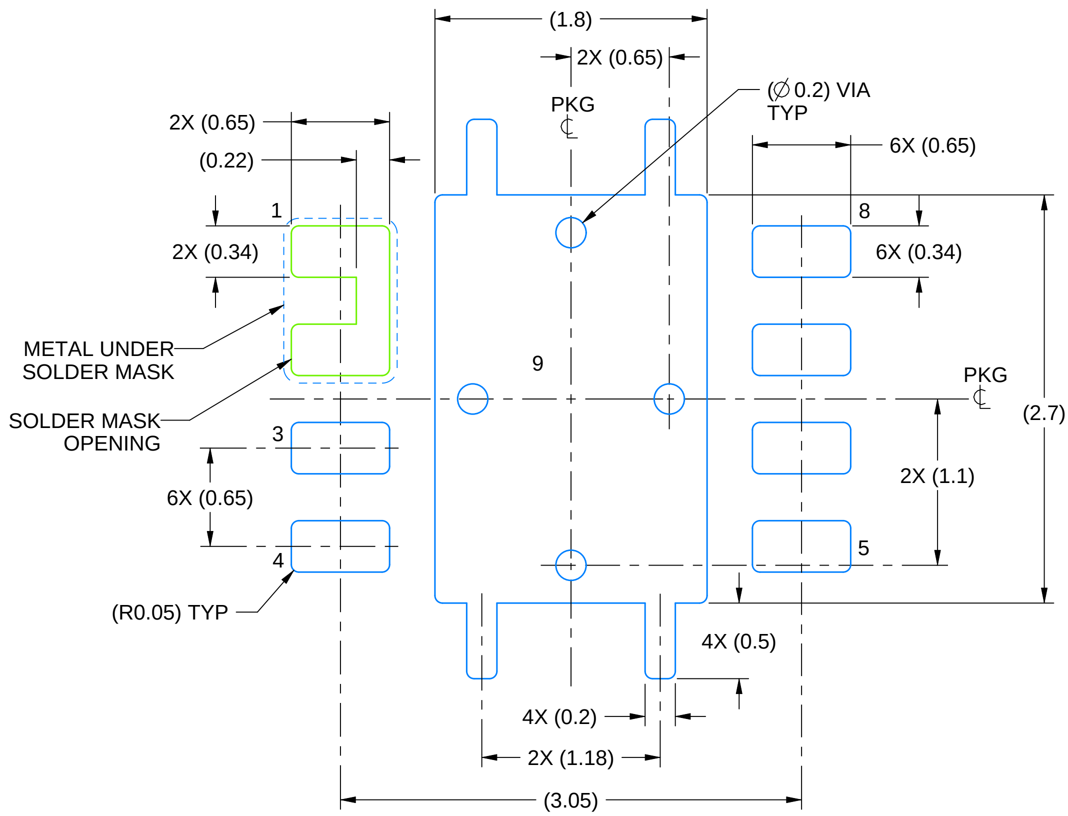
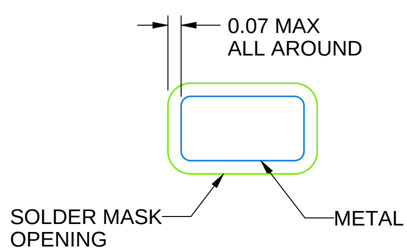
NOTES:

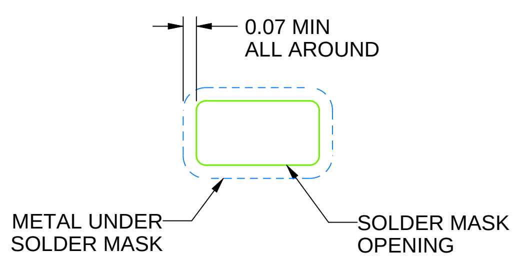
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance
4. Exposed metals on side wall may vary & not visible.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
PREFERRED FOR PADS 3-9



SOLDER MASK
DEFINED
PADS 1 & 2 (OPTIONAL FOR OTHERS)

SOLDER MASK DETAILS

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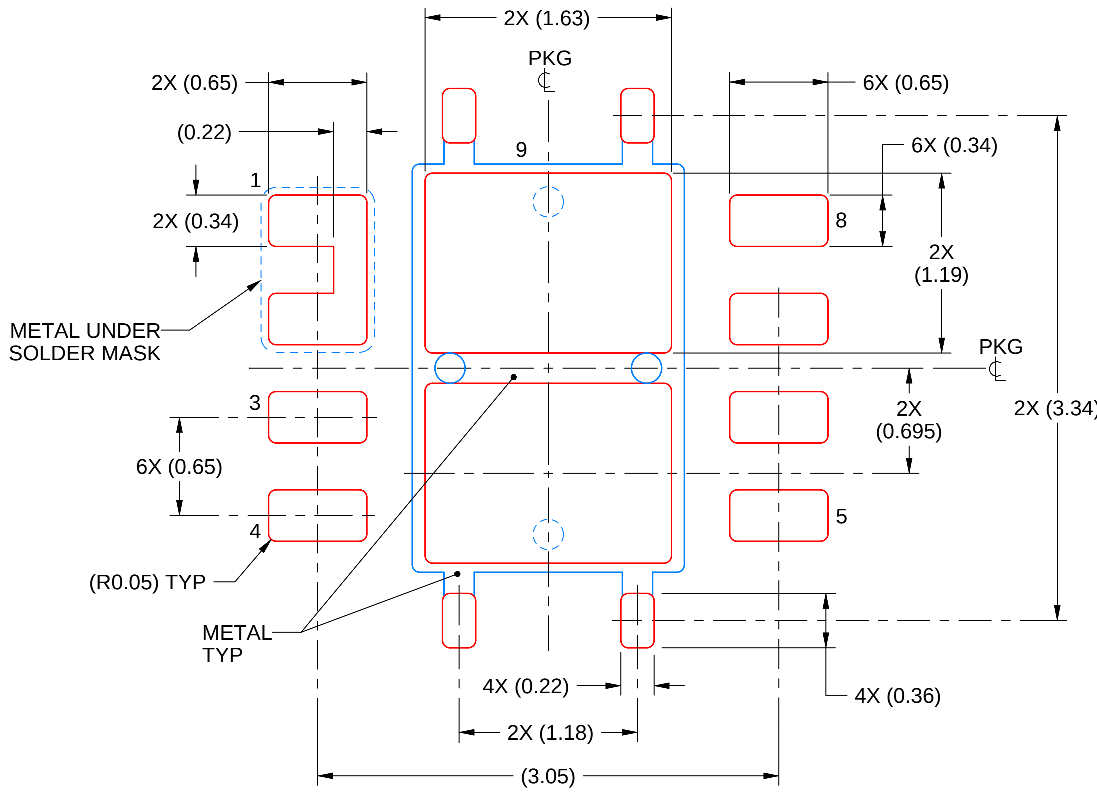
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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