双路 30V N 通道 NextFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

特性

- 共源连接
- 超低漏极到漏极导通电阻
- 节省空间的小外形尺寸无引线 **(SON) 3.3mm x 3.3mm** 塑料封装
- 针对 **5V** 栅极驱动进行了优化
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 **RoHS** 标准
- 无卤素

应用范围

- 针对笔记本个人电脑 **(PC)** 和平板电脑的适配器 **/ USB** 输入保护

说明

CSD87312Q3E 是一款设计用于适配器 / USB 输入保护的 30V 共源、双路 N 通道器件。 此类 SON 3.3mm x 3.3mm 器件有低漏极到漏极导通电阻，这大大减少了损耗并且为空间受限的多节电池充电类应用提供低组件数量。

产品概述

T_A=25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	6.3		nC
Q_{gd}	栅漏栅极电荷	0.7		nC
R_{DD}（导通）	漏极到漏极导通电阻 (Q1+Q2)	V_{GS}=4.5V	31	mΩ
		V_{GS}=8V	27	mΩ
$V_{GS(th)}$	阈值电压	1.0		V

订购信息

器件	封装	介质	数量	出货
CSD87312Q3E	小外形尺寸无引线 (SON) 3.3mm x 3.3mm 塑料封装	13 英寸卷带	2500	卷带封装

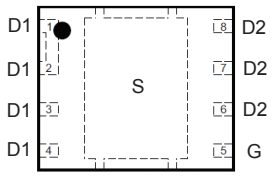
绝对最大额定值

T_A=25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	+10/-8	V
I_D	持续漏极电流，T_C=25°C 时测得(1)	27	A
I_{DM}	脉冲漏极电流 (2)	45	A
P_D	功率耗散	2.5	W
T_J, T_{STG}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D=24A，L=0.1mH，R_G=25Ω	29	mJ

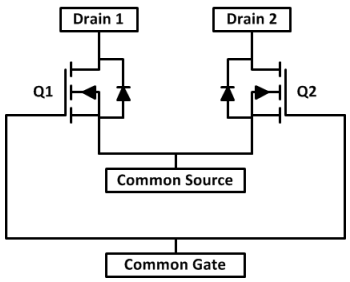
(1) R=63°C/W，这是在厚度为 0.060" 的环氧板印刷电路板 (FR4PCB) 上 1 in²（2 盎司）铜过渡垫片上测得的典型值

(2) 脉冲持续时间 ≤ 300μs，占空比 ≤ 2%

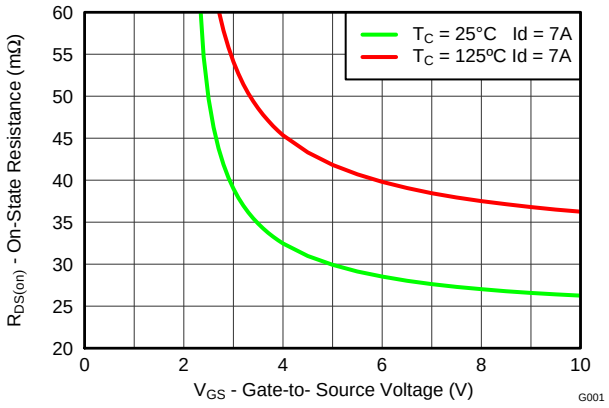
俯视图



电路图象



V_{GS}与 R_{DDon}间的关系



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10/-8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.8	1.0	1.3	V
$R_{DD(on)}$	Drain to Drain On Resistance (Q1 + Q2)	V_{GS} = 4.5V, I_D = 7A		31	38	mΩ
		V_{GS} = 8V, I_D = 7A		27	33	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 7A		39		S
Dynamic Characteristics(1)						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		960	1250	pF
C_{oss}	Output Capacitance			190	247	pF
C_{rss}	Reverse Transfer Capacitance			12	16	pF
R_G	Series Gate Resistance			5	10	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_D = 7A		6.3	8.2	nC
Q_{gd}	Gate Charge Gate to Drain			0.7		nC
Q_{gs}	Gate Charge Gate to Source			1.9		nC
$Q_{g(th)}$	Gate Charge at Vth			1.0		nC
Q_{oss}	Output Charge	V_{DS} = 15V, V_{GS} = 0V		4.0		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 7A, R_G = 2Ω		7.8		ns
t_r	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			17		ns
t_f	Fall Time			2.9		ns
Diode Characteristics(1)						
V_{SD}	Diode Forward Voltage	I_{SD} = 7A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 15V, I_F = 7A, di/dt = 300A/µs		5.3		nC
t_{rr}	Reverse Recovery Time			12.2		ns

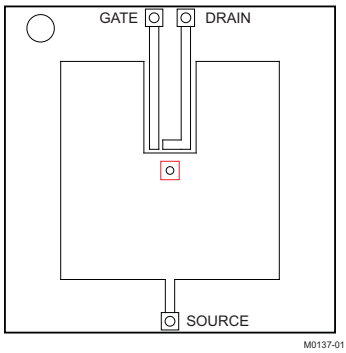
(1) All Dynamic and Diode Characteristics were measured with respect to one of the two drains, with the other left floating.

THERMAL CHARACTERISTICS

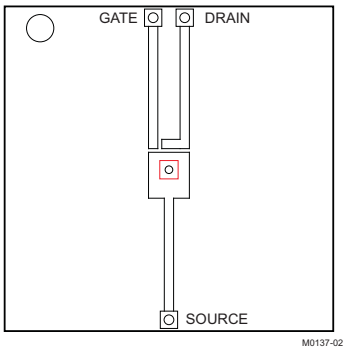
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			4.2	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)(2)			63	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 63°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 165°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

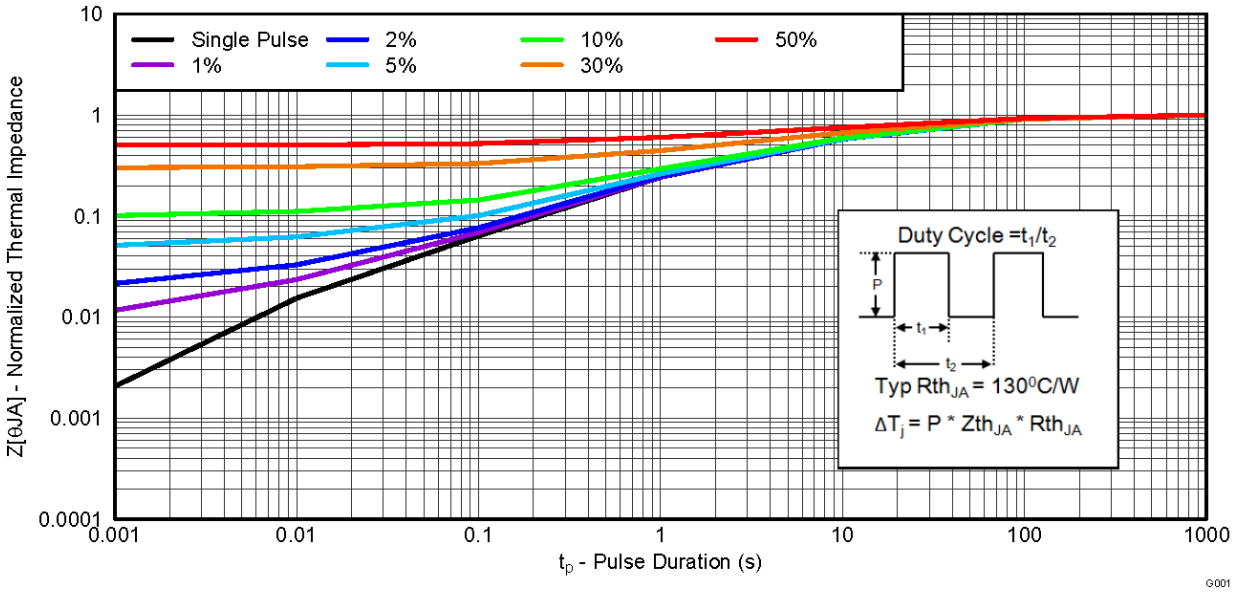


Figure 1. Transient Thermal Impedance

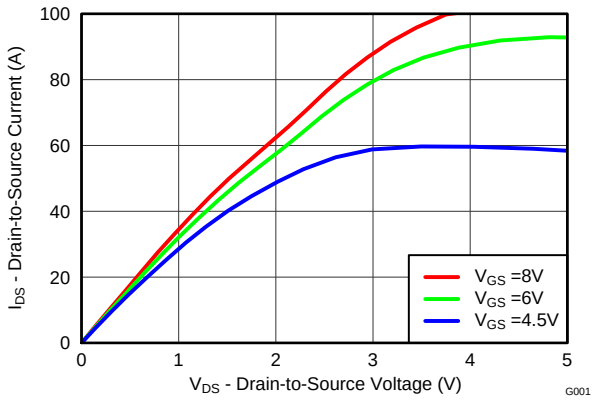


Figure 2. Saturation Characteristics

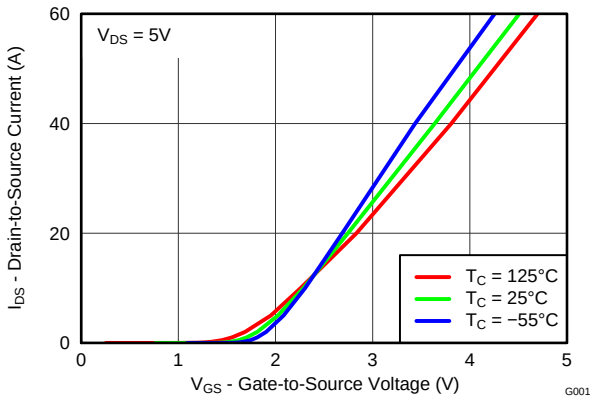


Figure 3. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

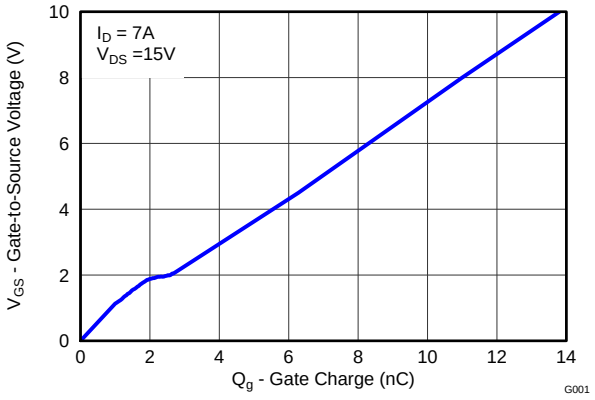


Figure 4. Gate Charge

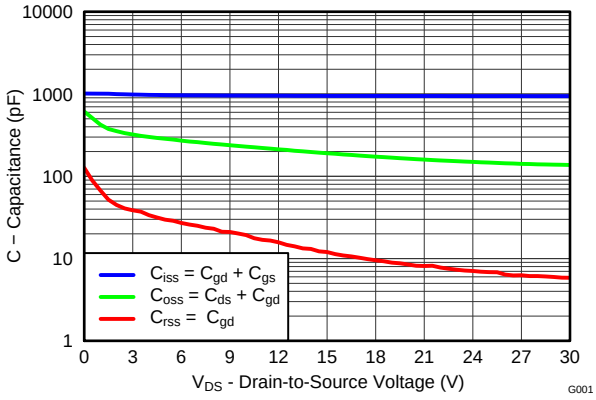


Figure 5. Capacitance

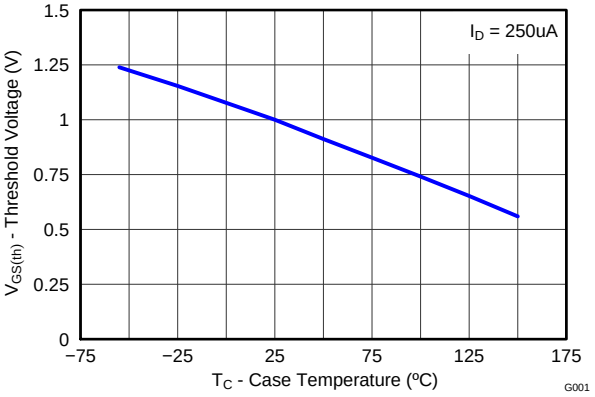


Figure 6. Threshold Voltage vs. Temperature

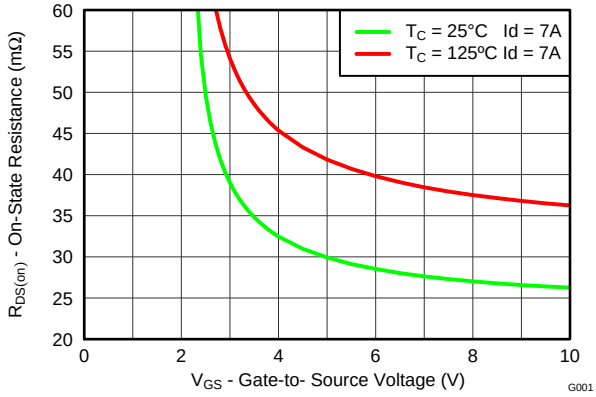


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

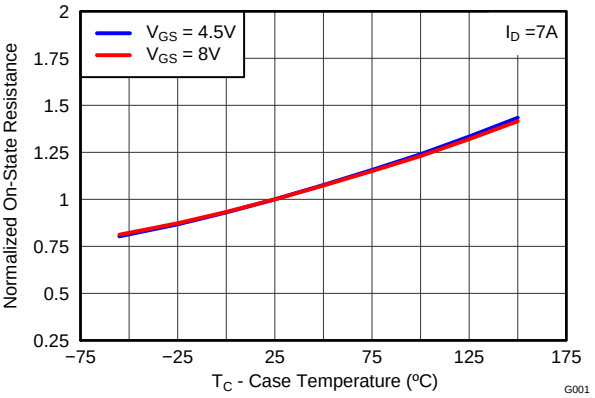


Figure 8. Normalized On-State Resistance vs. Temperature

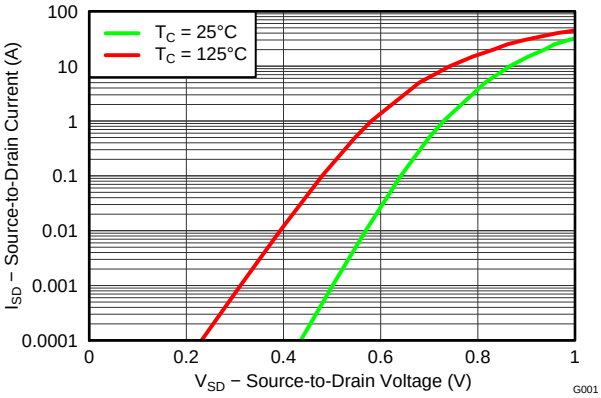


Figure 9. Typical Diode Forward Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

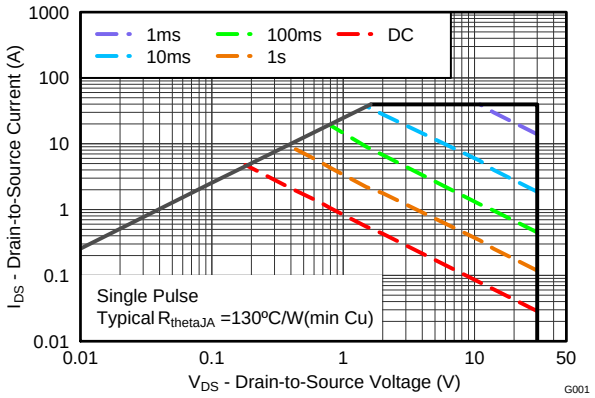


Figure 10. Maximum Safe Operating Area

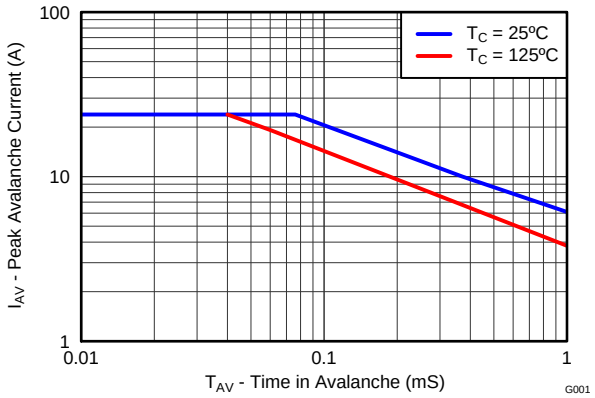


Figure 11. Single Pulse Unclamped Inductive Switching

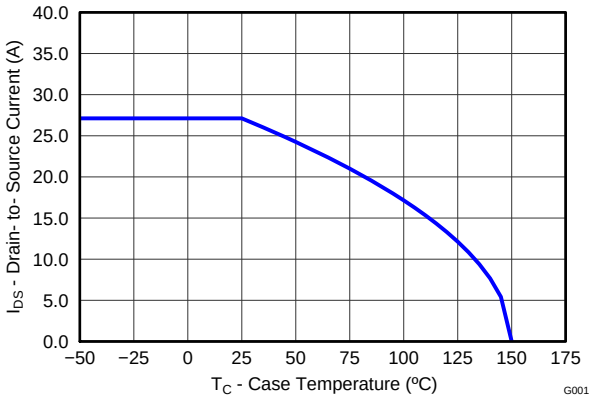
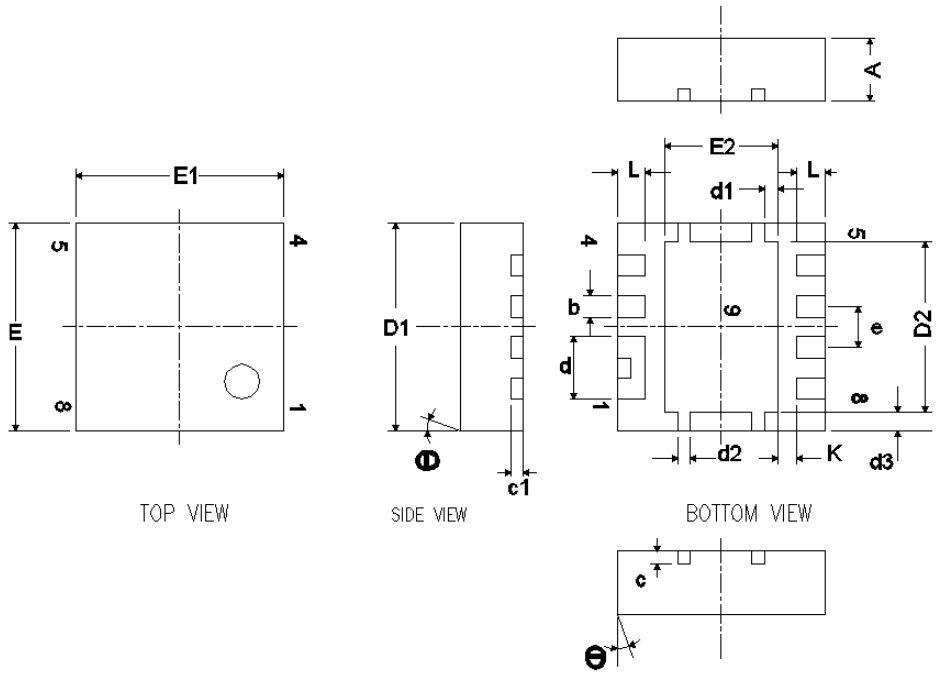


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q3E Package Dimensions

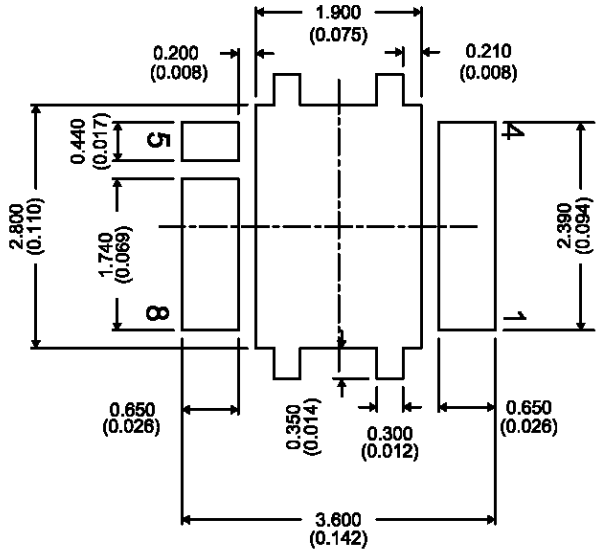


DIM	MILLIMETERS	
	MIN	MAX
A	0.850	1.050
b	0.280	0.400
c	0.150	0.250
c1	0.150	0.250
d	0.940	1.040
d1	0.160	0.260
d2	0.150	0.250
d3	0.250	0.350
D1	3.200	3.400
D2	2.650	2.750
E	3.200	3.400
E1	3.200	3.400
E2	1.750	1.850
e	0.650 TYP	
L	0.400	0.500
θ	0°	-
K	0.300 Typ	

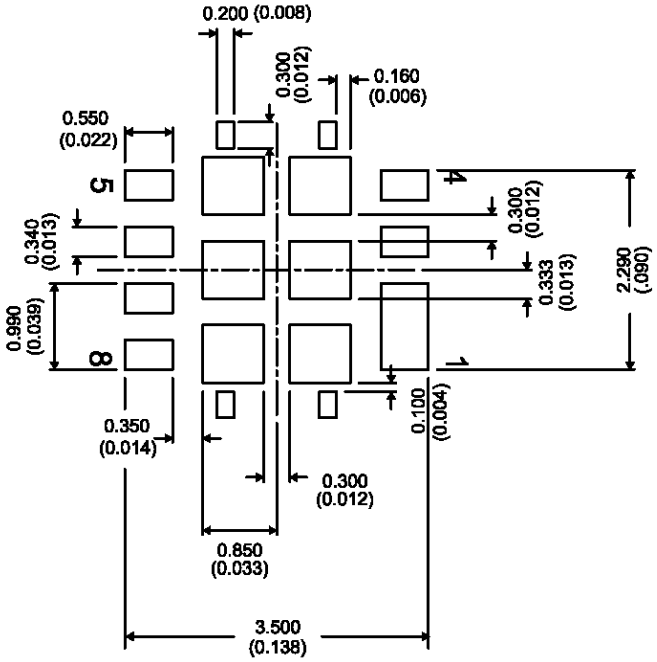
Notes:

1. Pin 1-4: Drain 1
2. Pin 5: Gate
3. Pin 6-8: Drain 2
4. Pin 9: Source

Recommended PCB Pattern

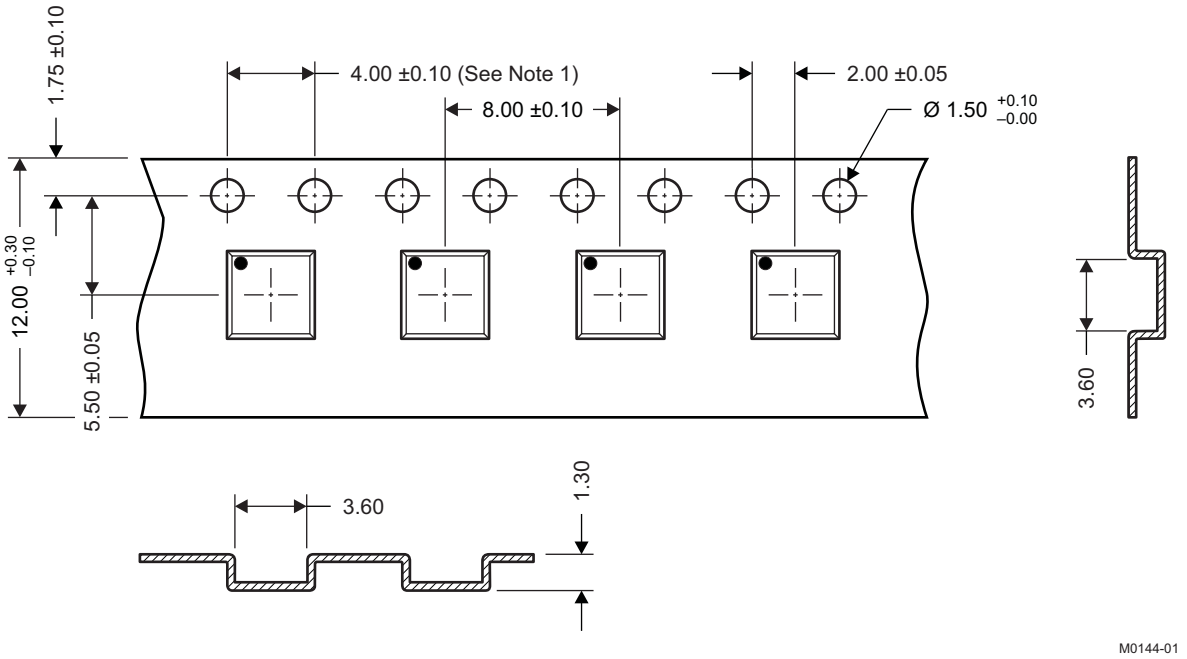


Recommended Stencil Opening



For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q3E Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material:black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ±0.05mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD87312Q3E	Active	Production	VSON (DPA) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87312E
CSD87312Q3E.B	Active	Production	VSON (DPA) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87312E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

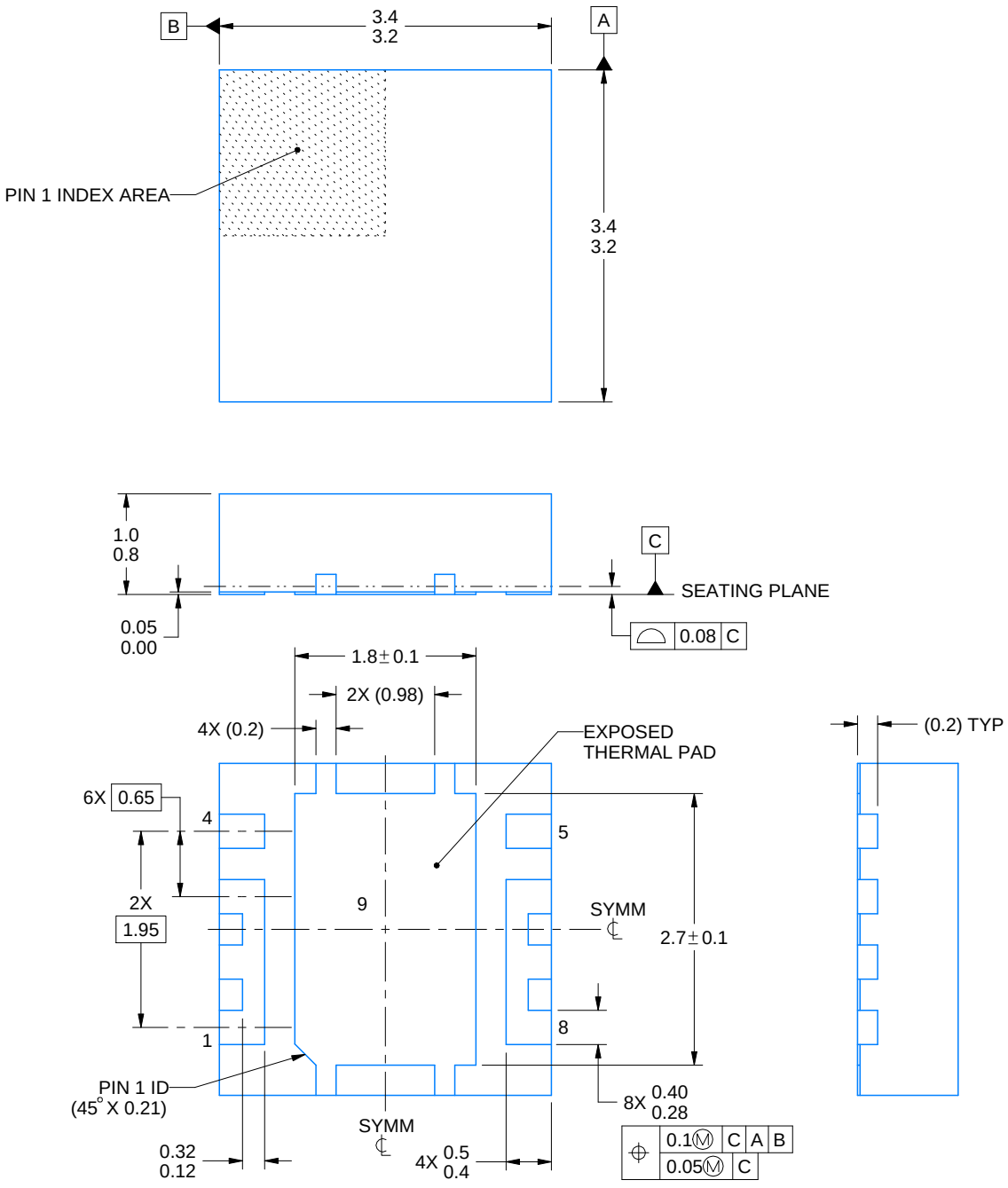
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DPA0008A

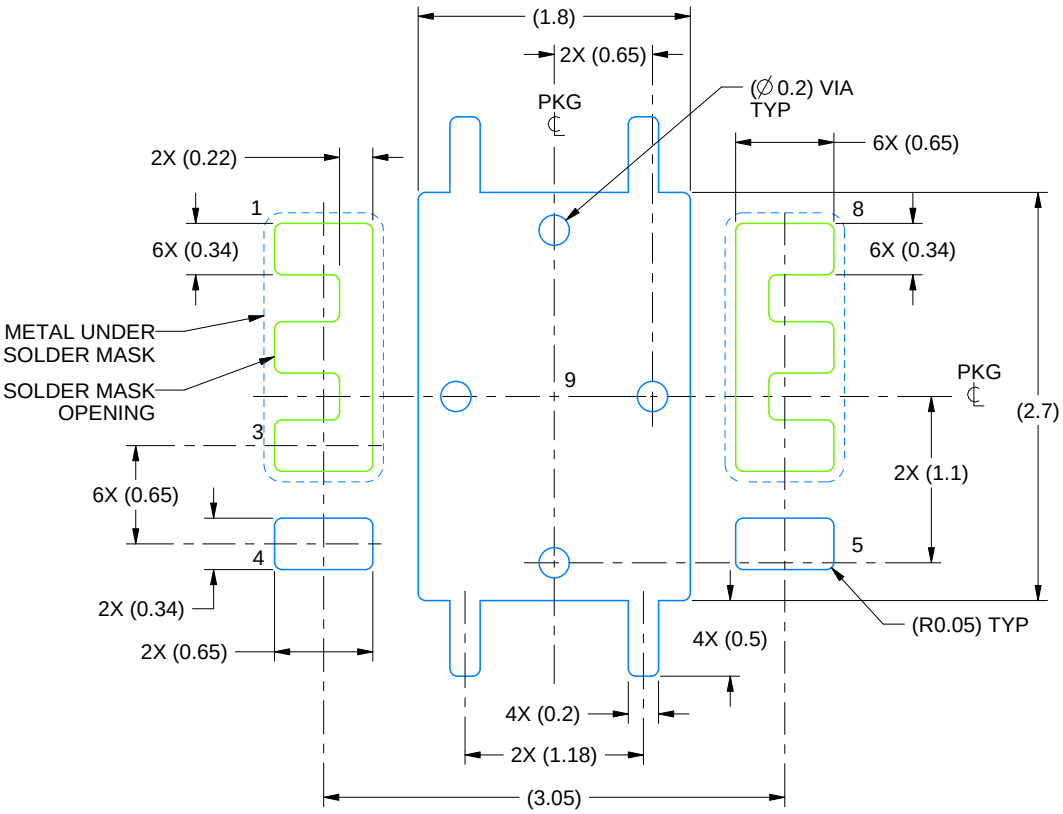
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

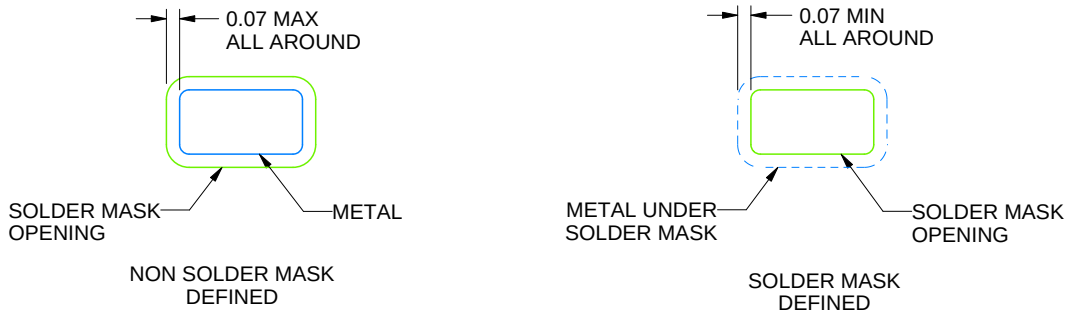


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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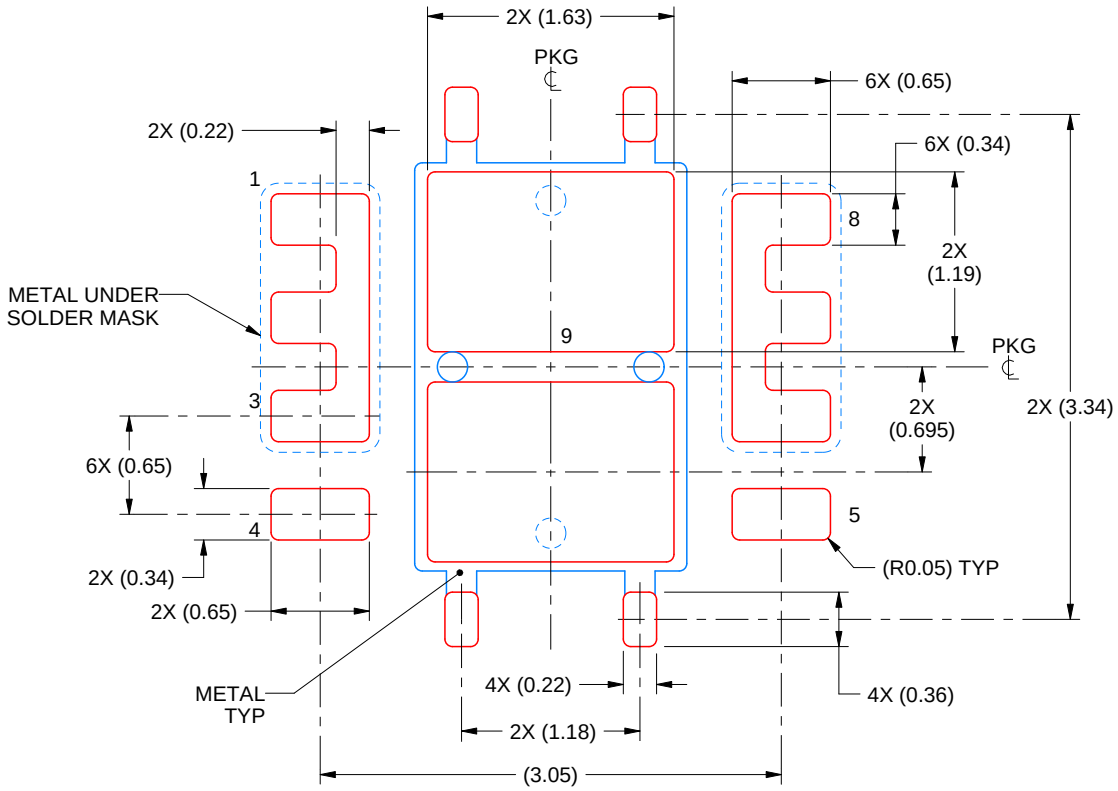
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4220449/A 07/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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