CSD25501F3 –20V P 沟道 FemtoFET™ MOSFET

1 特性

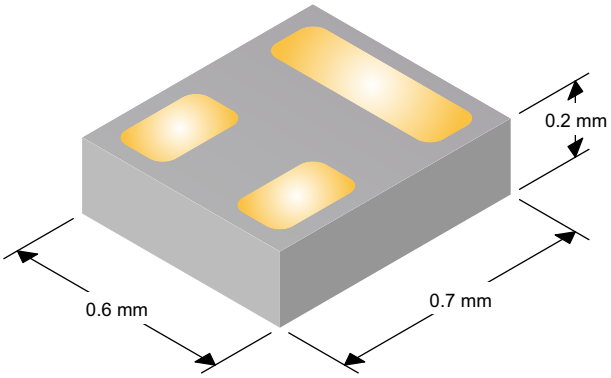
- 低导通电阻
- 超低 Q_g 和 Q_{gd}
- 超小尺寸
  - 0.7mm × 0.6mm
- 薄型封装
  - 最大厚度为 0.22mm
- 集成型 ESD 保护二极管
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 电池应用
- 手持式和移动类应用

3 说明

此 –20V、64mΩ P 沟道 FemtoFET™ MOSFET 经过设计和优化，能够更大限度地减小在许多手持式和移动应用中占用的空间。这项技术能够在替代标准小信号 MOSFET 的同时大幅减小封装尺寸。集成的 10kΩ 钳位电阻器 (R_C) 可根据占空比让栅极电压 (V_{GS}) 高于最大内部栅极氧化值 –6V。通过二极管的栅极泄漏 (I_{GSS}) 随着 V_{GS} 增加到高于 –6V 而增加。



典型器件尺寸

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	1.02		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.09		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -1.8V	120	mΩ
		V_{GS} = -2.5V	86	
		V_{GS} = -4.5V	64	
$V_{GS(th)}$	阈值电压	-0.75		V

器件信息

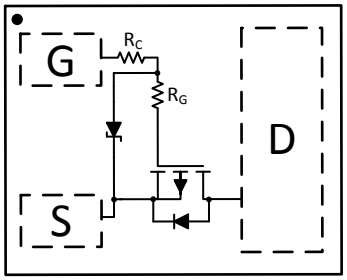
器件(1)	数量	介质	封装	运输
CSD25501F3	3000	7 英寸卷带	Femto 0.73mm × 0.64mm 基板栅格阵列 (LGA)	卷带包装
CSD25501F3T	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C（除非另外注明）		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-20	V
I_D	持续漏极电流(1)	-3.6	A
I_{DM}	脉冲漏极电流(1) (2)	-13.6	A
P_D	功率耗散(1)	500	mW
$V_{(ESD)}$	人体放电模型 (HBM)	4000	V
	充电器件模型 (CDM)	2000	
T_J、T_{stg}	工作结温，贮存温度	-55 至 150	°C

(1) 安装在覆铜区域最小的 FR4 电路板上时的典型 $R_{\theta JA}$ = 255°C/W。
(2) 脉冲持续时间 ≤100 μs，占空比 ≤1%。



顶视图

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4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_{DS} = –250 μA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = –16V			–50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = –6V			–50	nA
		V_{DS} = 0V, V_{GS} = –16V			–1	mA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.45	–0.75	–1.05	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8V, I_{DS} = –0.1A		120	260	mΩ
		V_{GS} = –2.5V, I_{DS} = –0.4A		86	125	
		V_{GS} = –4.5V, I_{DS} = –0.4A		64	76	
g_{fs}	Transconductance	V_{DS} = –2V, I_{DS} = –0.4A		3.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = –10V, f = 100kHz		295	385	pF
C_{oss}	Output capacitance			70	91	pF
C_{rss}	Reverse transfer capacitance			4.1	5.3	pF
R_G	Series gate resistance			33		Ω
R_C	Series clamp resistance			10,000		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10V, I_{DS} = –0.4A		1.02	1.33	nC
Q_{gd}	Gate charge gate-to-drain			0.09		nC
Q_{gs}	Gate charge gate-to-source			0.45		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.36		nC
Q_{oss}	Output charge	V_{DS} = –10V, V_{GS} = 0V		1.8		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10V, V_{GS} = –4.5V, I_{DS} = –0.4A, R_G = 0Ω		474		ns
t_r	Rise time			428		ns
$t_{d(off)}$	Turnoff delay time			1154		ns
t_f	Fall time			945		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.4A, V_{GS} = 0V		–0.73	–0.95	V
Q_{rr}	Reverse recovery charge	V_{DS} = –10V, I_F = –0.4A, di/dt = 200A/μs		3.0		nC
t_{rr}	Reverse recovery time			7.4		ns

4.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	255	°C/W

(1) Device mounted on FR4 material with 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

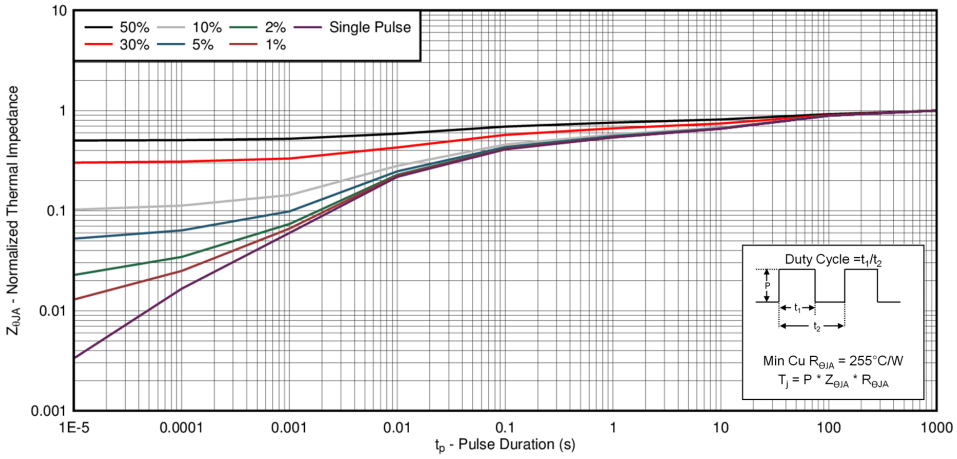


图 4-1. Transient Thermal Impedance

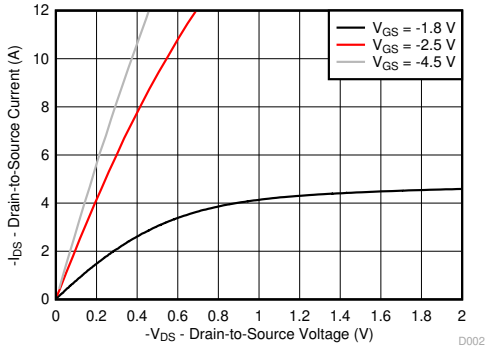
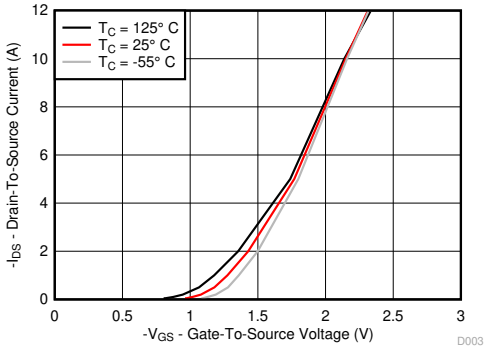
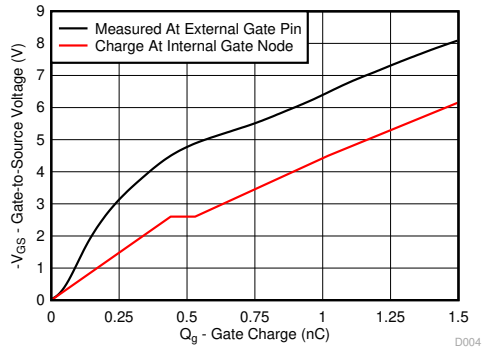


图 4-2. Saturation Characteristics



V_{DS} = – 5V

图 4-3. Transfer Characteristics



I_D = – 0.4A V_{DS} = – 10V

图 4-4. Gate Charge

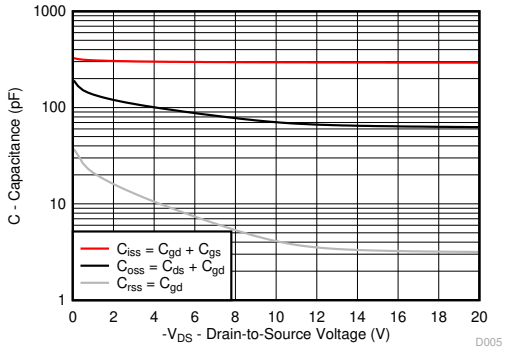
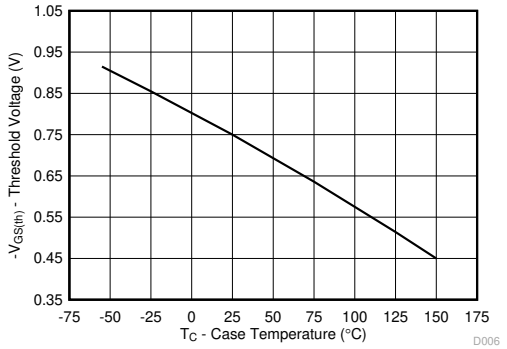


图 4-5. Capacitance

4.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = –250µA

图 4-6. Threshold Voltage vs Temperature

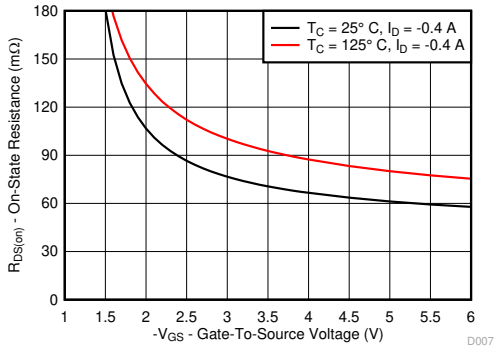
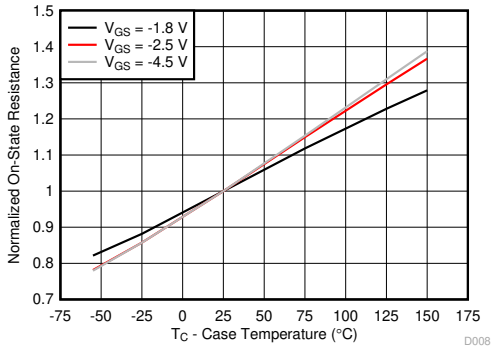


图 4-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –0.4A

图 4-8. Normalized On-State Resistance vs Temperature

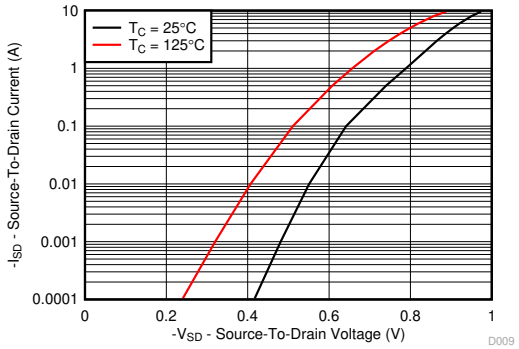
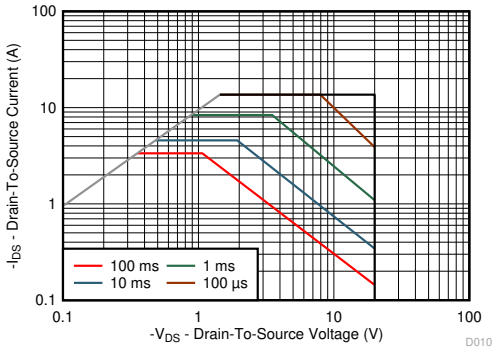
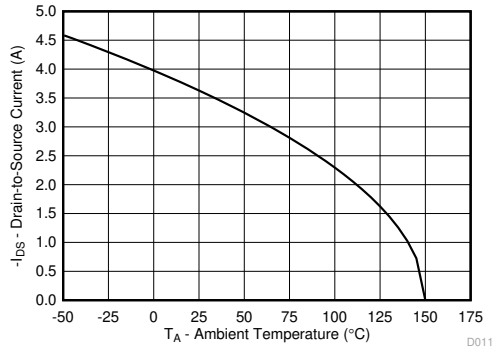


图 4-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 255°C/W

图 4-10. Maximum Safe Operating Area



Typical $R_{\theta JA}$ = 90°C/W

图 4-11. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.3 Trademarks

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5.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (October 2021) to Revision C (June 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

表 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25501F3	Active	Production	PICOSTAR (YJN) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	V
CSD25501F3.B	Active	Production	PICOSTAR (YJN) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	V
CSD25501F3T	Active	Production	PICOSTAR (YJN) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	V
CSD25501F3T.B	Active	Production	PICOSTAR (YJN) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

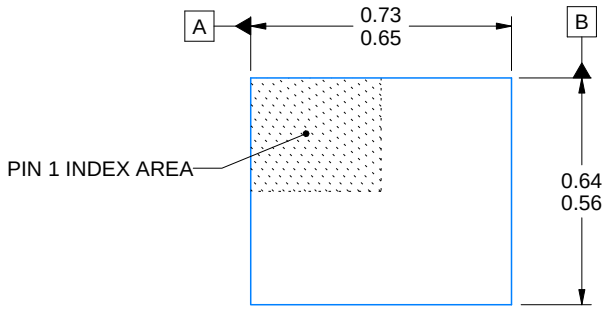
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

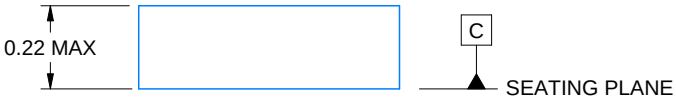
PACKAGE OUTLINE

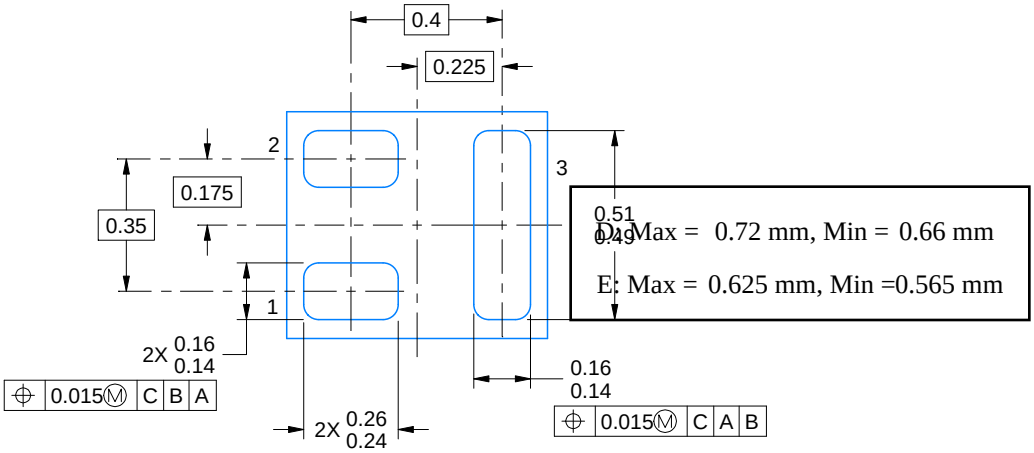
YJN0003A

PicoStar™ - 0.22 mm max height

PicoStar™





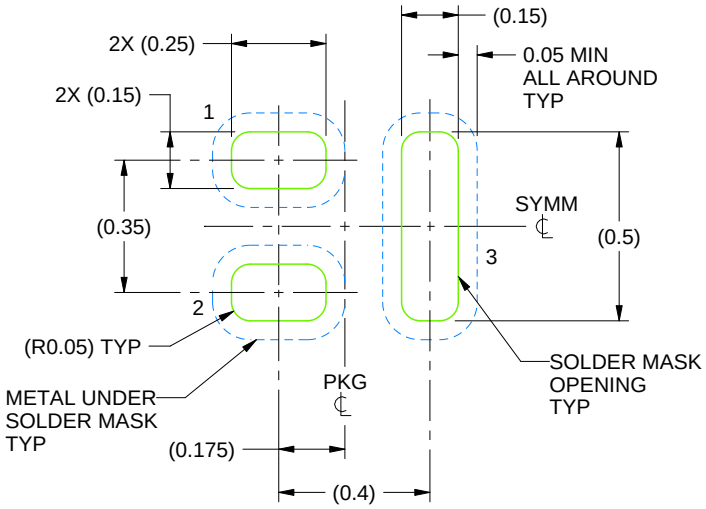


4223685/A 05/2017

NOTES:

PicoStar is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

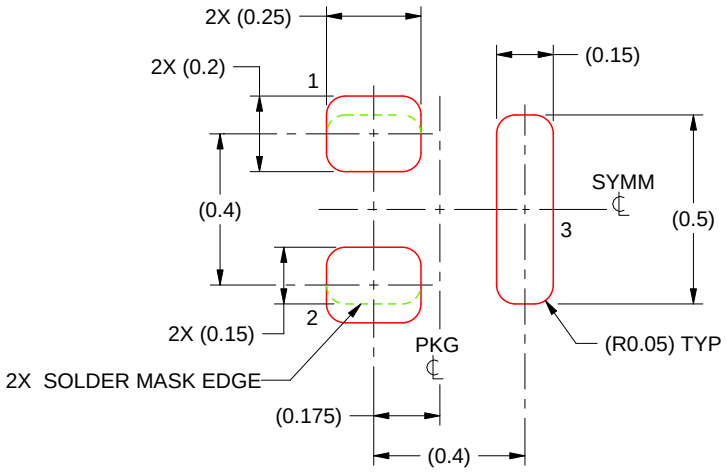


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4223685/A 05/2017

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4223685/A 05/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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