

CSD25483F4 20V P 沟道 FemtoFET™ MOSFET

1 特性

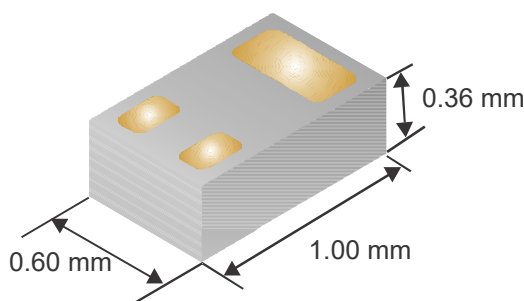
- 超低导通电阻
- 超低 Q_g 和 Q_{gd}
- 高漏极工作电流
- 超小封装尺寸 (0402 外壳尺寸)
 - $1.0\text{mm} \times 0.6\text{mm}$
- 超薄型封装
 - 最大高度: 0.36mm
- 集成型 ESD 保护二极管
 - 额定值 $> 4\text{kV}$ HBM
 - 额定值 $> 2\text{kV}$ CDM
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 电池应用
- 手持式和移动类应用

3 说明

此 $210\text{m}\Omega$ 、20V P 沟道 FemtoFET™ MOSFET 经过设计和优化, 能够最大限度地减小在许多手持式和移动应用中占用的空间。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小至少 60%。



典型器件尺寸

产品概要

$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	-20	V
Q_g	栅极电荷总量 (-4.5V)	959	pC
Q_{gd}	栅极电荷 (栅漏极)	161	pC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = -1.8\text{V}$	530 $\text{m}\Omega$
		$V_{GS} = -2.5\text{V}$	338 $\text{m}\Omega$
		$V_{GS} = -4.5\text{V}$	210 $\text{m}\Omega$
$V_{GS(th)}$	阈值电压	-0.95	V

订购信息⁽¹⁾

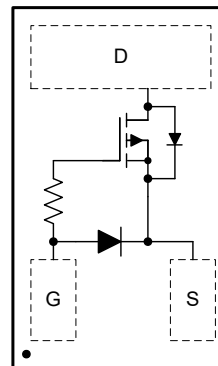
器件	数量	介质	封装	配送
CSD25483F4	3000	7 英寸卷带	Femto (0402)	卷带包装
CSD25483F4T	250		$1.0\text{mm} \times 0.6\text{mm}$ 基板栅格阵列 (LGA)	

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-12	V
I_D	持续漏极电流 ⁽¹⁾	-1.6	A
I_{DM}	脉冲漏极电流 ⁽²⁾	-6.5	A
I_G	持续栅极钳位电流	-35	mA
	脉冲栅极钳位电流 ⁽²⁾	-350	
P_D	功率耗散 ⁽¹⁾	500	mW
$V_{(ESD)}$	人体放电模型 (HBM)	4	kV
	充电器件模型 (CDM)	2	kV
T_J 、 T_{stg}	运行结温和贮存温度范围	-55 至 150	$^\circ\text{C}$

- (1) $R_{\theta JA} = 85^\circ\text{C/W}$ (0.06 英寸 (1.52mm) 厚 FR4 PCB 上 1 平方英寸 (6.45cm²) 2oz. (0.071mm) 厚的铜焊盘上的典型值)。
- (2) 脉冲持续时间 $\leq 300 \mu\text{s}$, 占空比 $\leq 2\%$



顶视图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (October 2021) to Revision F (January 2022)	Page
• 将特性中的最大高度从“0.35mm”更改为“0.36mm”	1
• 将典型器件尺寸的高度尺寸从“0.35mm”更改为“0.36mm”	1
• Changed maximum height dimension from "0.35 mm" to "0.36 mm" in <i>Mechanical Dimensions</i>	7
Changes from Revision D (October 2014) to Revision E (October 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Added footnote with link to support document.....	8
Changes from Revision C (July 2014) to Revision D (October 2014)	Page
• Corrected timing V_{DS} to read - 10 V	3
Changes from Revision B (February 2014) to Revision C (July 2014)	Page
• Corrected capacitance units to read pF in 图 5-5	4
Changes from Revision A (December 2013) to Revision B (February 2014)	Page
• 更新了特性中的“无铅且无卤素”	1
• 添加了 I_G 参数.....	1
• Lowered I_{DSS} limit.....	3
• Lowered I_{GSS} limit.....	3
Changes from Revision * (October 2013) to Revision A (December 2013)	Page
• 更正了电阻值的拼写错误.....	1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _{DS} = - 250 μ A	- 20			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = - 16 V	- 100			nA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = - 12 V	- 50			nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = - 250 μ A	- 0.70	- 0.95	- 1.2	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = - 1.8 V, I _{DS} = - 0.1 A		530	1070	mΩ
		V _{GS} = - 2.5 V, I _{DS} = - 0.5 A		338	390	mΩ
		V _{GS} = - 4.5 V, I _{DS} = - 0.5 A		210	245	mΩ
		V _{GS} = - 8 V, I _{DS} = - 0.5 A		175	205	mΩ
g _{fs}	Transconductance	V _{DS} = - 10 V, I _{DS} = - 0.5 A		1.4		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = - 10 V, f = 1 MHz		198		pF
C _{oss}	Output Capacitance			82		pF
C _{rss}	Reverse Transfer Capacitance			5.8		pF
R _G	Series Gate Resistance			20		Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = - 10 V, I _{DS} = - 0.5 A		959		pC
Q _{gd}	Gate Charge Gate-to-Drain			160		pC
Q _{gs}	Gate Charge Gate-to-Source			252		pC
Q _{g(th)}	Gate Charge at V _{th}			122		pC
Q _{oss}	Output Charge	V _{DS} = - 10 V, V _{GS} = 0 V		1081		pC
t _{d(on)}	Turn On Delay Time	V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _{DS} = - 0.5 A, R _G = 2 Ω		4.3		ns
t _r	Rise Time			3.7		ns
t _{d(off)}	Turn Off Delay Time			17.4		ns
t _f	Fall Time			7		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = - 0.5 A, V _{GS} = 0 V	- 0.75			V
Q _{rr}	Reverse Recovery Charge	V _{DS} = - 10 V, I _F = - 0.5 A, di/dt = 100 A/ μ s	1060			pC
t _{rr}	Reverse Recovery Time		7.5			ns

5.2 Thermal Information

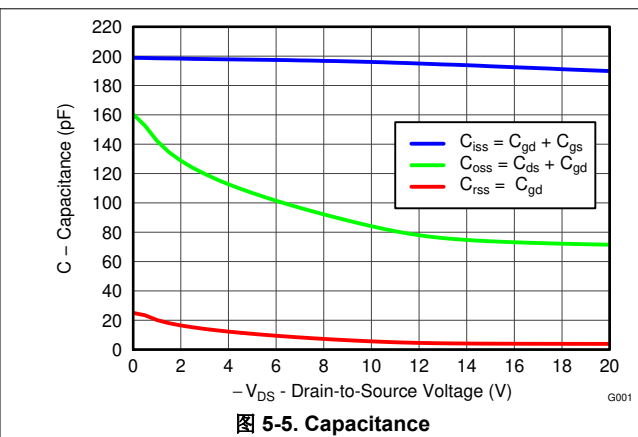
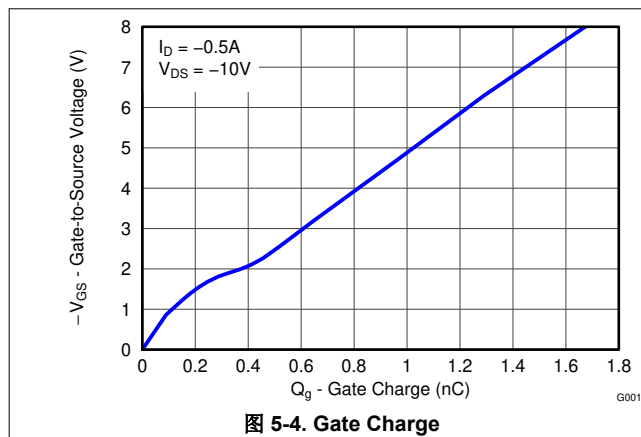
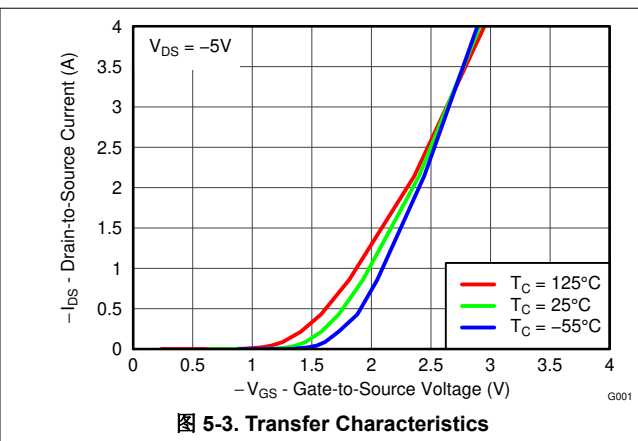
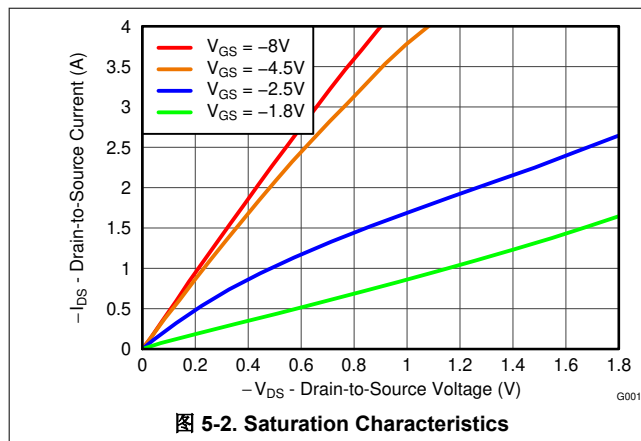
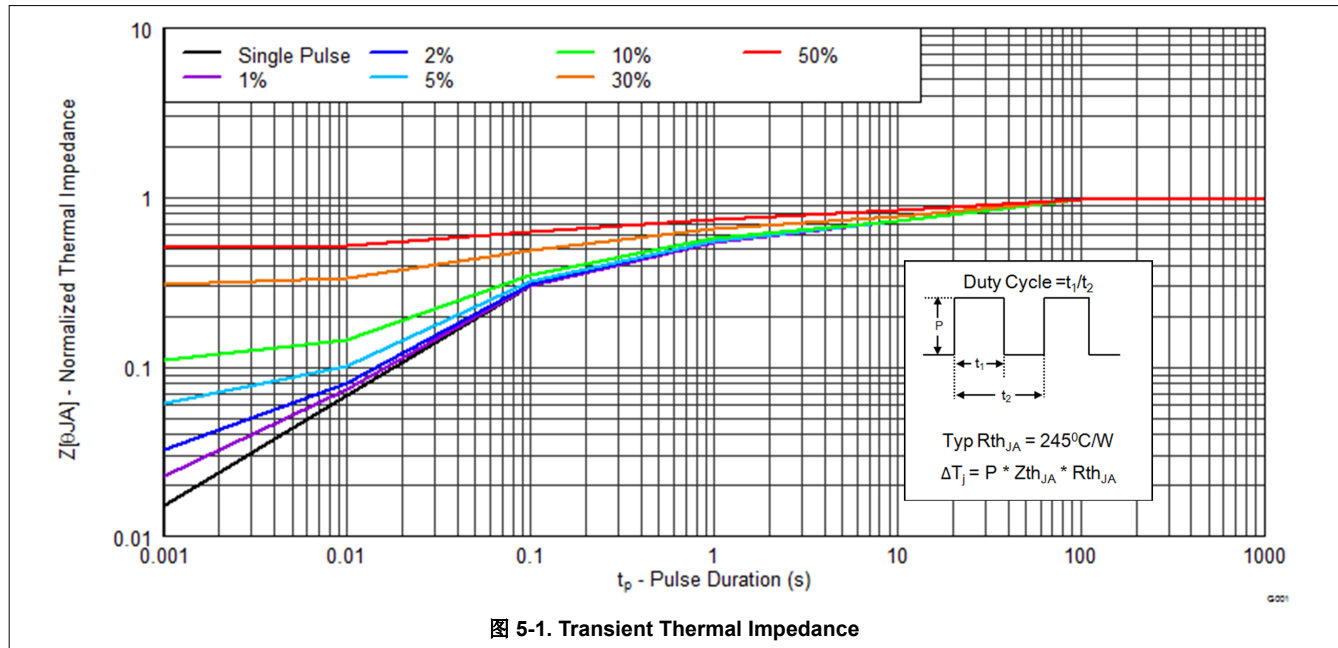
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾	85	°C/W
	Junction-to-Ambient Thermal Resistance ⁽²⁾	245	

- (1) Device mounted on FR4 material with 1-inch² (6.45 cm²), 2-oz. (0.071-mm thick) Cu.
 (2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



5.3 Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

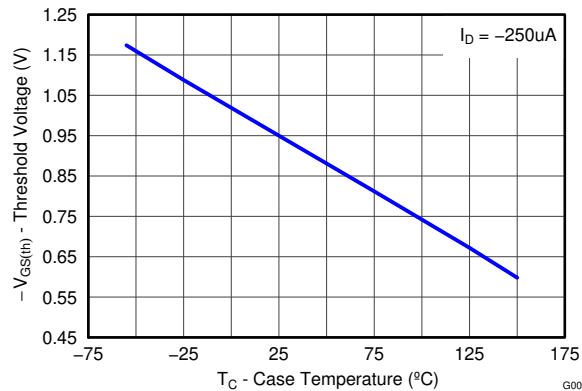


图 5-6. Threshold Voltage vs Temperature

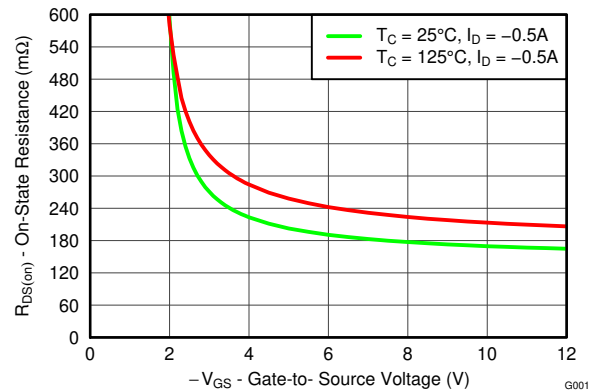


图 5-7. On-State Resistance vs Gate-to-Source Voltage

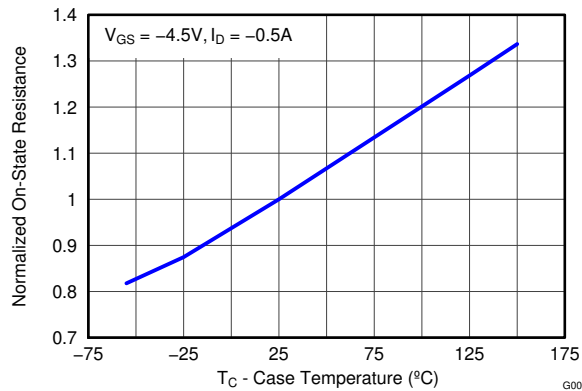


图 5-8. Normalized On-State Resistance vs Temperature

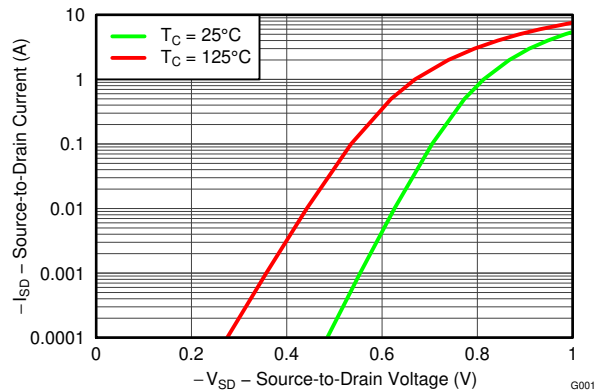


图 5-9. Typical Diode Forward Voltage

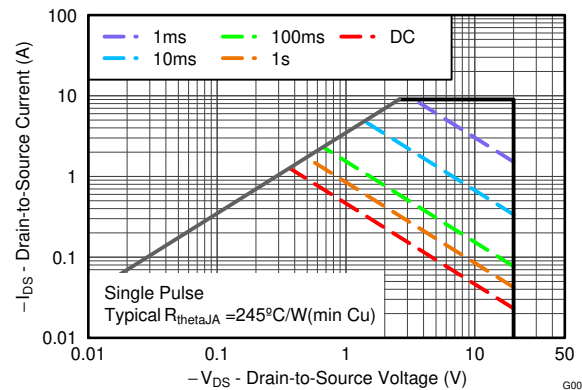


图 5-10. Maximum Safe Operating Area

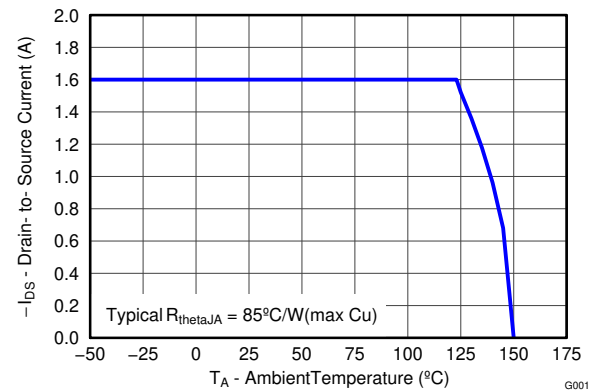


图 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

FemtoFET™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

6.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.3 术语表

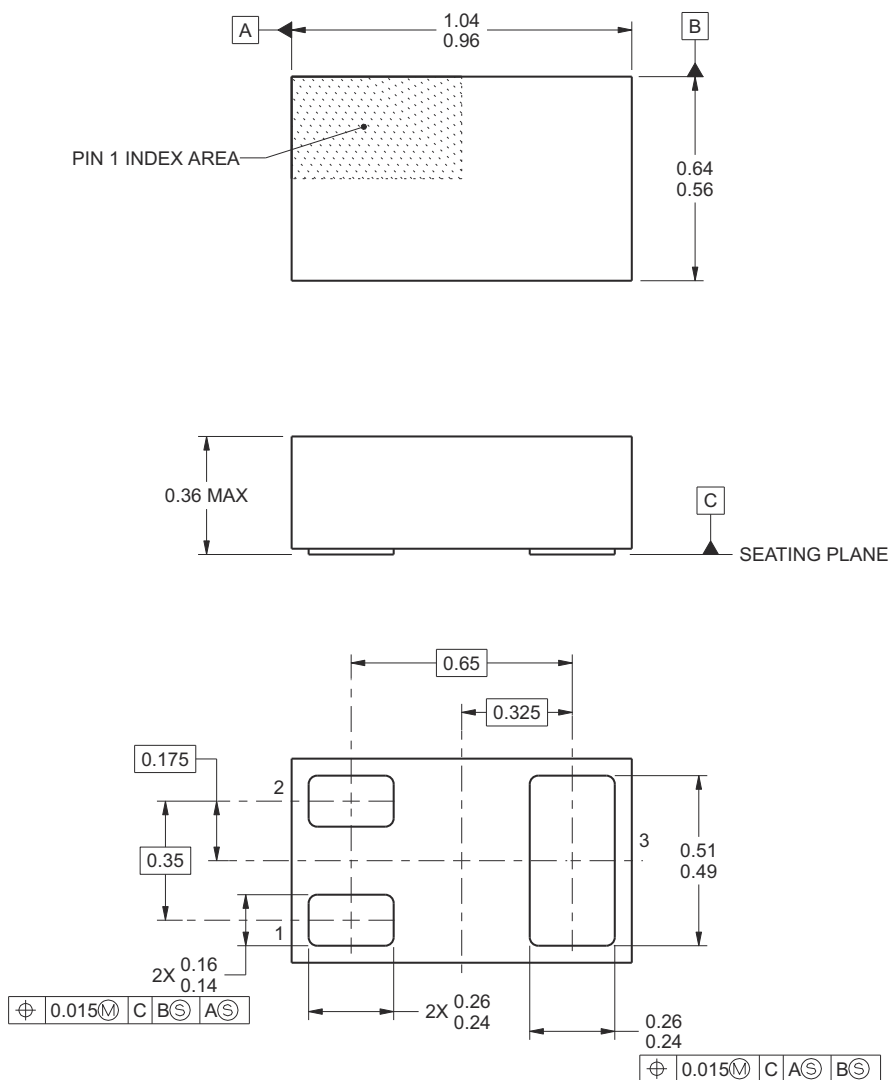
TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical Data

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

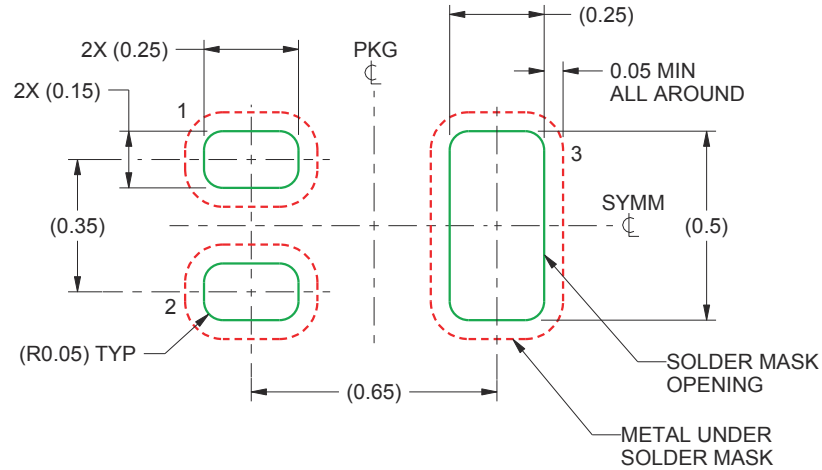


- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a PB-free solder land design.

Pin Configuration

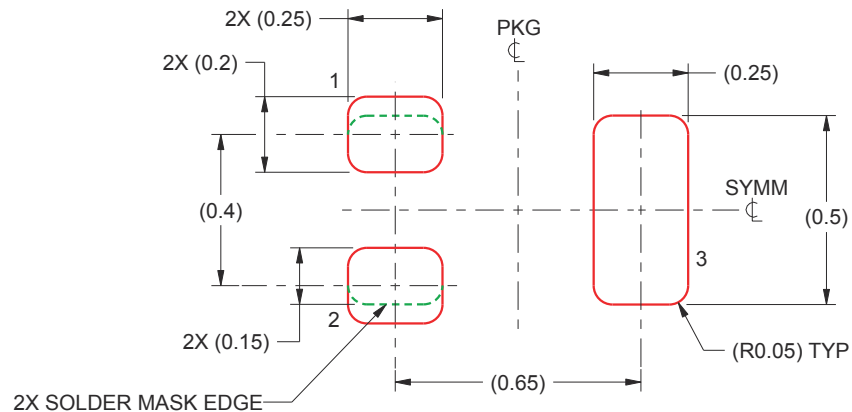
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



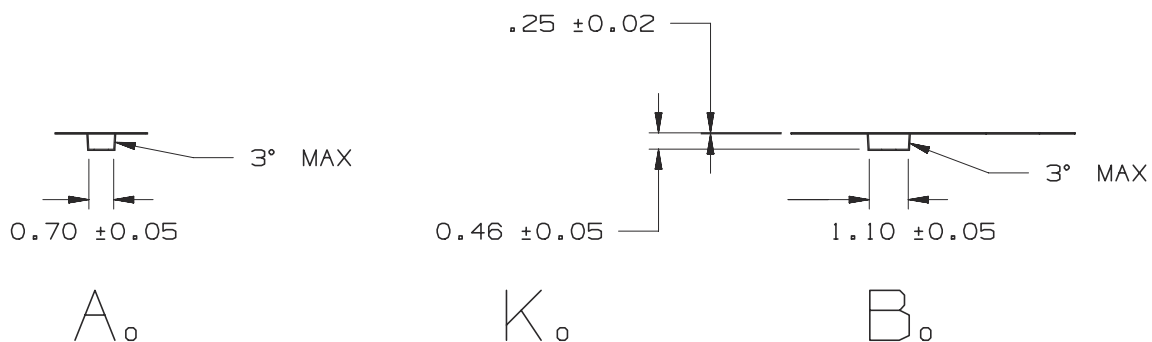
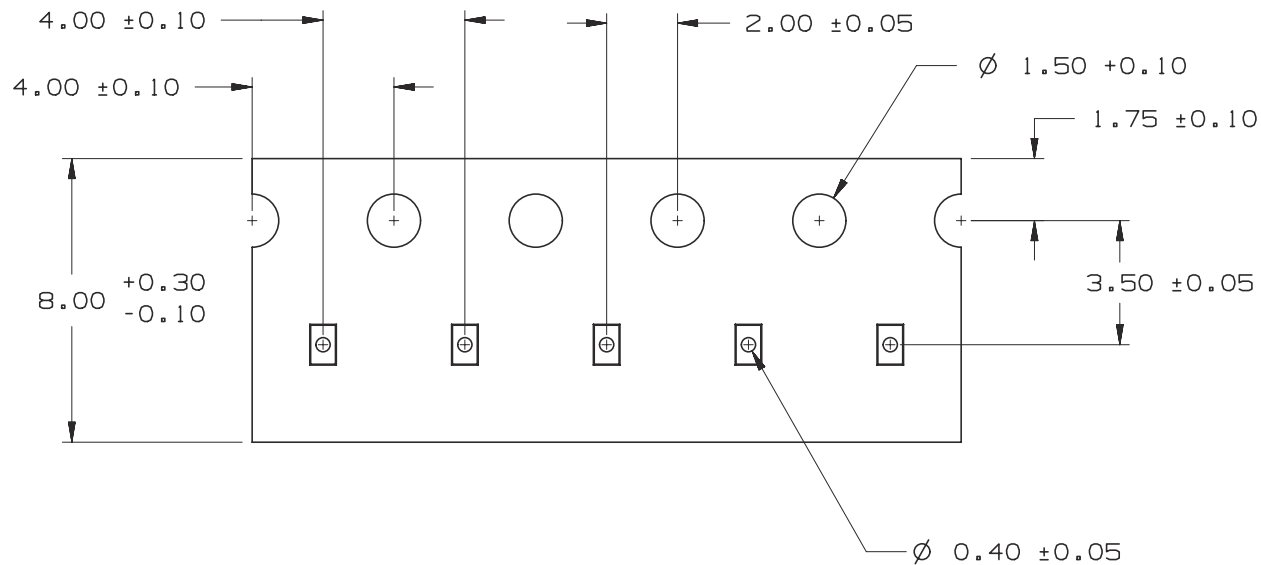
- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

7.4 CSD25483F4 Embossed Carrier Tape Dimensions



- A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25483F4	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DR
CSD25483F4.B	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DR
CSD25483F4T	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DR
CSD25483F4T.B	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	DR

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25483F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD25483F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25483F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD25483F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

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