CSD25211W1015 P 沟道 NexFET™ 功率 MOSFET

1 特性

- 超低导通电阻
- 超低 Q_g 和 Q_{gd}
- 1.0mm × 1.5mm 小尺寸封装
- 超薄型，高 0.62mm
- 无铅
- 栅源电压钳位
- 栅极 ESD 保护 - 3kV
- 符合 RoHS
- 无卤素

2 应用

- 电池管理
- 负载开关
- 电池保护

3 说明

此器件设计用于在超薄且具有出色散热特性的超小外形尺寸封装内产生尽可能低的导通电阻和栅极电荷。

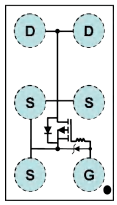


图 3-1. 顶视图

产品概要

T_A = 25°C 时测得，除非另外注明		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	3.4		nC
Q_{gd}	栅漏栅极电荷	0.2		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -2.5V	36	mΩ
		V_{GS} = -4.5V	27	mΩ
$V_{GS(th)}$	电压阈值	-0.8		V

订购信息

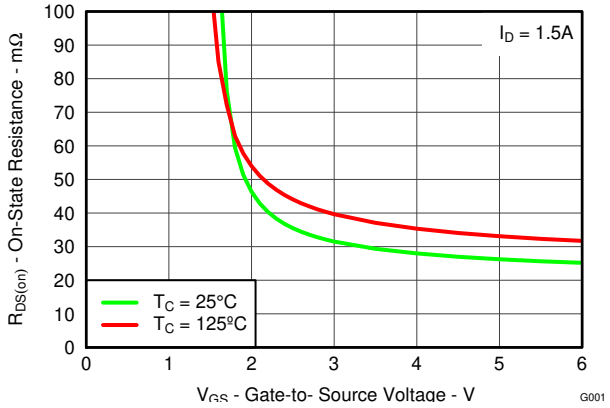
器件	封装	介质	数量	出货
CSD25211W1015	1 × 1.5 晶圆级封装	7 英寸卷带	3000	卷带包装

绝对最大额定值

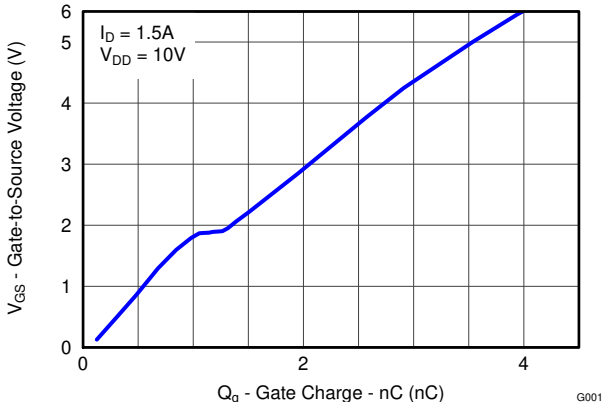
T_A = 25°C 时测得，除非另外注明		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流，T_A = 25°C(1)	-3.2	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	-9.5	A
I_G	持续栅极电流，T_A = 25°C	-0.5	A
	脉冲栅极电流	-7	A
P_D	功率耗散(1)	1	W
T_{STG}	储存温度范围	-55 至 150	°C
T_J	工作结温范围		

(1) 0.06 英寸厚 FR4 PCB 上采用 1 平方英寸、2 盎司铜焊盘时的 $R_{\theta JA}$ 典型值为 119°C/W

(2) 脉宽 ≤ 10 μs，占空比 ≤ 2%



$R_{DS(ON)}$与 V_{GS} 间的关系



栅极电荷

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (January 2014) to Revision B (September 2022)	Page
• 将“绝对最大额定值”表中的“持续漏极电流”更改为“持续栅极电流”	1
• 将“绝对最大额定值”表中的“脉冲漏极电流”更改为“脉冲栅极电流”	1

5 Electrical Characteristics

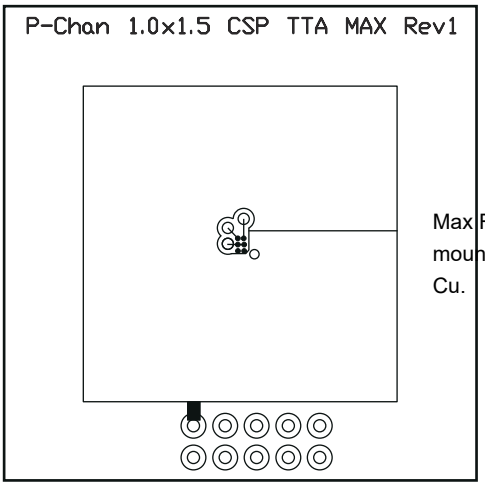
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = – 250 μA	– 20			V
BV_{GSS}	Gate-to-Source Voltage	V_{DS} = 0 V, I_G = – 250 μA	– 6.1		– 7.2	V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = – 16 V			– 1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = – 6 V			– 100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = – 250 μA	– 0.5	– 0.8	– 1.1	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = – 2.5 V, I_D = – 1.5 A		36	44	mΩ
		V_{GS} = – 4.5 V, I_D = – 1.5 A		27	33	mΩ
g_{fs}	Transconductance	V_{DS} = – 10 V, I_D = – 1.5 A		12		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = – 10 V, f = 1 MHz		475	570	pF
C_{OSS}	Output Capacitance			234	281	pF
C_{RSS}	Reverse Transfer Capacitance			10.5	13.1	pF
Q_g	Gate Charge Total (– 4.5 V)	V_{DS} = – 10 V, I_D = – 1.5 A		3.4	4.1	nC
Q_{gd}	Gate Charge Gate to Drain			0.2		nC
Q_{gs}	Gate Charge Gate to Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = – 10 V, V_{GS} = 0 V		3.8		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = – 10 V, V_{GS} = – 4.5 V, I_D = – 1.5 A R_G = 4 Ω		13.6		ns
t_r	Rise Time			8.8		ns
$t_{d(off)}$	Turn Off Delay Time			36.9		ns
t_f	Fall Time			14.2		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = – 1.5 A, V_{GS} = 0 V		– 0.8	– 1	V
Q_{rr}	Reverse Recovery Charge	V_{dd}= – 10 V, I_F = – 1.5 A, di/dt = 200 A/μs		6.9		nC
t_{rr}	Reverse Recovery Time			11.6		ns

6 Thermal Characteristics

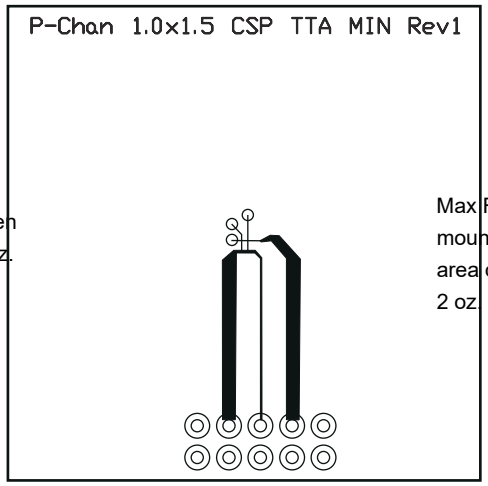
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			230	°C/W
	Thermal Resistance Junction to Ambient (1 in^2 Cu area)			149	°C/W



M0155-01

Max $R_{\theta JA}$ = 149°C/W when mounted on 1 $inch^2$ of 2 oz. Cu.



M0156-01

Max $R_{\theta JA}$ = 230°C/W when mounted on minimum pad area of 2 oz. Cu.

7 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

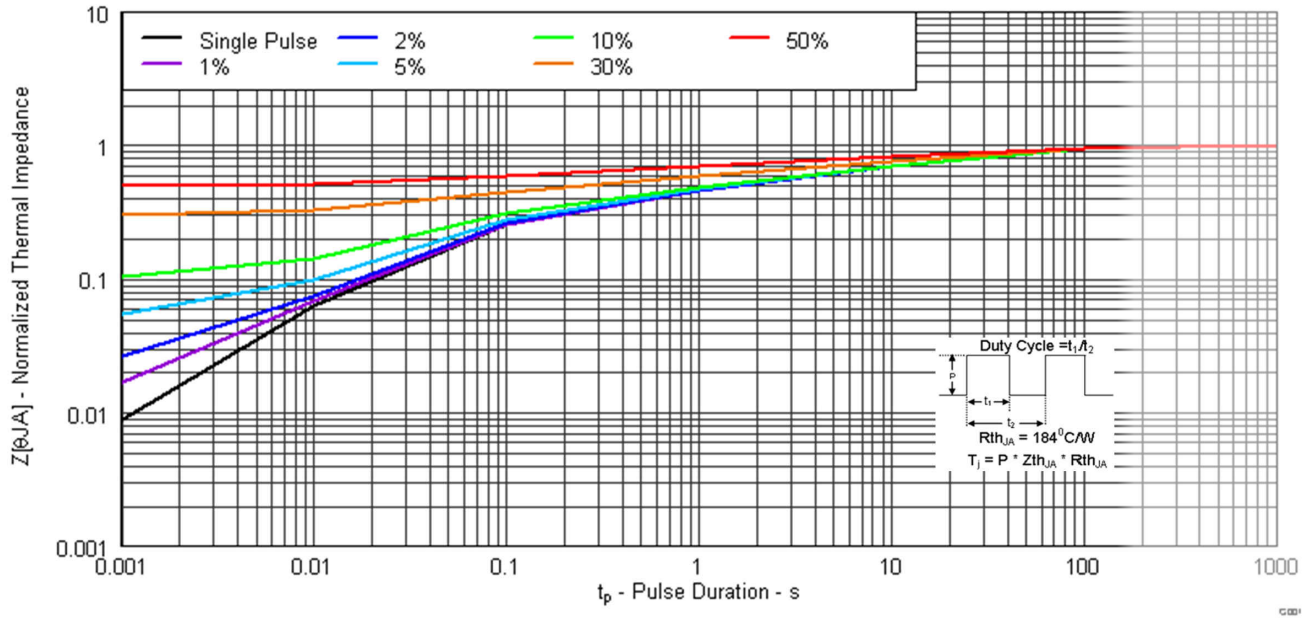


图 7-1. Transient Thermal Impedance

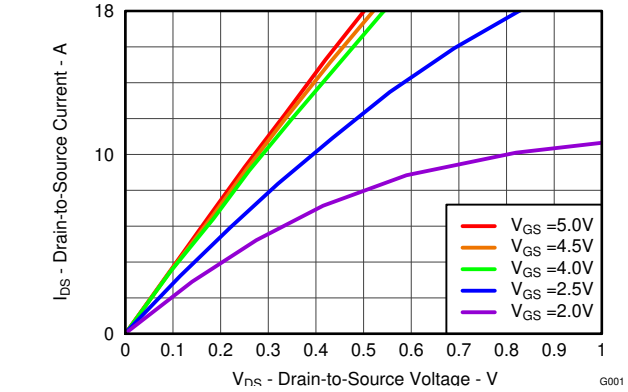


图 7-2. Saturation Characteristics

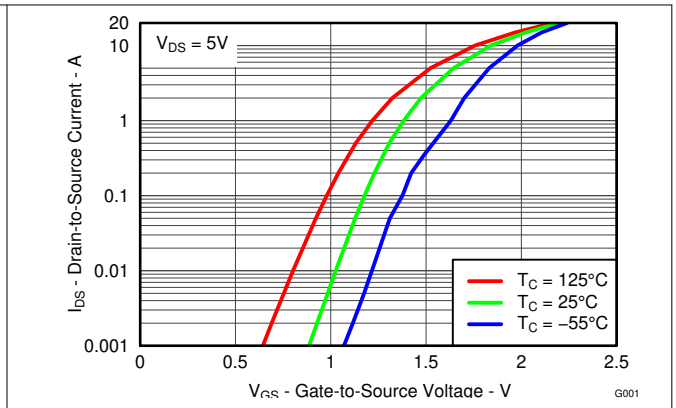


图 7-3. Transient Characteristics

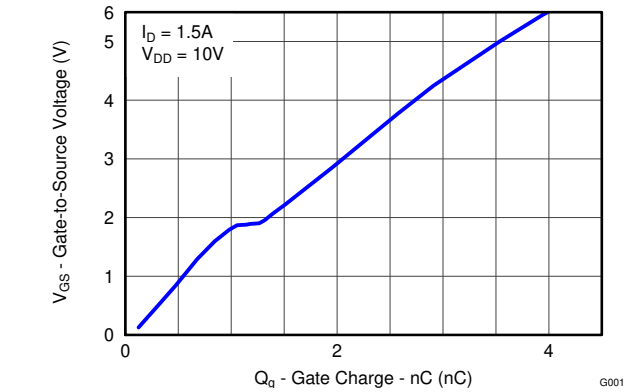


图 7-4. Gate Charge

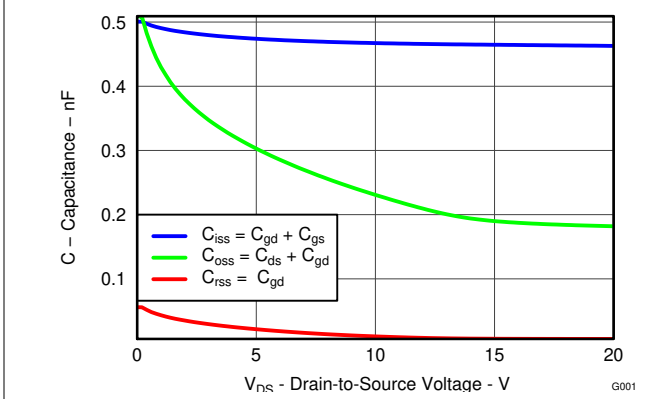


图 7-5. Capacitance

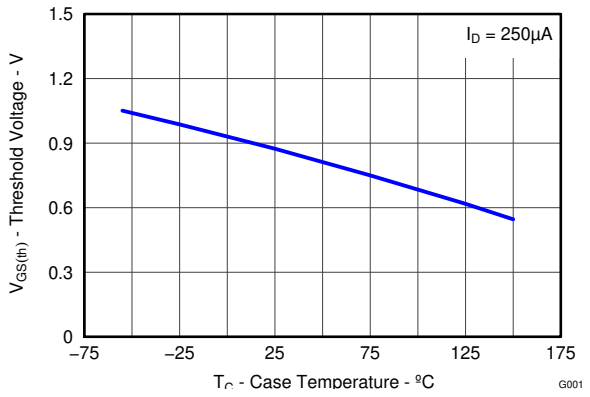


图 7-6. Threshold Voltage vs Temperature

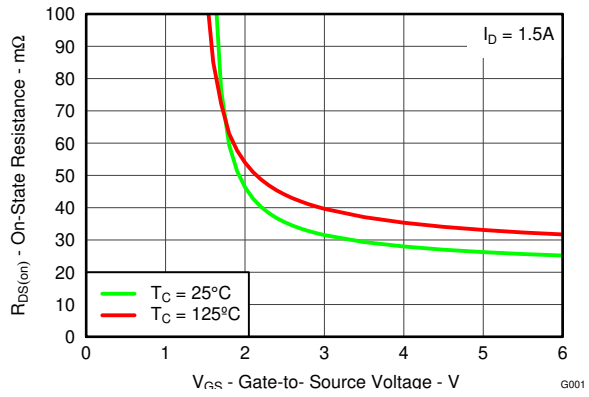


图 7-7. On Resistance vs Gate Voltage

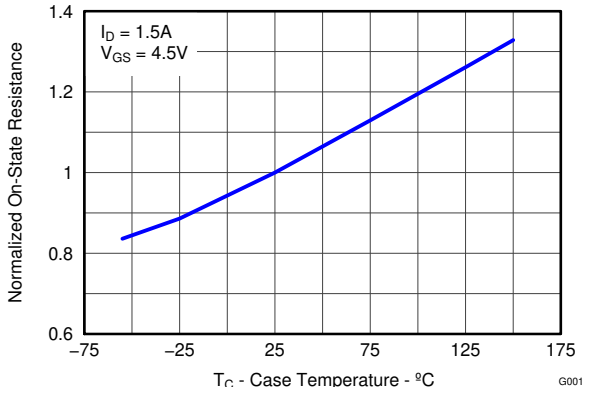


图 7-8. Normalized On Resistance vs Temperature

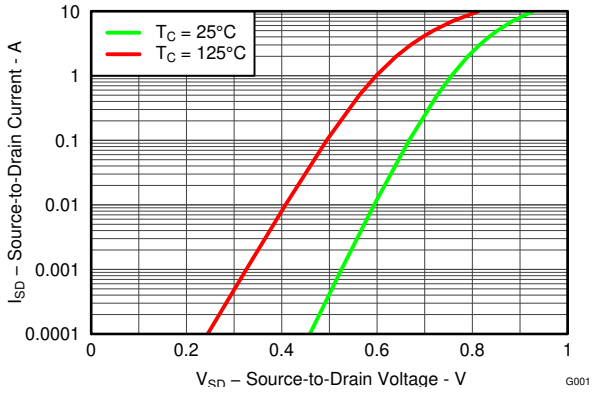


图 7-9. Typical Diode Forward Voltage

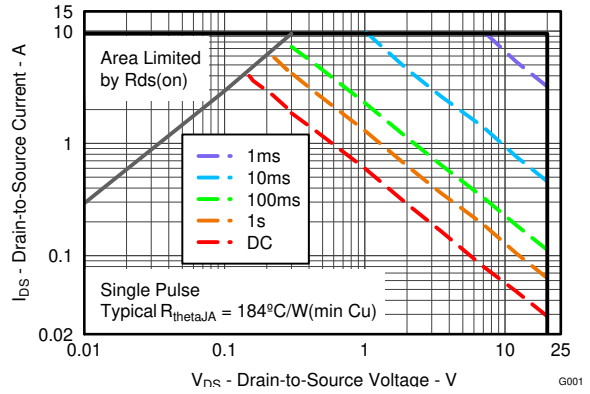


图 7-10. Maximum Safe Operating Area

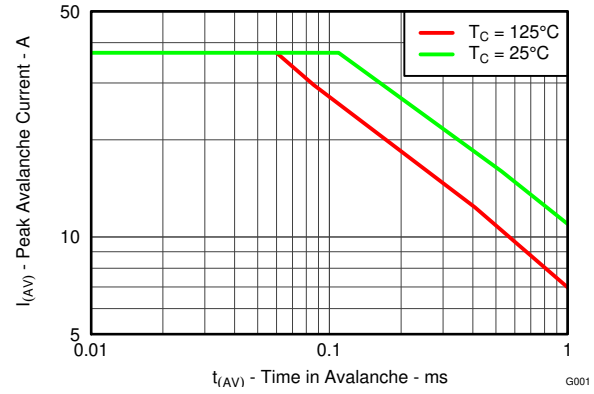


图 7-11. Single Pulse Unclamped Inductive Switching

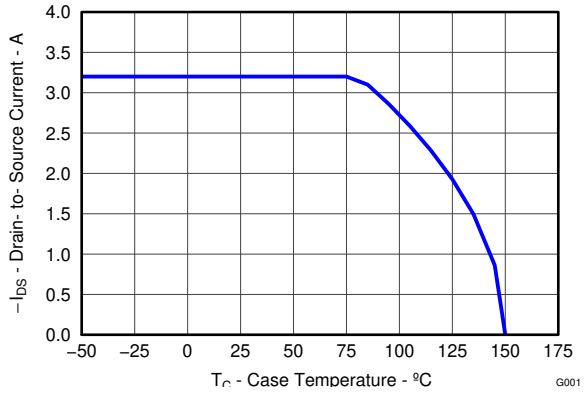
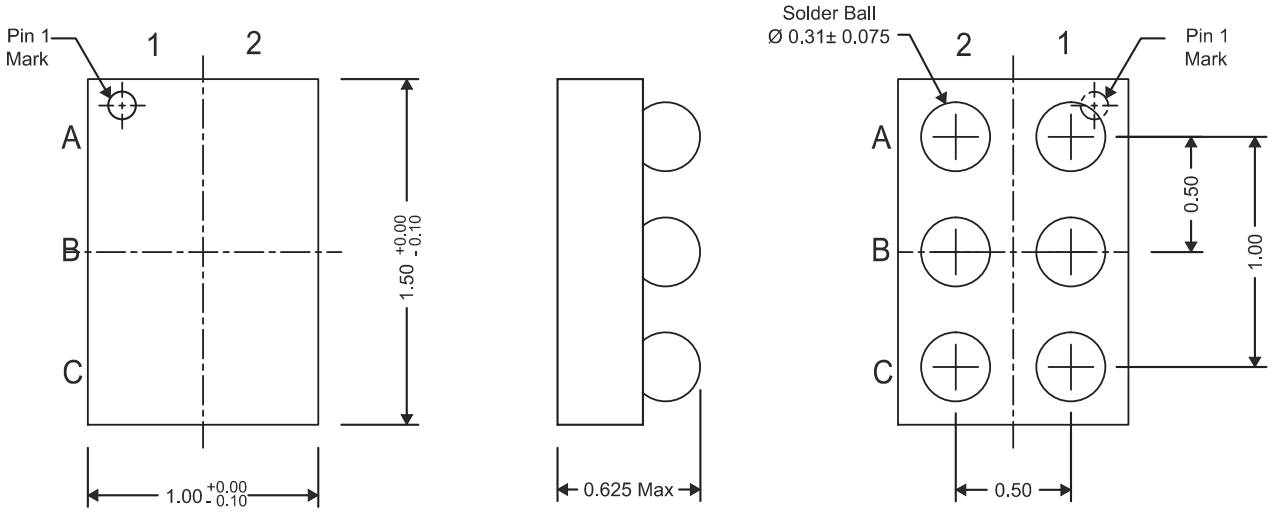
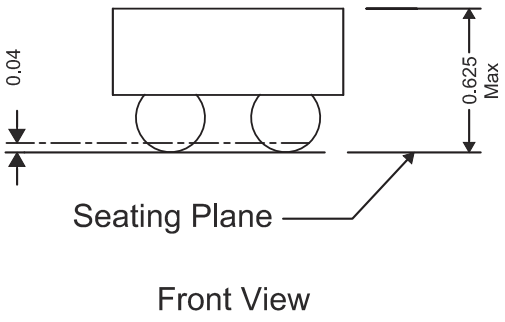


图 7-12. Maximum Drain Current vs Temperature

8 Mechanical Data

8.1 CSD25211W1015 Package Dimensions



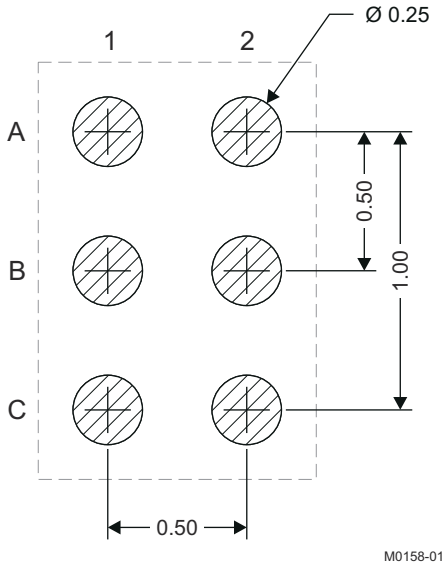


All dimensions are in mm (unless otherwise specified)

Pinout

POSITION	DESIGNATION
C1, C2	Drain
A1	Gate
A2, B1, B2	Source

8.2 Land Pattern Recommendation



All dimensions are in mm (unless otherwise specified)

9 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10 Device and Documentation Support

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25211W1015	Active	Production	DSBGA (YZC) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	25211
CSD25211W1015.B	Active	Production	DSBGA (YZC) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	25211

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

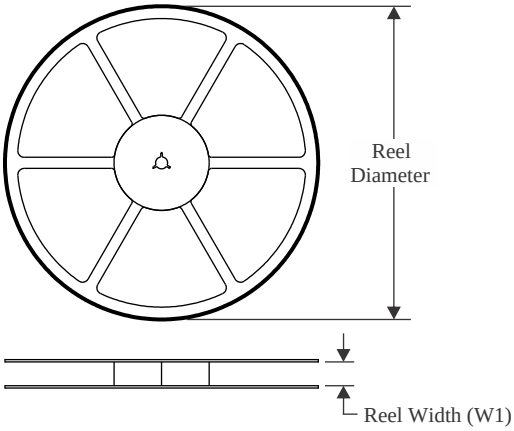
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

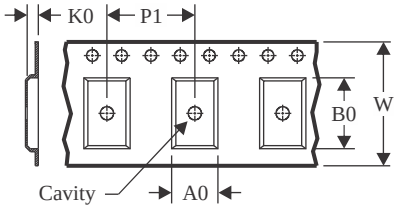
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

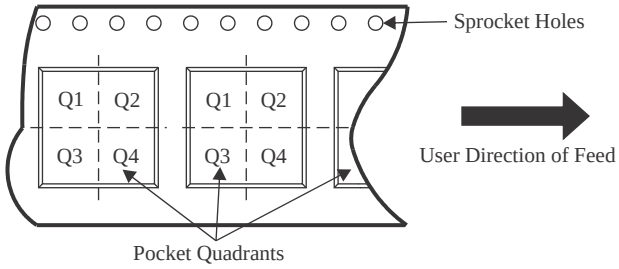


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

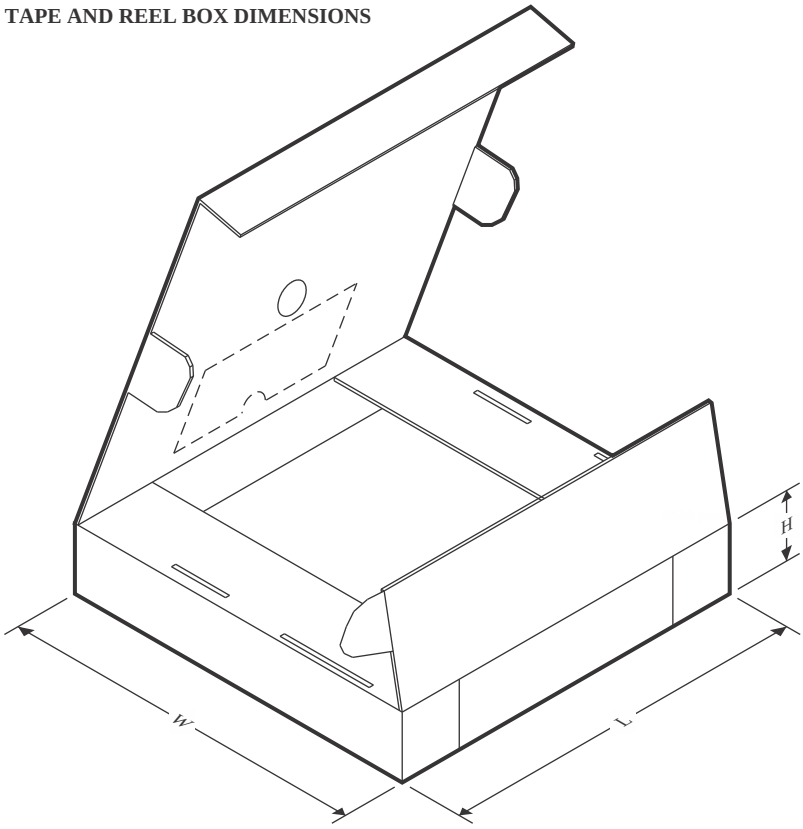
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25211W1015	DSBGA	YZC	6	3000	180.0	8.4	1.09	1.56	0.65	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25211W1015	DSBGA	YZC	6	3000	182.0	182.0	20.0

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