

CSD19538Q3A 100V、N 通道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 无铅
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

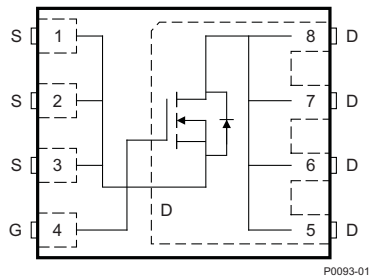
2 应用范围

- 以太网供电 (PoE)
- 电源设备 (PSE)
- 电机控制

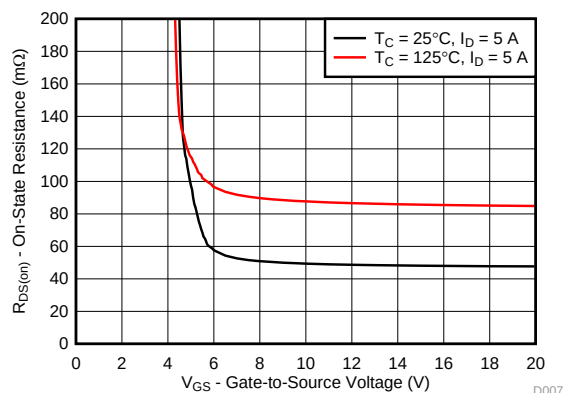
3 说明

这款 100V、49mΩ、SON 3.3mm × 3.3mm NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET) 旨在以最大限度降低导通损耗并减小以太网供电 (PoE) 应用中的电路板尺寸。

俯视图



P0093-01

 $R_{DS(on)}$ 与 V_{GS} 对比

D007

产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	100		V
Q_g	栅极电荷总量 (10V)	4.3		nC
Q_{gd}	栅极电荷 栅极到漏极	0.8		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 6\text{V}$	58	mΩ
		$V_{GS} = 10\text{V}$	49	
$V_{GS(th)}$	阈值电压	3.2		V

器件信息(1)

器件	包装介质	数量	封装	运输
CSD19538Q3A	13 英寸卷带	3000	小外形尺寸无引线 (SON)	卷带封装
CSD19538Q3AT	7 英寸卷带	250	3.30mm × 3.30mm 塑料封装	

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

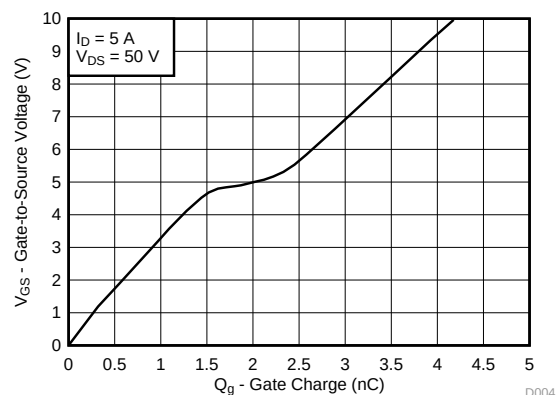
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	100	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流 (受封装限制)	15	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	14	
	持续漏极电流 ⁽¹⁾	4.9	
I_{DM}	脉冲漏极电流 ⁽²⁾	37	A
P_D	功率耗散 ⁽¹⁾	2.8	W
	功率耗散, $T_C = 25^\circ\text{C}$	23	
T_J, T_{stg}	工作结温, 储存温度	-55 至 150	°C
E_{AS}	雪崩能量, 单一脉冲 $I_D = 12.7\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	8.1	mJ

(1) $R_{\theta JA} = 45^\circ\text{C/W}$, 这是一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸², 2 盎司铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC} = 5.5^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。

栅极电荷



D004



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4 修订历史记录

Changes from Original (May 2016) to Revision A	Page
• 已更改 把栅极电荷曲线中的测试电压 V_{DS} 从 100V 更改为 50V	1
• Changed the test voltage V_{DS} in Figure 4 from 100 V : to 50 V	5
• 已添加 接收文档更新通知部分添加到器件和文档支持部分	7

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	100			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 80 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.8	3.2	3.8	V
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = 6 V, I _D = 5 A	58		72	mΩ
		V _{GS} = 10 V, I _D = 5 A	49		59	
g _{fs}	Transconductance	V _{DS} = 10 V, I _D = 5 A	6.1			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 50 V, f = 1 MHz		349	454	pF
C _{oss}	Output capacitance			69	90	pF
C _{rss}	Reverse transfer capacitance			12.6	16.4	pF
R _G	Series gate resistance		4.6	9.2		Ω
Q _g	Gate charge total (10 V)	V _{DS} = 50 V, I _D = 5 A		4.3		nC
Q _{gd}	Gate charge gate-to-drain			0.8		nC
Q _{gs}	Gate charge gate-to-source			1.6		nC
Q _{g(th)}	Gate charge at V _{th}			1		nC
Q _{oss}	Output charge	V _{DS} = 50 V, V _{GS} = 0 V		12.3		nC
t _{d(on)}	Turnon delay time	V _{DS} = 50 V, V _{GS} = 10 V, I _{DS} = 5 A, R _G = 0 Ω		5		ns
t _r	Rise time			3		ns
t _{d(off)}	Turnoff delay time			7		ns
t _f	Fall time			2		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 5 A, V _{GS} = 0 V		0.85	1	V
Q _{rr}	Reverse recovery charge	V _{DS} = 50 V, I _F = 5 A, di/dt = 300 A/μs		94		nC
t _{rr}	Reverse recovery time			32		ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

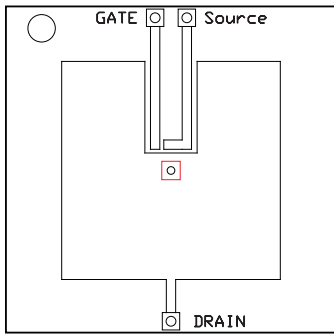
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance ⁽¹⁾			5.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			55	$^\circ\text{C}/\text{W}$

- $R_{\theta JC}$ is determined with the device mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.

CSD19538Q3A

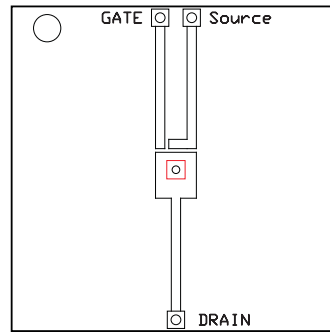
ZHCSF23A – MAY 2016 – REVISED MARCH 2017

www.ti.com.cn



M0161-01

Max $R_{\theta JA} = 55^{\circ}\text{C/W}$
when mounted on 1-in²
(6.45-cm²) of 2-oz
(0.071-mm) thick Cu.



M0161-02

Max $R_{\theta JA} = 195^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz (0.071-mm) thick
Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)

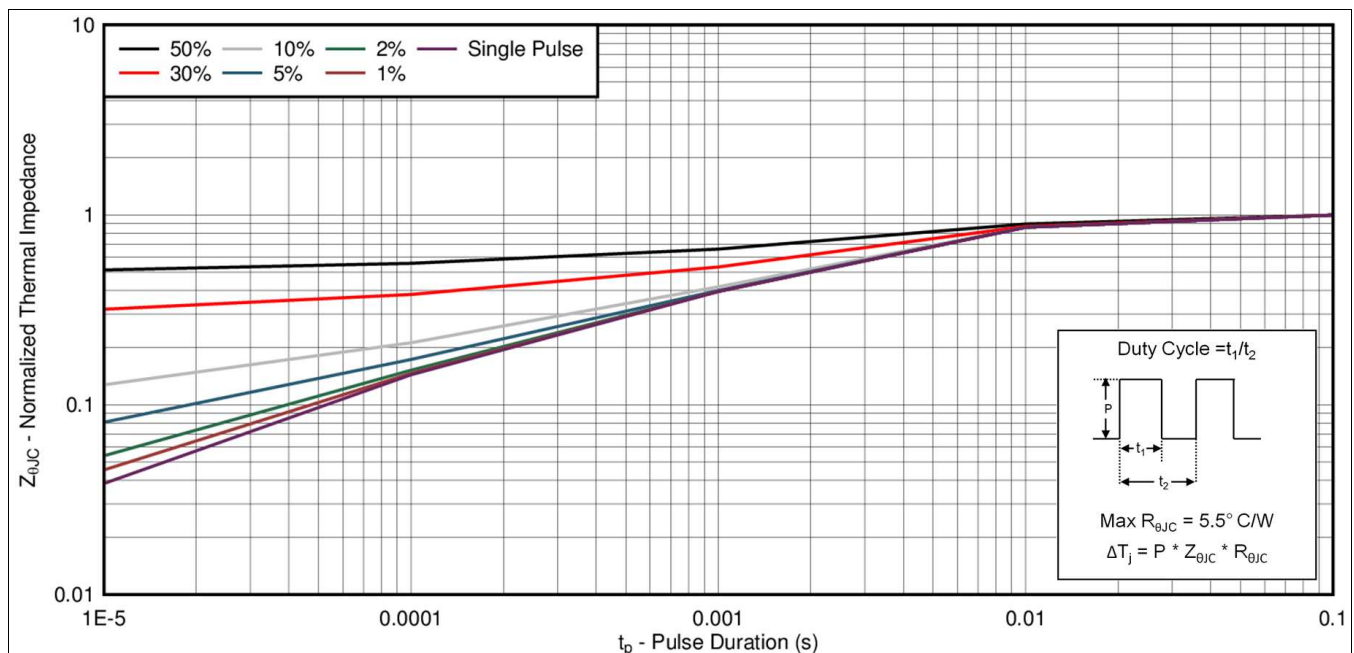


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

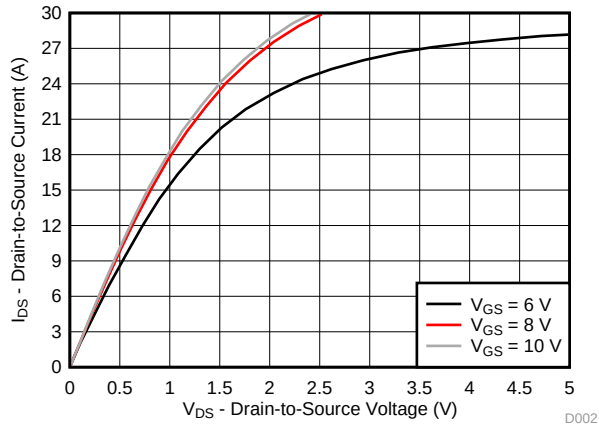


Figure 2. Saturation Characteristics

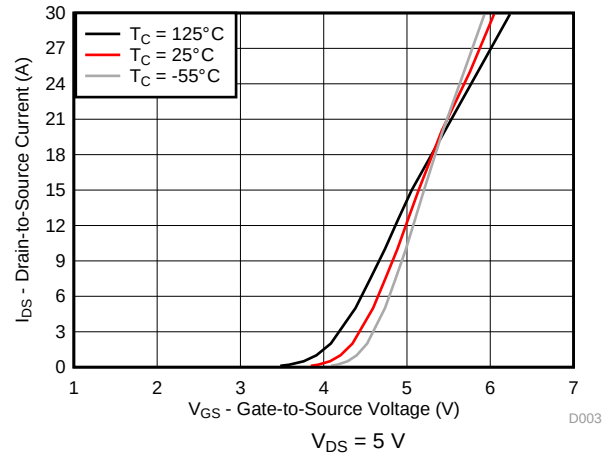


Figure 3. Transfer Characteristics

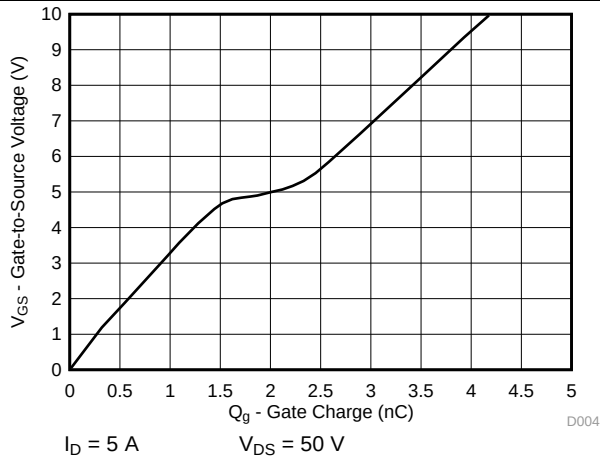


Figure 4. Gate Charge

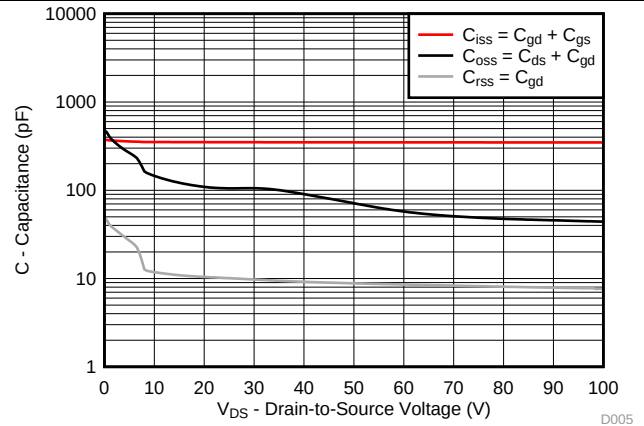


Figure 5. Capacitance

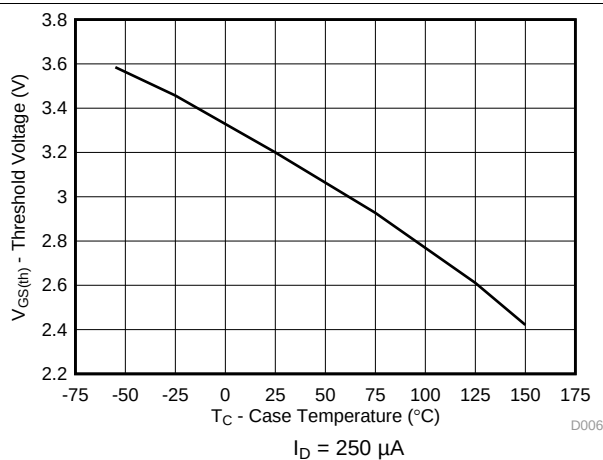


Figure 6. Threshold Voltage vs Temperature

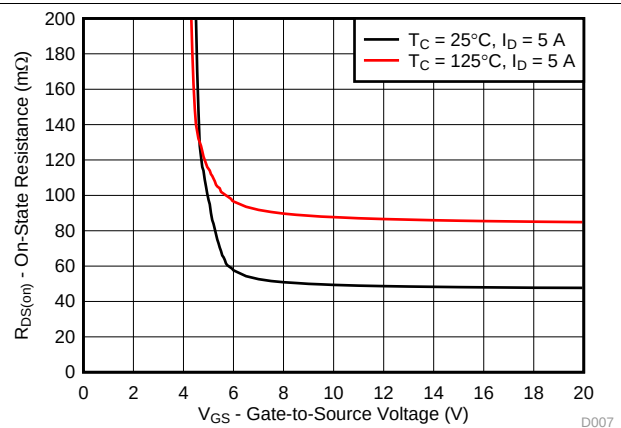


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

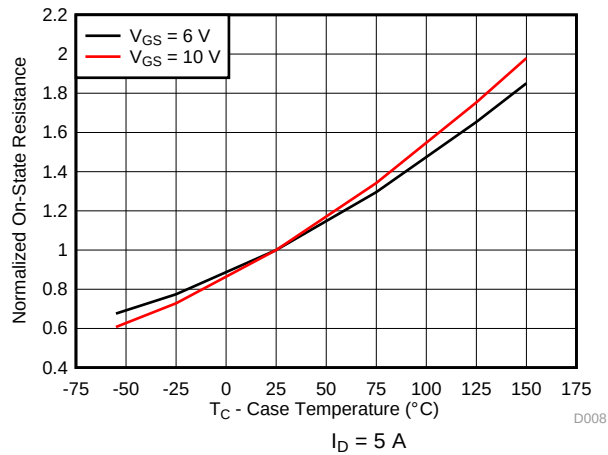


Figure 8. Normalized On-State Resistance vs Temperature

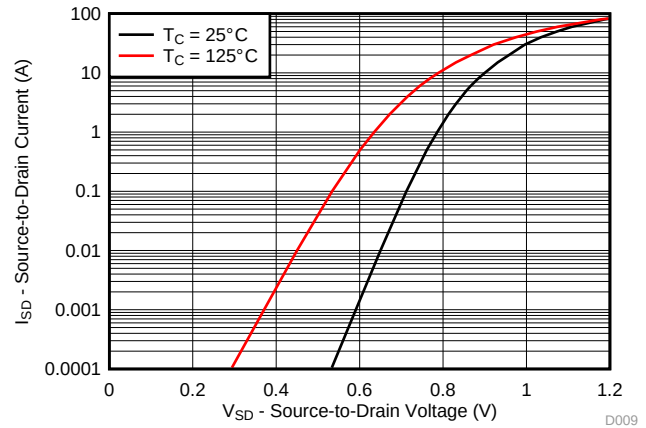


Figure 9. Typical Diode Forward Voltage

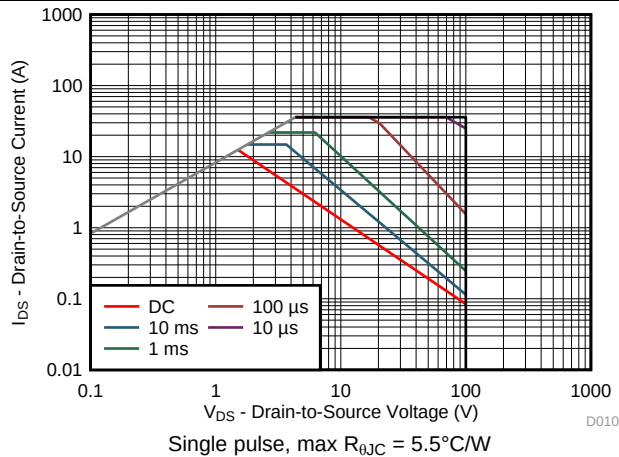


Figure 10. Maximum Safe Operating Area

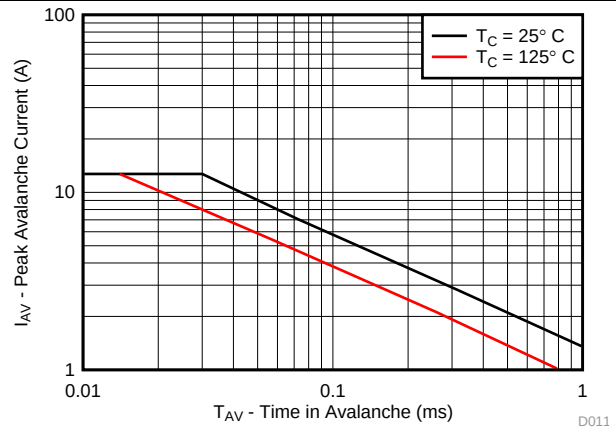


Figure 11. Single Pulse Unclamped Inductive Switching

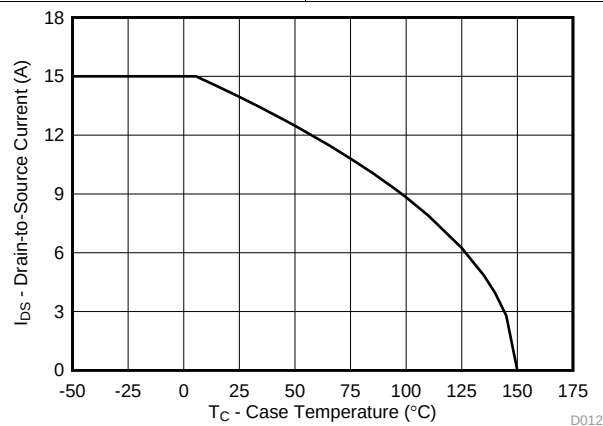


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

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TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

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All other trademarks are the property of their respective owners.

6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

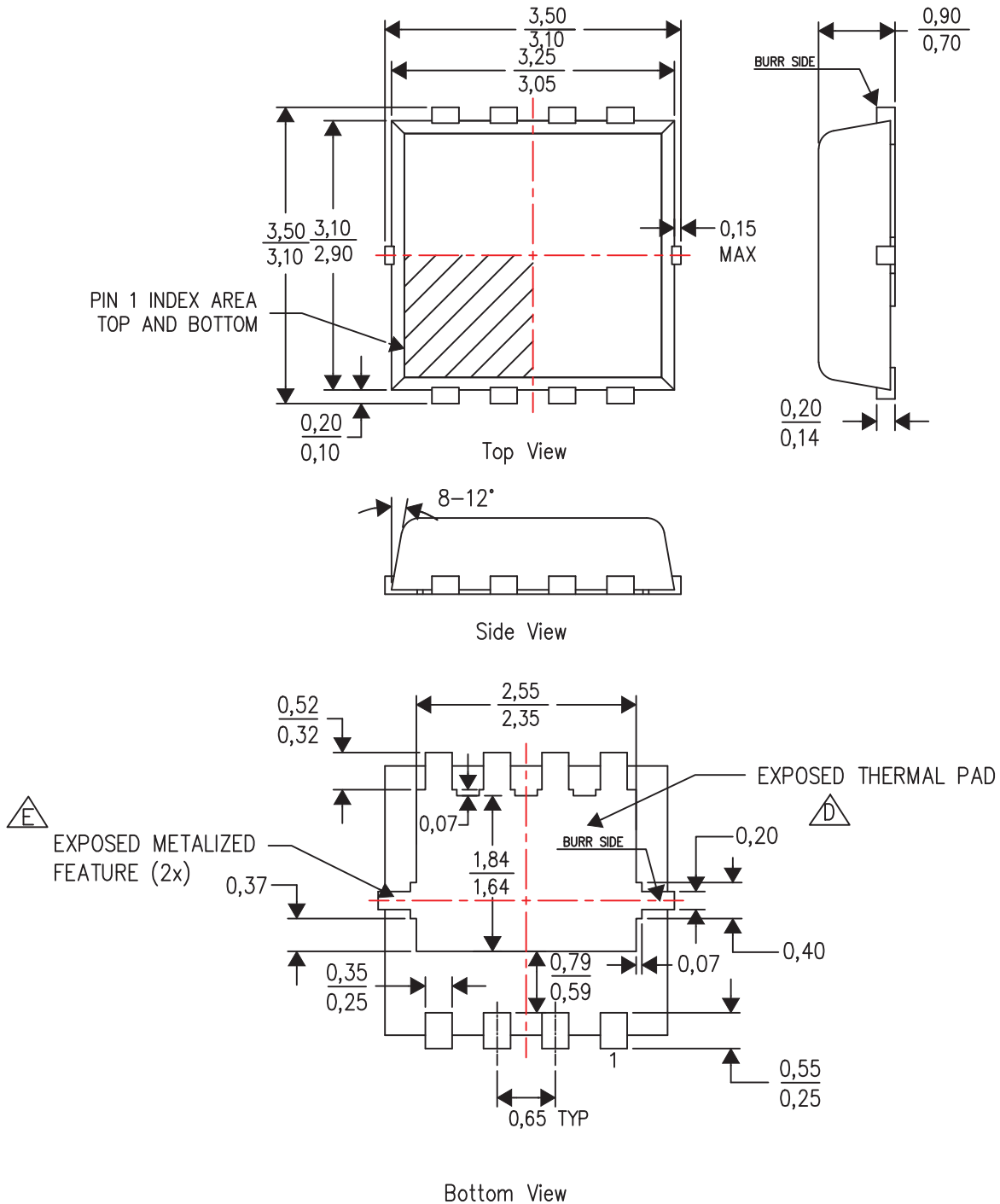
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

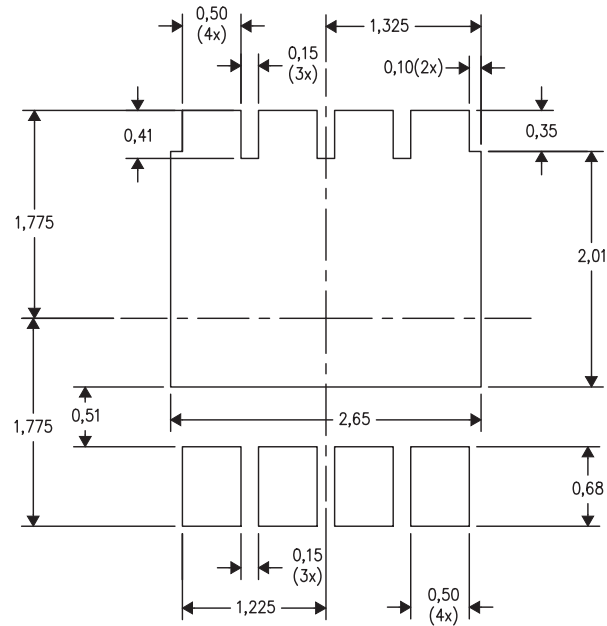
7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q3A 封装尺寸

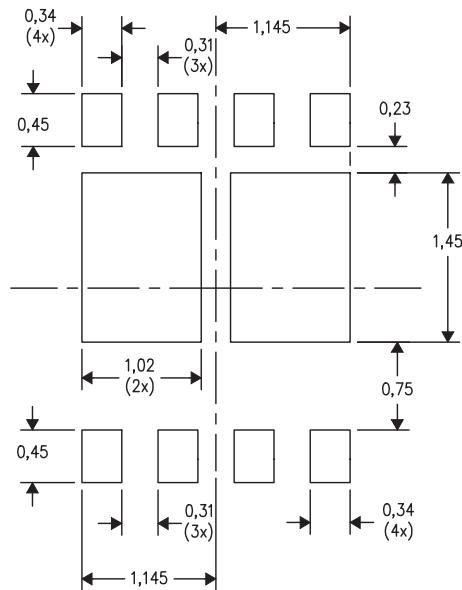


7.2 Q3A 建议的 PCB 布局

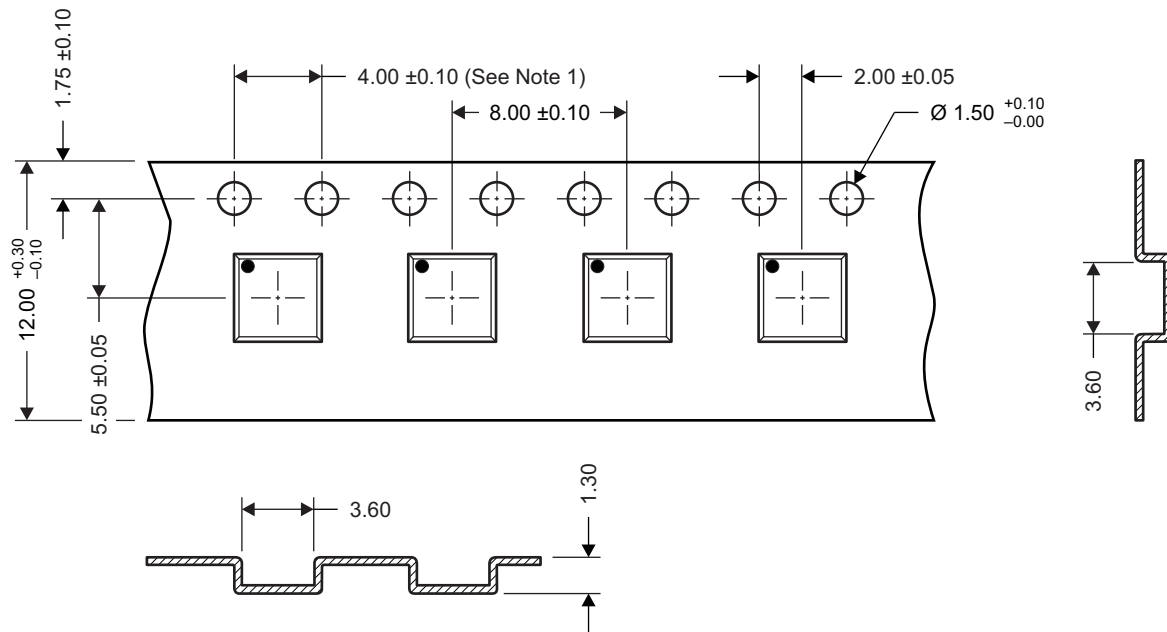


有关针对 PCB 设计的建议电路布局布线，请参见《[通过 PCB 布局布线技巧来减少振铃](#)》（文献编号：SLPA005）。

7.3 Q3A 建议的模板布局



7.4 Q3A 卷带信息



M0144-01

- Notes:
1. 10 链轮孔距累积容差为 ± 0.2
 2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
 3. 材料：黑色抗静电聚苯乙烯。
 4. 所有尺寸单位均为 mm，除非另外注明。
 5. 厚度： 0.3 ± 0.05 mm。
 6. MSL1 260°C（红外和对流）PbF 回流焊兼容。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD19538Q3A	Active	Production	VSONP (DNH) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	19538
CSD19538Q3A.B	Active	Production	VSONP (DNH) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	19538
CSD19538Q3AT	Active	Production	VSONP (DNH) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	19538
CSD19538Q3AT.B	Active	Production	VSONP (DNH) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	19538

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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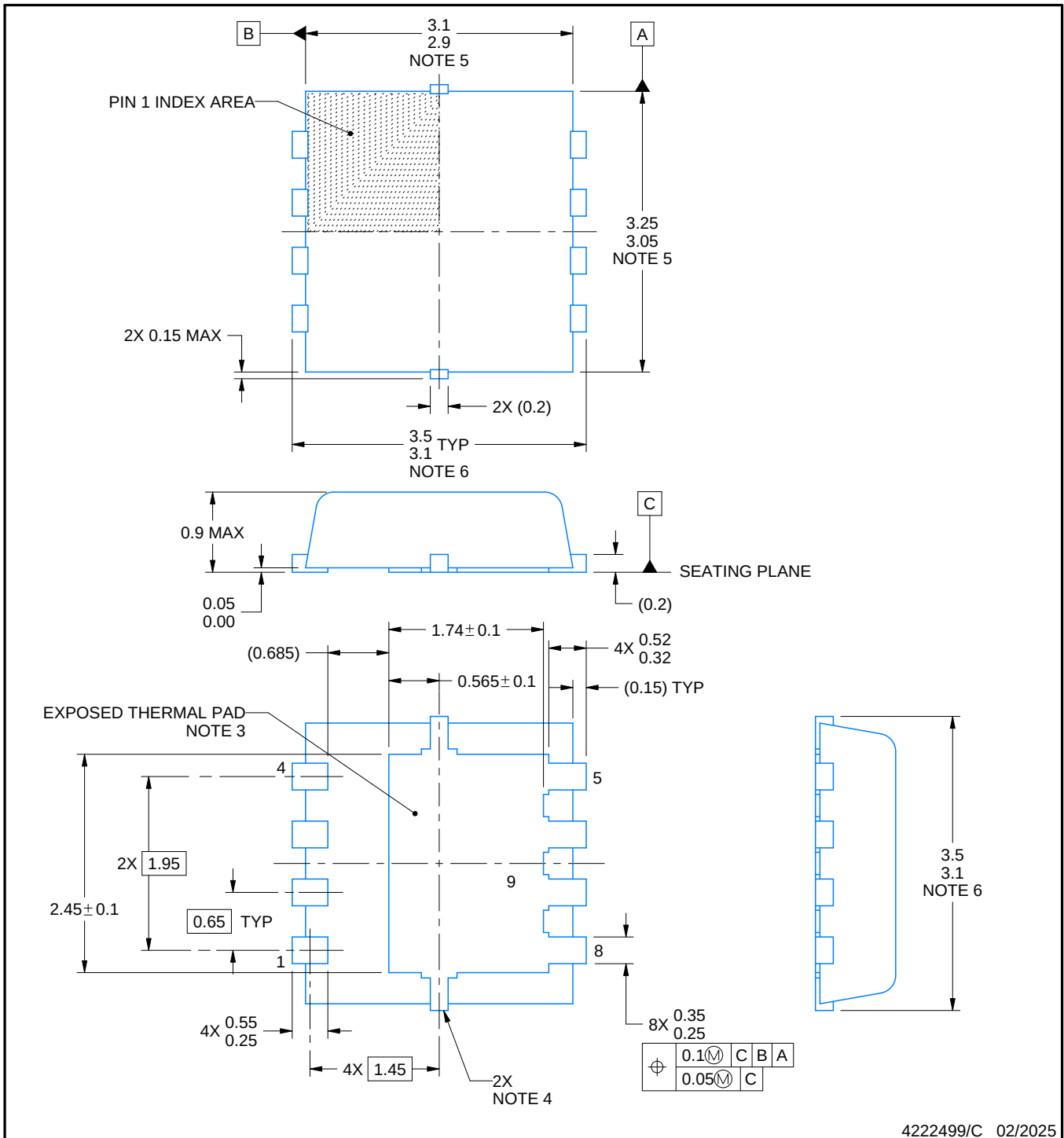
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DNH0008A

PACKAGE OUTLINE

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

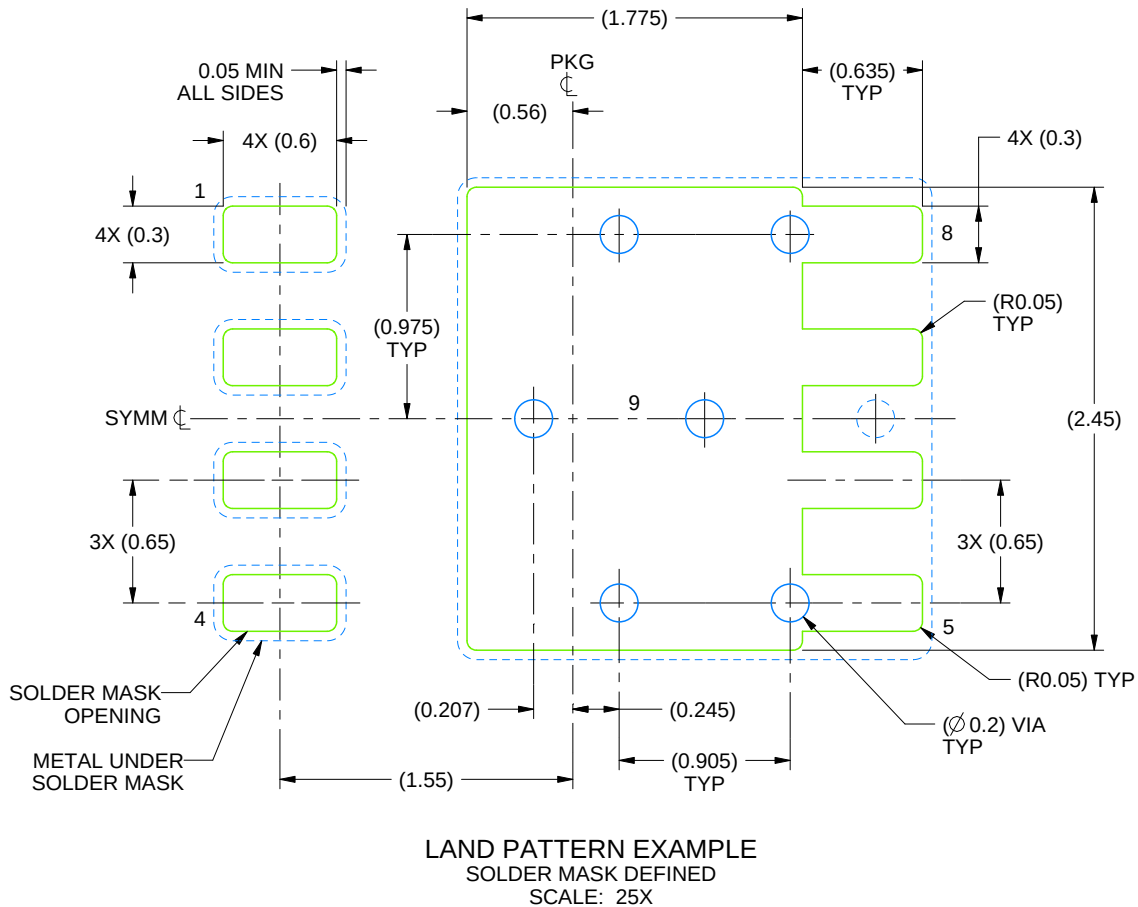
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222499/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

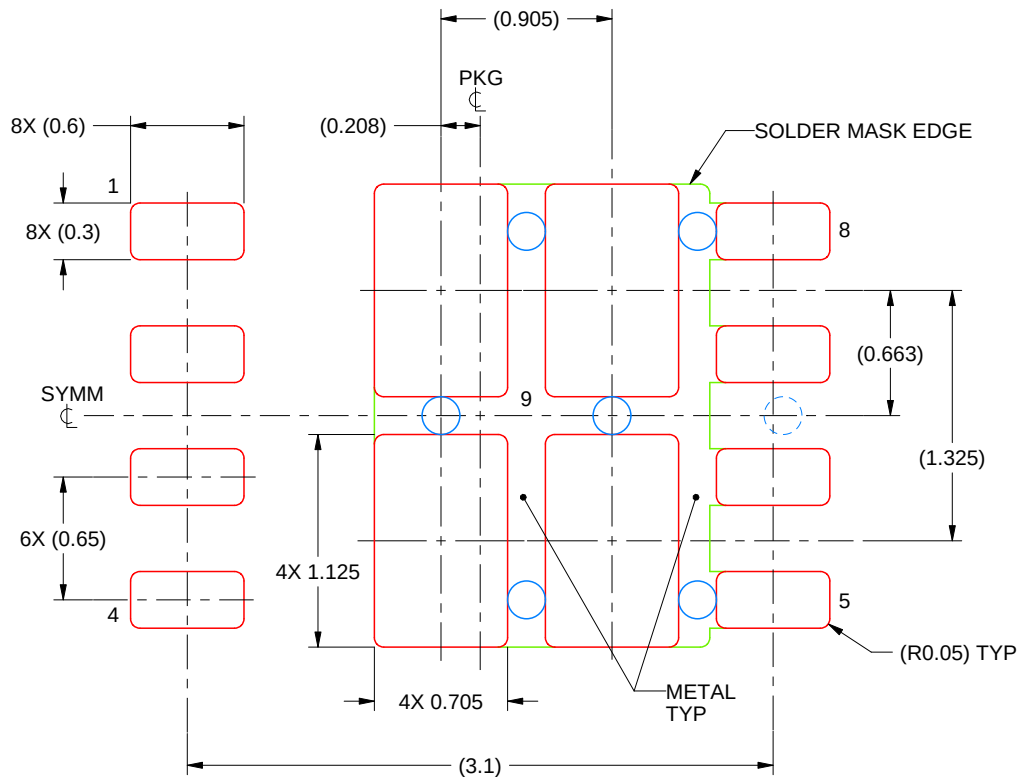
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4222499/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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